UM2248
User manual

Evaluation board with STM32L4R9AI MCU

Introduction

The STM32L4R9I-EVAL board is designed as a complete demonstration and development platform for the STMicroelectronics Arm® Cortex®-M4 core-based STM32L4R9AI microcontroller with four I²C buses, three SPI and six USART ports, CAN port, two SAI ports, 12-bit ADC, 12-bit DAC, internal 640-Kbyte SRAM and 2-Mbyte flash memory, two Octo-SPI memory interfaces, touch-sensing capability, USB OTG FS port, LCD-TFT controller, MIPI DSI® host controller, flexible memory controller (FMC), 8- to 14-bit camera interface and JTAG debugging support.

The STM32L4R9I-EVAL, shown in *Figure 3*, *Figure 4*, and *Figure 5*, is used as a reference design for user application development before porting to the final product.

The full range of hardware features on the board helps the user to evaluate all the peripherals (USB, USART, digital microphones, ADC and DAC, TFT LCD, MIPI DSI® display, LDR, SRAM, NOR flash memory device, Octo-SPI flash memory device, microSD™ card, sigma-delta modulators, CAN transceiver, EEPROM) and develop applications. Extension headers allow easy connection of a daughterboard or wrapping board for a specific application.

ST-LINK/V2-1 is integrated on the board, as the embedded in-circuit debugger and programmer for the STM32 MCU and the USB Virtual COM port bridge.

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1 Features

- STM32L4R9AII6 Arm®(a)-based microcontroller with 2 Mbytes of flash memory and 640 Kbytes of RAM in a UFBGA169 package
- 1.2” 390x390 pixels MIPI DSI® round LCD
- 4.3” 480x272 pixels TFT LCD with RGB mode
- Two ST-MEMS digital microphones
- 8-Gbyte microSD™ card bundled
- 16-Mbit (1 M x 16 bit) SRAM device
- 128-Mbit (8 M x 16 bit) NOR flash memory device
- 512-Mbit Octo-SPI flash memory device with double transfer rate (DTR) support
- 64-Mbit Octo-SPI SRAM memory device with HyperBus™ interface support
- EEPROM supporting 1 MHz I²C-bus communication speed
- Reset and wake-up/tamper buttons
- Joystick with four-way controller and selector
- Touch-sensing button
- Light-dependent resistor (LDR)
- Potentiometer
- Coin battery cell for power backup
- Board connectors:
  - Two jack outputs for a stereo audio headphone with independent content
  - Slot for microSD™ card supporting SD and SDHC
  - TFT LCD standard connector
  - MIPI DSI® display standard connector
  - EXT_I2C connector supports I²C bus
  - RS-232 port configurable for communication or MCU flashing
  - USB OTG FS Micro-AB port
  - CAN 2.0A/B-compliant port
  - Connector for ADC input and DAC output
  - JTAG/SWD connector
  - ETM trace debug connector
  - User interface through USB Virtual COM port
  - Embedded ST-LINK/V2-1 debug and flashing facility
  - TAG connector
  - STDC14 connector
  - Pmod™ connector
  - Extension connector for the daughterboard
  - Motor-control connector on the daughterboard

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

- Flexible power supply options: power jack, ST-LINK/V2-1 USB connector, USB OTG FS connector, daughterboard
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Microcontroller supply voltage: fixed 3.3 V or adjustable range of 1.71 to 3.6 V
- MCU current consumption measurement circuit
- Access to the comparator and operational amplifier of STM32L4R9AII6
- Comprehensive free software libraries and examples available with the STM32Cube package
- Support of a wide choice of integrated development environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

arm

2 Ordering information

To order the STM32L4R9I-EVAL Evaluation board, refer to *Table 1*. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board reference	Targeted STM32
STM32L4R9I-EVAL	– MB1313(1) – MB1314(2) – MB1315(3)	STM32L4R9AII6

1. Main board
2. DSI display daughterboard
3. TFT LCD daughterboard

2.1 Codification

The meaning of the codification is explained in *Table 2*.

Table 2. Codification explanation

STM32XXYY-EVAL	Description	Example: STM32L4R9I-EVAL
XX	MCU series in STM32 Arm Cortex MCUs	STM32L4 series
YY	STM32 product line in the series	STM32L4R9
I	STM32 flash memory size: – I for 2 Mbytes	2 Mbytes
EVAL	Evaluation board	Evaluation board

3 Development environment

3.1 System requirements

- Multi-OS support Windows®(a) 10, Linux®(b) 64-bit, or macOS®(c)
- USB Type-A or USB Type-C® to Micro-B cable

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(d)
- Keil® - MDK-ARM(d)
- STMicroelectronics - STM32CubeIDE

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

a. Windows is a trademark of the Microsoft group of companies.

b. Linux® is a registered trademark of Linus Torvalds.

c. macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.
All other trademarks are the property of their respective owners.

d. On Windows® only.

4 Conventions

Table 3 defines some conventions used in the present document.

Table 3. ON/OFF conventions

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered

5 Delivery recommendations

Before the first use, make sure that no damage occurred to the boards during shipment and that no socketed components are loosened in their sockets or fallen into the plastic bag.

In particular, pay attention to the following components:

1. microSD™ card in its receptacle (CN8)
2. MB1314 DSI display daughterboard in its connector (CN16)

For product information related to the STM32L4R9AII6 microcontroller, visit the *www.st.com* website.

6 Hardware layout and configuration

The STM32L4R9I-EVAL board is designed around the STM32L4R9AII6 target microcontroller in a UFBGA 169-pin package. *Figure 1* illustrates the STM32L4R9AII6 connections with peripheral components. *Figure 2* shows the location of the main components on the main board. *Figure 3*, *Figure 4*, and *Figure 5* are the three images showing the
STM32L4R9I-EVAL main board top view with round DSI display, top view with TFT LCD, and bottom view.

Figure 1. STM32L4R9I-EVAL hardware block diagram

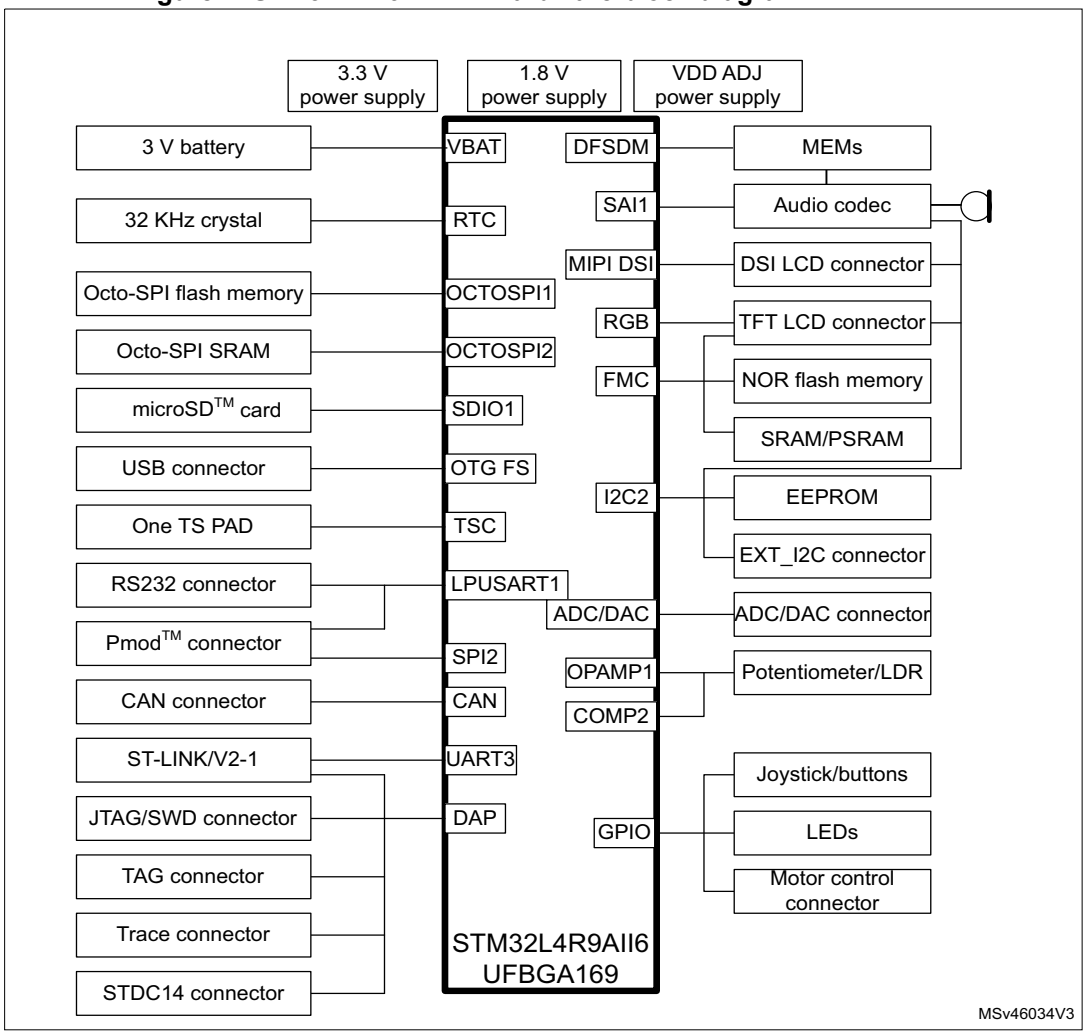
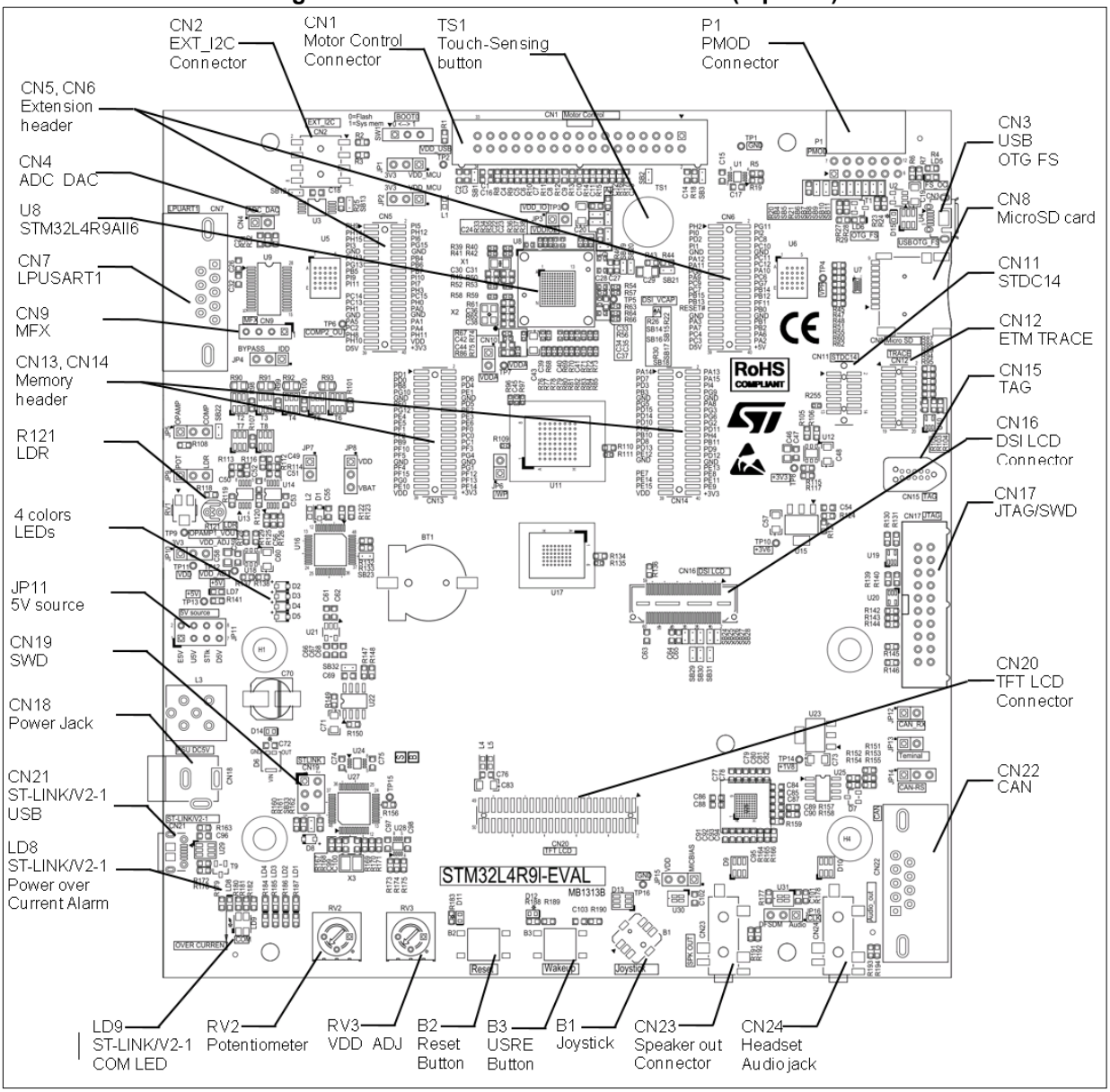
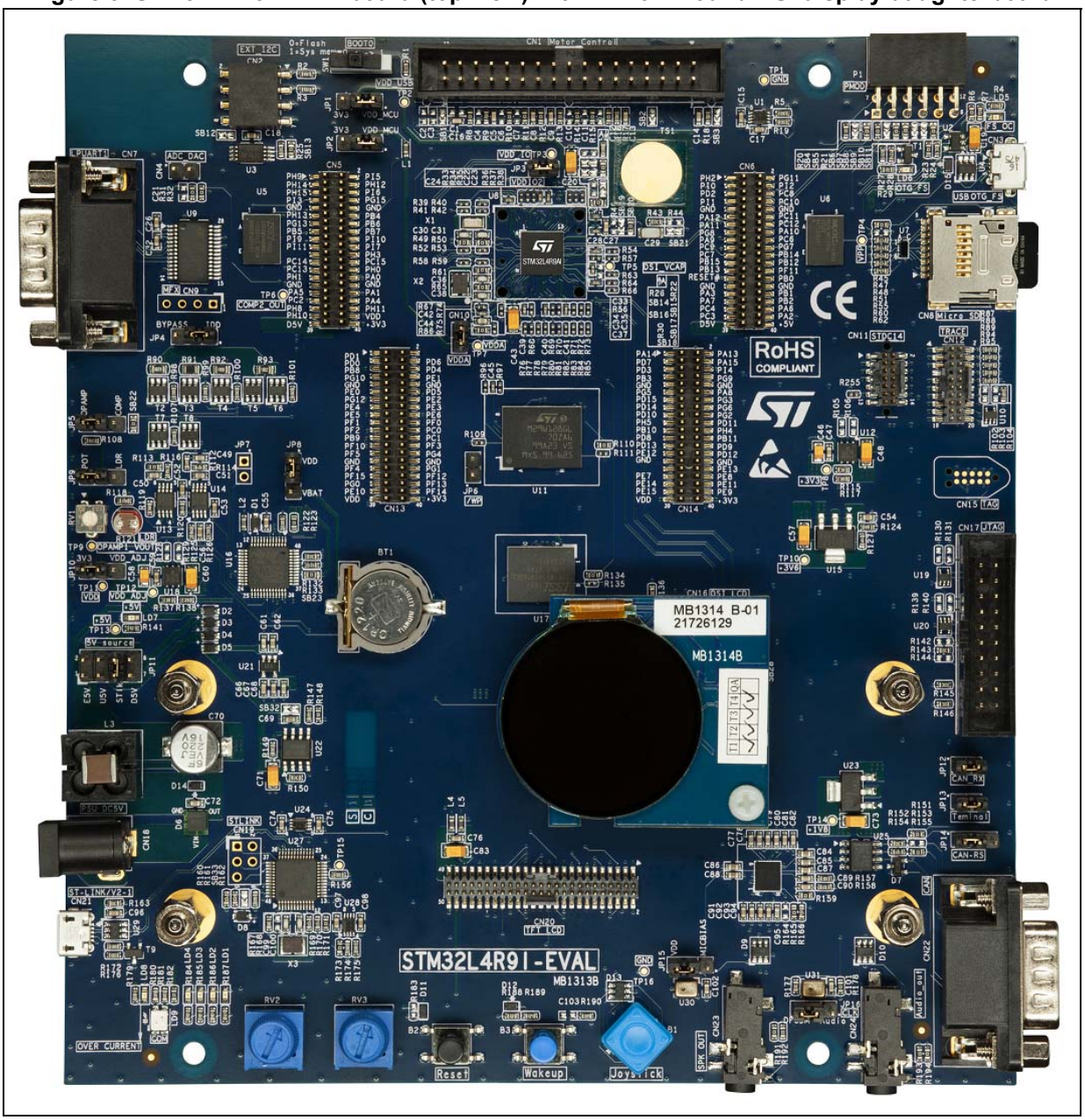


Figure 2. STM32L4R9I-EVAL main board (top side)



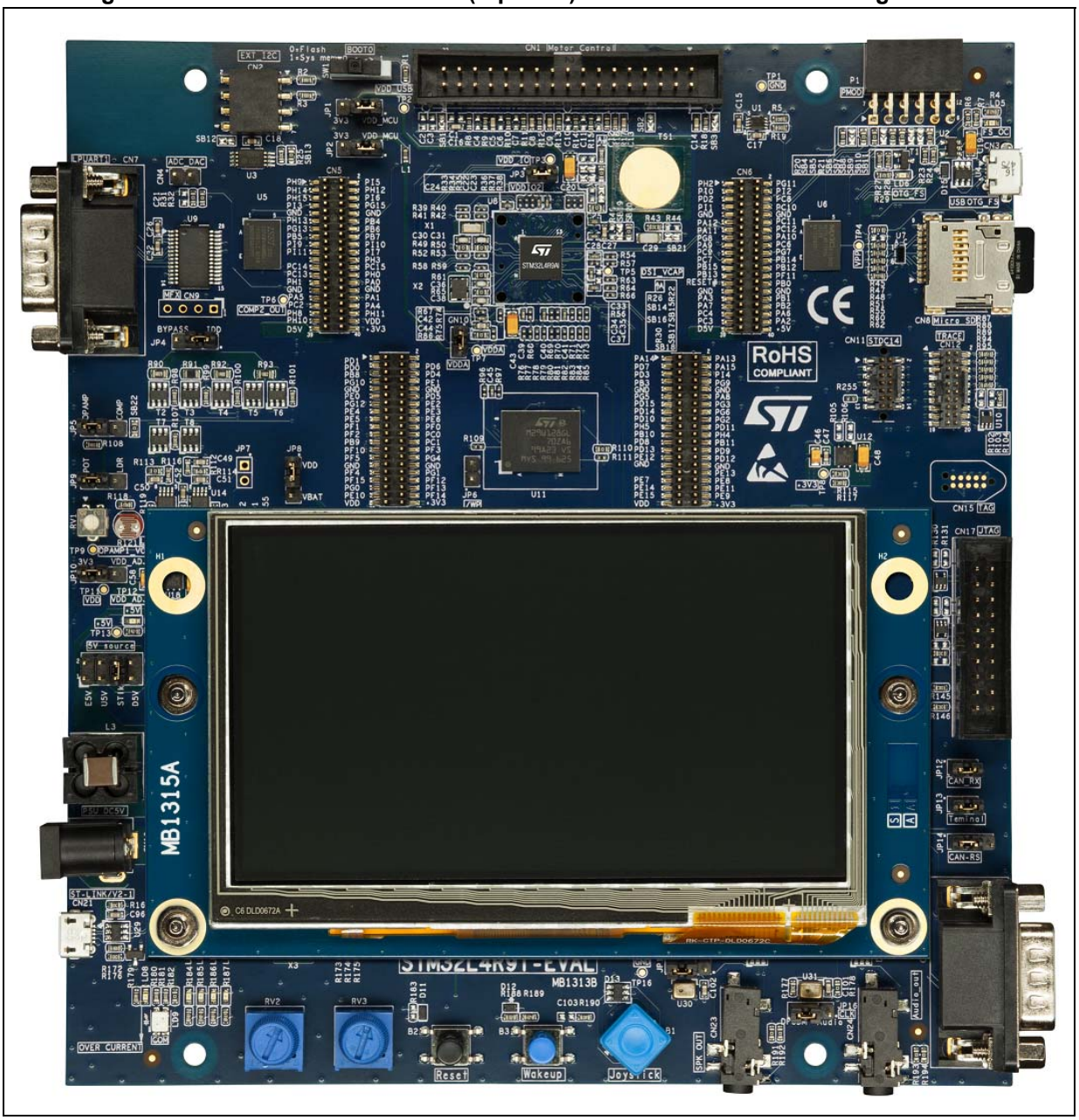
6.1 STM32L4R9I-EVAL main board views

Figure 3. STM32L4R9I-EVAL board (top view) with MB1314 round DSI display daughterboard



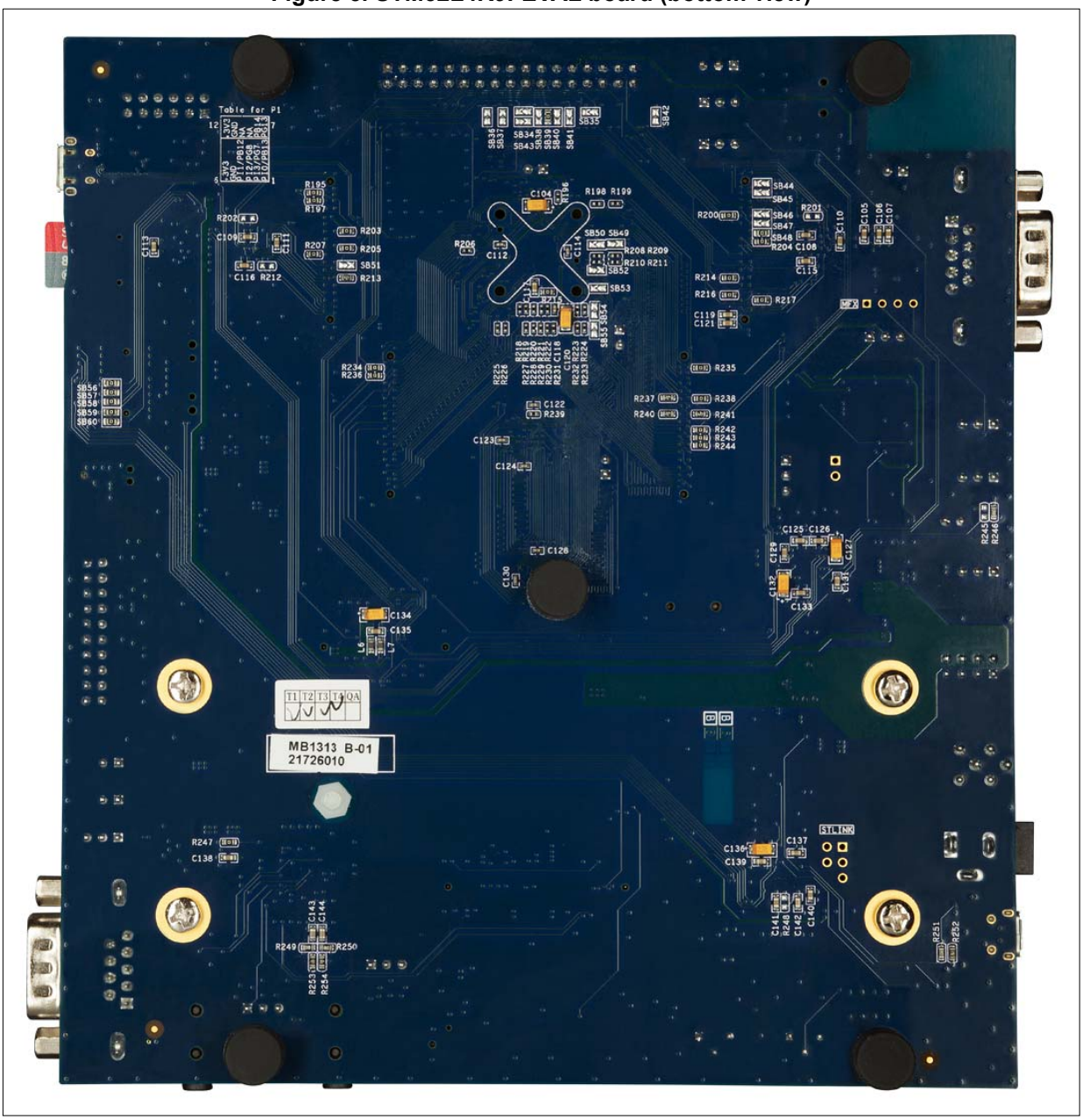
Picture is not contractual.

Figure 4. STM32L4R9I-EVAL board (top view) with MB1315 TFT LCD daughterboard



Picture is not contractual.

Figure 5. STM32L4R9I-EVAL board (bottom view)



Picture is not contractual.

6.2 Mechanical dimensions

Figure 6. MB1313 STM32L4R9I-EVAL main board

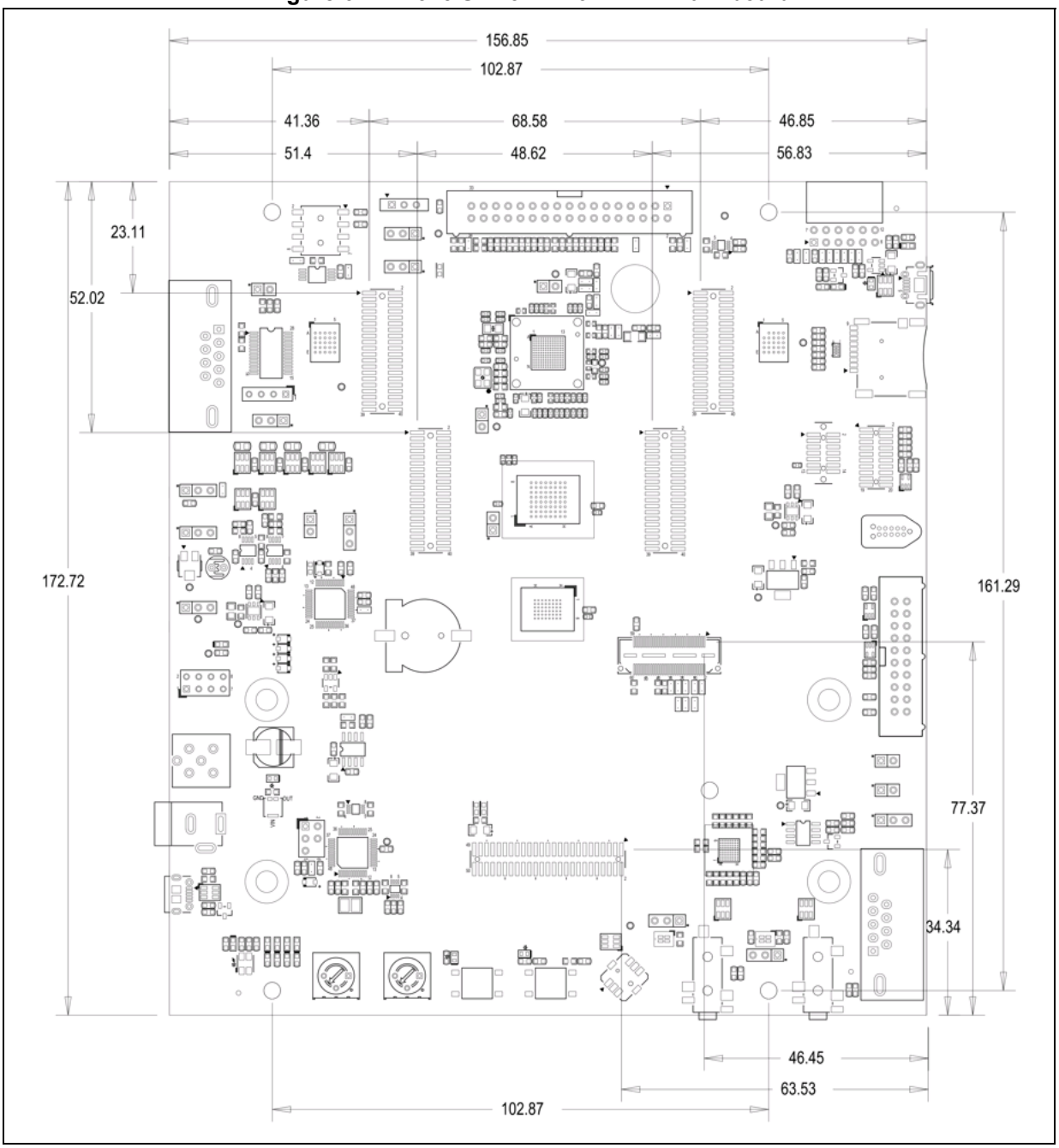
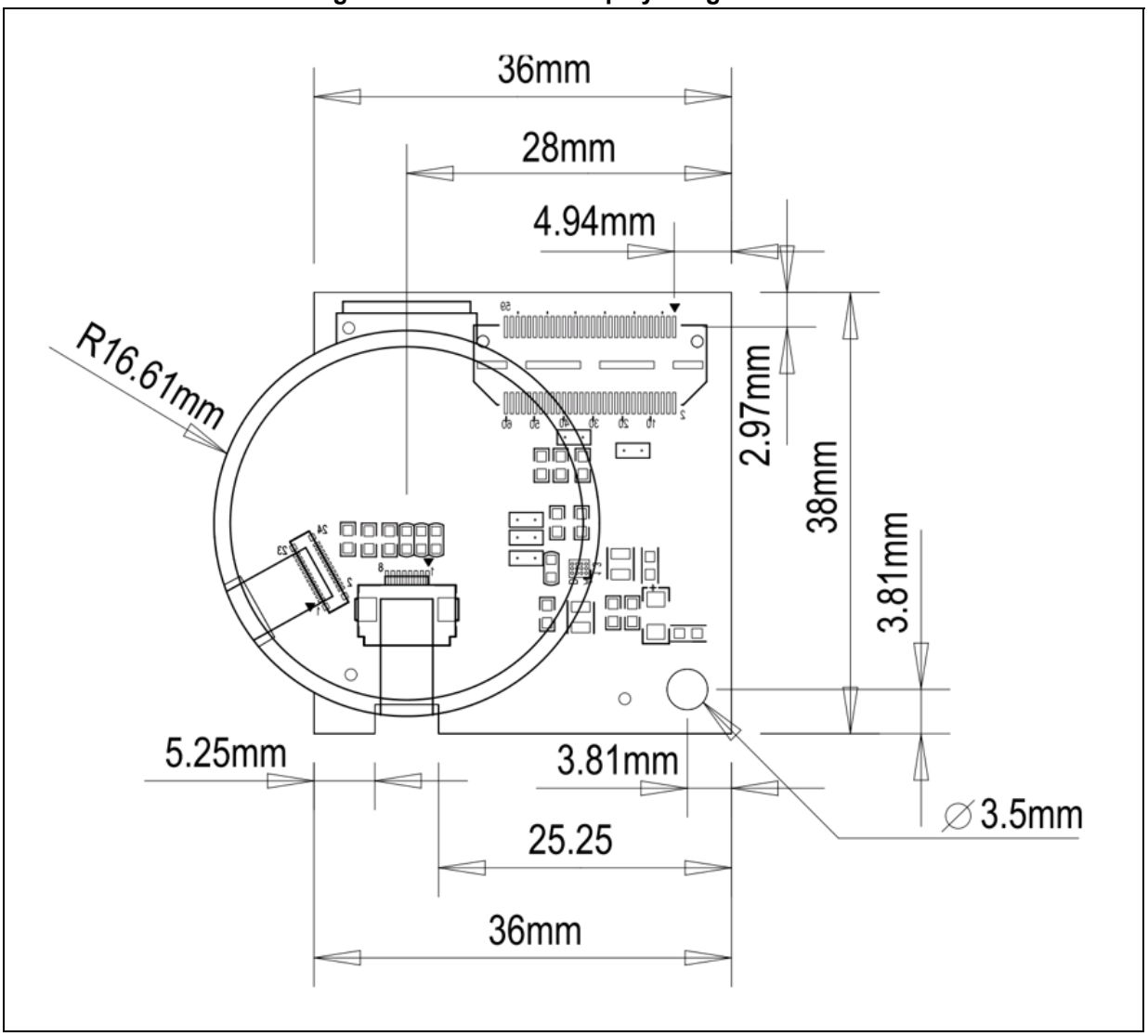


Figure 7. MB1314 DSI display daughterboard



6.3 ST-LINK/V2-1

ST-LINK/V2-1 facility for debugging and flashing of the STM32L4R9AII6 is integrated on the STM32L4R9I-EVAL main board.

Compared to the ST-LINK/V2 standalone tool available from STMicroelectronics, ST-LINK/V2-1 offers new features and drops some others.

New features:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA current on USB

Features dropped:

- SWIM interface

The USB connector (CN21) can be used to power STM32L4R9I-EVAL regardless of the ST-LINK/V21 facility used for debugging or for flashing STM32L4R9AII6. This holds also when the ST-LINK/V2 standalone tool is connected to the CN12, CN17, CN11, or CN15 connector and used for debugging or flashing STM32L4R9AII6. *Section 6.5* provides more details on powering STM32L4R9I-EVAL.

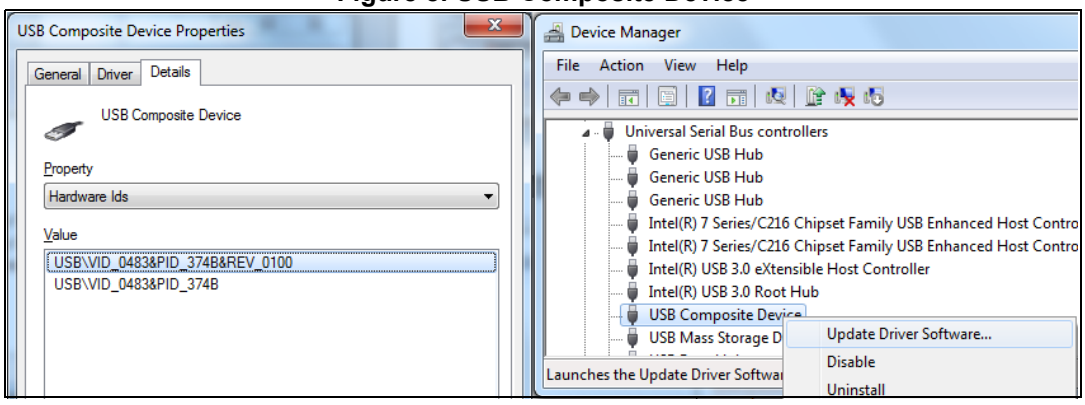
For full detail on both versions of the debug and flashing tool, the standalone ST-LINK/V2 and the embedded ST-LINK/V2-1, refer to *www.st.com*.

6.3.1 Drivers

Before connecting STM32L4R9I-EVAL to a Windows® 8 or older PC via USB, a driver for ST-LINK/V2-1 must be installed. It is available from *www.st.com*.

In case the STM32L4R9I-EVAL main board is connected to the PC before installing the driver, the Windows device manager might report some USB devices found on STM32L4R9I-EVAL as *Unknown*. To recover from this situation, after installing the dedicated driver downloaded from *www.st.com*, the association of *Unknown* USB devices found on STM32L4R9I-EVAL to this dedicated driver must be updated in the device manager manually. Proceed using the USB Composite Device line, as shown in *Figure 8*.

Figure 8. USB Composite Device



6.3.2 ST-LINK/V2-1 firmware upgrade

For its operation, ST-LINK/V2-1 employs a dedicated MCU with flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance. The firmware might evolve during the life span of STM32L4R9I-EVAL to include new functionality, fix bugs, or support new target microcontroller families. It is therefore recommended to keep ST-LINK/V2-1 firmware up to date. The latest version is available from *www.st.com*.

6.4 ETM trace

The trace connector (CN12) is available to output trace signals used for debugging. By default, the Evaluation board is configured such that, STM32L4R9AII6 signals PE2, PE5, and PE6 are not connected to trace outputs Trace_CK, Trace_D2, and Trace_D3 of CN12. They are used for other functions.

Table 4 shows the setting of configuration elements to shunt PE2, PE5, and PE6 MCU ports to the CN12 connector, to use them as debug trace signals.

Table 4. Setting of configuration elements for trace connector (CN12)

Element	Setting	Configuration
R53 SB56	R53 ON SB56 OFF	Default setting.: PE2 connected to memory address line A23.
	R53 OFF SB56 ON	PE2 connected to Trace_CK on CN12. A23 pulled down.
R209 SB59	R209 ON SB59 OFF	Default setting: PE5 connected to memory address line A21.
	R209 OFF SB59 ON	PE5 connected to Trace_D2 on CN12. A21 pulled down.
R211 SB60	R211 ON SB60 OFF	Default setting: PE6 connected to memory address line A22.
	R211 OFF SB60 ON	PE6 connected to Trace_D3 on CN12. A22 pulled down.

Warning: Enabling the CN12 trace outputs through the hardware modifications described in *Table 4* results in reducing the memory address bus width to 20 address lines and so the addressable space to 1 Mword of 16 bits. As a consequence, the onboard SRAM and NOR flash memory usable capacity is reduced to 16 Mbits.

6.5 Power supply

The STM32L4R9I-EVAL main board must be powered from a 5 V DC power source. It incorporates a precise polymer Zener diode (Poly-Zen) protecting the main board from damage due to the wrong power supply. One of the following four 5 V DC power inputs is usable with an appropriate main board configuration:

- Power jack (CN18) marked PSU_DC5V on the main board. A jumper must be placed in the E5V location (JP11). The positive pole is on the center pin as illustrated in *Figure 20*.
- Micro-B USB receptacle (CN21) of ST-LINK/V2-1 provides up to 500 mA to the main board. The offering enumeration feature is described in *Section 6.5.1*.
- Micro-AB USB receptacle (CN3) of the USB OTG interface marked USB OTG_FS on the board supplies up to 500 mA to the main board.
- Pin 39 of CN5 and pin 39 of CN6 extension connectors for a custom daughterboard, marked D5V on the main board.

The power source must comply with the EN 62368-1:2014+A11:2017 standard and must be safety extralow voltage (SELV) with limited power capability.

No external power supply is provided with the main board.

LD7 red LED turns on when the voltage on the power line marked as +5 V is present. All supply lines required for the operation of the components on STM32L4R9I-EVAL are derived from that +5 V line.

Table 5 describes the setting of all jumpers related to powering the STM32L4R9I-EVAL and its extension board. VDD_MCU is an STM32L4R9AII6 digital supply voltage line. It is possible to drive the boards with either fixed 3.3 V or with an adjustable voltage regulator controlled by the RV3 potentiometer and producing a range of voltages from 1.71 to 3.6 V.

6.5.1 Supplying the main board through the ST-LINK/V2-1 USB port

To power STM32L4R9I-EVAL in this way, the USB Host (a PC) gets connected with the STM32L4R9I-EVAL main board Micro-B USB receptacle, via a USB cable. This event is the beginning of the USB enumeration procedure. In its initial phase, the host's USB port current supply capability is limited to 100 mA. It is enough because only the ST-LINK/V2-1 part of STM32L4R9I-EVAL draws power at that time. If the SB33 solder bridge is OFF, the ST890 power switch (U22) is set in the OFF position, which isolates the remainder of STM32L4R9I-EVAL from the power source. In the next phase of the enumeration procedure, the host PC informs the ST-LINK/V2-1 facility of its capability to supply up to 300 mA of current. If the answer is positive, the ST-LINK/V2-1 sets the ST890 switch (U22) to the ON position to supply power to the remainder of the STM32L4R9I-EVAL main board. If the PC USB port is not capable of supplying up to 300 mA of current, the power jack (CN18) is available to supply the main board.

If a short circuit occurs on the main board, the ST890 power switch protects the USB port of the host PC against a current exceeding 600 mA. In such an event, the LD8 LED lights up.

The STM32L4R9I-EVAL main board can also be supplied by a USB power source not supporting enumeration, such as a USB charger, as shown in *Table 5*. ST-LINK/V2-1 turns the ST890 power switch ON regardless of the enumeration procedure result and passes the power unconditionally to the main board.

The LD7 red LED turns on whenever the whole main board is powered.

6.5.2 Using ST-LINK/2-1 along with powering via the power jack

If the main board requires more than 300 mA of supply current, the host PC, connected to the ST-LINK/2-1 USB port and used for debugging or flashing STM32L4R9AII6, cannot provide such a current. In such a case, the main board is supplied through CN18 (marked PSU_DC5V on the main board).

To do this, it is important to power the main board before connecting it with the host PC, which requires the following sequence to be respected:

1. Set the jumper on the header (JP11) in the E5V position,
2. Connect the external 5 V power source to CN18,
3. Check that the red LED LD7 is turned on,
4. Connect the host PC to the USB connector (CN12).

In case the main board requires more than 300 mA and the host PC is connected via USB before the main board is powered from CN18, there is a risk of the following events occurring, in the order of severity:

1. The host PC can supply 300 mA (the enumeration succeeds) but it does not incorporate any overcurrent protection on its USB port. It is damaged due to the overcurrent.
2. The host PC can supply 300 mA (the enumeration succeeds) and it has built-in overcurrent protection on its USB port, limiting or shutting down the power out of its

USB port when the excessive current requirement from STM32L4R9I-EVAL is detected. This causes an operating failure to STM32L4R9I-EVAL.

3. The host PC is not capable of supplying 300 mA (the enumeration fails) so ST-LINK/V2-1 does not supply the remainder of STM32L4R9I-EVAL from its USB port V_{BUS} line.

Table 5. Power-supply-related jumpers settings

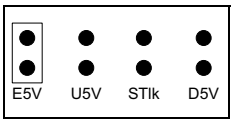
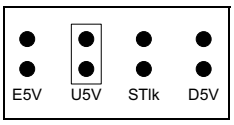
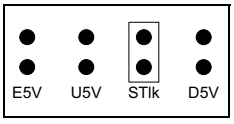
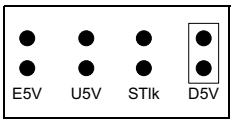
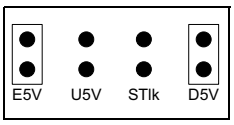
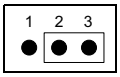
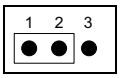
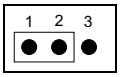
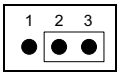
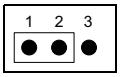
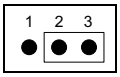
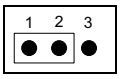
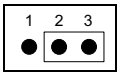
Jumper / solder bridge	Setting	Configuration
Power source selector (JP11)		STM32L4R9I-EVAL is supplied via the power jack marked PSU_DC5V (CN18). CN5 and CN6 extension connectors do not pass the 5 V of STM32L4R9I-EVAL to the daughterboard.
		STM32L4R9I-EVAL is supplied through the Micro-AB USB connector (CN3). CN5 and CN6 extension connectors do not pass the 5 V of STM32L4R9I-EVAL to the daughterboard.
		Default setting: STM32L4R9I-EVAL is supplied through the Micro-B USB connector (CN21). CN5 and CN6 extension connectors do not pass the 5 V of STM32L4R9I-EVAL to the daughterboard.
		STM32L4R9I-EVAL is supplied through pin 39 of CN5 and pin 39 of CN6 extension connectors.
		STM32L4R9I-EVAL is supplied via the power jack (CN18). CN5 and CN6 extension connectors pass the 5 V of STM32L4R9I-EVAL to the daughterboard. Make sure to disconnect from the daughterboard, any power supply that might generate conflict with the power supply on the power jack (CN18).
Vbat connection (JP8)		Vbat is connected to the battery.
		Default setting: Vbat is connected to VDD.
VDD_MCU connection (JP10)		Default setting: VDD_MCU (VDD terminals of STM32L4R9AII6) is connected to fixed +3.3 V.
		VDD_MCU is connected to voltage in the range from +1.71 V to +3.6 V, adjustable with potentiometer RV3.
VDD_USB connection (JP1)		Default setting: VDD_USB (VDD USB terminal of STM32L4R9AII6) is connected with VDD_MCU.
		VDD_USB is connected to +3.3 V.

Table 5. Power-supply-related jumpers settings (continued)

Jumper / solder bridge	Setting	Configuration
VDDA connection (JP2)		Default setting: VDDA terminal of STM32L4R9AII6 is connected with VDD_MCU.
		VDDA terminal of STM32L4R9AII6 is connected to +3.3 V.
VDD_IO connection (JP3)		Default setting: VDD_IO (VDDIO2 terminals of STM32L4R9AII6) is connected with VDD_MCU.
		VDD_IO is open.
Powering through USB of ST-LINK/V2-1 (SB33)	SB33 Off	Default setting: The ST-LINK/V2-1 Micro-B USB connector (CN21) can be used to supply power to the STM32L4R9I-EVAL main board remainder, depending on the powering capability of the host PC USB port declared in the enumeration.
	SB33 On	The ST-LINK/V2-1 Micro-B USB connector (CN21) supplies power to the STM32L4R9I-EVAL main board remainder. This is the setting for powering the main board through CN21 using a USB charger(1).

1. On all ST-LINK/V2-1 boards, the target application is now able to run even if the ST-LINK/V2-1 is either not connected to a USB host, or powered through a USB charger or a nonenumerating USB Host).

6.6 Clock references

Two clock references are available on STM32L4R9I-EVAL for the STM32L4R9AII6 microcontroller.

- 32.768 kHz crystal X1, for embedded RTC
- 16 MHz crystal X2, for the main clock generator

The main clock generation is possible via an internal RC oscillator, disconnected by removing resistors R61 and R65 when the internal RC clock is used.

Table 6. X1 crystal-related solder bridge settings

Solder bridge	Setting	Configuration
SB50	OFF	Default setting: PC14 OSC32_IN terminal is not routed to the CN5 extension connector. X1 is used as the clock reference.
	ON	PC14 OSC32_IN is routed to the CN5 extension connector. Resistor R50 must be OFF, for the X1 quartz circuit not to disturb the clock reference or source on the daughterboard.

Table 6. X1 crystal-related solder bridge settings (continued)

Solder bridge	Setting	Configuration
SB49	OFF	Default setting: PC15 OSC32_OUT terminal is not routed to the CN5 extension connector. X1 is used as the clock reference.
	ON	PC15 OSC32_OUT is routed to the CN5 extension connector. Resistor R49 must be OFF, for the X1 quartz circuit not to disturb the clock reference on the daughterboard.

Table 7. X2 crystal-related solder bridge settings

Solder bridge	Setting	Configuration
SB52	OFF	Default setting: PH0 OSC_IN terminal is not routed to the CN5 extension connector. X2 is used as the clock reference.
	ON	PH0 OSC_IN is routed to the CN5 extension connector. Resistor R61 must be OFF, in order not to disturb the clock reference or source on the daughterboard.
SB53	OFF	Default setting: PH1 OSC_OUT terminal is not routed to the CN5 extension connector. X2 is used as the clock reference.
	ON	PH1 OSC_OUT is routed to the CN5 extension connector. Resistor R65 must be OFF, in order not to disturb the clock reference or source on the daughterboard.

6.7 Reset sources

The reset signal of the STM32L4R9I-EVAL main board is active LOW.

Sources of reset are listed below:

- Reset button (B2)
- Reset from debugging tools: JTAG/SWD connector (CN17), ETM trace connector (CN12), STDC14 connector (CN11), and TAG connector (CN15)
- Reset from daughterboard: through pin 27 of the CN6 extension connector
- Embedded ST-LINK/V2-1

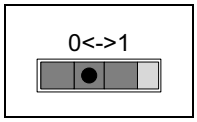
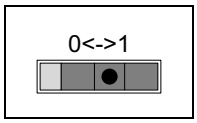
6.8 Boot option

After reset, the STM32L4R9AII6 MCU boot is available from the following embedded memory locations:

- Main (user, nonprotected) flash memory
- System (protected) flash memory
- RAM, for debugging

The boot option is configured by setting switch SW1 (BOOT) and the boot base address programmed in the nBOOT1, nBOOT0, and nSWBOOT0 of FLASH_OPTR option bytes.

Table 8. Boot selection switch

Switch	Setting	Description
SW1		Default setting: The BOOT0 line is tied low. STM32L4R9AII6 boots from the main flash memory or system memory.
		The BOOT0 line is tied high. STM32L4R9AII6 boots from system flash memory (nBOOT1 bit of FLASH_OPTR register is set high) or from RAM (nBOOT1 is set low).

6.8.1 Bootloader limitations

Boot from system flash memory results in executing bootloader code stored in the system flash memory protected against writing and erasing. This allows in-system programming (ISP), that is, flashing the STM32 user flash memory. It also allows writing data into RAM. The data come in via one communication interface such as USART, SPI, I^2C bus, USB, or CAN.

The bootloader version is identified by reading the bootloader ID at the address `0x1FFF6FFE`: the content is `0x91` for bootloader V9.1 and `0x92` for V9.2.

The STM32L4R9AII6 part soldered on the STM32L4R9I-EVAL main board is marked with a date code corresponding to its date of manufacturing. STM32L4R9AII6 parts with a date code before or equal to week 37 of 2017 are installed with bootloader V9.1 affected by the limitations to be worked around, as described hereunder. Parts with the date code starting from week 38 of 2017 contain bootloader V9.2 in which the limitations no longer exist.

To locate the visual date code information on the STM32L4R9II6 package, refer to its datasheet (DS12023) available at *www.st.com*, section Package information. The date code-related portion of the package marking takes Y WW format, where Y is the last digit of the year and WW is the week. For example, a part manufactured in week 38 of 2017 bears the date code 7 38.

There is also another way to identify the need for a workaround: before opening the blister of the Discovery kit, just check the backside of the blister. At the bottom left side, if the reference number is equal to or higher than 32L4R9IDISCO/ 02-0, it means that the bootloader version is V9.2 and there is no need to apply a workaround. Any other inferior number like
01-0 needs the workaround.

The bootloader ID for the bootloader V9.1 is `0x91`.

The following limitation exists in the bootloader V9.1:

Some user flash memory data get corrupted when written via the SPI interface.

Description:

During bootloader SPI, write flash memory operation, some random 64 bits (two double words) might be left blank at `0xFF`.

Workarounds:

WA1: add a delay between sending the write command and its ACK request. Its duration must be the duration of the 256-Byte flash write time.

WA2: read back after each writing operation (256 bytes or at the end of user code flashing) and in case of an error start writing again.

WA3: Using the bootloader, load a patch code in RAM to write in flash memory through the same memory write protocol as the bootloader (code provided by STMicroelectronics).

6.9 Audio

A codec connected to the STM32L4R9AII6 SAI interface supports the DSAI port TDM feature. This offers STM32L4R9AII6 the capability to stream simultaneously two independent stereo audio channels to two separate stereo analog audio outputs.

There are two digital microphones on the STM32L4R9I-EVAL main board.

6.9.1 Digital microphones

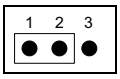
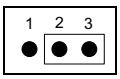
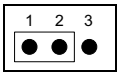
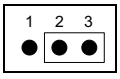
U30 and U31 on the STM32L4R9I-EVAL main board are MP34DT01TR MEMS digital omnidirectional microphones providing PDM (pulse density modulation) outputs. To share the same data line, their outputs are interlaced. The combined data output of the microphones is directly routed to STM32L4R9AII6 terminals, thanks to the integrated input digital filters. The microphones are supplied with a programmable clock generated directly by STM32L4R9AII6.

As an option, the microphones are connected to the WM8994 Wolfson audio codec device (U26). In that configuration, U26 also supplies the PDM clock to the microphones.

Regardless of where the microphones are routed to, STM32L4R9AII6 or WM8994, their power supplier is either the VDD or MICBIAS1 output of the WM8994 codec device.

Table 9 shows the settings of all jumpers associated with the digital microphones on the main board.

Table 9. Digital microphone-related jumper settings

Jumper	Setting	Configuration
JP16		The PDM clock for digital microphones comes from the WM8994 codec.
		Default setting: The PDM clock for digital microphones comes from STM32L4R9AII6.
JP15		The power supply of digital microphones is generated by WM8994 codec.
		Default setting: The power supply of digital microphones is V_{DD}.

6.9.2 Headphones outputs

The STM32L4R9I-EVAL main board potentially drives two sets of stereo headphones. Identical or different stereo audio contents are played back in each set of headphones. STM32L4R9AII6 sends up to two independent stereo audio channels, via its SAI1 TDM port, to the WM8994 codec device. The codec device converts the digital audio stream to stereo analog signals. It then boosts them to drive directly headphones connecting to 3.5 mm stereo jack receptacles on the main board, CN24 for Audio-output1, and CN23 for Audio_output2.

The audio jack (CN23) takes its signal from the WM8994 codec device output intended for driving an amplifier for loudspeakers. A hardware adaptation is incorporated on the main board to make it compatible with a direct headphone drive. The adaptation consists of coupling capacitors blocking the DC component of the signal, attenuator, and antipop resistors. Software in the Class-AB Linear mode and not in the Class-D Switching mode must configure the loudspeaker output of the WM8994 codec device.

The I²C-bus address of WM8994 is `0b0011 010x`.

6.9.3 Limitations in using audio features

Due to the share of some terminals of STM32L4R9AII6 by multiple peripherals, the following limitations apply in using the audio features:

- If the SAI1_MCLKA and SAI1_FSA are used as part of the SAI1 port, they cannot be used as CAN peripherals.
- If the SAI1_SDB is used as part of the SAI1 port, it cannot be used as the Comp2_OUT signal.
- If the SAI1 port of STM32L4R9AII6 is used for streaming audio to the WM8994 codec IC, STM32L4R9AII6 cannot control the motor.
- If the digital microphones are attached to STM32L4R9AII6, control of the motor cannot be driven.

6.10 USB OTG FS port

The STM32L4R9I-EVAL main board supports USB OTG full-speed (FS) communication. The USB OTG connector (CN3) is of the Micro-AB type.

6.10.1 STM32L4R9I-EVAL used as a USB Device

When a *USB Host* connection to the Micro-AB USB connector (CN3) of STM32L4R9I-EVAL is detected, the main board starts behaving like a *USB Device*. Depending on the powering capability of the USB host, the main board potentially takes power from the V_{BUS} terminal of CN3. In the main board schematic diagrams, the corresponding power voltage line is called U5V.

Section 6.5 provides information on how to set associated jumpers for this powering option. The resistor R23 must be left OFF to prevent STM32L4R9I-EVAL from sourcing the 5 V to the V_{BUS} terminal, which would cause conflict with the 5 V sourced by the USB host. This might happen if the software of the MFX MCU controls MFX_GPIO6 such that, it enables the output of the power switch (U2).

6.10.2 STM32L4R9I-EVAL used as a USB Host

When a *USB Device* connection to the CN3 Micro-AB USB connector is detected, the STM32L4R9I-EVAL main board starts behaving like a *USB Host*. It sources 5 V on the V_{BUS} terminal of the Micro-AB USB connector (CN3) to power the USB device. For this to happen, the STM32L4R9AII6 sets the STMPS2151STR power switch (U2) to the ON state. The LD6 green LED marked OTG_FS indicates that the peripheral is supplied from the main board. The LD5 red LED marked FS_OC lights up if an overcurrent is detected. The resistor R23 must be ON to allow the MFX_GPIO6 from the MFX MCU to control the power switch (U2).

In any other STM32L4R9I-EVALpowering option, the resistor R23 must be OFF, to avoid accidental damage caused to an external USB host.

6.10.3 Limitations in using the USB OTG FS port

The USB OTG FS port operation is exclusive to motor control.

6.10.4 Operating voltage

The USB-related operating supply voltage of STM32L4R9AII6 (VDD_USB line) must be within the range of 3.0 to 3.6 V.

6.11 RS232 port

The STM32L4R9I-EVAL main board offers one RS-232 communication port. The RS-232 communication port uses the DB9 male connector (CN7). RX, TX, RTS, and CTS signals of the STM32L4R9AII6 LPUSART1 interface are routed to CN7.

6.11.1 Operating voltage

The RS-232 operating supply voltage of STM32L4R9AII6 (VDD line) must be within the range of 1.71 to 3.6 V.

6.12 microSD™ card

The slot for the microSD™ card (CN8) is routed to the STM32L4R9AII6 SDIO port, accepting SD (up to 2 Gbytes) and SDHC (up to 32 Gbytes) cards. One 8-Gbyte microSD™ card is delivered as part of STM32L4R9I-EVAL. The card insertion switch is routed to the MFX_GPIO5 of the MFX MCU port.

6.12.1 Limitations

Due to the sharing of the SDIO port, the following limitations apply:

- The microSD™ card cannot be operated simultaneously with motor control.
- The microSD™ card cannot be operated for 4 bits date when SDIO_D1 and SDIO_D2 used as Trace_D0 and Trace_D1 signals.

6.12.2 Operating voltage

The supply voltage for the STM32L4R9I-EVAL microSD™ card operation must be within the range of 2.7 to 3.6 V.

6.13 Motor control

The CN1 connector is designed to receive a motor-control (MC) module. *Table 10* shows the assignment of CN1 and STM32L4R9AII6 terminals.

Table 10 also lists the modifications to be made on the main board versus its by-default configuration. Refer to *Section 6.13.1* for further details.

Table 10. Motor-control terminal and function assignment

Motor-control connector (CN1)		STM32L4R9AII6 microcontroller			
Terminal	**Terminal name**	**Port name**	**Function**	**Alternate function**	**Board modifications for enabling motor control**
1	Emergency Stop	PI4	TIM8_BKIN	-	SB3 ON R234 OFF
2	GND	-	GND	-	-
3	PWM_1H	PC6	TIM8_CH1	-	SB21 ON R44 OFF or no daughterboard
4	GND	-	GND	-	-
5	PWM_1L	PH13	TIM8_CH1N	-	SB46 ON R186 OFF
6	GND	-	GND	-	-
7	PWM_2H	PC7	TIM8_CH2	-	SB19 ON SB20 OFF R46 OFF or no daughterboard
8	GND	-	GND	-	-
9	PWM_2L	PH14	TIM8_CH2N	-	SB44 ON R185 OFF
10	GND	-	GND	-	-
11	PWM_3H	PC8	TIM8_CH3	-	SB2 ON R195 OFF
12	GND	-	GND	-	-
13	PWM_3L	PH15	TIM8_CH3N	-	SB45 ON R184 OFF
14	Bus Voltage	PC4	ADC1_IN13	-	SB55 ON R75 OFF
15	PhaseA current+	PC0	ADC1_IN1	-	SB36 ON R242 OFF

Table 10. Motor-control terminal and function assignment (continued)

Motor-control connector (CN1)		STM32L4R9AII6 microcontroller			
Terminal	**Terminal name**	**Port name**	**Function**	**Alternate function**	**Board modifications for enabling motor control**
16	PhaseA current-	-	GND	-	-
17	PhaseB current+	PC1	ADC1_IN2	-	SB37 ON R244 OFF
18	PhaseB current-	-	GND	-	-
19	PhaseC current+	PC2	ADC1_IN3	-	SB43 ON R217 OFF
20	PhaseC current-	-	GND	-	-
21	ICL Shutout	PG9	GPIO	-	SB34 ON R236 OFF
22	GND	-	GND	-	-
23	Dissipative Brake	PG13	GPIO	-	SB47 ON SB29 OFF and no board on the Pmod™ connector
24	PFC indirect current	PA0	ADC1_IN5	-	SB38 ON R214 and SB39 OFF
25	+5V	-	5 V	-	-
26	Heatsink Temp.	PA1	ADC1_IN6	-	SB40 ON R216 OFF
27	PFC Sync	PB14	TIM15_CH1	-	SB41 ON R207 OFF and no board on the Pmod™ connector
28	+3.3V	-	3.3 V	-	-
29	PFC PWM	PB15	TIM15_CH2	-	SB51 ON R187 OFF
30	PFC Shutdown	PA9	TIM15_BKIN	-	SB35 ON R203 OFF
31	Encoder A	PB6	TIM4_CH1	ADC12_IN	SB14 ON SB15 and SB16 OFF R26 OFF or no daughterboard
32	PFC Vac	PC3	ADC1_IN4	-	SB54 ON R67 OFF

Table 10. Motor-control terminal and function assignment (continued)

Motor-control connector (CN1)		STM32L4R9AII6 microcontroller			
Terminal	**Terminal name**	**Port name**	**Function**	**Alternate function**	**Board modifications for enabling motor control**
33	Encoder B	PB7	TIM4_CH2	ADC12_IN	SB17 ON SB18 OFF R30 OFF or no daughterboard.
34	Encoder Index	PB8	TIM4_CH3	ADC12_IN	SB42 ON R235 and JP12 OFF

6.13.1 Board modifications to enable motor control

Figure 9 (top side) and *Figure 10* (bottom side) illustrate the main board modifications listed in *Table 10*, required for the operation of motor control. The red color denotes a component to be removed. The green color denotes a component to be installed.

6.13.2 Limitations

The motor-control operation is exclusive to the OCTOSPIP1 flash memory device, audio codec, potentiometer, LDR, microSD™ card, LED1 to LED4 drive, MEMS, MFX, Pmod™, USB OTG_FS, TFT LCD connector, DSI display connector, and touch sensing.

Figure 9. PCB top-side rework for motor control

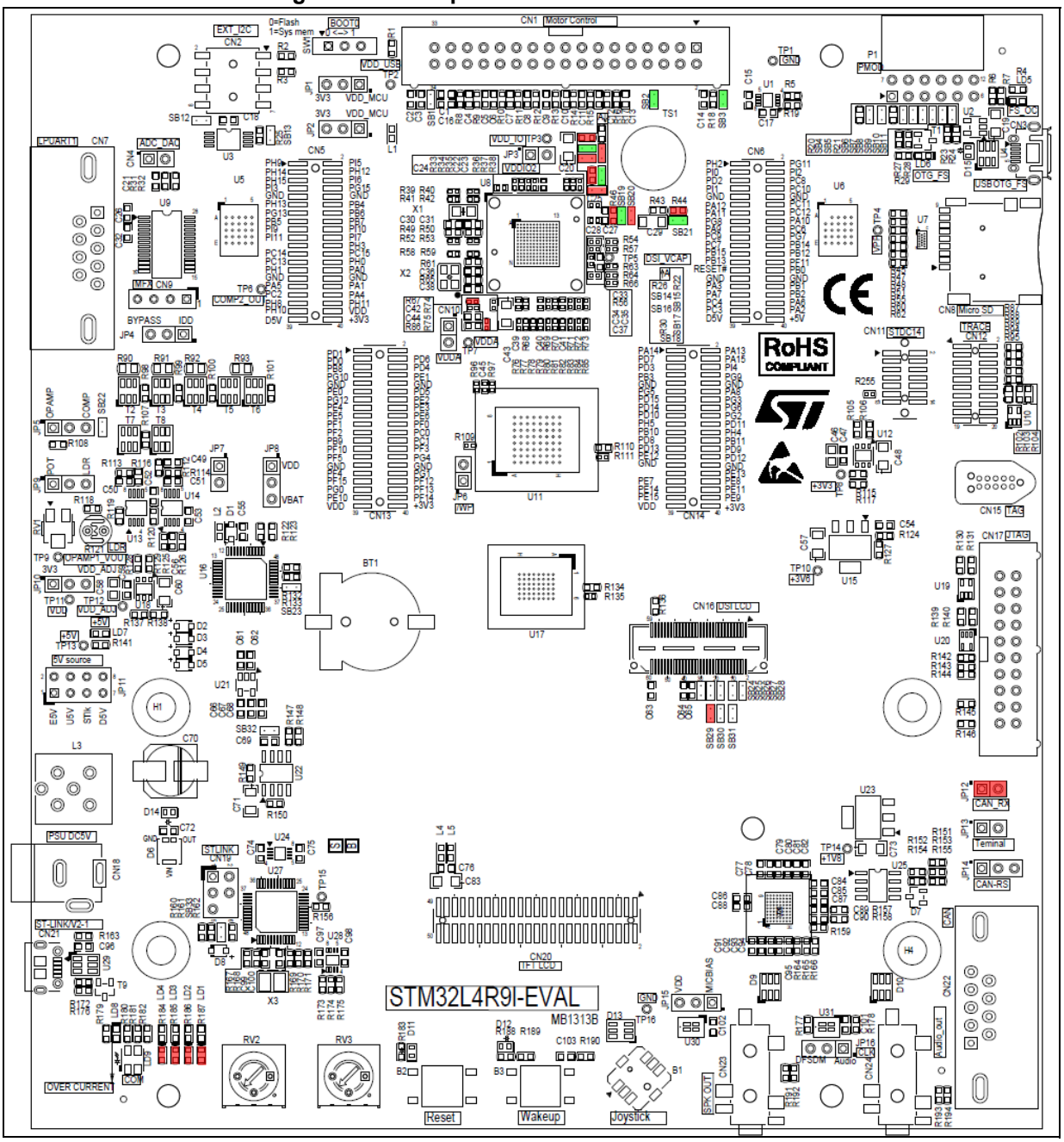
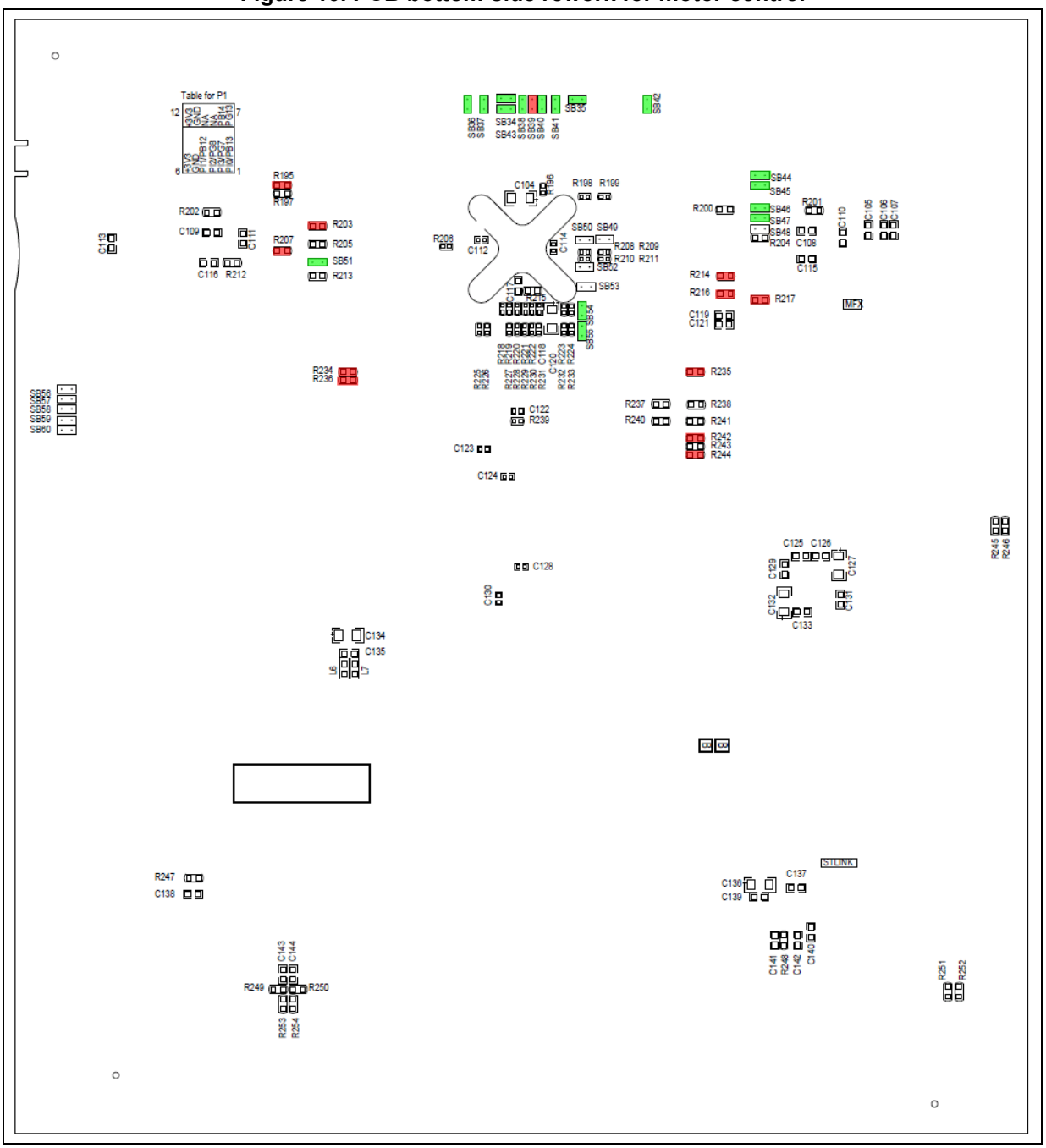


Figure 10. PCB bottom-side rework for motor control



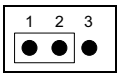
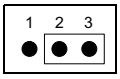
6.14 CAN

The STM32L4R9I-EVAL main board supports one CAN2.0A/B channel compliant with CAN specification. The DB9 male connector (CN22) is available as the CAN interface.

A 3.3 V CAN transceiver is installed between the CN22 connector and the CAN controller port of STM32L4R9AII6.

The jumper (JP14) selects one of the High-speed, Standby, and Slope-control modes of the CAN transceiver. The jumper (JP13) allows the integration of a CAN termination resistor. The jumper (JP12) is used to connect the CAN transceiver avoiding unknown signals from the CAN transceiver.

Table 11. CAN related jumpers

Jumper	Setting	Configuration
JP14		Default setting: CAN transceiver operates in High-speed mode.
		CAN transceiver is in Standby mode.
JP13		Default setting: Termination resistor on CAN physical link.
		No termination resistor on CAN physical link.
JP12		Default setting: CAN_TX is not used for the CAN transceiver.
		CAN_TX is used from the STM32L4R9AII6 terminal.

6.14.1 Limitations

CAN operation is exclusive to the audio codec and MC operation.

6.14.2 Operating voltage

The supply voltage for STM32L4R9I-EVAL CAN operation must be within the range of 3.0 to 3.6 V.

6.15 Extension connectors (CN5, CN6, CN13, and CN14)

The CN5, CN6, CN13, and CN14 headers complement to give access to all GPIOs of the STM32L4R9AII6 microcontroller. In addition to GPIOs, the following signals and power supply lines are also routed on CN5, CN6, CN13, or CN14:

- GND
- +5 V
- +3.3 V
- D5V
- VDD
- RESET#
- Clock terminals PC14-OSC32_IN, PC15-OSC32_OUT, PH0-OSC_IN, PH1-OSC_OUT

Each header has two rows of 20 pins, with 1.27 mm pitch and 2.54 mm row spacing. For extension modules, SAMTEC RSM-120-02-L-D-xxx and SMS-120-x-x-D are recommendable as SMD and through-hole receptacles, respectively (x is a wild card).

6.16 User LEDs

Four general-purpose color LEDs (LD1, LD2, LD3, LD4) are available as light indicators. Each LED is ON with a low level of the corresponding ports of STM32L4R9AII6.

And the four LEDs are exclusive to MC operation.

6.17 Physical input devices

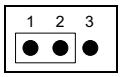
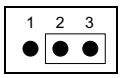
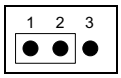
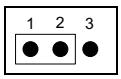
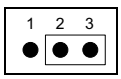
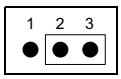
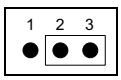
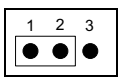
The STM32L4R9I-EVAL main board provides several input devices for physical human control, listed below:

- Four-way joystick controller with select key (B1)
- Wake-up/ tamper button (B3)
- Reset button (B2)
- 10 kΩ potentiometer (RV2)
- Light-dependent resistor, LDR (R121)

The potentiometer and the light-dependent resistor are mutually exclusively routable to either the PB4 or PA0 port of STM32L4R9AII6. *Table 12* depicts the setting of associated configuration jumpers.

As illustrated in the schematic diagram, the PB4 port is routed, in the STM32L4R9AII6, to the noninverting input of comparator Comp2. The PA0 is routed to the noninverting input of the operational amplifier OpAmp1.

Table 12. Port assignment for control of physical input devices

Jumper	Setting	Routing
JP9		A potentiometer is routed to pin PB4 o fSTM32L4R9AII6.
JP5		
JP9		Default setting.: A potentiometer is routed to pin PA0 of STM32L4R9AII6.
JP5		
JP9		LDR is routed to pin PB4 of STM32L4R9AII6.
JP5		
JP9		LDR is routed to pin PA0 of STM32L4R9AII6.
JP5		

6.17.1 Limitations

The potentiometer and the light-dependent resistor are exclusive to MFX, the audio codec, OCTOSPIP1, the debugging connector, and MC operation. They are mutually exclusive.

6.18 Operational amplifier and comparator

6.18.1 Operational amplifier

STM32L4R9AII6 provides two onboard operational amplifiers, one of which, OpAmp1, is made accessible on STM32L4R9I-EVAL. OpAmp1 has its inputs and its output routed to I/O ports PA0, PA1, and PA3, respectively. The noninverting input PA0 is accessible on terminal 1 of the jumper header (JP5). On top of the possibility of routing either the potentiometer or LDR to PA0, an external source is also connectable to it, using terminal 1 of JP5.

The PA3 output of the operational amplifier is accessible on test point TP9. Refer to the schematic diagram.

The ratio of the variable resistor RV1 and the resistor R246 determines the OpAmp1 gain, as shown in the following equation:

Gain = 1 + RV1 / R246

With the RV1 ranging from 0 to 10 kΩ and R246 being 1 kΩ, the gain varies from 1 to 11.

The R108 resistor in series with PA0 is beneficial for reducing the output offset.

Table 13 shows the configuration elements and their settings allowing them to access the OpAmp1 function.

Table 13. Configuration elements related to OpAmp1

Element	Setting	Configuration
SB39 SB38 R214	SB38 OFF SB39 ON R214 OFF	OpAmp1_INP is routed to pin PA0 of STM32L4R9AII6.
	SB38 OFF SB39 ON R214 ON	Default setting: PA0 port of STM32L4R9AII6 is routed to MFX_IRQ_OUT or motor control signal.
	SB38 ON SB39 OFF R214 OFF	PA0 port of STM32L4R9AII6 is routed to the motor-control signal.
R216 SB40	R216 ON SB40 OFF	Default setting: OpAmp1_INM is routed to pin PA1 of STM32L4R9AII6.
	R216 OFF SB40 ON	PA1 port of STM32L4R9AII6 is routed to the motor-control signal.
R215 R221	R215 ON R221 OFF	OpAmp1_VOUT is routed to pin PA3 of STM32L4R9AII6.
	R215 OFF R221 ON	Default setting: OpAmp1_VOUT is not routed to pin PA3 of STM32L4R9AII6. PA3 port of STM32L4R9AII6 is routed to OCTOSPI1_CLK.

6.18.2 Comparator

STM32L4R9AII6 provides two on-board comparators, one of which, Comp2, is made accessible on STM32L4R9I-EVAL. Comp2 has its noninverting input and its output routed to

I/O ports PB4 and PB5, respectively. The input is accessible on terminal 3 of the jumper header (JP5). On top of the possibility of routing either the potentiometer or LDR to PB4, an external source is connectable to it, using terminal 3 of JP5.

The PB5 output of the comparator is accessible on test point TP6. Refer to the schematic diagram.

Table 14 shows the configuration elements and their settings allowing them to access the Comp2 function.

Table 14. Configuration elements related to Comp2

Element	Setting	Configuration
R200 SB22	R200 OFF SB22 ON	Default setting: Comp2_INP is routed to pin PB4 of STM32L4R9AII6.
	R200 ON SB22 OFF	PB4 port of STM32L4R9AII6 is routed to the TRST signal.
R204 SB48	R204 OFF SB48 OFF	Comp2_OUT is routed to pin PB5 of STM32L4R9AII6.
	R204 ON SB48 ON	Default setting: Comp2_OUT is not routed to pin PB4 of STM32L4R9AII6. PB4 port of STM32L4R9AII6 is routed to SAI1_SDB.

6.18.3 Limitations

The OpAmp1 is exclusive to MFX, OCTOSPIP1, and MC operation.

The Comp2 is exclusive to the debugging connector and SAI1.

6.19 Analog input, output, VREF

STM32L4R9AII6 provides an on-board analog-to-digital converter ADC and digital-to-analog converter DAC. The port PA4 is configurable to operate either as ADC input or as DAC output. PA4 is routed to the two-way header (CN4) allowing it to fetch signals to or from PA4 or to ground it by fitting a jumper into CN4.

Parameters of the ADC input low-pass filter formed with R31 and C21 are adjustable by replacing these components according to application requirements. Similarly, the parameters of the DAC output low-pass filter formed with R32 and C21 are modifiable by replacing these components according to application requirements.

The VREF+ terminal of STM32L4R9AII6 is used as the reference voltage for both ADC and DAC. By default, it is routed to VDDA through a jumper installed into the two-way header (CN10). The jumper is removable and an external voltage is applied to terminal 1 of CN10, for specific purposes.

6.20 SRAM device

IS61WV102416BLL, a 16-Mbit static RAM (SRAM), 1 M x 16 bit (U17), is installed on the STM32L4R9I-EVAL main board. The STM32L4R9I-EVAL main board, as well as the addressing capabilities of FMC, allow hosting SRAM devices up to 64 Mbytes. This is the reason why the schematic diagram mentions several SRAM devices.

The SRAM device is attached to the 16-bit data bus and accessed with FMC. The base address is `0x6000 0000`, corresponding to NOR/SRAM1 bank1. The SRAM device is selected with the FMC_NE1 chip selection. FMC_NBL0 and FMC_NBL1 signals allow the selection of 8- and 16-bit data word operating modes.

By removal of R134, a zero-ohm resistor, the SRAM is deselected, and the STM32L4R9AII6 ports PD7, PE0, and PE1 corresponding to FMC_NE1, FMC_NBL0, and FMC_NBL1 signals, respectively, are usable for other application purposes.

Table 15. SRAM chip select configuration

Resistor	Fitting	Configuration
R134	ON	Default setting: SRAM chip select is controlled with FMC_NE1
	OFF	SRAM is deselected. FMC_NE1 is freed for other application purposes.

6.20.1 Limitations

The SRAM addressable space is limited if some or all of the A21 FMC address lines are shunted to the CN12 connector for debug trace purposes. In such a case, pull-down resistors drive the disconnected addressing SRAM inputs. *Section 6.4* provides information on the associated configuration elements.

6.20.2 Operating voltage

The SRAM operating voltage is in the range of 2.4 to 3.6 V.

6.21 NOR flash memory device

M29W128GL70ZA6E, a 128-Mbit NOR flash memory, 8 M x16 bit (U11), is installed on the STM32L4R9I-EVAL main board. The STM32L4R9I-EVAL main board, as well as the addressing capabilities of FMC, allow hosting M29W256GL70ZA6E, a 256-Mbit NOR flash memory device. This is the reason why the schematic diagram mentions both devices.

The NOR flash memory device is attached to the 16-bit data bus and accessed with FMC. The base address is `0x6800 0000`, corresponding to NOR/SRAM2 bank1. The NOR flash memory device is selected with the FMC_NE3 chip select signal. A pull-up resistor connected to the BYTE terminal of the NOR flash memory selects the 16-bit data word Operating mode. The jumper (JP6) is dedicated to the write-protect configuration.

By default, the FMC_NWAIT signal is not routed to the RB port of the NOR flash memory device, and, to know its ready status, its status register is polled by the demo software installed in STM32L4R9I-EVAL. This is modifiable with configuration elements, as shown in *Table 16*.

Table 16. NOR flash memory-related jumper

Jumper	Setting	Configuration
JP6		Default setting: NOR flash memory write is enabled.
		NOR flash memory write is inhibited. Write protect is activated.

6.21.1 Limitations

The addressable space of the NOR flash memory device is limited if any of the A21, A22, or A23 FMC address lines are shunted to the CN12 connector for debug trace purposes.
In such a case, pull-down resistors drive the disconnected addressing NOR inputs. *Section 6.4* provides information on the associated configuration elements.

6.21.2 Operating voltage

The NOR flash memory operating voltage must be in the range of 1.65 to 3.6 V.

6.22 EEPROM

M24128-DFDW6TP, a 128-Kbit I²C-bus EEPROM device (U3), is installed on the STM32L4R9I-EVAL main board. It is accessed with I²C-bus lines I2C2_SCL and I2C2_SDA of STM32L4R9AII6. It supports all I²C-bus modes with speeds up to 1 MHz. The base I²C-bus address is `0xA0`. Write-protecting the EEPROM is possible by opening the SB13 solder bridge. By default, SB13 is ON and writing into the EEPROM enabled.

6.22.1 Operating voltage

The M24128-DFDW6TP EEPROM device's operating voltage must be in the range of 1.7 to 3.6 V.

6.23 EXT_I2C connector

The connection of CN2 EXT_I2C to the I²C bus daughterboard is possible. MFX_GPIO8 of MFX MCU provides the EXT_RSET signal, and the SB12 solder bridge is used to connect the +5 V power supply of the daughterboard.

6.24 Octo-SPI flash memory device

MX25LM51245GXDI00, a 512-Mbit Octo-SPI flash memory device, is installed on the STM32L4R9I-EVAL main board, in the U6 position. It allows evaluating the STM32L4R9AII6 Octo-SPI interface.

MX25LM51245GXDI00 operates in a single transfer rate (STR) mode or a double transfer rate (DTR) mode.

Table 17 shows the configuration elements and their settings allowing them to access the Octo-SPI flash memory device.

Table 17. Configuration elements related to Octo-SPI flash device

Element	Setting	Configuration
R221 R215	R221 in R215 out	Default setting: OCTOSPI1_CLK is available on the Octo-SPI flash memory device.
	R221 out R215 in	OCTOSPI1_CLK is not available on the Octo-SPI flash memory device. PA3 port of STM32L4R9AII6 is routed to the OpAmp1_Vout signal.
R67 SB54	R67 ON SB54 OFF	Default setting: OCTOSPI1_IO6 data line is available to the Octo-SPI flash memory device.
	R67 OFF SB54 ON	OCTOSPI1_IO6 is not available on the Octo-SPI flash memory device. PC3 port of SSTM32L4R9AII6 is routed to the motor-control signal.
R75 SB55	R75 ON SB55 OFF	Default setting: OCTOSPI1_IO7 data line is available to the Octo-SPI flash memory device.
	R75 OFF SB55 ON	OCTOSPI1_IO7 is not available on the Octo-SPI flash memory device. PC4 port of STM32L4R9AII6 is routed to the motor-control signal.

6.24.1 Limitations

Octo-SPI flash memory device operation is exclusive to OpAmp1 and with motor control.

6.24.2 Operating voltage

The voltage of the Octo-SPI flash memory device MX25LM51245GXDI00 is in the range of 2.7 V to 3.6 V.

6.25 Octo-SPI DRAM device

IS66WVH8M8BLL-100BLI, a 64-Mbit self-refresh dynamic RAM (DRAM) device with a HyperBus™ interface, is installed on the STM32L4R9I-EVAL main board, in the U5 position. It allows the evaluation of the STM32L4R9AII6 Octo-SPI interface.

6.25.1 Operating voltage

The voltage of the Octo-SPI DRAM device IS66WVH8M8BLL-100BLI is in the range of 2.7 V to 3.6 V.

6.25.2 Limitations

The board does not support Octo-SPI operations with IS66WVH8M8BLL-100BLI. No workaround is available. Refer to the errata sheet *STM32L4Rxxx and STM32L4Sxxx device errata* (ES0393).

6.26 Touch-sensing button

The STM32L4R9I-EVAL main board supports a touch-sensing button based on either RC charging or the charge-transfer technique. The latter is enabled, by default.

The touch-sensing button is connected to the PC6 port of STM32L4R9AII6 and the related charge capacitor is connected to PC7.

An active shield is designed in layer 2 of the main PCB, under the button footprint. It allows the reduction of disturbances from other circuits to prevent false touch detections.

The active shield is connected to the PB6 port of STM32L4R9AII6 through the resistor R22. The related charge capacitor is connected to PB7.

Table 18 shows the configuration elements related to the touch-sensing function. Some of them serve to enable or disable its operation. However, most of them serve to optimize the touch-sensing performance, by isolating copper tracks to avoid disturbances due to their antenna effect.

Table 18. Touch-sensing-related configuration elements

Element	Setting	Configuration
R44	ON	PC6 port is routed to the CN6 connector of the daughterboard. This setting is not good for the robustness of touch sensing.
	OFF	Default setting: PC6 port is cut from CN6.
SB21	OFF	Default setting: PC6 is not routed to motor control.
	ON	PC6 is routed to motor control. This setting is not good for the robustness of touch sensing.
R46	ON	PC7 port is routed to the CN6 connector of the daughterboard. This setting is not good for the robustness of touch sensing.
	OFF	Default setting: PC7 port is cut from CN6.
SB19	OFF	Default setting: PC7 is not routed to motor control.
	ON	PC7 is routed to motor control. This setting is not good for the robustness of touch sensing.
SB20	OFF	PC7 is not routed to the sampling capacitor. Touch sensing cannot operate.
	ON	Default setting: PC7 is routed to the sampling capacitor. Touch sensing is available.
R26	ON	PB6 port is routed to the CN5 connector of the daughterboard. This setting is not good for the robustness of touch sensing.
	OFF	Default setting: PB6 port is cut from CN5.
SB14	OFF	Default setting: PB6 is not routed to motor control.
	ON	PB6 is routed to motor control. This setting is not good for the robustness of touch sensing.
SB15	OFF	PB6 is not routed to the active shield under the touch-sensing button. This setting is not good for the robustness of touch sensing.

Table 18. Touch-sensing-related configuration elements (continued)

Element	Setting	Configuration
	ON	Default setting: PB6 is routed to the active shield under the touch-sensing button. This setting is not good for the robustness of touch sensing.
SB16	OFF	Default setting: PB6 is not routed to the DSI display connector (CN16).
	ON	PB6 is routed to the DSI display connector (CN16). This setting is not good for the robustness of touch sensing.
R30	ON	PB7 port is routed to the CN5 connector of the daughterboard. This setting is not good for the robustness of touch sensing.
	OFF	Default setting: PB7 port is cut from CN5.
SB17	OFF	Default setting: PB7 is not routed to motor control.
	ON	PB7 is routed to motor control. This setting is not good for the robustness of touch sensing.
SB18	OFF	PB7 is not routed to the sampling capacitor of the active shield under the touch-sensing button. This setting is not good for the robustness of touch sensing.
	ON	Default setting: PB6 is routed to the sampling capacitor of the active shield under the touch-sensing button. This setting is not good for the robustness of touch sensing.

6.26.1 Limitations

The touch-sensing button is exclusive to the DSI display connector, motor control, and daughterboard connector.

6.27 MFX MCU

The MFX MCU is used as MFX (multifunction expander) and IDD measurement.

The MFX circuit on the STM32L4R9I-EVAL main board acts as an IO expander. The communication interface between MFX and STM32L4R9AII6 is the I2C2 bus. The signals connected to MFX are listed in *Table 19*.

Table 19. MFX signals

Pin number of MFX	Pin name of MFX	MFX functions	Function of STM32L4R9AII6	Direction (for MFX)	Terminal device
15	PA5	MFX_GPIO5	uS_Detect	Input	microSD™
16	PA6	MFX_GPIO6	USB _PSON	Output	USB_FS
17	PA7	MFX_GPIO7	USB_OVRCR	Input	USB_FS
18	PB0	MFX_GPIO0	JOY_SEL	Input	Joystick
19	PB1	MFX_GPIO1	JOY_DOWN	Input	Joystick

Table 19. MFX signals (continued)

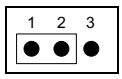
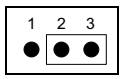
Pin number of MFX	Pin name of MFX	MFX functions	Function of STM32L4R9AII6	Direction (for MFX)	Terminal device
20	PB2	MFX_GPIO2	JOY_LEFT	Input	Joystick
26	PB13	MFX_GPIO13	-	-	-
27	PB14	MFX_GPIO14	-	-	-
28	PB15	MFX_GPIO15	-	-	-
29	PA8	MFX_GPIO8	EXT_RESET	Output	EXT_I2C
30	PA9	MFX_GPIO9	DSI_RST	Output	DSI LCD
31	PA10	MFX_GPIO10	-	-	-
32	PA11	MFX_GPIO11	LCD_DISP	Output	TFT LCD
33	PA12	MFX_GPIO12	LCD_RST	Output	TFT LCD
39	PB3	MFX_GPIO3	JOY_RIGHT	Input	Joystick
40	PB4	MFX_GPIO4	JOY_UP	Input	Joystick

6.28 IDD measurement

STM32L4R9AII6 has a built-in circuit to measure its current consumption (IDD) in Run and Low-power modes, except for Shutdown mode. It is strongly recommended that the MCU supply voltage (VDD_MCU line) does not exceed 3.3 V. This is because there are components on STM32L4R9I-EVAL supplied from 3.3 V that communicate with the MCU through I/O ports. Voltage exceeding 3.3 V on the MCU output port might inject current into 3.3 V-supplied peripheral I/Os and false the MCU current consumption measurement.

Table 20 shows the setting of jumpers associated with the IDD measurement on the main board.

Table 20. IDD measurement-related jumper setting

Jumper	Setting	Configuration
JP4		Default setting: STM32L4R9AII6 has a built-in circuit allowing to measure its current consumption.
		IDD measurement is not available, Bypass mode only for STM32L4R9AII6 VDD_MCU power supply.

6.29 MIPI DSI® display connector

The CN16 connector is designed to connect a DSI display daughterboard. MB1314 daughterboard is available to mount on the STM32L4R9I-EVAL main board. *Table 21* shows the assignment of CN16 and STM32L4R9AII6 terminals.

Table 21. DSI display module connector (CN16)

Pin No.	Description	Pin connection	Pin No.	Description	Pin connection
1	GND	-	2	-	-
3	DSI_CK_P	-	4	DSI_INT	PC2
5	DSI_CK_N	-	6	GND	-
7	GND	-	8	RFU	GND
9	DSI_D0_P	-	10	RFU	GND
11	DSI_D0_N	-	12	GND	-
13	GND	-	14	RFU	GND
15	DSI_D1_P	-	16	RFU	GND
17	DSI_D1_N	-	18	GND	-
19	GND	-	20	-	-
21	BLVDD (5 V)	-	22	SPI_CS	PG12
23	BLVDD (5 V)	-	24	SPI_CLK/UART_CK	PI1/PG13
25	-	-	26	SPI_SDI/UART_TX	PI3/PB6
27	BLGND	-	28	SPI_DCX	PI2
29	BLGND	-	30	-	-
31	-	-	32	-	-
33	-	-	34	-	-
35	SCLK/MCLK	PA8	36	3.3 V	-
37	LRCLK	PB9	38	VDD	-
39	I2S_DATA	PC1	40	I2C_SDA	PH5
41	-	-	42	-	-
43	SWIRE	PG6	44	I2C_SCL	PH4
45	CEC_CLK	NA	46	-	-
47	CEC	NA	48	-	-
49	DSI_TE	PF11	50	-	-
51	-	-	52	-	-
53	DSI_BL_CTRL	PB14	54	-	-
55	-	-	56	-	-
57	DSI_RST	MFX_GPIO9	58	-	-
59	-	-	60	1.8 V	-

6.29.1 Limitations

The DSI display module connector signal INT is used both for TFT LCD and DSI display connectors.

6.30 TFT LCD (RGB and FMC mode) connector

The 50-pin 1.27 mm-pitch female connector (CN20) is designed to connect the TFT LCD daughterboard, supporting RGB and FMC modes. MB1315 daughterboard is available to mount on the STM32L4R9I-EVAL main board with RGB mode. *Table 22* shows the assignment of CN20 and STM32L4R9AII6 terminals.

Table 22. TFT LCD module connector (CN20)

Pin No.	RGB mode description	FMC mode description	Pin connection	Pin No.	RGB mode description	FMC mode description	Pin connection
1	GND	GND	-	2	GND	GND	-
3	R0	-	PE2	4	G0	-	PF14
5	R1	RS(A19)	PE3	6	G1	-	PF15
7	R2	D12	PE15	8	G2	D6	PE9
9	R3	D13	PD8	10	G3	D7	PE10
11	R4	D14	PD9	12	G4	D8	PE11
13	R5	D15	PD10	14	G5	D9	PE12
15	R6	-	PD11	16	G6	D10	PE13
17	R7	-	PD12	18	G7	D11	PE14
19	GND	GND	-	20	GND	GND	-
21	B0	-	PE4	22	DE	TE	PF11
23	B1	-	PF13	24	LCD_DSIP	-	MFX_ GPIO11
25	B2	D0	PD14	26	HSYNC	-	PE0
27	B3	D1	PD15	28	VSYNC	-	PE1
29	B4	D2	PD0	30	GND	GND	-
31	B5	D3	PD1	32	PCLK	-	PD3
33	B6	D4	PE7	34	GND	GND	-
35	B7	D5	PE8	36	RST#	RST#	MFX_ GPIO12
37	GND	GND	-	38	SDA	SDA	PH5
39	INT	INT	PC2	40	SCL	SCL	PH4
41	-	RS	PE2	42	-	NOE	PD4
43	BL_CTRL	BL_CTRL	PA5	44	-	NWE	PD5
45	BL+5 V	BL+5 V	-	46	-	CS	PG12

Table 22. TFT LCD module connector (CN20) (continued)

Pin No.	RGB mode description	FMC mode description	Pin connection	Pin No.	RGB mode description	FMC mode description	Pin connection
47	BLGND	BLGND	-	48	VDD	VDD	-
49	BLGND	BLGND	-	50	+3.3 V	+3.3 V	-

6.30.1 Limitations

The TFT LCD module connector supports RGB mode or FMC mode only at the same time. The signal INT is used both for TFT LCD and DSI display connectors. When RGB mode TFT LCD is used, STM32L4R9AII6 cannot access the on-board SRAM and NOR flash memory.

6.31 Pmod™ connector

The Pmod™-standard connector (P1) is available on the STM32L4R9I-EVAL main board to support flexibility in small form factor applications. The Pmod™ connector implements the Pmod™ type 2A and 4A on the STM32L4R9I-EVAL main board.

Table 23. Pmod™ connector (P1)

Pin number	Description	Pin number	Description
1	SS/CTS (PI0/PB13)	7	INT (PG13)
2	MOSI/TXD (PI3/PG7)	8	RESET (PB14)
3	MISO/RXD (PI2/PG8)	9	-
4	SCK/RTS (PI1/PB12)	10	-
5	GND	11	GND
6	3.3 V	12	3.3 V

6.32 MB1314 DSI display daughterboard

MB1314 is the DSI display daughterboard that is available to mount on the STM32L4R9I-EVAL main board via the CN1 connector. GVO IEG1120TB103GF-001 is selected for round LCD with one data lane, 390x390 resolution, 24 bpp with capacitive touch panel (FocalTech FT3x67 driver). *Table 24* shows the pin function description of the MB1314 daughterboard CN1 connector.

Table 24. Pin function description of the MB1314 daughterboard connector (CN1)

Pin number	Description	Pin number	Description
1	GND	2	-
3	DSI_CK_P	4	DSI_INT
5	DSI_CK_N	6	GND
7	GND	8	RFU

Table 24. Pin function description of the MB1314 daughterboard connector (CN1)

Pin number	Description	Pin number	Description
9	DSI_D0_P	10	RFU
11	DSI_D0_N	12	GND
13	GND	14	RFU
15	RFU	16	RFU
17	RFU	18	GND
19	GND	20	-
21	BLVDD (5 V)	22	RFU
23	BLVDD (5 V)	24	RFU
25	-	26	RFU
27	BLGND	28	RFU
29	BLGND	30	-
31	-	32	-
33	-	34	-
35	RFU	36	3.3 V
37	RFU	38	VDD
39	RFU	40	I2C_SDA
41	-	42	-
43	SWIRE	44	I2C_SCL
45	RFU	46	-
47	RFU	48	-
49	DSI_TE	50	-
51	-	52	-
53	DSI_BL_CTRL	54	-
55	-	56	-
57	DSI_RST	58	-
59	-	60	RFU

Warning: Permanent image sticking might occur if AMOLED displays the same image for an extended time.

6.33 MB1315 TFT LCD daughterboard

MB1315 is the TFT LCD daughterboard supporting RGB mode, available to mount on the STM32L4R9I-EVAL main board via the CN1 connector.

The 4.3” TFT LCD uses LCD RK043FN48H-CT672B with a capacitive touch panel, which only supports 3.3 V power and interface. So, a level shifter SN74LVC16T245DGGR is requested on the TFT RGB LCD daughterboard to support a wide power supply range. *Table 25* shows the pin function description of the MB1315 daughterboard connector (CN1).

Table 25. Pin function description of the MB1315 daughterboard connector (CN1)

Pin number	Description	Pin number	Description
1	GND	2	GND
3	R0	4	G0
5	R1	6	G1
7	R2	8	G2
9	R3	10	G3
11	R4	12	G4
13	R5	14	G5
15	R6	16	G6
17	R7	18	G7
19	GND	20	GND
21	B0	22	DE
23	B1	24	LCD_DSIP
25	B2	26	HSYNC
27	B3	28	VSYNC
29	B4	30	GND
31	B5	32	PCLK
33	B6	34	GND
35	B7	36	RST#
37	GND	38	SDA
39	INT	40	SCL
41	-	42	-
43	BL_CTRL	44	-
45	BL+5 V	46	-
47	BLGND	48	VDD
49	BLGND	50	+3.3 V

7 Connectors

7.1 Motor-control connector (CN1)

Figure 11. Motor-control connector (CN1) top view

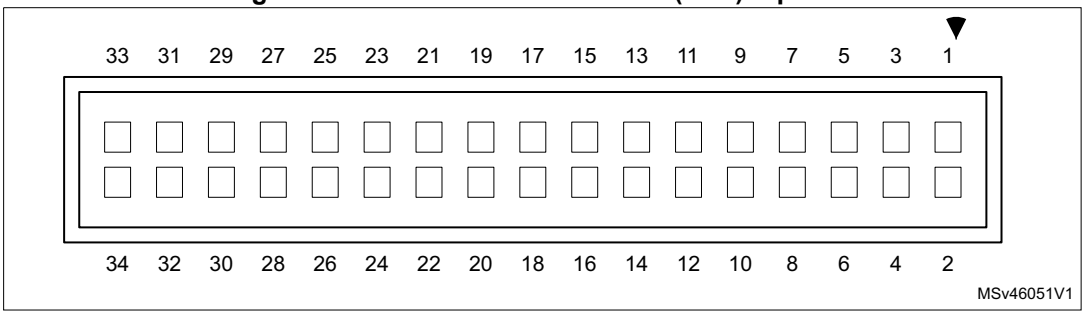


Table 26. Motor-control connector (CN1)

Description	STM32L4R9AII6 pin	CN1 pin number	CN1 pin number	STM32L4R9AII6 pin	Description
Emergency STOP	PI4	1	2	-	GND
PWM_1H	PC6	3	4	-	GND
PWM_1L	PH13	5	6	-	GND
PWM_2H	PC7	7	8	-	GND
PWM_2L	PH14	9	10	-	GND
PWM_3H	PC8	11	12	-	GND
PWM_3L	PH15	13	14	PC4	BUS VOLTAGE
CURRENT A	PC0	15	16	-	GND
CURRENT B	PC1	17	18	-	GND
CURRENT C	PC2	19	20	-	GND
ICL Shutout	PG9	21	22	-	GND
DISSIPATIVE BRAKE	PG13	23	24	PA0	PCD Ind. Current
+5 V power	-	25	26	PA1	Heatsink temperature
PFC SYNC	PB14	27	28	-	3.3 V power
PFC PWM	PB15	29	30	PA9	PFC Shut Down
Encoder A	PB6	31	32	PC3	PFC Vac
Encoder B	PB7	33	34	PB8	Encoder Index

7.2 External I²C connector (CN2)

Figure 12. EXT_I2C connector (CN2) front view

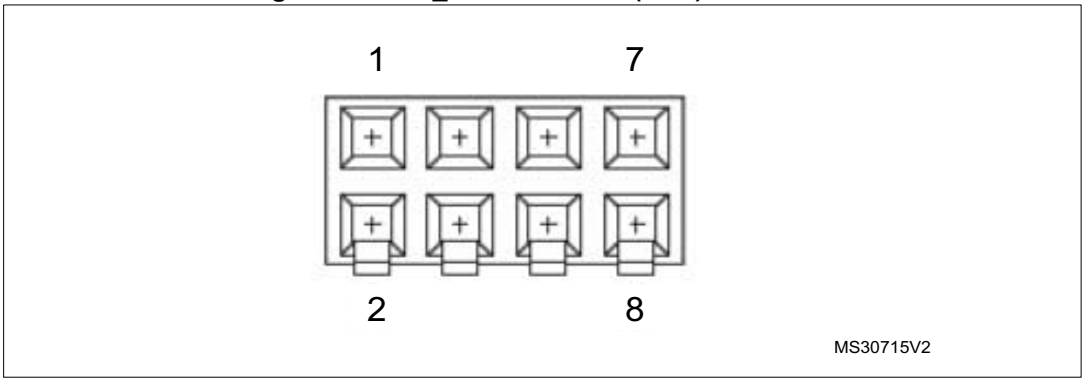


Table 27. EXT_I2C connector (CN2)

Pin number	Description	Pin number	Description
1	I2C1_SDA (PH5)	5	VDD
2	NC	6	NC
3	I2C_SCL (PH4)	7	GND
4	EXT_RESET (MFX_GPIO8)	8	NC

7.3 USB OTG FS Micro-AB connector (CN3)

Figure 13. USB OTG FS Micro-AB connector (CN3) front view

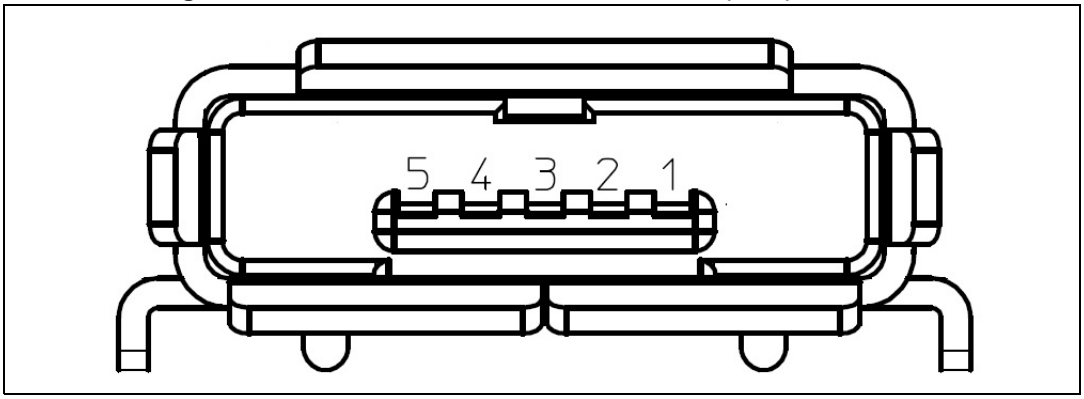


Table 28. USB OTG FS Micro-AB connector (CN3)

Pin number	Description	Pin number	Description
1	V_{BUS} (PA9)	4	ID (PA10)
2	DM (PA11)	5	GND
3	DP (PA12)	-	-

7.4 Analog input-output connector (CN4)

Figure 14. Analog input-output connector (CN4) top view

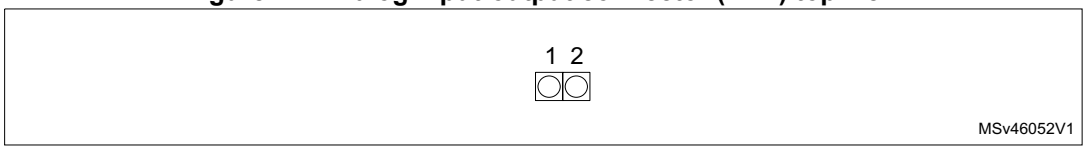


Table 29. Analog input-output connector (CN4)

Pin number	Description	Pin number	Description
1	GND	2	Analog input-output PA4

7.5 Extension connectors (CN5, CN6, CN13, and CN14)

All GPIO signals from STM32L4R9AII6 are connected to extension connectors (CN5, CN6, CN13, and CN14). CN13 and CN14 extension connectors are also used for the FMC device.

Table 30. Daughterboard extension connector (CN5)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PH9	OCTOSPI2_IO4	U5 removed
3	PH14	LED3, MC	R185 and SB44 OFF
5	PH15	LED4, MC	R184 and SB45 OFF
7	PI3	SPI2_MOSI	No connection for CN16 and P1
9	GND	-	-
11	PH13	LED2, MC	R186 and SB46 OFF
13	PG13	PMOD_INT, USART1_CK, MC	SB29 and SB47 OFF and no connection for P1
15	PB5	SAI1_SDB, Comp2_OUT	R204 and SB48 OFF
17	PI9	OCTOSPI2_IO2	U5 removed
19	PI11	OCTOSPI2_IO0	U5 removed
21	NC	-	-
23	PC14	OSC32_IN	R50 OFF, SB50 ON
25	PC13	Wakeup	R188 OFF
27	PH1	OSC_OUT	R65 OFF, SB53 ON
29	GND	-	-
31	PA5	TFT LCD_BL_CTRL	No connection for CN20
33	PC2	DSI LCD_INT, TFT LCD_INT, MC	R217 and SB43 OFF

Table 30. Daughterboard extension connector (CN5) (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
35	PH8	OCTOSPI2_IO3	U5 removed
37	PH10	OCTOSPI2_IO5	U5 removed
39	D5V	-	-
2	PI5	OCTOSPI2_NCS	U5 removed
4	PH12	OCTOSPI2_IO7	U5 removed
6	PI6	OCTOSPI2_CLK	U5 removed
8	PG15	OCTOSPI2_DQS	U5 removed
10	GND	-	-
12	PB4	Comp2_INP, TRST	R200 and SB22 OFF
14	PB6	TS_SHIELD, USART1_TX, MC	R26 ON SB14, SB16, and SB15 OFF
16	PB7	TS_SHIELD_CS, MC	R30 ON SB17 and SB18 OFF
18	PI10	OCTOSPI2_IO1	U5 removed
20	PI7	-	-
22	PH3	BOOT0	R1 OFF
24	PC15	OSC32_OUT	R49 OFF, SB49 ON
26	PH0	OSC_IN	R61 OFF, SB52 ON
28	PA0	MFX_IRQ_OUT, OpAmp1_INP, MC	R214, SB38, and SB39 OFF
30	GND	-	-
32	PA1	OpAmp1_INM, MC	R216 and SB40 OFF
34	PA4	ADC_DAC	R32 OFF
36	PH11	OCTOSPI2_IO6	U5 removed
38	VDD	-	-
40	+3V3	-	-

Table 31. Daughterboard extension connector (CN6)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PH2	OCTOSPI1_IO4	U6 removed
3	PI0	SPI2_NSS	No connection for P1
5	PD2	SDIO1_CMD	R55 OFF and no SD card inserted
7	PI1	SPI2_SCK	No connection for CN16 and P1
9	GND	-	-

Table 31. Daughterboard extension connector (CN6) (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
11	PA12	USB OTG_DP	No connection for CN3
13	PA11	USB OTG_DM	No connection for CN3
15	PG8	LPUART1_RX	U9 removed
17	PA9	VBUS_FS, MC	R203 and SB35 OFF
19	PC9	SDIO1_D1, Trace_D0	R205 and SB57 OFF
21	PC7	TS_KEY_CS, MC	R46 ON, SB19 and SB20 OFF
23	PB15	LED1, MC	R187 and SB51 OFF
25	PB13	LPUART1_CTS	U9 removed
27	RESET#	-	-
29	GND	-	-
31	PA3	OpAmp1_VOUT, OCTOSPI1_CLK	R221 and R215 OFF
33	PA7	OCTOSPI1_IO2	U6 removed
35	PC4	OCTOSPI1_IO7, MC	R75 and SB55 OFF
37	PC3	OCTOSPI1_IO6, MC	R67 and SB54 OFF
39	D5V	-	-
2	PG11	OCTOSPI1_IO5	U6 removed
4	PI2	SPI2_MISO	No connection for CN16 and P1
6	PC8	SDIO1_D0, MC	R195 and SB2 OFF
8	PC10	SDIO1_D2, Trace_D1	R197 and SB58 OFF
10	GND	-	-
12	PC11	SDIO1_D3	R60 OFF and no SD card inserted
14	PC12	SDIO1_CLK	No SD card inserted
16	PA10	USB OTG_ID	No connection for CN3
18	PC6	TS_KEY, MC	R44 ON, SB21 OFF
20	PG7	LPUART1_TX	R19 OFF and U1 removed
22	PB14	DSI LCD_BL_CTRL, PMOD_RST, MC	R207 and SB41 OFF and no connection for P1
24	PB12	LPUART1_RTS	R5 OFF and U1 removed
26	PF11	DSI LCD_TE, TFT LCD_DE	No connection for CN16 and CN20
28	PB0	OCTOSPI1_IO1	U6 removed
30	GND	-	-
32	PB1	OCTOSPI1_IO0	U6 removed
34	PB2	OCTOSPI1_DQS	U6 removed

Table 31. Daughterboard extension connector (CN6) (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
36	PA6	OCTOSPI1_IO3	U6 removed
38	PA2	OCTOSPI1_NCS	U6 removed
40	+5V	-	-

Table 32. Daughterboard extension connector (CN13)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PD1	FMC_D3	-
3	PD0	FMC_D2	-
5	PB8	SAI1_MCLKA, CAN_RX, MC	R235, SB42, and JP12 OFF
7	PG10	FMC_NE3	-
9	GND	-	-
11	PE0	FMC_NBL0	-
13	PG12	FMC_NE4, SPI	R238 and SB26 OFF
15	PE4	FMC_A20	-
17	PE5	FMC_A21	Keep CN12 OFF
19	PF1	FMC_A1	-
21	PF2	FMC_A2	-
23	PB9	SAI1_FSA, CAN_TX	R243 and R247 OFF
25	PF10	DFSDM_CLK	JP16 OFF
27	PF5	FMC_A5	-
29	GND	-	-
31	PF4	FMC_A4	-
33	PF15	FMC_A9	-
35	PG0	FMC_A10	-
37	PE10	FMC_D7	-
39	VDD	-	-
2	NC	-	-
4	PD6	FMC_NWAIT	-
6	PD4	FMC_NOE	-
8	PE1	FMC_NBL1	-
10	GND	-	-
12	PD5	FMC_NWE	-
14	PE2	FMC_A23	Keep CN12 OFF

Table 32. Daughterboard extension connector (CN13) (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
16	PE3	FMC_A19	-
18	PE6	FMC_A22	Keep CN12 OFF
20	PF0	FMC_A0	-
22	PC0	DFSDM, MC	R242 and SB36 OFF
24	PC1	SAI1, MC	R244 and SB37 OFF
26	PF3	FMC_A3	-
28	PG4	FMC_A14	-
30	GND	-	-
32	PG1	FMC_A11	-
34	PF12	FMC_A6	-
36	PF13	FMC_A7	-
38	PF14	FMC_A8	-
40	+3V3	-	-

Table 33. Daughterboard extension connector (CN14)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
1	PA14	JTAG_TCK/SWCLK	Do not use CN11, CN12, CN15, and CN17 for debug connector.
3	PD7	FMC_NE1	-
5	PD3	TFT LCD_CLK	No connection for CN20
7	PB3	JTAG_TDO/SWO	Do not use CN11, CN12, CN15, and CN17 for debug connector.
9	GND	-	-
11	PG5	FMC_A15	-
13	PD15	FMC_D1	-
15	PD14	FMC_D0	-
17	PD10	FMC_D15	-
19	PH5	I2C2_SDA	R2 OFF
21	PB10	UART3_TX	R173 OFF and no connection for CN11
23	PD8	FMC_D13	-
25	PD13	FMC_A18	-
27	PE12	FMC_D9	-
29	GND	-	-
31	NC	-	-

Table 33. Daughterboard extension connector (CN14) (continued)

Pin number	Description	Alternative functions	How to disconnect alternative functions to use on the extension connector
33	PE7	FMC_D4	-
35	PE14	FMC_D11	-
37	PE15	FMC_D12	-
39	VDD	-	-
2	PA13	JTAG_TMS/SWDIO	Do not use CN11, CN12, CN15, and CN17 for debug connector.
4	PA15	JTAG_TDI	Do not use CN11, CN12, CN15, and CN17 for debug connector.
6	PI4	Audio_INT, MC	R234 and SB3 OFF
8	PG9	MFX_WAKUP, MC	R236 and SB34 OFF
10	GND	-	-
12	PA8	SAI1_SCKA	U26 removed
14	PG3	FMC_A13	-
16	PG6	DSI LCD_SWIRE	No connection for CN16
18	PG2	FMC_A12	-
20	PD11	FMC_A16	-
22	PH4	I2C2_SCL	R3 OFF
24	PB11	UART3_RX	R171 OFF and no connection for CN11
26	PD9	FMC_D14	-
28	PD12	FMC_A17	-
30	GND	-	-
32	PE13	FMC_D10	-
34	PE8	FMC_D5	-
36	PE11	FMC_D8	-
38	PE9	FMC_D6	-
40	+3V3	-	-

7.6 RS232 connector (CN7)

Figure 15. RS232 D-sub male connector (CN7) front view

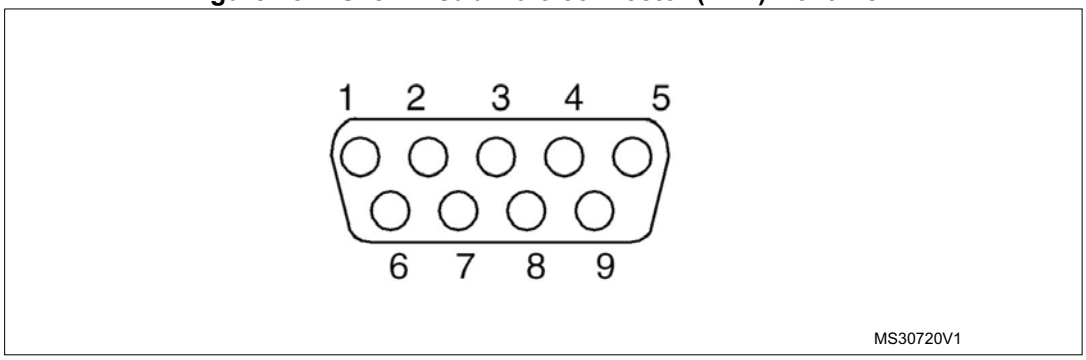


Table 34. RS232 D-sub male connector (CN7)

Pin number	Description	Pin number	Description
1	NC	6	NC
2	RS232_RX (PG8)	7	RS232_RTS (PB12)
3	RS232_TX (PG7)	8	RS232_CTS (PB13)
4	NC	9	NC
5	GND	-	-

7.7 microSD™ connector (CN8)

Figure 16. microSD™ connector (CN8) top view

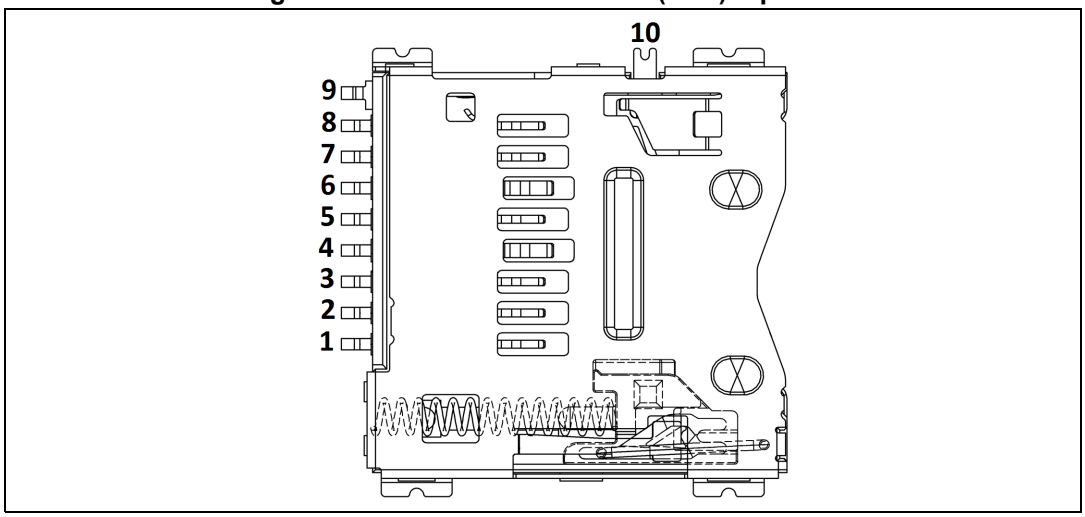


Table 35. microSD™ connector (CN8)

Pin number	Description	Pin number	Description
1	SDIO_D2 (PC10)	6	Vss/GND
2	SDIO_D3 (PC11)	7	SDIO_D0 (PC8)
3	SDIO_CMD (PD2)	8	SDIO_D1 (PC9)
4	VDD	9	GND
5	SDIO_CLK (PC12)	10	MicroSDcard_detect (MFX GPIO15)

7.8 MFX programming connector (CN9)

The CN9 connector is used only for embedded MFX (multifunction expander) programming during board manufacturing. It is not populated by default and is not for the end user.

7.9 STDC14 connector (CN11)

Figure 17. STDC14 debugging connector (CN11) top view

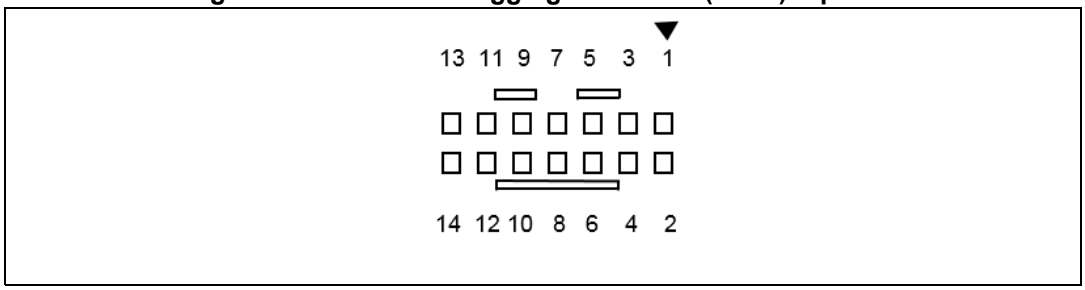


Table 36. STDC14 debugging connector (CN11)

Terminal	Function / MCU port	Terminal	Function / MCU port
1	-	2	-
3	VDD	4	SWDIO/TMS (PA13)
5	GND	6	SWDCLK/TCK (PA14)
7	GND	8	SWO/TDO (PB3)
9	KEY	10	TDI (PA15)
11	GND	12	RESET#
13	VCP_RX (PB11)(1)	14	VCP_TX (PB10)(1)

1. Due to discrepancies between the port terminal and sheet symbol, VCP_RX and VCP_TX are not connected to MCU.

7.10 Trace debugging connector (CN12)

Figure 18. ETM trace debugging connector (CN12) top view

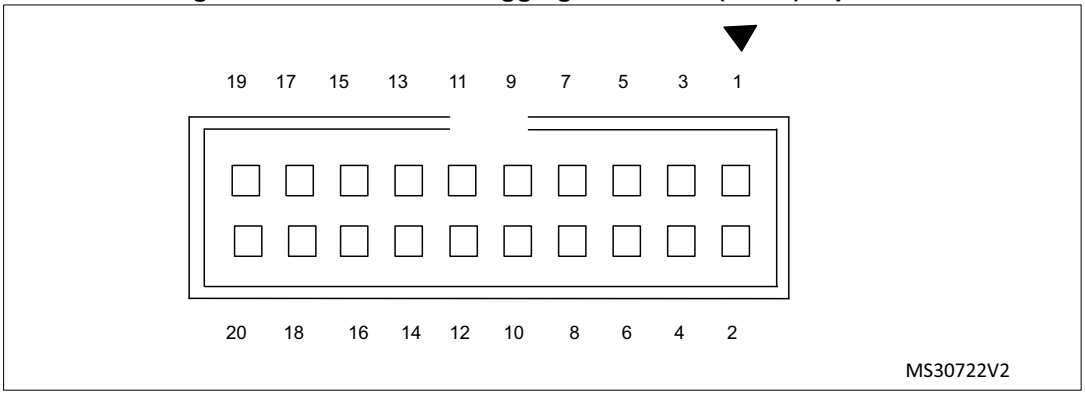


Table 37. Trace debugging connector (CN12)

Pin number	Description	Pin number	Description
1	+3.3 V	2	TMS/PA13
3	GND	4	TCK/PA14
5	GND	6	TDO/PB3
7	KEY	8	TDI/PA15
9	GND	10	RESET#
11	GND	12	Trace_CLK/PE2
13	GND	14	Trace_D0/PC9 or SWO/PB3
15	GND	16	Trace_D1/PC10 or nTRST/PB4
17	GND	18	Trace_D2/PE5
19	GND	20	Trace_D3/PE6

7.11 TAG connector (CN15)

Table 38. TAG debugging connector (CN15)

Terminal	Function / MCU port	Terminal	Function / MCU port
1	VDD	2	SWDIO/TMS (PA13)
3	GND	4	SWDCLK/TCK (PA14)
5	GND	6	SWO/TDO (PB3)
7	NC	8	TDI (PA15)
9	TRST (PB4)	10	RESET#

7.12 MIPI DSI® display connector (CN16)

A TFT color LCD with the MIPI DSI® interface daughterboard is mounted on the CN16 connector. Refer to *Section 6.29* for detail.

7.13 JTAG connector (CN17)

Figure 19. JTAG/SWD debugging connector (CN17) top view

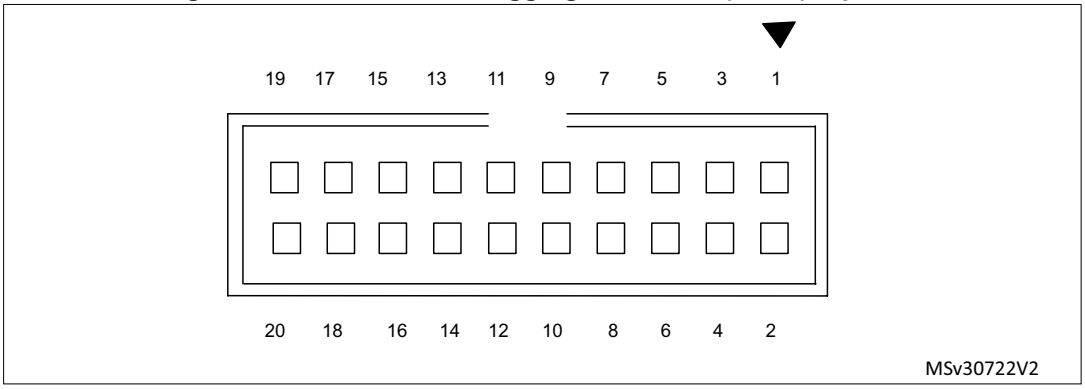


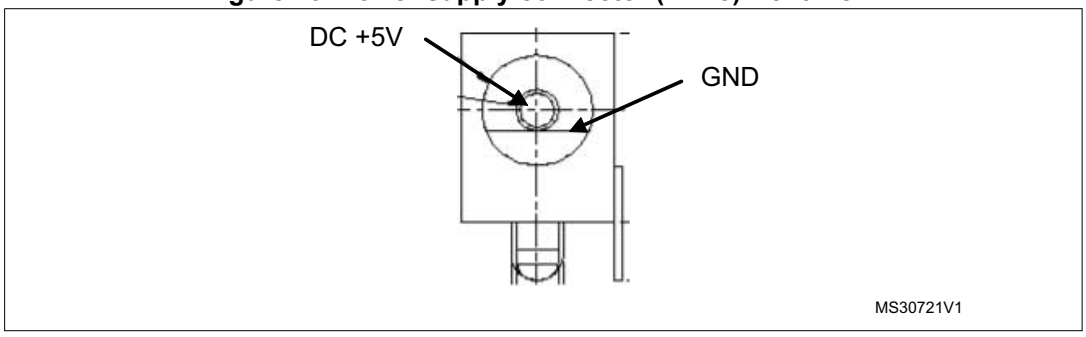
Table 39. JTAG/SWD debugging connector (CN17)

Pin number	Description	Pin number	Description
1	VDD power	2	VDD power
3	PB4	4	GND
5	PA15	6	GND
7	PA13	8	GND
9	PA14	10	GND
11	NC	12	GND
13	PB3	14	GND
15	RESET#	16	GND
17	-	18	GND
19	-	20	GND

7.14 Power connector (CN18)

The STM32L4R9I-EVAL main board is power-able with a DC 5 V power supply via the external power supply socket (CN18) shown in *Figure 20*. The central pin of CN18 must be positive.

Figure 20. Power supply connector (CN18) front view



7.15 ST-LINK/V2-1 programming connector (CN19)

The CN19 connector is used only for embedded ST-LINK/V2-1 programming during board manufacturing. It is not populated by default and is not for end-users.

7.16 RGB TFT LCD connector (CN20)

A TFT-color LCD daughterboard is mounted on the CN20 connector. Refer to *Section 6.30* for details.

7.17 ST-LINK/V2-1 USB Micro-B connector (CN21)

The USB connector (CN21) is used to connect the on-board ST-LINK/V2-1 facility to a PC for programming and debugging purposes.

Figure 21. USB Micro-B connector (CN21) front view

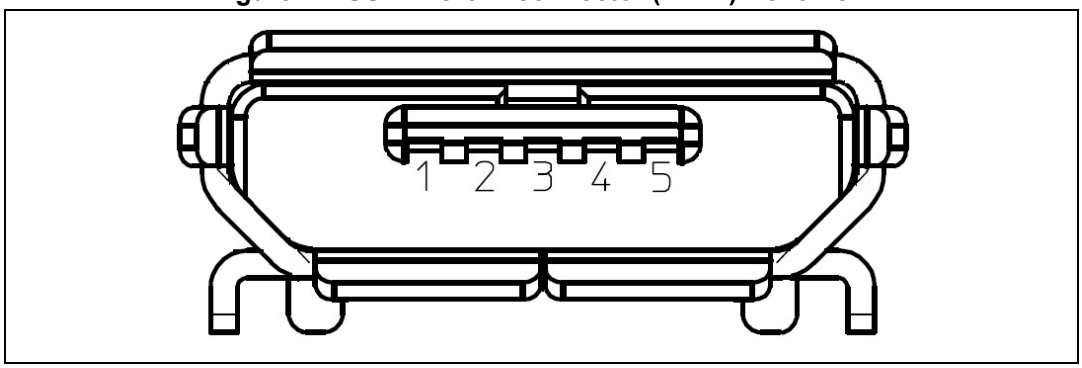


Table 40. USB Micro-B connector (CN21) front view

Pin number	Description	Pin number	Description
1	V_{BUS} (power)	4	GND
2	DM	5	Shield
3	DP	-	-

7.18 CAN D-type male connector (CN22)

Figure 22. CAN D-type 9-pin male connector (CN22) front view

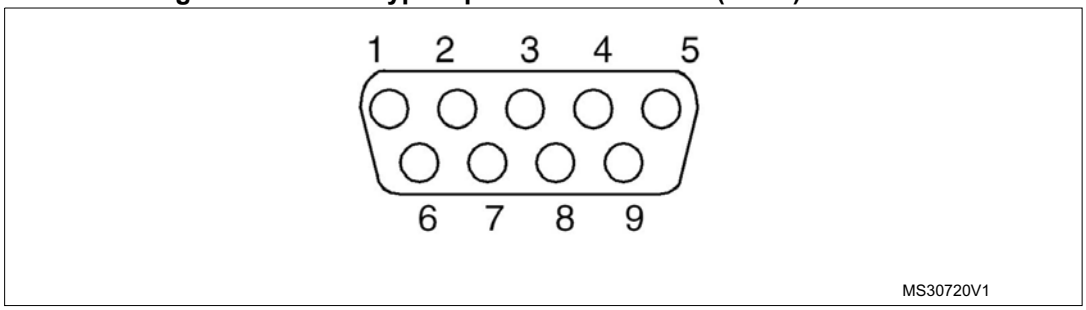


Table 41. CAN D-type 9-pin male connector (CN22)

Pin number	Description	Pin number	Description
1,4,8,9	NC	7	CANH
2	CANL	3,5,6	GND

8 I/O assignment

Table 42. STM32L4R9I-EVAL I/O assignment

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
1	K12	DSI_CKN	-	-	-
2	K11	DSI_CKP	-	-	-
3	L12	DSI_D0N	-	-	-
4	L11	DSI_D0P	-	-	-
5	J12	DSI_D1N	-	-	-
6	J11	DSI_D1P	-	-	-
7	L13	VCAPDSI	-	-	-
8	[L13]	VDD12DSI	-	-	-
9	[L13]	VDD12DSI	-	-	-
10	J13	VSSDSI	-	-	-
11	K13	VSSDSI	-	-	-
12	H3	NRST	NRST	-	-
13	K3	PA0	OPAMP1_VINP || MFX_IRQ_OUT	-	PFC indirect current
14	M1	PA1	OPAMP1_VINM	-	Heatsink Temp.
15	N1	PA2	OCTOSPIP1_NCS	-	-
16	M2	PA3	OCTOSPIP1_ CLK || OPAMP1_VOUT	-	-
17	N2	PA4	ADC/DAC	-	-
18	L3	PA5	LCD_BL_CTRL	-	-
19	L4	PA6	OCTOSPIP1_IO3	-	-
20	M4	PA7	OCTOSPIP1_IO2	-	-
21	E11	PA8	SAI1_SCK_A	-	-
22	E12	PA9	OTG_FS_VBUS	-	PFC shutdown
23	D11	PA10	OTG_FS_ID	-	-
24	E13	PA11	OTG_FS_DM	-	-
25	D13	PA12	OTG_FS_DP	-	-
26	A11	PA13	JTMS/SWDIO	-	-
27	A10	PA14	JTCK/SWCLK	-	-
28	A9	PA15	JTDI	-	-
29	N4	PB0	OCTOSPIP1_IO1	-	-
30	L5	PB1	OCTOSPIP1_IO0	-	-
31	N5	PB2	OCTOSPIP1_DQS	-	-

Table 42. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
32	A6	PB3	JTDO/TRACESWO	-	-
33	A5	PB4	NJTRST || COMP2_INP	-	-
34	B5	PB5	SAI1_SD_B || COMP2_OUT	-	-
35	C5	PB6	TSC_G2_IO3 || USART1_TX	-	Encoder A
36	D5	PB7	TSC_G2_IO4	-	Encoder B
37	C4	PB8	SAI1_MCLK_A || CAN1_RX	-	Encoder Index
38	D4	PB9	SAI1_FS_A || CAN1_TX	-	-
39	N9	PB10	UART3_TX	-	-
40	H7	PB11	UART3_RX	-	-
41	N12	PB12	LPUART1_RTS_DE	-	-
42	N13	PB13	LPUART1_CTS	-	-
43	M12	PB14	PMOD_RST/DSI_BL_CTRL	-	PFC sync
44	L10	PB15	LED1	-	PFC PWM
45	J2	PC0	DFSDM1_DATIN4	-	PhaseA Current+
46	J3	PC1	SAI1_SD_A	-	PhaseB Current+
47	J4	PC2	LCD_INT	-	PhaseC Current+
48	K1	PC3	OCTOSPIP1_IO6	-	PFC Vac
49	K4	PC4	OCTOSPIP1_IO7	-	Bus Voltage
50	F11	PC6	TSC_G4_IO1	-	MC_PWM_1H
51	G11	PC7	TSC_G4_IO2	-	MC_PWM_2H
52	F9	PC8	uSD1_D0	-	MC_PWM_3H
53	G13	PC9	uSD1_D1 || TRACED0	-	-
54	D9	PC10	uSD1_D2 || TRACED1	-	-
55	E9	PC11	uSD1_D3	-	-
56	F8	PC12	uSD1_CK	-	-
57	E1	PC13	TAMP1/WKUP2	-	-
58	F1	PC14-OSC32_IN	OSC32_IN	-	-
59	G1	PC15-OSC32_OUT	OSC32_OUT	-	-
60	B8	PD0	FMC_D2	LCD_B4	-
61	C8	PD1	FMC_D3	LCD_B5	-
62	D8	PD2	uSD1_CMD	-	-
63	E8	PD3	-	LCD_CLK	-
64	C7	PD4	FMC_NOE	LCD_NOE	-

Table 42. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
65	D7	PD5	FMC_NWE	LCD_NWE	-
66	E7	PD6	FMC_NWAIT	LCD_DE	-
67	F7	PD7	FMC_NE1	-	-
68	K10	PD8	FMC_D13	LCD_R3	-
69	K9	PD9	FMC_D14	LCD_R4	-
70	J10	PD10	FMC_D15	LCD_R5	-
71	J9	PD11	FMC_A16	LCD_R6	-
72	J8	PD12	FMC_A17	LCD_R7	-
73	H8	PD13	FMC_A18	-	-
74	H11	PD14	FMC_D0	LCD_B2	-
75	H10	PD15	FMC_D1	LCD_B3	-
76	A4	PE0	FMC_NBL0	LCD_HSYNC	-
77	B4	PE1	FMC_NBL1	LCD_VSYNC	-
78	D3	PE2	FMC_A23 || TRACECK	LCD_R0	-
79	D2	PE3	FMC_A19	LCD_R1	-
80	D1	PE4	FMC_A20	LCD_B0	-
81	E4	PE5	FMC_A21 || TRACED2	-	-
82	E3	PE6	FMC_A22 || TRACED3	-	-
83	L7	PE7	FMC_D4	LCD_B6	-
84	K6	PE8	FMC_D5	LCD_B7	-
85	J6	PE9	FMC_D6	LCD_G2	-
86	H6	PE10	FMC_D7	LCD_G3	-
87	N8	PE11	FMC_D8	LCD_G4	-
88	M8	PE12	FMC_D9	LCD_G5	-
89	L8	PE13	FMC_D10	LCD_G6	-
90	K7	PE14	FMC_D11	LCD_G7	-
91	J7	PE15	FMC_D12	LCD_R2	-
92	F5	PF0	FMC_A0	-	-
93	F4	PF1	FMC_A1	-	-
94	F3	PF2	FMC_A2	-	-
95	G3	PF3	FMC_A3	-	-
96	G4	PF4	FMC_A4	-	-
97	G5	PF5	FMC_A5	-	-
98	H4	PF10	DFSDM1_CKOUT	-	-

Table 42. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
99	M5	PF11	DSI_TE/LCD_DE	-	-
100	N6	PF12	FMC_A6	-	-
101	M6	PF13	FMC_A7	LCD_B1	-
102	L6	PF14	FMC_A8	LCD_G0	-
103	K5	PF15	FMC_A9	LCD_G1	-
104	J5	PG0	FMC_A10	-	-
105	H5	PG1	FMC_A11	-	-
106	H9	PG2	FMC_A12	-	-
107	G8	PG3	FMC_A13	-	-
108	G7	PG4	FMC_A14	-	-
109	G9	PG5	FMC_A15	-	-
110	G12	PG6	SWIRE	-	-
111	G10	PG7	LPUART1_TX	-	-
112	F10	PG8	LPUART1_RX	-	-
113	B7	PG9	MFX_WAKEUP	-	ICL shutout
114	D6	PG10	FMC_NE3	-	-
115	E6	PG11	OCTOSPIP1_IO5	-	-
116	F6	PG12	SPI_CS	LCD_NE4	-
117	G6	PG13	PMOD_INT/ USART1_CK	-	Dissipative Brake
118	C6	PG15	OCTOSPIP2_DQS	-	-
119	H1	PH0-OSC_IN	OSC_IN	-	-
120	J1	PH1-OSC_OUT	OSC_OUT	-	-
121	A2	PH2	OCTOSPIP1_IO4	-	-
122	E5	PH3-BOOT0	-	-	-
123	K8	PH4	I2C2_SCL	-	-
124	L9	PH5	I2C2_SDA	-	-
125	N10	PH8	OCTOSPIP2_IO3	-	-
126	C11	PH9	OCTOSPIP2_IO4	-	-
127	M9	PH10	OCTOSPIP2_IO5	-	-
128	M10	PH11	OCTOSPIP2_IO6	-	-
129	B13	PH12	OCTOSPIP2_IO7	-	-
130	C9	PH13	LED2	-	MC_PWM_1L
131	A13	PH14	LED3	-	MC_PWM_2L
132	B12	PH15	LED4	-	MC_PWM_3L

Table 42. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
133	A12	PI0	SPI2_NSS	-	-
134	B11	PI1	SPI2_SCK	-	-
135	B10	PI2	SPI2_MISO	-	-
136	C10	PI3	SPI2_MOSI	-	-
137	D10	PI4	Audio_INT	-	MC_EmergencySTOP
138	E10	PI5	OCTOSPIP2_NCS	-	-
139	B9	PI6	OCTOSPIP2_CLK	-	-
140	B2	PI7	-	-	-
141	B1	PI9	OCTOSPIP2_IO2	-	-
142	A1	PI10	OCTOSPIP2_IO1	-	-
143	C3	PI11	OCTOSPIP2_IO0	-	-
144	E2	VBAT	-	-	-
145	N11	VDD	-	-	-
146	H13	VDD	-	-	-
147	C1	VDD	-	-	-
148	A3	VDD	-	-	-
149	C13	VDD	-	-	-
150	N3	VDD	-	-	-
151	G2	VDD	-	-	-
152	N7	VDD	-	-	-
153	A8	VDD	-	-	-
154	M13	VDDDSI	-	-	-
155	L2	VDDA	-	-	-
156	F12	VDDIO2	-	-	-
157	B6	VDDIO2	-	-	-
158	D12	VDDUSB	-	-	-
159	L1	VREF+	-	-	-
160	K2	VREF-	-	-	-
161	A7	VSS	-	-	-
162	C2	VSS	-	-	-
163	H12	VSS	-	-	-
164	M11	VSS	-	-	-
165	B3	VSS	-	-	-

Table 42. STM32L4R9I-EVAL I/O assignment (continued)

Primary key	UFBGA 169 DSI	Pin name	Pinout assignment	RGB LCD with FMC mode	Motor-control connector
166	C12	VSS	-	-	-
167	H2	VSS	-	-	-
168	F2	VSS	-	-	-
169	M7	VSS	-	-	-
170	M3	VSS	-	-	-
171	F13	VSS	-	-	-

9 STM32L4R9I-EVAL product information

9.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

- First sticker: product order code and product identification, generally placed on the main board featuring the target device.
  Example:

  Product order code
  Product identification

- Second sticker: board reference with revision and serial number, available on each PCB.
  Example:

  MBxxxx-Variant-yzz
  syywwxxxxx

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: *“MBxxxx-Variant-yzz”*, where *“MBxxxx”* is the board reference, *“Variant”* (optional) identifies the mounting variant when several exist, *"y"* is the PCB revision and *"zz"* is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as *"ES"* or *"E"* are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"E" or *"ES"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

9.2 STM32L4R9I-EVAL product history

Table 43. Product history

Order code	Product identification	Product details	Product change description	Product limitations
STM32L4R9I-EVAL	STM32L4R9I-EVAL/	MCU: – STM32L4R9AII6 silicon revision “Y”	Initial revision	The main board does not support Octo-SPI operation with PSRAM. No workaround available. Refer to STM32L4Rxxx and STM32L4Sxxx device errata.
		MCU errata sheet: – *STM32L4Rxxx and STM32L4Sxxx device errata (ES0393)*		
		Boards: – MB1313-B01 (main board) – MB1314-B01 (DSI display daughterboard) – MB1315-A01 (TFT LCD daughterboard)		
	VA32L4R9I$AU1	MCU: – STM32L4R9AII6 silicon revision “V”	Update board version: MB1313-L4R9I-B02 MB1314-Default-C01 MB1315-Default-A02	The main board does not support Octo-SPI operation with PSRAM. No workaround available. Refer to STM32L4Rxxx and STM32L4Sxxx device errata.
		MCU errata sheet: – *STM32L4Rxxx and STM32L4Sxxx device errata (ES0393)*		
		Boards: – MB1313-L4R9I-B02 (main board) – MB1314-Default-C01 (DSI display daughterboard) – MB1315-Default-A02 (TFT LCD daughterboard)		

Table 43. Product history (continued)

Order code	Product identification	Product details	Product change description	Product limitations
STM32L4R9I-EVAL	VA32L4R9I$AU2	MCU: – STM32L4R9AII6 silicon revision “V”	Updated new packaging, label, stickers, and welcome letter	The main board does not support Octo-SPI operation with PSRAM. No workaround available. Refer to STM32L4Rxxx and STM32L4Sxxx device errata.
		MCU errata sheet: – *STM32L4Rxxx and STM32L4Sxxx device errata (ES0393)*		
		Boards: – MB1313-L4R9I-B02 (main board) – MB1314-Default-C01 (DSI display daughterboard) – MB1315-Default-A02 (TFT LCD daughterboard)		

9.3 Board revision history

Table 44. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB1313 (main board)	B01	Initial revision	The main board does not support Octo-SPI operation with PSRAM. No workaround available. Refer to STM32L4Rxxx and STM32L4Sxxx device errata sheet.
	L4R9I-B02	– L3 changed into Murata BNX002-11 – T2, T3, T4, T5, T6, T7, T8 changed from STT7P2UH7 into NXP PMN30XP – U11 changed into Macronix MT28EW128ABA1LPC-0SIT – U30, U31 changed into STMicroelectronics IMP34DT05TR – U5 ISSI IS66WVH8M8BLL-100BLI changed into 'Not fitted'	
MB1314 (DSI display daughterboard)	B01	Initial revision	No limitation
	Default-C01	– CN2 part number changed to BM20B(0.8)-24DS-0.4V(51) – CN3 Add 2 PADs connected to GND. – ZZ1 part number changed to IEG1120TB105GG-00	
MB1315 (TFT LCD daughterboard)	Default-A01	Initial revision	No limitation
	Default-A02	– L1 and L2 are changed from FCM1608KF-601T05 to FCM1608KF-601T03. – R1 is changed from RC0805FR-7W10RL to RNCP0805FTD10R0. – T1 and T2 are changed from BSN20 to BSN20BK.	

10 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

10.1 FCC Compliance Statement

Part 15.19

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible party (in the USA)

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USA
Telephone: +1 781-472-9634

10.2 ISED Compliance Statement

Compliance Statement

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (B) / NMB-3 (B).

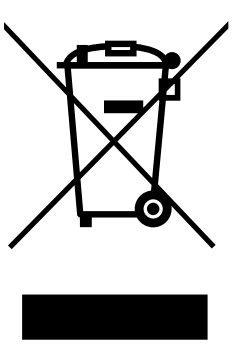
Déclaration de conformité

Étiquette de conformité à la NMB-003 d'ISDE Canada: CAN ICES-3 (B) / NMB-3 (B).

11 Product disposal

Disposal of this product: WEEE (Waste Electrical and Electronic Equipment)

(Applicable in Europe)



This symbol on the product, accessories, or accompanying documents indicates that the product and its electronic accessories should not be disposed of with household waste at the end of their working life.

To prevent possible harm to the environment and human health from uncontrolled waste disposal, please separate these items from other type of waste and recycle them responsibly to the designated collection point to promote the sustainable reuse of material resources.

Household users:

You should contact either the retailer where you buy the product or your local authority for further details of your nearest designated collection point.

Business users:

You should contact your dealer or supplier for further information.

Revision history

Table 45. Document revision history

Date	Revision	Changes
18-Aug-2017	1	Initial version
25-Oct-2017	2	Added: – STM32L4R9I-EVAL board bottom view in *Figure 5* – Bootloader limitation in *Chapter 9.8.1* – Warning on AMOLED display in *Chapter 9.32* Updated: – Cover views *Figure 3* and *Figure 4* moved to *Section 9.1* – *Table 27* and *Table 39* alternative functions removed – *Figure 23*, *Figure 24*, and *Figure 37* in *Electrical schematics*
09-Jan-2018	3	Updated: – *Section 9.8.1*: WA3 simplified – *Table 34*: PE3 replaced by PC9, PE4 replaced by PC10
09-Sep-2020	4	Reorganized the entire document Updated: – *Features*, *Ordering information*, *Development environment*, *Development toolchains,* and *Demonstration software* Added: – *Codification*, *Section 6.25.2: Limitations*, and *Section 8: STM32L4R9I-EVAL board information* Removed: – *Electrical schematics*
06-Jul-2023	5	Added: – *Section 9.2: STM32L4R9I-EVAL product history* – MB1313 B02 version added to new formatted *Section 9.3: Board revision history* Removed: – *Technology partners*
10-Mar-2025	6	Updated *Section 6.5: Power supply*, *Section 6.6: Clock references*, and *Section 10.1: FCC Compliance Statement*. Added *Section 11: Product disposal*.