

Introduction

The 32L4R9IDISCOVERY kit is a complete demonstration and development platform for the STMicroelectronics Arm® Cortex®-M4 core-based STM32L4R9AI microcontroller. Leveraging the innovative ultra-low-power oriented features, 640 Kbytes of embedded RAM, graphics performance (Chrom-ART Accelerator™) and DSISM controller offered by the STM32L4R9AI, the 32L4R9IDISCOVERY kit enables users to easily prototype applications with state-of-the-art energy efficiency, as well as providing stunning audio and graphics rendering with direct support for an AMOLED DSI round display. For even more user-friendliness, the on-board ST-LINK/V2-1 debugger provides out-of-the-box programming and debugging capabilities.

The STM32L4R9AI microcontroller features four I²Cs, five USARTs, one ULP UART, three SPIs, two SAIs, one SDIO, one USB 2.0 full-speed OTG, two CANs, one FMC parallel synchronous interface, one 12-bit ADC, one 12-bit DAC, two ULP analog comparators, two op-amps, one 2 data-lane DSI display, one digital filter for sigma-delta modulation and SWP interface, two Octo-SPI interfaces, 8- to 14-bit camera interface, one touch-sensing controller interface, JTAG and SWD debugging support.

This Discovery board offers everything required for users to get started quickly and develop applications easily. The hardware features on the board help to evaluate the following peripherals: USB OTG FS, microSD™ card, 8-bit camera interface, 16-Mbit PSRAM, PMOD, and STMod+ connectors, IDD measurement, full-duplex I²S with an audio codec and stereo headset jack including an analog microphone, DFSDM with a pair of MEMS digital microphones on board, 512-Mbit Octo-SPI Flash memory device, I²C extension connector, 1.2" AMOLED display using a one data-lane DSI interface with a capacitive touch panel. The ARDUINO® compatible connectors expand the functionality with a wide choice of specialized shields. The integrated ST-LINK/V2-1 provides an embedded in-circuit debugger and programmer for the STM32 MCU.

Figure 1. 32L4R9IDISCOVERY top view

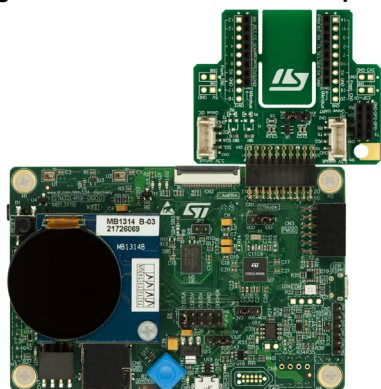
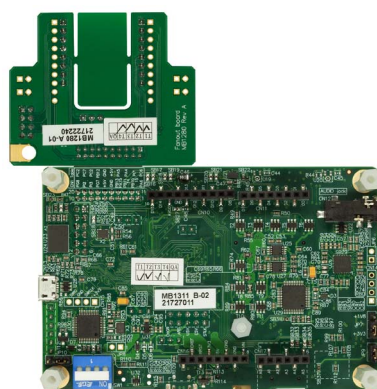


Figure 2. 32L4R9IDISCOVERY bottom view



Pictures are not contractual.

Contents

1	Features	7
2	Ordering information	8
2.1	Product marking	8
2.2	Codification	8
3	Development environment	9
3.1	System requirements	9
3.2	Development toolchains	9
3.3	Demonstration software	9
4	Technology partners	9
5	Bootloader limitations	10
6	AMOLED display limitation	11
7	Hardware layout and configuration	11
7.1	32L4R9IDISCOVERY layout	13
7.2	32L4R9IDISCOVERY mechanical drawing	15
7.3	Embedded ST_LINK/V2-1	16
7.3.1	Drivers	17
7.3.2	ST-LINK/V2-1 firmware upgrade	17
7.4	Low-power consumption status	17
7.5	TAG and SWD	18
7.6	Power supply	19
7.6.1	Power supply sources	19
7.6.2	MCU power supply options	21
7.6.3	Supplying 32L4R9IDISCOVERY through ST-LINK/V2-1 USB	22
7.6.4	Measurement of MCU current consumption	22
7.6.5	Program or debug when power supply not from ST-LINK/V2-1	23
7.7	Clock sources	24
7.8	Reset Source	24

7.9	Boot configuration	24
7.10	Audio codec	25
7.11	DFSDM	25
7.12	PSRAM	25
7.13	USB OTG FS	26
7.13.1	32L4R9IDISCOVERY as a USB device	26
7.13.2	32L4R9IDISCOVERY as a USB host	26
7.14	Octo-SPI Flash memory	27
7.15	Virtual COM port	27
7.16	Buttons and LEDs	27
8	Connectors	29
8.1	ARDUINO® Uno V3 connectors CN10, CN11, CN16, and CN17	29
8.2	DSI display, backlight and touch panel connector CN4	31
8.2.1	DSI AMOLED display	33
8.2.2	Backlight and OLED power supplies generation	33
8.2.3	Touch panel	33
8.3	USB OTG FS connector CN9	34
8.4	ST-LINK/V2-1 USB Micro-B connector CN13	35
8.5	microSD card connector CN6	35
8.6	STMod+ connector CN1	36
8.7	PMOD connector CN3	38
8.8	Camera module connector CN2	39
8.9	TAG connector CN8	40
8.10	SWD header CN5	40
8.11	EXT_I2C connector CN7	41
8.12	Stereo headset and headphone jack CN12	41
	Appendix A GPIO assignment and sharing	43
	Appendix B Solder bridges	51
	Appendix C STMod+ GPIO sharing and multiplexing	53
	Appendix D Schematics	55

Appendix E	Fanout board (MB1280)	72
E.1	MikroElektronika mikroBUS™ compatible connector (Fanout CN10 / CN11)	72
E.2	ESP-01 Wi-Fi® board compatible connector	73
E.3	Compatible connectors for the Grove boards	73
E.3.1	Compatible connector for I ² C Grove boards (Fanout CN3)	73
E.3.2	Compatible connector for UART Grove boards (Fanout CN2)	74
Appendix F	Federal Communications Commission (FCC) and Industry Canada (IC) Compliance	75
Revision history		76

List of tables

Table 1.	Ordering information	8
Table 2.	Codification explanation	8
Table 3.	JP10: VDD_STL setting	18
Table 4.	SW1 switch setting	18
Table 5.	32L4R9IDISCOVERY power sources configuration	19
Table 6.	JP4: power source selector setting	21
Table 7.	JP5: ARD 5 V input/output voltage selection setting	21
Table 8.	JP7: VDD setting	22
Table 9.	JP1: IDD_MCU measurement setting	23
Table 10.	JP3: VDDA and VDDUSB, settings	23
Table 11.	Boot modes	25
Table 12.	LD1 and LD2 details	27
Table 13.	Buttons and LEDs	28
Table 14.	ARDUINO® Uno V3 compatible connectors	29
Table 15.	JP3, VDDA and VDDUSB, settings	30
Table 16.	DSI display connector CN4	31
Table 17.	USB OTG FS Micro-AB connector CN9	34
Table 18.	USB Micro-B connector CN13	35
Table 19.	microSD connector CN6	36
Table 20.	STMod+ connector CN1	37
Table 21.	Quad SPDT switch configuration	37
Table 22.	PMOD connector CN3	38
Table 23.	Camera module connector CN2	39
Table 24.	TAG connector CN8	40
Table 25.	SWD header CN5	40
Table 26.	EXT_I2C connector CN7	41
Table 27.	I2C1 onboard addresses	41
Table 28.	Audio jack connector CN12	42
Table 29.	32L4R9IDISCOVERY GPIO assignment and sharing	43
Table 30.	MFX_V3 GPIO assignment (LQFP48)	49
Table 31.	32L4R9IDISCOVERY solder bridges	51
Table 32.	STMod+ GPIO sharing and multiplexing	53
Table 33.	SPDT quad switch	54
Table 34.	Description of the mikroBUS™ connectors (CN11 and CN10)	72
Table 35.	Description of the ESP-01 Wi-Fi board connector pins	73
Table 36.	Description of the I ² C Grove board connector pins (CN3)	74
Table 37.	Description of the UART Grove board connector pins (CN2)	74
Table 38.	Document revision history	76

List of figures

Figure 1.	32L4R9IDISCOVERY top view	1
Figure 2.	32L4R9IDISCOVERY bottom view	1
Figure 3.	Hardware block diagram	12
Figure 4.	32L4R9IDISCOVERY top side layout	13
Figure 5.	32L4R9IDISCOVERY bottom side layout	14
Figure 6.	32L4R9IDISCOVERY mechanical drawing (top view, in mm)	15
Figure 7.	32L4R9IDISCOVERY mechanical drawing (bottom view, in mm)	16
Figure 8.	How to update driver software	17
Figure 9.	JP4 default configuration	20
Figure 10.	DSI display connector CN4	31
Figure 11.	USB OTG FS Micro-AB connector CN9	34
Figure 12.	USB Micro-B connector CN13	35
Figure 13.	microSD connector CN6 (top view)	36
Figure 14.	STMod+ connector CN1	37
Figure 15.	PMOD connector CN3	38
Figure 16.	Camera module connector CN2	39
Figure 17.	TAG connector CN8	40
Figure 18.	EXT_I2C connector CN7	41
Figure 19.	Stereo headset with microphone jack CN12	42
Figure 20.	32L4R9IDISCOVERY board interconnections (MB1311C)	56
Figure 21.	32L4R9IDISCOVERY power	57
Figure 22.	32L4R9IDISCOVERY ARDUINO® Uno V3 connectors	58
Figure 23.	32L4R9IDISCOVERY ST-LINK/V2-1	59
Figure 24.	32L4R9IDISCOVERY Octo-SPI Flash memory	60
Figure 25.	32L4R9IDISCOVERY peripherals	61
Figure 26.	32L4R9IDISCOVERY USB OTG FS	62
Figure 27.	32L4R9IDISCOVERY Round DSI display interface	63
Figure 28.	32L4R9IDISCOVERY IDD measurement and Multi Function eXpander	64
Figure 29.	32L4R9IDISCOVERY microcontroller	65
Figure 30.	32L4R9IDISCOVERY PSRAM	66
Figure 31.	32L4R9IDISCOVERY camera	67
Figure 32.	32L4R9IDISCOVERY STMOD+ interface	68
Figure 33.	32L4R9IDISCOVERY Audio and DFSDM	69
Figure 34.	Round DSI display board (MB1314)	70
Figure 35.	Fanout board (MB1280)	71
Figure 36.	STMod+ fanout module plugged into CN1 connector	72

1 Features

- STM32L4R9AI Arm^(a)-based microcontroller with 2-Mbyte Flash memory and 640-Kbyte RAM in UFBGA169 package
- 1.2" 390x390 pixel AMOLED round display panel with 16 million colors depth, MIPI[®] DSI interface and capacitive touch panel
- USB OTG FS
- On-board current measurement
- SAI audio codec
- ST-MEMS digital microphones
- 16-Mbit asynchronous PSRAM
- 512-Mbit Octo-SPI Flash
- 2 user LEDs
- 1 reset push-button
- 4-direction joystick with selection button
- Board connectors:
 - 8-bit camera
 - USB OTG FS with Micro-AB
 - Stereo headset jack including analog microphone input
 - microSD[™] card
 - ARDUINO[®] Uno V3 expansion connectors
 - STMod+ expansion connector
 - PMOD expansion connector
 - EXT_I2C expansion connector
- Flexible power supply options:
 - ST-LINK USB V_{BUS} or external sources
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port and debug port
- Comprehensive free software libraries and examples available with the STM32Cube package
- Support of a wide choice of integrated development environments (IDEs), including IAR[™], Keil[®] and STM32CubeIDE



a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the 32L4R9IDISCOVERY kit, refer to [Table 1](#).

Table 1. Ordering information

Order code	Board references	Target STM32
STM32L4R9I-DISCO	– MB1311 – MB1280⁽¹⁾ – MB1314⁽²⁾	STM32L4R9AI16

1. Fanout board.

2. Round DSI LCD board.

2.1 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and are therefore not ready to be used as reference designs or in production. Any consequences arising from such usage will not be at ST’s charge. In no event will ST be liable for any customer usage of these engineering sample tools as reference designs or in production.

‘E’ or ‘ES’ marking examples of location:

- on the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the section ‘Package information’ of the STM32 datasheet at www.st.com).
- next to the evaluation tool ordering part number, that is stuck or silkscreen printed on the board

This board features a specific STM32 device version, which allows the operation of any stack or library. This STM32 device shows a ‘U’ marking option at the end of the standard part number and is not available for sales.

2.2 Codification

The meaning of the codification is explained in [Table 2](#). The order code is mentioned on a sticker placed on the top side of the board.

Table 2. Codification explanation

32XXYYZDISCOVERY	Description	Example:32L4R9IDISCOVERY
32XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32L4+ Series
YY	MCU product line in the series	STM32L4R9
Z	STM32 Flash memory size: – 1 for 2 Mbytes	2 Mbytes

3 Development environment

3.1 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit or macOS®(a)(b)
- USB Type-A to Micro-B cable

3.2 Development toolchains

- IAR™ - EWARM^(c)
- Keil® - MDK-ARM^(c)
- STMicroelectronics - STM32CubeIDE

3.3 Demonstration software

The demonstration software, included in the STM32Cube package corresponding to the on-board MCU, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation are downloadable from the www.st.com/stm32l4-discovery web page.

4 Technology partners

MACRONIX:

512-Mbit Octo-SPI NOR Flash memory device, part number MX25LM51245GXD100

GOVISIONOX OPTOELECTRONICS:

1.2 inch 390x390 AMOLED display, part number G1120TB103GF-001

-
- a. macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.
 - b. All other trademarks are the property of their respective owners.
 - c. On Windows® only.

5 Bootloader limitations

Boot from system Flash memory results in executing bootloader code stored in the system Flash memory protected against writing and erasing. This allows in-system programming (ISP), that is, flashing the STM32 user Flash memory. It also allows writing data into RAM. The data come in via one of the communication interfaces such as USART, SPI, I²C bus, USB or CAN.

The bootloader version is identified by reading the bootloader ID at the address `0x1FFF6FFE`. Its value is `0x91` for bootloader V9.1 and `0x92` for V9.2.

The STM32L4R9AI6 part soldered on the 32L4R9IDISCOVERY mainboard is marked with a date code corresponding to its date of manufacturing. STM32L4R9AI6 parts with a date code prior or equal to week 37 of 2017 are fitted with bootloader V9.1 affected by the limitations to be worked around, as described hereunder. Parts with the date code starting from week 38 of 2017 contain bootloader V9.2 in which the limitations no longer exist.

To locate the visual date code information on the STM32L4R9II6 package, refer to its datasheet (DS12023) available at www.st.com, section Package Information. Date code related portion of the package marking takes Y WW format, where Y is the last digit of the year and WW is the week. For example, a part manufactured in week 38 of 2017 bares the date code 7 38.

There is also another way to identify the need for a workaround: before opening the blister of the Discovery Kit, just check the backside of the blister. At the bottom left corner, if the reference number is equal or higher than 32L4R9IDISCO/ 02-0, it means the bootloader version is V9.2 and there is no need to apply the workaround. Any other inferior number like 01-0 needs the workaround.

Bootloader ID for the bootloader V9.1 is `0x91`.

The following limitation exists in the bootloader V9.1:

Some user Flash memory data get corrupted when written via SPI interface

Description:

During bootloader SPI Write Flash operation, some random 64-bits (2 double-words) may be left blank at `0xFF`

Workarounds:

WA1: add a delay between sending Write command and its ACK request. Its duration must be the duration of the 256-Byte Flash write time.

WA2: read back after each writing operation (256 bytes or at end of user code flashing) and in case of error start writing again.

WA3: Using bootloader, load a patch code in RAM to write in Flash memory through the same Write Memory write protocol as bootloader (code provided by ST). The patch code is available for download from www.st.com website with a readme.txt file containing usage instructions.

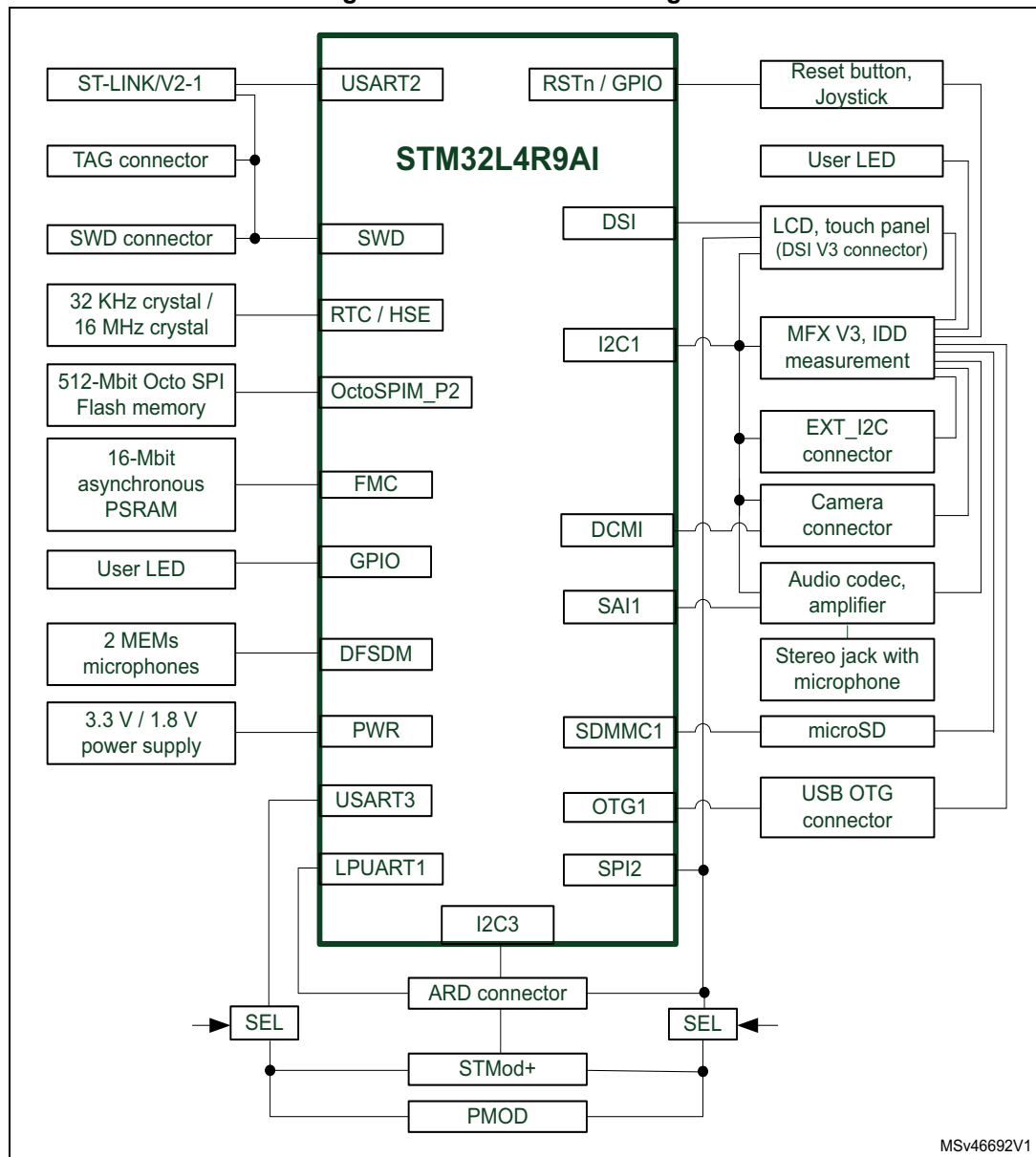
6 AMOLED display limitation

Warning: Permanent image sticking may occur if AMOLED displays the same image for an extended period of time.

7 Hardware layout and configuration

32L4R9IDISCOVERY board is designed around the STM32L4R9AI (169 ball UFBGA package DSI version). The hardware block diagram [Figure 3](#) illustrates the connection between STM32L4R9AI and peripherals (PSRAM, Octo-SPI Flash, DSI color display, USB OTG connector, USART, audio, camera connector, STMod+ and PMOD connectors, IDD measurement, joystick, microSD card, I²C extension connector, ARDUINO® Uno V3 shields and embedded ST-LINK). [Figure 4](#) and [Figure 5](#) help the user to locate these features on the board. Mechanical drawing for 32L4R9IDISCOVERY and round DSI display boards is described in [Figure 6](#).

Figure 3. Hardware block diagram



7.1 32L4R9IDISCOVERY layout

Figure 4. 32L4R9IDISCOVERY top side layout

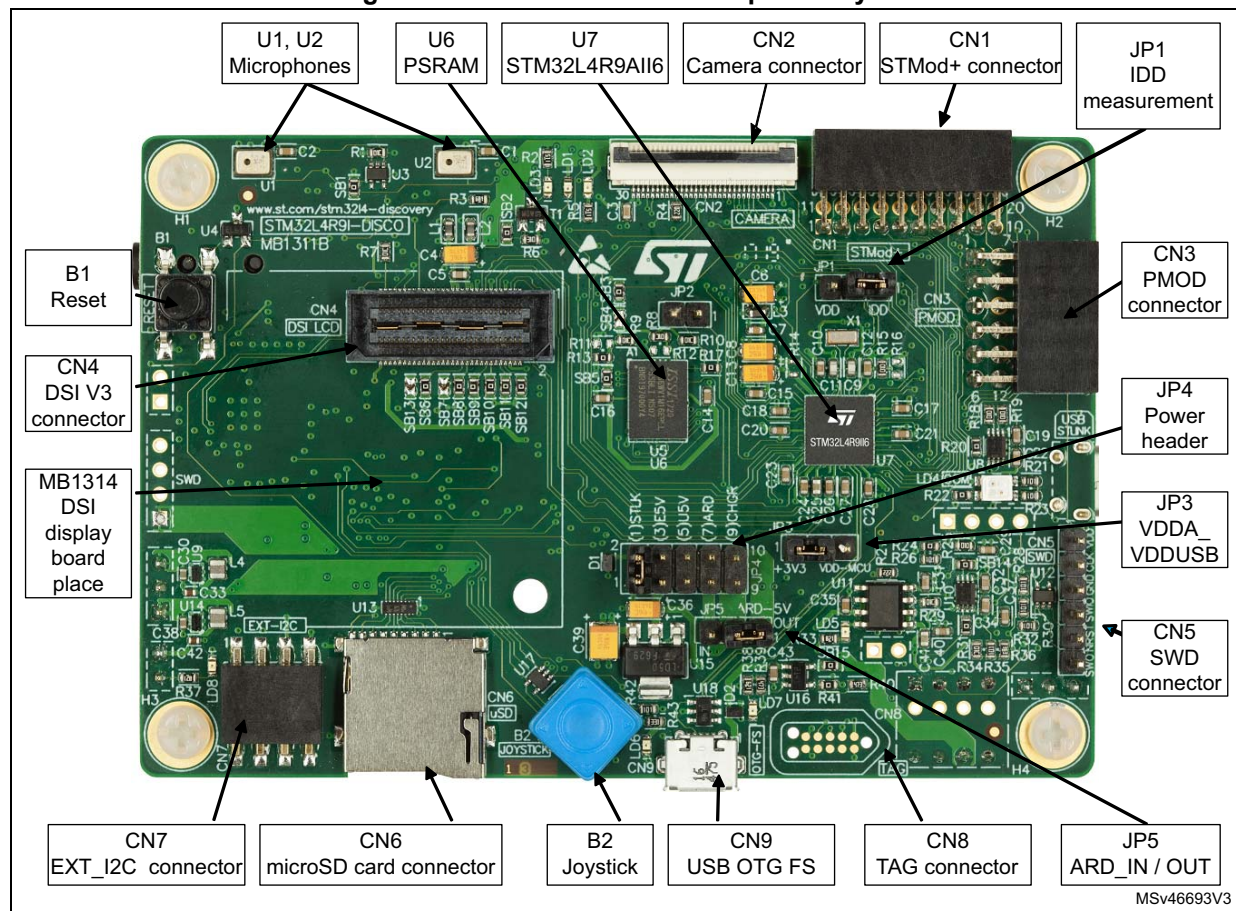
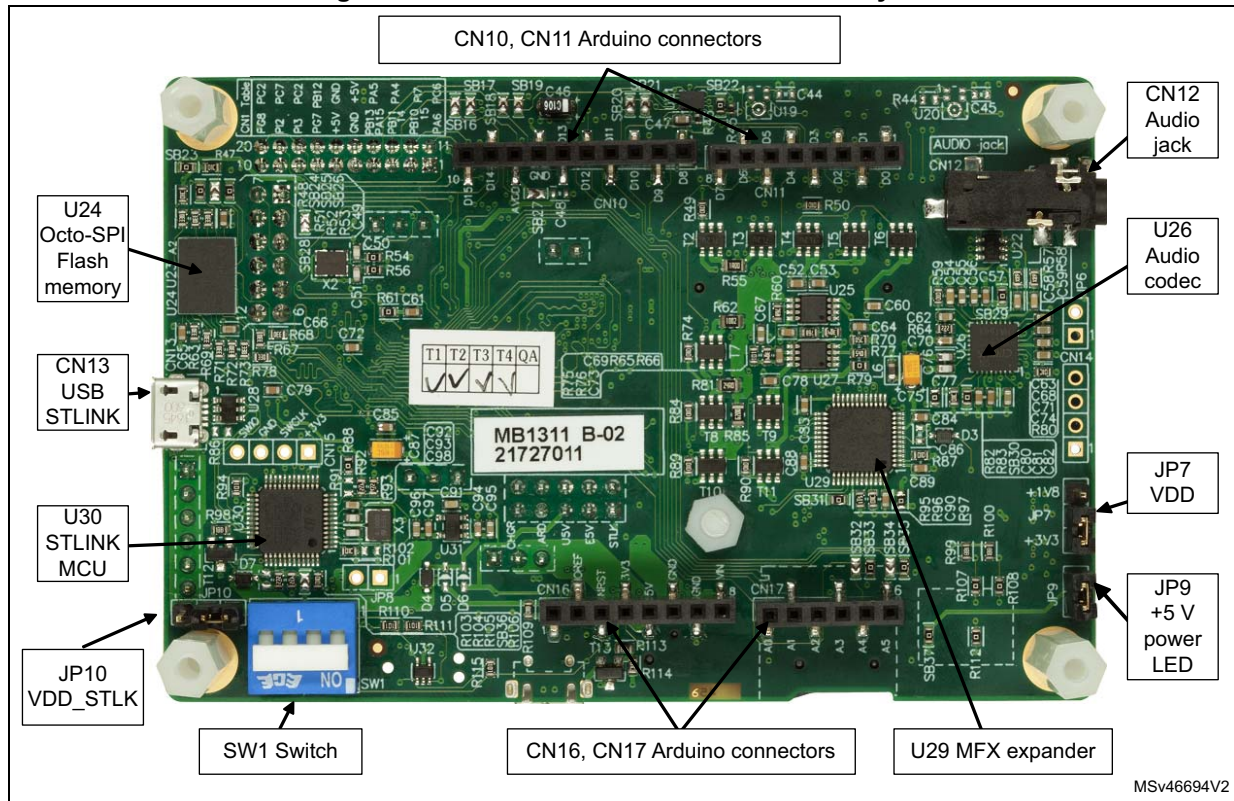


Figure 5. 32L4R9IDISCOVERY bottom side layout



7.2 32L4R9IDISCOVERY mechanical drawing

Figure 6. 32L4R9IDISCOVERY mechanical drawing (top view, in mm)

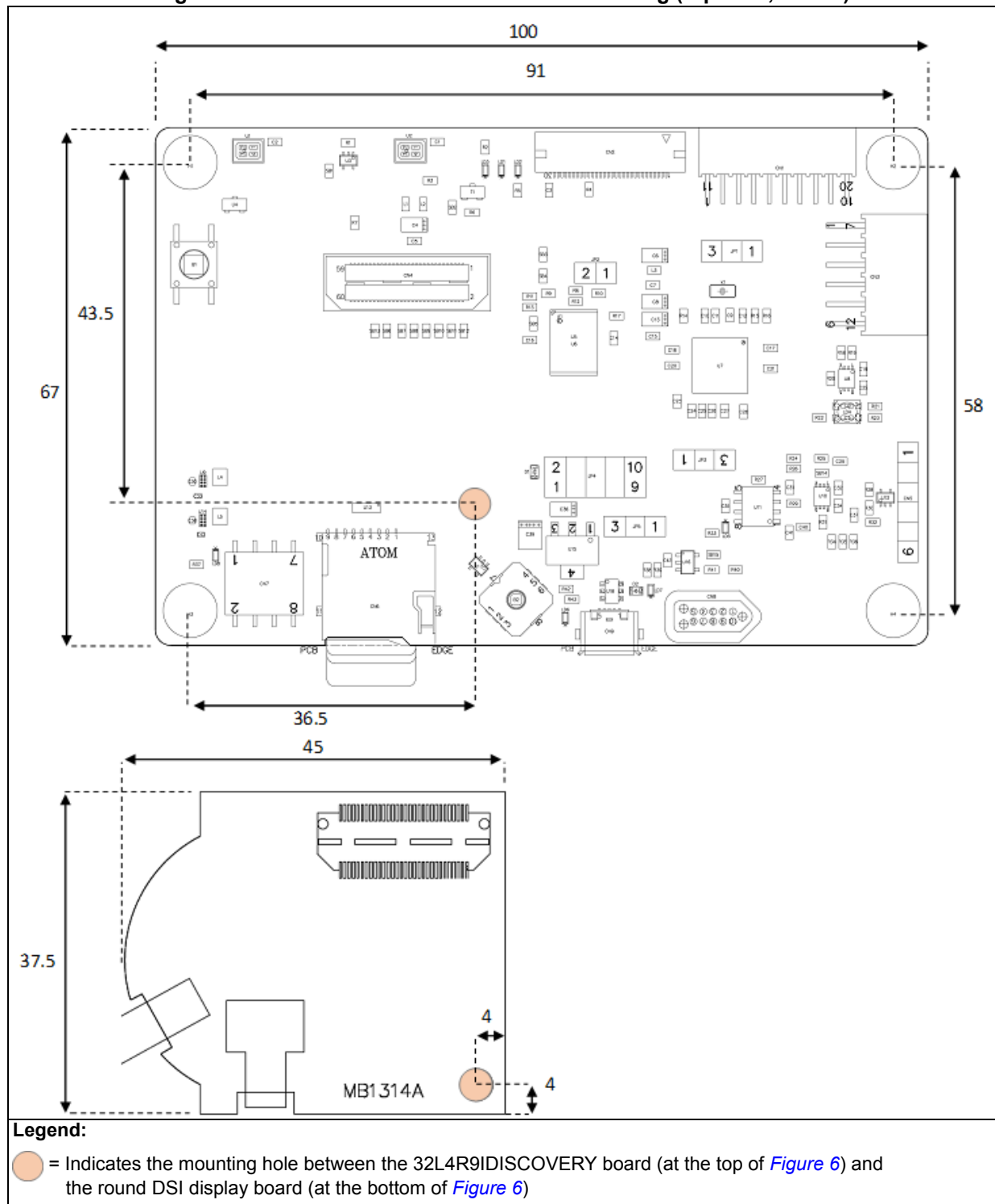
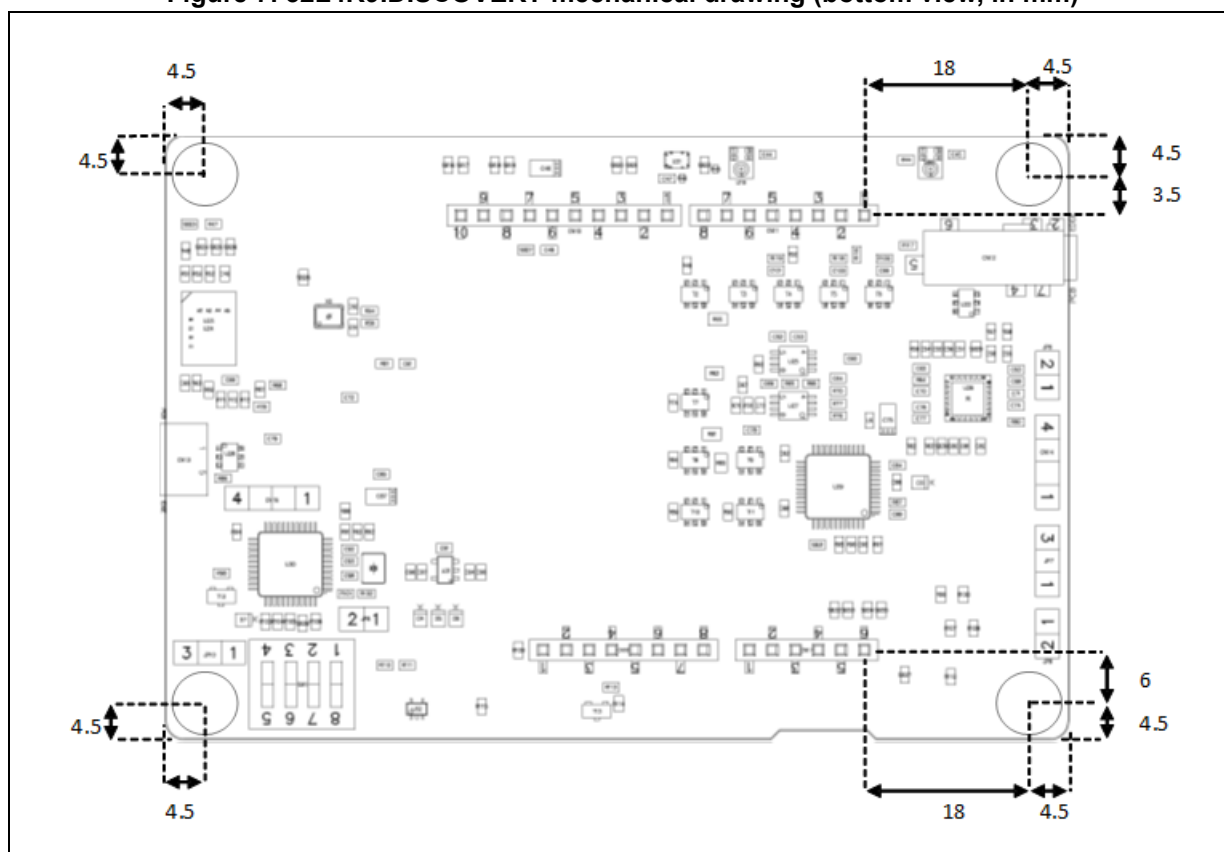


Figure 7. 32L4R9IDISCOVERY mechanical drawing (bottom view, in mm)



Plastic spacer height = 13 mm, overall height = 26 mm ± 1 mm

7.3 Embedded ST_LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated on the 32L4R9IDISCOVERY board. Compared to ST-LINK/V2, the changes are listed below:

- new features supported on ST-LINK/V2-1:
 - USB software re-enumeration
 - Virtual COM port interface on USB
 - Mass storage interface on USB
 - USB power management request for more than 100 mA power on USB
- features no more supported on ST-LINK/V2-1:
 - SWIM interface
 - Application voltage lower than 3 V

For general information concerning the debugging and programming features that are common to both versions V2 and V2-1, refer to ST-LINK/V2 in-circuit debugger/programmer.

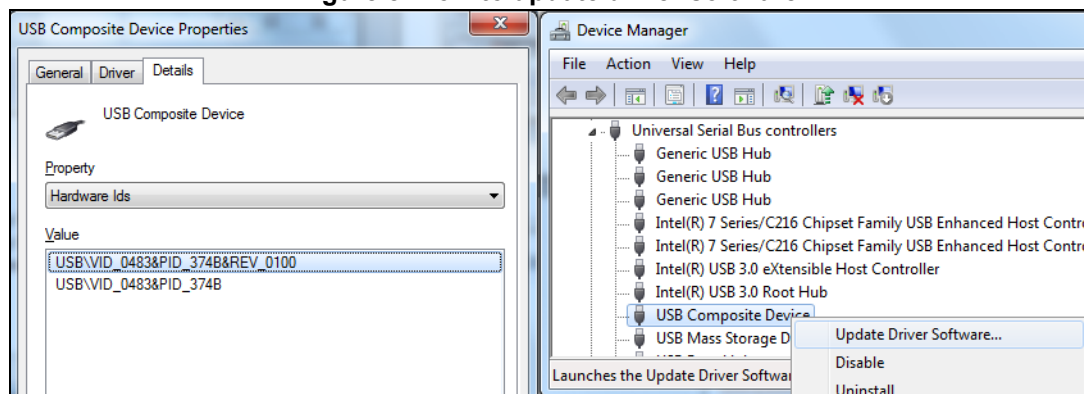
7.3.1 Drivers

Before connecting the 32L4R9IDISCOVERY to a Windows (7, 8, 10) PC via USB, a driver for ST-LINK/V2-1 must be installed. It is available on the www.st.com website.

If 32L4R9IDISCOVERY is connected to the PC before the driver is installed, some interfaces of the board may be declared as 'Unknown' in the PC device manager. In this case, the user must install the driver files, and update the driver of the connected device from the device manager as shown in [Figure 8: How to update driver software](#)

Note: Prefer using the 'USB Composite Device' handle for a full recovery.

Figure 8. How to update driver software



7.3.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware upgrade mechanism for an in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the ST-LINK/V2-1 product (such as new functionality, bug fixes or support for new microcontroller families), it is recommended to visit www.st.com before starting to use the 32L4R9IDISCOVERY and periodically, in order to stay up-to-date with the latest firmware version.

7.4 Low-power consumption status

There is a way to make the board get into very low power consumption status in which the current on +5 V may be below 20 uA. How to get into the low power mode:

1. The connections between ST-LINK/V2-1 and MCU must be disconnected by microswitch SW1 manually (Refer to [Table 4](#) below). Set JP4 on (7) ARD position, and put JP5 in ARD-5V IN position. Remove JP10. Then, connect an external 5 V power supply on CN16 pin 5 5V and on GND.
2. Peripherals (including display, CTP, and PSRAM) are powered off by MOSFET which is controlled by MFX_GPIO8 / MFX_aGPIO2 (put them as input floating), and by setting

all peripherals related I/Os to inactive level (Input pull-down or input is a good option according to I/Os).

3. Disconnect JP9 to remove +5 V from LD8 power LED, disconnect JP10 (or put it in 2-3 position), power off OCTOSPI (remove SB23/SB24) and configure related I/Os as input pull down.
4. Peripherals may be set up by FW to reach power-down mode. All I/Os must be configured in non-consuming states. Set MFX_V3 to sleep mode, get the SD card out of its socket slot. Set the audio codec in power down.

7.5 TAG and SWD

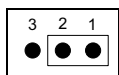
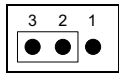
One TAG interface footprint CN8 is reserved on 32L4R9IDISCOVERY and available to debug and program the on-board MCU.

Note: The microswitch SW1 must be put in the OFF position. R24 and R31 must be disconnected.

The SWD 6-pin header CN5 added on 32L4R9IDISCOVERY, connected to onboard ST-LINK MCU, is available to debug and program an external MCU.

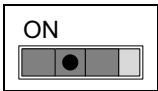
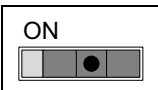
VDD from the external board is 1.8 V or 3.3 V, thanks to the onboard voltage converter.

Table 3. JP10: VDD_STL setting

Jumper	Setting	Description
JP10		Default setting. VDD_STL gets power from 32L4R9IDISCOVERY. ST-LINK is then usable to program the onboard MCU.
		VDD_STL gets power from external through CN5. ST-LINK is then usable to program an external MCU.

SW1 switch enables the debug and programing functions through USB STLK CN13 connector. SW1 is accessible on the bottom side of 32L4R9IDISCOVERY. By default, SW1 is in the ON position. To put the microswitch in the OFF position, just push away the switch from ON position as shown in [Table 4](#).

Table 4. SW1 switch setting

Switch	Setting	Description
SW1		Default setting. SW1 switch is On. It allows debug and program capabilities through USB STLK CN13 connector. When SW1 is On, a V _{BUS} power must be present on USB STLK CN13 connector.
		SW1 is OFF. Set this position if USB STLK CN13 is not used. Debug and program functions are not available.

7.6 Power supply

7.6.1 Power supply sources

32L4R9IDISCOVERY is designed to be powered by the +5 V DC power supply. It is possible to configure the 32L4R9IDISCOVERY to use any of the sources listed in [Table 5](#). Check also detailed configuration on the next page.

By Default, 32L4R9IDISCOVERY is powered through USB STLINK connector CN13, JP4 header has a jumper on (1) STLK, and SW1 is placed in ON position to allow debug and program features.

Choosing any other power source connector than CN13 requires either:

- to place SW1 in OFF position (with no debug/program possibility)
- to let SW1 in ON position, but connecting a USB PC host or Charger on CN13 is mandatory (For this configuration, refer to [Section 7.6.5](#) for correct powering sequence)

For the SW1 switch setting description, refer to [Table 4](#).

Table 5. 32L4R9IDISCOVERY power sources configuration

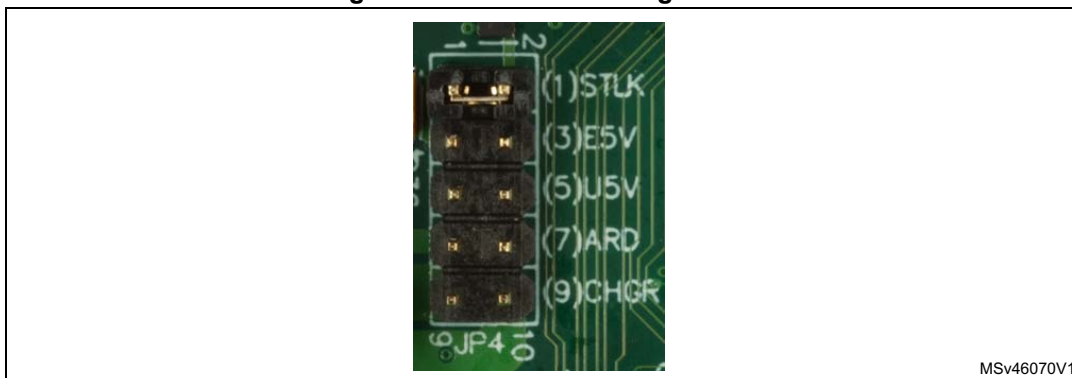
JP4 configuration (function)	Power source connector (pin name)	Voltage	Available current
(1) STLK (USB_STLINK)	CN13 (V _{BUS})	5 V	500 mA
(3) E5V (ARDUINO)	CN16 (VIN)	6 V - 9 V => 5 V	ARDUINO® Uno V3 shield dependent
(5) U5V (USB_OTG_FS)	CN9 (V _{BUS})	5 V	V _{BUS} supply dependent
(7) ARD (ARDUINO)	CN16 (ARD-5V) ⁽¹⁾	5 V	ARDUINO® Uno V3 shield dependent
(9) CHGR (USB_STLINK)	CN13 (V _{BUS})	5 V	V _{BUS} supply dependent

1. ARD-5V is a power output pin to ARDUINO® Uno V3 connector CN16 (default) or a power input pin from ARDUINO® Uno V3 connector CN16, according to JP5 setting. Refer to [Table 7](#) below.

Note: 32L4R9IDISCOVERY must be powered by a power supply unit or by a piece of auxiliary equipment complying with the standard EN-60950-1: 2006+A11/2009, and must be safety extra-low voltage (SELV) with limited power capability.

[Figure 9](#) shows a physical description of the 10-pin header JP4 default configuration.

Figure 9. JP4 default configuration



MSv46070V1

A detailed description of all JP4 possible configurations is listed below and in [Table 6](#):

- **STLK**: 5 V from the ST-LINK/V2-1 USB connector CN13 with 500 mA current limitation. The power mechanism of supplying the board by STLINK/V2-1 is explained in [Section 7.6.3](#). A jumper must be placed in location STLK of JP4, connecting pins 1 and 2. The green LED LD8 is lit on to confirm the presence of 5 V voltage.
- **E5V**: 5 V from the 6 V to 9 V DC from VIN pin of ARDUINO® Uno V3 compatible connector CN16 (the U15 regulator is converting VIN into a 5 V voltage). The VIN input voltage is limited to 9 V to keep the temperature of the regulator U15 within its thermal safe area. A jumper must be placed connecting pins 3 and 4 of JP4. The green LED LD8 is lit on to confirm the presence of 5 V voltage. Place SW1 in OFF position, or let SW1 in ON position and follow [Section 7.6.5](#).
- **U5V**: 5 V from the 5 V DC of USB OTG FS user connector CN9. A jumper must be placed in location USB of JP4, connecting pins 5 and 6. The green LED LD8 is lit on to confirm the presence of 5 V voltage. Place SW1 in OFF position, or let SW1 in ON position and follow [Section 7.6.5](#).
- **ARD**: 5 V from the 5V pin of ARDUINO® Uno V3 compatible connector CN16. A jumper must be placed in location ARD of JP4, connecting pins 7 and 8. Connect the pins 2 and 3 of JP5 to get power from ARDUINO® Uno V3 (Refer to [Table 7](#)). The green LED LD8 is lit on to confirm the presence of 5 V power from ARDUINO® Uno V3. Place SW1 in OFF position, or let SW1 in ON position and follow [Section 7.6.5](#).
- **CHGR**: 5 V from 5 V DC power charger connected to USB STLINK (CN13). A jumper must be placed in location CHGR of JP4, connecting pins 9 and 10. The green LED LD8 is lit on to confirm the presence of 5 V voltage. When this CHGR input is chosen, the 500 mA on-board limitation is no more effective. If 32L4R9IDISCOVERY is powered by an external USB charger, then the debug on CN13 is not available. If 32L4R9IDISCOVERY is powered by an external USB PC port, the user must pay attention that this USB PC supports the sourcing of required current. SW1 may be placed in the OFF position if debug or program features are not used.

Table 6. JP4: power source selector setting

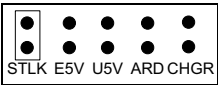
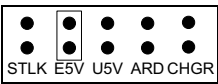
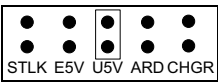
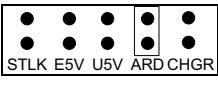
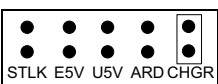
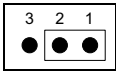
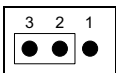
Jumper	Setting	Description
JP4		Default setting. 32L4R9IDISCOVERY is supplied through CN13 Micro-B ST-LINK/V2-1 connector.
		32L4R9IDISCOVERY is supplied through ARDUINO® Uno V3 connector CN16 (VIN). Place SW1 in OFF position, or let SW1 in ON position and follow Section 7.6.5 .
		32L4R9IDISCOVERY is supplied through USB OTG FS connector CN9. Place SW1 in OFF position, or let SW1 in ON position and follow Section 7.6.5 .
		32L4R9IDISCOVERY powers ARDUINO or is supplied by ARDUINO, according to the JP5 setting in Table 7 below. Place SW1 in OFF position, or let SW1 in ON position and follow Section 7.6.5 .
		32L4R9IDISCOVERY is supplied through CN13 Micro-B ST-LINK/V2-1 connector.

Table 7. JP5: ARD 5 V input/output voltage selection setting

Jumper	Setting	Description
JP5		Default setting. 32L4R9IDISCOVERY supplies 5 V to ARDUINO® Uno V3 connector CN16 (on 5V pin).
		32L4R9IDISCOVERY is supplied by 5 V from ARDUINO® Uno V3 connector CN16 (from 5V pin). In that case, JP4 must be placed in the ARD position.

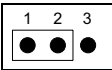
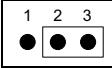
7.6.2 MCU power supply options

32L4R9IDISCOVERY offers the possibility to supply the MCU under 1.8 V or 3.3 V. The JP7 jumper must be placed on +3V3 to supply the MCU with 3.3 V, connecting pins 1 and 2. The jumper may be placed on +1V8 of JP7 to supply the MCU with 1.8 V, connecting pins 2 and 3 (Refer to [Table 8](#)).

Functions listed below are not compatible with the +1V8 setting of JP7:

- OCTOSPI
- PSRAM
- ARDUINO® Uno Revision 3
- CAMERA
- microSD card
- ADC measurements (except if JP3 is set at +3V3, or except if VREF+ configuration is changed)
- USB OTG FS (except if JP3 is set at +3V3)

Table 8. JP7: VDD setting

Jumper	Setting	Description
JP7		Default setting. VDD is powered by the +3V3 regulator.
		VDD is powered by the +1V8 regulator.

7.6.3 Supplying 32L4R9IDISCOVERY through ST-LINK/V2-1 USB

To power the board through ST-LINK/V2-1, the USB host (a PC) must be connected with the 32L4R9IDISCOVERY standard Micro-B USB receptacle, via a USB cable. This event starts with the USB enumeration procedure. In its initial phase, the current supply capability of the USB host port is limited to 100 mA. It is enough because only the ST-LINK/V2-1 part of 32L4R9IDISCOVERY draws power at that time. If the solder bridge SB36 is open (default setting), the U11 ST890 power switch is set to the OFF position, which isolates the remainder of the board from the power source. In the next phase of the enumeration procedure, the host PC informs the ST-LINK/V2-1 facility of its capability to supply up to 500 mA current. If the answer is positive, the ST-LINK/V2-1 sets the U11 ST890 switch to On position to supply power to the remainder of the board. If the PC USB port is not capable of supplying up to 500 mA, another power source must be used (Refer to [Section 7.6.1](#) for details).

The ST890 power switch protects the host USB port against current demand exceeding 625 mA, in case a short circuit occurs on the board (the red LED fault LD5 lights on).

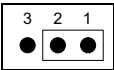
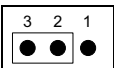
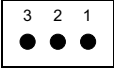
32L4R9IDISCOVERY may also be supplied by the STLINK USB power source with no enumeration, such as a USB charger. In this particular case, ST-LINK/V2-1 turns the ST890 power switch on regardless of the enumeration procedure result and passes the power unconditionally to the board. The green LED LD8 lights on whenever the whole board is powered.

7.6.4 Measurement of MCU current consumption

Jumper JP1 allows the consumption of STM32L4R9AI to be measured directly by a built-in MCU current ammeter circuit (MFX_V3, able to measure from 60 nA to 50 mA) or by removing the jumper and replace it by an external ammeter (Refer to [Table 9](#)).

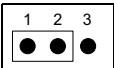
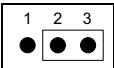
To measure the MCU consumption in standby or shutdown modes, MFX_V3 needs to run the software. To wake up MCU from these modes, it is necessary to press the Reset button B1 or to wait a few seconds.

Table 9. JP1: IDD_MCU measurement setting

Jumper	Setting	Description
JP1		Default setting. A module on the board is designed to measure from 60 nA to 50 mA by using several MOSFETs, and switching automatically depending on the reached value.
		STM32L4R9AI is powered by VDD. MCU current measurement is not possible
		No jumper on JP1: an ammeter may be connected on pins 2 and 3 to measure STM32L4R9AI current (if there is no ammeter, STM32L4R9AI is not powered).

VDDA and VDDUSB power inputs from STM32L4R9AI may be connected to two different power sources, +3V3 or VDD_MCU. These power inputs may be included or not in the IDD current measurement of VDD_MCU, depending on the JP3 jumper configurations described in [Table 10](#).

Table 10. JP3: VDDA and VDDUSB, settings

Jumper	Setting	Description
JP3		Default setting. VDDA and VDDUSB power pins of STM32L4R9AI are supplied with +3V3. the IDD measurement does not include their current consumption. USB OTG FS is functional even if JP7 is set on +1V8.
		VDDA and VDDUSB power pins of STM32L4R9AI are supplied with VDD_MCU. The IDD measurement includes their current consumption.

7.6.5 Program or debug when power supply not from ST-LINK/V2-1

To power the board from another connector than CN13, while keeping debug and program features possible, the following power sequence procedure must be respected:

1. Put a jumper on JP4 at the desired location and set SW1 switch to ON position.
2. Connect the corresponding external power source.
3. Check the green LED LD8 is turned on.
4. Connect the PC to ST-LINK/V2-1 USB connector CN13.

Proceeding this way ensures that the enumeration succeeds, thanks to the external power source. If this order is not respected, the board may be powered by V_{BUS} first from ST-LINK, and the following risks may be encountered:

- If more than 500 mA current is needed by the board, PC may be damaged or current is limited by PC. As a consequence, the board is not powered correctly.
- 500 mA is requested at the enumeration, so there is a risk that the request is rejected and enumeration does not succeed if the PC does not provide such current.

7.7 Clock sources

Two clock sources are used by STM32L4R9AI: one on LSE input and another on HSE input.

LSE clock source

The available clock source is **X1**, 32 kHz crystal for the STM32L4R9AI embedded RTC.

HSE clock source

The second clock source available by default is **X2**, 16 MHz crystal for the STM32L4R9AI HSE system clock.

Note that another HSE clocking option is available on PCB: MCO output from STLINK MCU to STM32L4R9AI HSE input. Refer to [Appendix B: Solder bridges](#).

7.8 Reset Source

The general reset of 32L4R9IDISCOVERY is active low. The reset sources are listed below:

- Reset button B1
- Embedded ST-LINK/V2-1, SW1 micro-switch set to On (default setting)
- ARDUINO® Uno V3 compatible connector CN16 pin 3

The general reset is connected to following peripheral reset functions:

- STM32L4R9AI MCU reset
- Octo-SPI Flash reset
- MFX_V3 reset
- Camera reset

7.9 Boot configuration

After reset, STM32L4R9AI boots from one of the three different embedded memory locations, depending on BOOT0 and BOOT1 bits:

- Boot from the main Flash memory (MCU internal Flash). This is the default configuration.
- Boot from the system memory ISP (in-system programming).
- Boot from the SRAM1.

On the 32L4R9IDISCOVERY board, the boot configuration of the MCU is controlled by the BOOT0 signal on the PH3 pin.

BOOT0 is by default grounded through the R15 pull-down resistor.

It is possible to set BOOT0 HIGH by removing resistor R15 and populating resistor R16 with a 0 Ω resistor. In this case, take care that PH3 (multiplexed with BOOT0 function) is not used as a GPIO.

Check below [Table 11](#) for other boot modes.

Table 11. Boot modes

nBOOT1 FLASH_OPTR[23]	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	Boot Memory Space Alias
X	X	0	1	Main Flash memory is selected as boot area
X	1	X	0	Main Flash memory is selected as boot area
0	X	1	1	Embedded SRAM1 is selected as boot area
0	0	X	0	Embedded SRAM1 is selected as boot area
1	X	1	1	System memory is selected as boot area
1	0	X	0	System memory is selected as boot area

7.10 Audio codec

A Cirrus codec CS42L51-CN2 connected to the SAI1 interface of STM32L4R9AI offers the possibility to connect a stereo headphone or headset with a mono analog microphone.

The I²C-bus addresses of CS42L51-CN2 are 0x95 and 0x94.

7.11 DFSDM

Two ST-MEMS MP34DT01TR digital microphones U1 and U2 are available on 32L4R9IDISCOVERY. The two microphones are located at a distance of 21 mm from each other. They are connected to the STM32 DFSDM by the PC2 port, generating the clock, and by PB12 port, collecting the PDM interleaved data. These microphones are powered by MIC_VDD (PH2 of STM32L4R9AI).

The two DFSDM clock and data interface signals are also accessible on the STMod+ connector CN1. Before using STMod+, the user must follow the recommendations below:

- If STMod+ pin 17 is used, SB1 (DOUT) must be disconnected first.
- If STMod+ pins 18 or 20 are used, MIC_VDD GPIO (PH2) must be activated at the HIGH level first.

7.12 PSRAM

Two PSRAM footprints are supported on the design, both connected to STM32L4R9AI FMC interface:

- A 16-Mbit asynchronous PSRAM (U5), using up to A19 address, is soldered by default. Reference is IS66WV1M16EBLL-55BLI.
- A 32-Mbit synchronous PSRAM (U6), using up to A20 address, may be used. Reference is IS66WVC2M16ECLL-7010BLI.
By default, this PSRAM (U6) is exclusive with the CAMERA function (due to DCMI_D4 function multiplexed with A20 of MCU). In case the camera is used at the same time as

PSRAM, it is possible to change two solder bridges to deactivate A20 on PSRAM (Tied to HIGH, usable density 16 Mbits) and DCMI_D4 is used for CAMERA.

Limitation: the two PSRAMs are not compatible with the JP7 setting at +1V8.

Refer to [Appendix B: Solder bridges](#) for possible PSRAM configuration change.

7.13 USB OTG FS

32L4R9IDISCOVERY supports USB OTG FS (full-speed) communication via the USB Micro-AB connector (CN9) and USB power switch (U16) connected to V_{BUS} .

A green LED LD6 is lit in one of the following cases:

- Power switch (U16) is On and 32L4R9IDISCOVERY works as a USB host.
- V_{BUS} is powered by another USB host when 32L4R9IDISCOVERY works as a USB device.

The red LED LD7 is lit in case of overcurrent.

7.13.1 32L4R9IDISCOVERY as a USB device

The 32L4R9IDISCOVERY board may work as a USB device on CN9 in any power source configuration. If the board is supplied by an external power source on CN9 (JP4 on (5)U5V), the user must pay attention that power source delivers a sufficient amount of current for the complete 32L4R9IDISCOVERY board setup. Refer to [Section 7.6.1](#) for detailed configuration.

7.13.2 32L4R9IDISCOVERY as a USB host

When the board works as a USB host on CN9, it supplies the 5 V to the USB peripheral using one of the following sources:

- ST-LINK/V2-1 USB Micro-B connector CN13 (jumper put in STLK or CHGR location of JP4)
- an external 5 V source connected to pin 5 of the ARDUINO® Uno V3 connector CN16 (jumper put in ARD location of JP4)
- an external source between 6 V and 9 V, connected to VIN pin of ARDUINO® Uno V3 connector CN16 (jumper put in E5V location of JP4)

The green LED LD8 is lit on to confirm the presence of the 5 V source.

The power switch STMP2141STR is controlled by the port MFX_GPIO13 to deliver the 5 V power to the USB device connected to the USB connector CN9. When MFX_GPIO13 is pulled down to the ground, the power switch is closed, and the green LED LD6 confirms the 5 V presence for the USB device. The red LED LD7 FAULT is lit when an over-current occurs.

For more details, refer to [Section 7.6: Power supply](#).

Limitation: when the 32L4R9IDISCOVERY board is configured as a USB host, and if a USB High-power device is to be used on CN9, it may be necessary to change default JP4 setting to power the board from another Power source than (1) STLK or (9) CHGR. Take care sufficient amount of current is available from this other power source and refer to [Section 7.6.1](#) for detailed configuration.

7.14 Octo-SPI Flash memory

A 512-Mbit Octo-SPI user Flash memory (MX25LM51245GXDI00 from MACRONIX) is connected to the OCTOSPIM_P2 interface of STM32L4R9AI. By default, OCTOSPI_RESET of Flash memory has been connected to the general reset of 32L4R9IDISCOVERY.

Refer to [Appendix B: Solder bridges](#) for possible Octo-SPI Flash configuration change.

Limitation: the Octo-SPI Flash memory is not compatible with the JP7 setting at +1V8.

7.15 Virtual COM port

The serial interface USART2 is directly available as a Virtual COM port of the PC, connected to the ST-LINK/V2-1 USB connector CN13. Check the application software settings related to the Virtual COM port.

7.16 Buttons and LEDs

The blue button B2 is a four-direction joystick with a selection mode when pressed in the center. The logic state is HIGH when one of the five-position switch (left, right, up, down, selection) is pressed. The center position (Select function) is connected to a wake-up pin of the microcontroller PC13. The other four directions are mapped on MFX GPIOs.

The black button B1 near the display is the Reset button. It is used to reset the board and may wake-up MCU from standby and shutdown IDD measurement modes.

Two user LEDs located near the camera connector CN2 are available for the user (Refer to [Figure 4](#)): LD1, LD2, from left to right, with orange and green color respectively. To light on a LED, a low logic state 0 must be written in the corresponding GPIO.

- LD1 (orange) is managed by MFX function
- LD2 (green) is managed by STM32L4R9AI main MCU

Table 12. LD1 and LD2 details

LED	MCU port control	color
LD1	PB0 (MFX_GPIO0 from MFX)	Orange
LD2	PH4 (from main MCU)	Green

Other LEDs are present on the 32L4R9IDISCOVERY. Find below a summary list of all buttons and LEDs, with their description.

Table 13. Buttons and LEDs

Reference	Color	Function	Comment
B1	black	RESET	For MCU, OCTO-SPI Flash, MFX_V3, CAMERA
B2	blue	SELECT	with Wake-up alternate function, PC13
		UP	MFX_GPIO1, PB1
		DOWN	MFX_GPIO2, PB2
		RIGHT	MFX_GPIO3, PB3
		LEFT	MFX_GPIO4, PB4
LD1	orange	USER1	MFX_GPIO0, PB0
LD2	green	USER2	PH4
LD3	green	ARDUINO	PB13
LD4	red/green	ST-LINK COM	Green during communication
LD5	red	ST-LINK USB FAULT	Current higher than 625 mA
LD6	green	V _{BUS} USB OTG FS	Status also available on PA9
LD7	red	USB OTG FS OVCR	Overcurrent detection, also on MFX_GPIO14, PB14
LD8	green	5V POWER	Lit on to confirm +5V presence on board

8 Connectors

8.1 ARDUINO® Uno V3 connectors CN10, CN11, CN16, and CN17

CN10, CN11, CN16, and CN17 are female connectors compatible with ARDUINO® Uno Revision 3 standard. Most of the shields designed for ARDUINO® Uno V3 fit to 32L4R9IDISCOVERY board.

Table 14. ARDUINO® Uno V3 compatible connectors

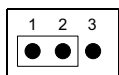
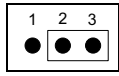
Left connectors					Right connectors				
CN No.	Pin No.	Pin Name	MCU Pin	Function	Function	MCU Pin	Pin Name	Pin No.	CN No.
					I2C3_SCL	PG7	D15	10	CN10 Digital
					I2C3_SDA	PG8	D14	9	
					AVDD	-	AVDD	8	
					Ground	-	GND	7	
CN16 Power	1	-	-	E5V test	SPI2_SCK	PB13	D13	6	
	2	IOREF	-	VDD	SPI2_MISO	PB14	D12	5	
	3	NRST	NRST	Reset	TIM3_CH2, SPI2_MOSI	PB15	D11	4	
	4	3V3	-	3V3output (note 1)	TIM5_CH4, SPI2_NSS	PI0	D10	3	
	5	5V	-	5Vinput/output	TIM8_CH1N	PH13	D9	2	
	6	GND	-	Ground	-	PH15	D8	1	
	7	GND	-	Ground					
	8	VIN	-	+6V to +9V power input (note 2)					
CN17 Analog	1	A0	PA7	ADC1_IN12	-	PA4	D7	8	CN11 Digital
	2	A1	PC4	ADC1_IN13	TIM3_CH1	PB4	D6	7	
	3	A2	PC3	ADC1_IN4	TIM5_CH2	PA1	D5	6	
	4	A3	PB0	ADC1_IN15	-	PG6	D4	5	
	5	A4	PA0 or PG8 (note 3)	ADC1_IN5 or I2C3_SDA (note 3)	TIM15_CH2	PF10	D3	4	
	6	A5	PA5 or PG7 (note 3)	ADC1_IN10 or I2C3_SCL (note 3)	-	PG11	D2	3	
					LPUART1_TX	PC1	D1	2	
					LPUART1_RX	PC0	D0	1	

1. The 3V3 on ARD connector PIN4 is not a power input for 32L4R9IDISCOVERY board, to simplify power architecture.
2. The external voltage applied to pin VIN must be in the range 6 to 9V at 25°C ambient temperature. If a higher voltage is applied to the U15 regulator, it may overheat and could be damaged.
3. By default, pin 5 and pin 6 of CN17 connector are connected to ADC MCU input ports PA0 and PA5 respectively, thanks to configuration of solder bridges: SB33 and SB35 closed, SB32 and SB34 opened. In case it is necessary to connect I²C interface signals on pins 5 and 6 of CN17 instead of ADC inputs, open SB33 and SB35, and close SB32 and SB34.

Before using any ARDUINO® Uno V3 Shield, it is important to refer to [Section 7.6.1](#) for a correct configuration of JP4 and JP5. VREF+, the voltage reference used by the internal DAC and ADC of STM32L4R9AI, has three different power sourcing capabilities:

- from STM32L4R9AI MCU Internal buffer generation (Default). VREFBUF internal ADC / DAC voltage reference is set to 2.5V by default.
- from an external ARDUINO® Uno V3 shield, connected to connector CN10. In that case, SB27 needs to be connected to bring AVDD on VREF+, a 100nF is necessary on C48 and VREFBUF need to be de-activated.
- from a VDDA power supply generated on 32L4R9IDISCOVERY board. VDDA is also connected to VDDUSB of STM32L4R9AI. In that case, mounting a 0 Ω resistor on R14 is necessary. VREFBUF needs to be de-activated. A jumper JP3 also needs to be set as below description.

Table 15. JP3, VDDA and VDDUSB, settings

Jumper	Setting	Description
JP3 VDDA Setting		Default setting. The jumper is on PIN1/2, VDDA get power from +3V3.
		The jumper is on PIN2/3, VDDA get power form VDD_MCU (Refer to the warning below).

Warning: When VDDA=VDD_MCU and if VDD_MCU=1.8 V (check JP7 setting), there are a huge leakage current and a risk of damaging MCU I/Os in case 3.3 V logic level is connected to ADC input I/Os of STM32L4R9AI. Also, ADC measurement is not functional in the default configuration.

Caution: The I/Os of STM32 microcontroller are 3V3 compatible instead of 5 V for ARDUINO® Uno V3.

Note: *Limitation: the ARDUINO® Uno V3 is not compatible with the JP7 setting at +1V8.*
Refer to [Appendix B: Solder bridges](#) for possible ARDUINO® Uno V3 configuration change.

8.2 DSI display, backlight and touch panel connector CN4

All the necessary signals to interface with the round DSI display board are available through the DSI V3 connector CN4.

Figure 10. DSI display connector CN4

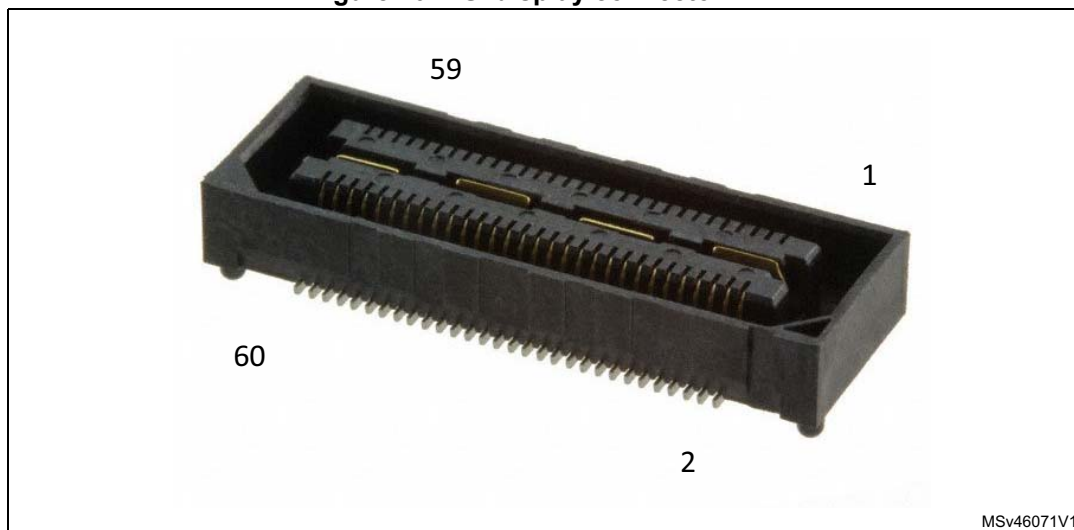


Table 16. DSI display connector CN4

Function	GPIO port	Signal name	CN6 pin number		Signal name	GPIO port	Function
General ground	-	GND	1	2	NC	-	-
Differential DSI clock	-	DSI_CK_P	3	4	TOUCH_INT	MFx_GPIO9	Touch panel interrupt
Differential DSI clock	-	DSI_CK_N	5	6	GND	-	General ground reference
General ground	-	GND	7	8	DSI_D2_P	-	Not connected
Differential DSI data 0	-	DSI_D0_P	9	10	DSI_D2_N	-	Not connected
	-	DSI_D0_N	11	12	GND	-	General ground
General ground	-	GND	13	14	DSI_D3_P	-	Not connected
Differential DSI data 1	-	DSI_D1_P	15	16	DSI_D3_N	-	Not connected
	-	DSI_D1_N	17	18	GND	-	General ground
General ground	-	GND	19	20	NC	-	-
Power output	-	+5v	21	22	SPI_CS	PH14	SPI chip select

Table 16. DSI display connector CN4 (continued)

Function	GPIO port	Signal name	CN6 pin number		Signal name	GPIO port	Function
Power output	-	+5v	23	24	SPI2_SCK	PB13	SPI clock
-	-	NC	25	26	SPI2_MOSIp	PB15	SPI data
SM3321 ground	-	BLGND	27	28	SPI_DCX	PB14	SPI data/control
SM3321 ground	-	BLGND	29	30	NC	-	-
-	-	NC	31	32	RESERVED	-	-
-	-	NC	33	34	NC	-	-
-	-	NC	35	36	3V3	-	3V3 voltage reference
-	-	NC	37	38	VDDIO	-	IOVDD reference
-	-	NC	39	40	I2C1_SDA	PG13	Touch panel I ² C data
-	-	NC	41	42	NC	-	-
DSI_SWIRE control output	PA8	DSI_SWIRE	43	44	I2C1_SCL	PB6	Touch panel I ² C clock
-	-	NC	45	46	NC	-	-
-	-	NC	47	48	NC	-	-
DSI tearing effect input	PF11	TE	49	50	NC	-	-
-	-	NC	51	52	NC	-	-
DSI Backlight control output	PB1	DSI_BL_CTRL	53	54	NC	-	-
-	-	NC	55	56	NC	-	-
DSI and Touch panel Reset output	MFX_GPIO10	DSI_RESET	57	58	NC	-	-
-	-	NC	59	60	1V8	-	1.8V voltage reference
General ground	-	GND	61	62	GND	-	General ground
General ground	-	GND	63	64	GND	-	General ground

Refer to [Appendix B: Solder bridges](#) for possible DSI display configuration change.

8.2.1 DSI AMOLED display

Warning: Permanent image sticking may occur if AMOLED displays the same image for an extended period of time.

The DSI display is based on a round AMOLED touch-sensitive panel of 1.2 inches and 390x390 pixels. The display module reference is IEG1120TB103GF-001 from Govisionox Optoelectronics. It displays up to 16M colors. The round DSI display module board reference is MB1314. The DSI interface of MB1314 is only one data-lane width and a clock lane, but the 32L4R9IDISCOVERY board supports DSI displays with up to two data-lane widths. The DSI_V3 connector interface also enables the use of dedicated low power modes of display, thanks to the available SPI2 interface (MB1314 does not use it). It is also possible to use some of the USART3 signals to control a low power mode (SB6 and SB8 are respectively exclusive with SB13 and SB7).

The DSI_TE signal PF11 is used as an input of the main microcontroller connected to the display signal TE (tearing effect). DSI_TE signal is used to synchronize the refresh of the display memory by the microcontroller with the display scan, this to avoid visible artifacts.

DSI_3V3_PWRON signal (MFX_GPIO8, low level active) controls the 3V3 level power supplies provided on the DSI_V3 connector interface. DSI_1V8_PWRON signal (MFX_aGPIO2) controls the 1V8 level power supplies provided on the DSI_V3 connector interface. Both must be used to enable or disable the display, TP and PSRAM. They allow disconnecting those peripherals when doing low power IDD measurement.

DSI_RESET signal (MFX_GPIO10, low level active) controls the reset for the display and the Touch panel.

An optional DSI_SWIRE signal PA8 offers the additional possibility to control the voltage for any display supply during initialization (not used by MB1314 by default). PA8 is exclusive with another function from 32L4R9IDISCOVERY board: CAMERA clock Interface (MCO), which is the default setting.

8.2.2 Backlight and OLED power supplies generation

This function is handled by the power driver circuit SM3321, included on the MB1314 DSI display Board. SM3321 is a switching mode boost converter supplied by the 3V3 rail of the DSI_V3 connector interface. SM3321 is controlled either by the AMOLED driver circuit itself (default configuration), either by DSI_BL_CTRL (PB1) from the main MCU, either from the DSI_SWIRE (PA8) interface from main MCU. SM3321 provides all necessary voltage references to AMOLED display.

If used, the signal DSI_BL_CTRL switches on the backlight with a HIGH level. It is possible to dim the backlight intensity by applying a low-frequency PWM signal to DSI_BL_CTRL (1 to 10 kHz typically).

8.2.3 Touch panel

The touch panel is a capacitive touch panel using an I²C interface. The touch panel IC reference is FT3267 and is located on the MB1314 board. The FT3267 I2C1 default addresses are 0x71 and 0x70.

Touch panel interrupt output DSI_TOUCH_INT is connected to MFX_GPIO9. It is used as a touch panel detection indication. MFX_GPIO10 resets capacitive touch panel and DSI display.

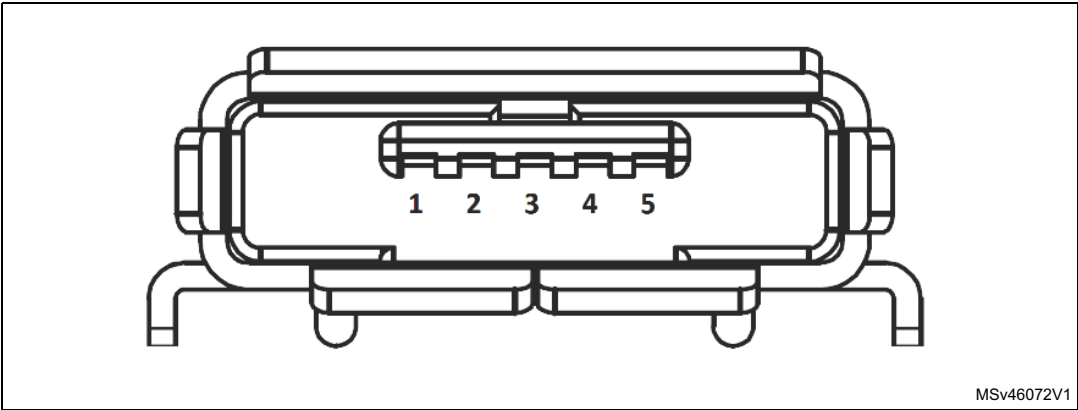
8.3 USB OTG FS connector CN9

A USB OTG full speed communication link is available at USB Micro AB receptacle connector CN9. Micro AB receptacle enables USB host and USB Device features.

MFX_GPIO13 is used to enable onboard V_{BUS} power when in host mode.

Limitation: when the 32L4R9IDISCOVERY board is configured as a USB host, and if a USB High-power device is to be used on CN9, it may be necessary to change default JP4 setting to power the board from another Power source than (1) STLK or (9) CHGR. Take care sufficient amount of current is available from this other Power source and refer to [Section 7.6.1](#) for detailed configuration.

Figure 11. USB OTG FS Micro-AB connector CN9



MSv46072V1

Table 17. USB OTG FS Micro-AB connector CN9

Pin number	Description	Pin number	Description
1	V _{BUS} (PA9)	4	ID (PA10)
2	DM (PA11)	5	GND
3	DP (PA12)	-	-

8.4 ST-LINK/V2-1 USB Micro-B connector CN13

The USB connector CN13 is used to connect the embedded ST-LINK/V2-1 to the PC.

Figure 12. USB Micro-B connector CN13

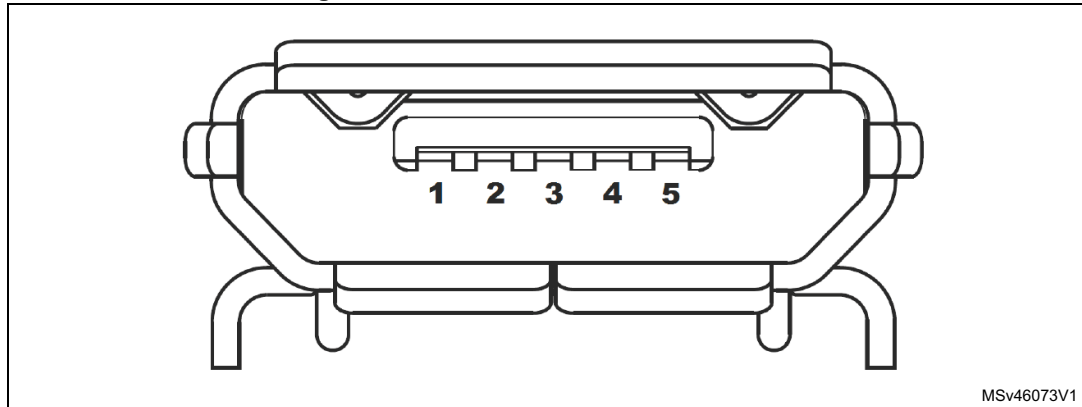


Table 18. USB Micro-B connector CN13

Pin number	Description	Pin number	Description
1	V _{BUS} (power)	4	GND
2	DM	5,6	Shield
3	DP	-	-

8.5 microSD card connector CN6

microSD cards with 4 Gbytes or more capacity are inserted in the receptacle CN6. Four data bits of the SDMMC1 interface, CLK and CMD signals of the STM32L4R9AI are used to communicate with the microSD card at +3V3 only. The card insertion is detected by the MFX_GPIO5: when a microSD card is inserted, the logic level is 0, otherwise, it is 1.

Figure 13. microSD connector CN6 (top view)

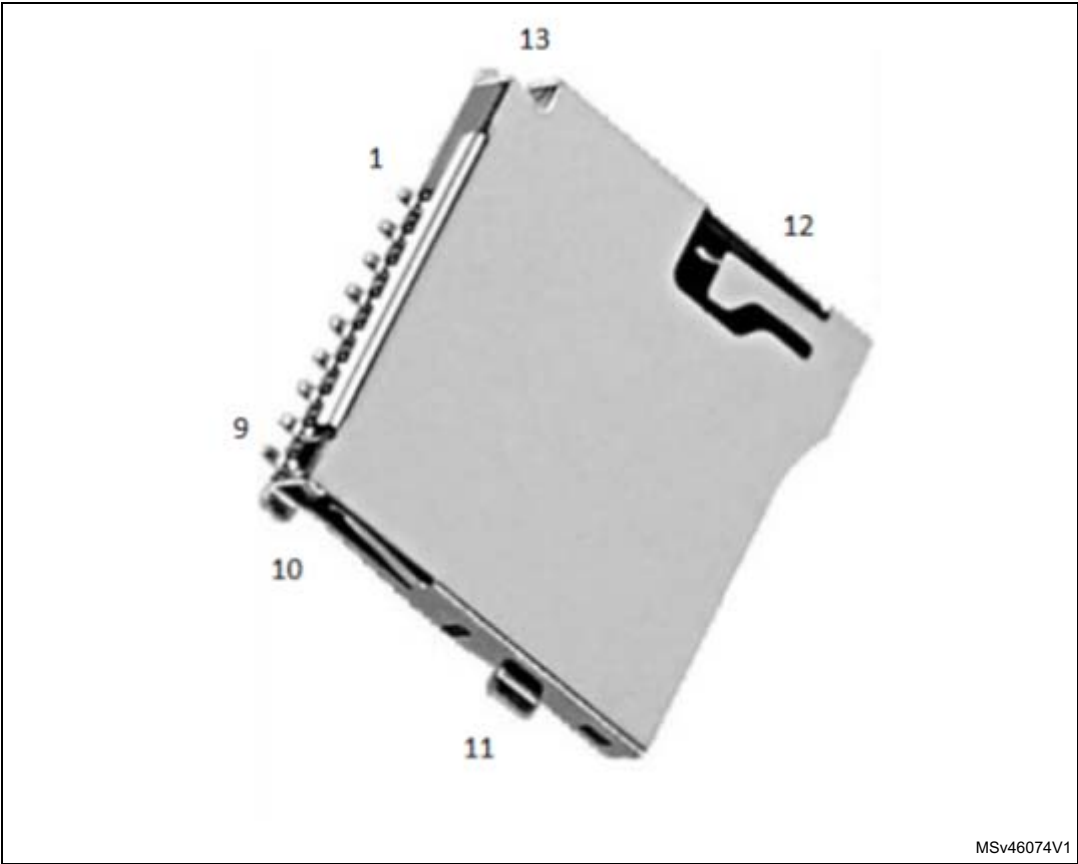


Table 19. microSD connector CN6

Pin number	Description	Pin number	Description
1	SDMMC1_D2 (PC10)	6	GND
2	SDMMC1_D3 (PC11)	7	SDMMC1_D0 (PC8)
3	SDMMC1_CMD (PD2)	8	SDMMC1_D1 (PC9)
4	VDD (+3V3)	9	μSD_DETECT (MFX_GPIO5)
5	SDMMC1_CLK (PC12)	10-11-12	GND (casing)

Note: Limitation: the microSD is not compatible with the JP7 setting at +1V8.

8.6 STMod+ connector CN1

The standard 20-pin STMod+ connector is available on 32L4R9IDISCOVERY board to increase compatibility with external boards and modules from the Ecosystem of microcontrollers. By default, it is designed to support an ST dedicated fanout board, which allows connecting different modules or board extensions from different manufacturers. fanout board also embeds a 3V3 regulator and I²C level shifters. Schematics of the fanout

board is available in [Figure 35.: Fanout board \(MB1280\)](#). For more detailed information, refer to the ST fanout board user manual and to relevant datasheets of associated modules. For details about STMod+ interface, refer to STMod+ connector interface specification.

Figure 14. STMod+ connector CN1

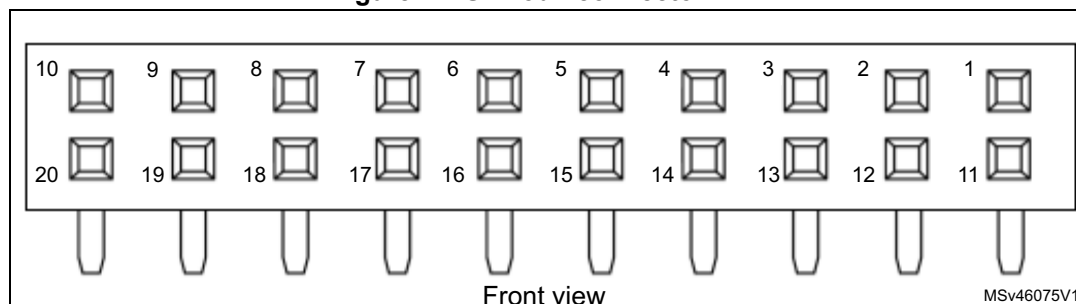


Table 20. STMod+ connector CN1

Pin number	Description	Pin number	Description
1	SPI2_CS/USART3_CTS (PA6)	11	INT (PC6)
2	SPI2_MOSIp/USART3_TXD (PB15/PB10)	12	RST (PI7)
3	SPI2_MISOp/USART3_RXD (PB14/PB11)	13	ADC (PA4)
4	SPI2_SCK/USART3_RTS (PB13/PA15)	14	PWM (PA5)
5	GND	15	+5V
6	+5V	16	GND
7	I2C3_SCL (PG7)	17	GPIO (PB12)
8	SPI2_MOSIs (PI3)	18	GPIO (PC2)
9	SPI2_MISOs (PI2)	19	GPIO (PC7)
10	I2C3_SDA (PG8)	20	GPIO (PC2)

In order to be able to support the selection of SPI or UART functions connection on STMod+ by software, a quad SPDT switch has been added. It is controlled by two GPIOs from the MFX circuit and enables MCU signal selection for pins 2, 3 and 4. By default, STMod+ connector is selected, and STMOD+_SEL_0 and STMOD+_SEL_1 of MFX circuit are set to support one of the STMod+ interface configuration.

Table 21. Quad SPDT switch configuration

Pin number	SPI	UART / SPI ⁽¹⁾	UART
STMOD+_SEL_0 (GPIO6 of MFX_V3)	0	1	1
STMOD+_SEL_1 (GPIO7 of MFX_V3)	0	0	1
STMod+ pin 1 (directly connected to PA6)	SPI_CS	SPI_CS	USART3_CTS
STMod+ pin 2	SPI2_MOSIp	USART3_TX	USART3_TX
STMod+ pin 3	SPI2_MISOp	USART3_RX	USART3_RX
STMod+ pin 4	SPI2_SCK	SPI2_SCK	USART3_RTS

1. UART / SPI defines default configuration for STMOD+_SEL_0 and STMOD+_SEL_1.

Take care that this connector shares many GPIOs with other functions on the Board: for more detailed information refer to [Appendix A: GPIO assignment and sharing](#).

In addition, to have a quick look at STMod+ GPIO sharing and multiplexing, and to get a quick view on other alternate functions available on its pins, refer to [Appendix C: STMod+ GPIO sharing and multiplexing](#).

Limitation: The STMod+ interface is not compatible with the JP7 setting at +1V8.

Limitation: if STMod+ pin 17 is used, take care to disconnect SB1 first. If STMod+ pin 18 or 20 is used, activate MIC_VDD GPIO (PH2) at a HIGH level first.

8.7 PMOD connector CN3

The standard 12-pin PMOD connector is available on the STM32L4R9I-DISCO Discovery board to support low frequency, low I/O pin count peripheral modules. The PMOD interface which has been implemented on the STM32L4R9I-DISCO Discovery board is compatible with the PMOD type 2A & 4A I/O signal assignment convention.

Figure 15. PMOD connector CN3

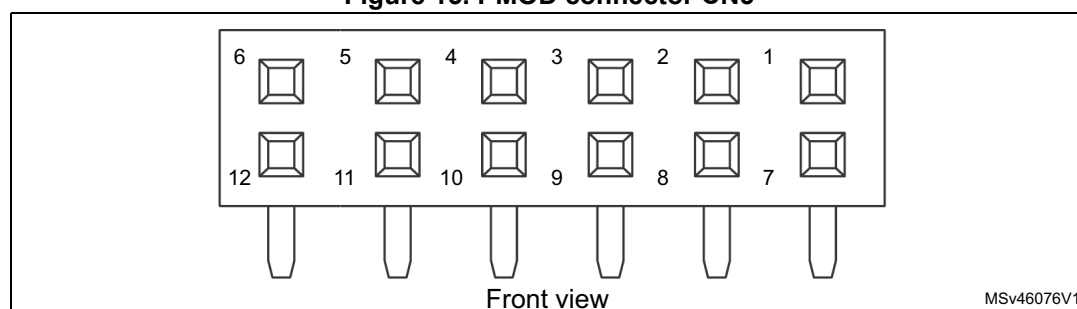


Table 22. PMOD connector CN3

Pin number	Description	Pin number	Description
1	SPI2_CS/USART3_CTS (PA6)	7	INT (PC6)
2	SPI2_MOSIp/USART3_TXD (PB15/PB10)	8	RESET (PI7)
3	SPI2_MISOp/USART3_RXD (PB14/PB11)	9	NA
4	SPI2_SCK/USART3_RTS (PB13/PA15)	10	NA
5	GND	11	GND
6	3V3	12	3V3

In order to be able to support the selection of SPI or UART functions connection on PMOD by software, a quad SPDT switch has been added on board. It is controlled by two GPIOs from MFX_V3 circuit and enables MCU signal choice for pins 2, 3 and 4: refer to [Table 21](#) STMod+ chapter for switch description details (pin 1, 2, 3 and 4 of PMOD are common with STMod+).

By default, the STMod+ connector is selected, so STMOD+_SEL_0 and STMOD+_SEL_1 need to be modified to support one of the PMOD interface configurations. Also, PMOD shares GPIOs with other functions of the Board: for more detailed information refer to [Appendix A: GPIO assignment and sharing](#).

Note: *Limitation: the PMOD interface is not compatible with the JP7 setting at +1V8.*

8.8 Camera module connector CN2

An 8-bit camera module function is supported thanks to the 30-pin dedicated ZIF connector CN2. The camera module reference is STM32F4DIS-CAM. This module has to be connected with caution before powering on the STM32L4R9I-DISCO Discovery board. The camera module I²C addresses are 0x61 and 0x60. The camera is usable by default, but one must take care of GPIO sharing and multiplexing with other function, in order to program the good configuration. For more detailed information refer to [Appendix A: GPIO assignment and sharing](#).

Note: *Limitation: the camera is not compatible with the JP7 setting at +1V8.*

Figure 16. Camera module connector CN2

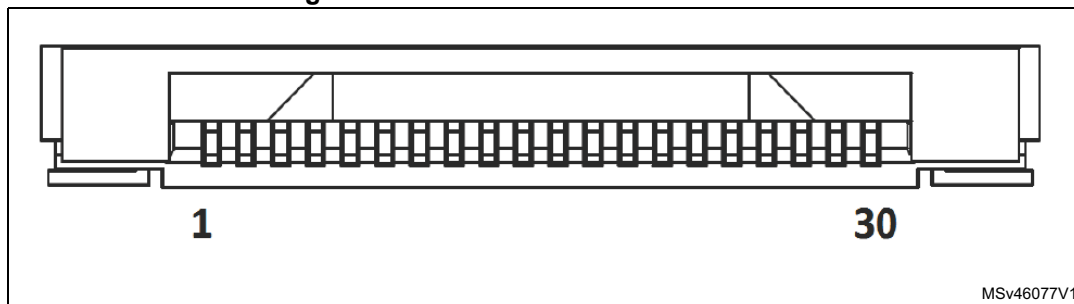


Table 23. Camera module connector CN2

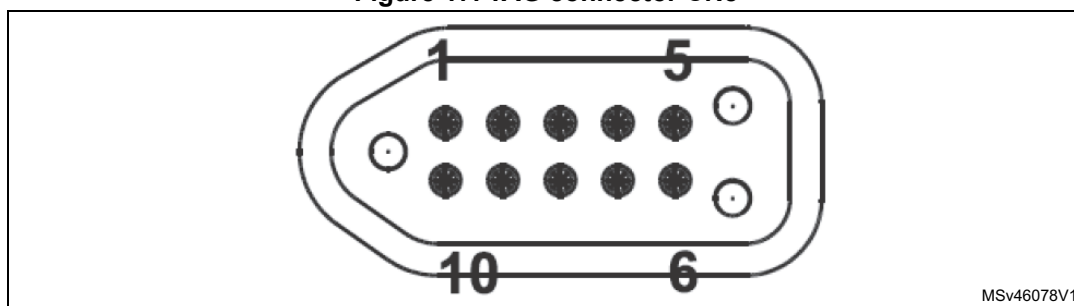
Pin number	Description	Pin number	Description
1	GND	16	GND
2	NC	17	DCMI_HSYNC (PA4)
3	NC	18	NC
4	DCMI_D0 (PC6)	19	DCMI_VSYNC (PI5)
5	DCMI_D1 (PC7)	20	VDD
6	DCMI_D2 (PH11)	21	DCMI_CLK (PA8)
7	DCMI_D3 (PH12)	22	NC
8	DCMI_D4 (PE4)	23	GND
9	DCMI_D5 (PI4)	24	NC
10	DCMI_D6 (PB8)	25	DCMI_PWR_EN (MFX_GPIO12)
11	DCMI_D7 (PI7)	26	DCMI_Nrst (NRST from MCU)
12	NC	27	I2C1_SDA (PG13)
13	NC	28	I2C1_SCL (PB6)

Table 23. Camera module connector CN2 (continued)

Pin number	Description	Pin number	Description
14	GND	29	GND
15	DCMI_PIXCK (PH5)	30	VDD

8.9 TAG connector CN8

The TAG connector footprint CN8 is used to connect STM32L4R9AI microcontroller for programming or debugging the board.

Figure 17. TAG connector CN8**Table 24. TAG connector CN8**

Pin number	Description	Pin number	Description
1	VDD	10	NRST (PH3, RESET#)
2	SWDIO (PA13)	9	NA
3	GND	8	NA
4	SWCLK (PA14)	7	NA
5	GND	6	SWO (PB3)

8.10 SWD header CN5

The 6-pin SWD header is used to program or debug an MCU in an external application board using a dedicated cable connected to it. To use this SWD header interface, pins 2 and 3 of JP10 need to be connected with a jumper. Furthermore, SW1 must be set in the OFF position while R24 and R31 need to be disconnected.

By default, STLINK/V2-1 is used to program or debug onboard MCU. Pin1 and 2 of JP10 are connected, SW1 is in ON position, R24 and R31 are connected.

Table 25. SWD header CN5

Pin number	Description	Pin number	Description
1	VDD	4	SWDIO (PA13)
2	SWCLK (PA14)	5	NRST
3	GND	6	SWO (PB3)

8.11 EXT_I2C connector CN7

The EXT_I2C connector socket is used to connect external modules to the I2C1 interface or to monitor the I2C1 interface.

Figure 18. EXT_I2C connector CN7

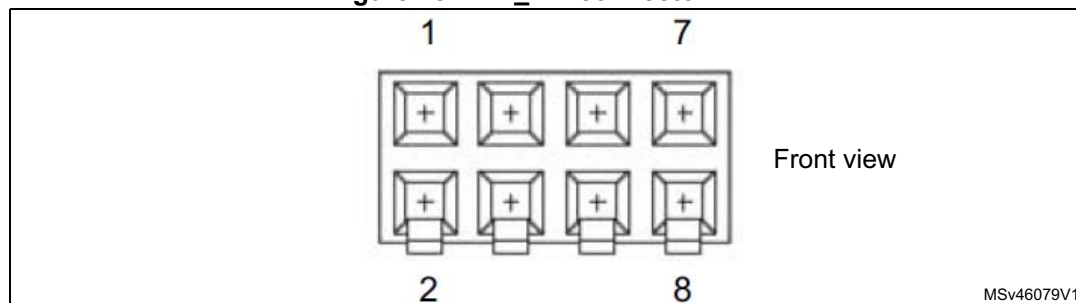


Table 26. EXT_I2C connector CN7

Pin number	Description	Pin number	Description
1	I2C1_SDA (PG13)	5	+3V3
2	NC	6	NC
3	I2C1_SCL (PB6)	7	GND
4	EXT_RESET (MFX_GPIO11)	8	NC

As the I2C1 is available for external use, it is important to note that those following I2C1 applications and addresses are already used on-board:

Table 27. I2C1 onboard addresses

Application	R/W I ² C address	I ² C max. speed	Comment
DSI display Touch Panel	0x71/0x70	400 kHz	Default I ² C address
Audio codec	0x95/0x94	100 kHz	Default I ² C address
CAMERA	0x61/0x60	400 kHz	For STM32F4DIS-CAM Module
MFX_V3	0x85/0x84	400 kHz	Default I ² C address

Depending on the I²C module plugged into CN7, I2C1 could even be used up to Fast mode + (1 MHz) if the audio codec is set to OFF mode with AUDIO_RST Low.

8.12 Stereo headset and headphone jack CN12

A stereo headphone or a stereo headset with an analog microphone is pluggable into the 3.5 mm standard jack socket CN12.

Figure 19. Stereo headset with microphone jack CN12

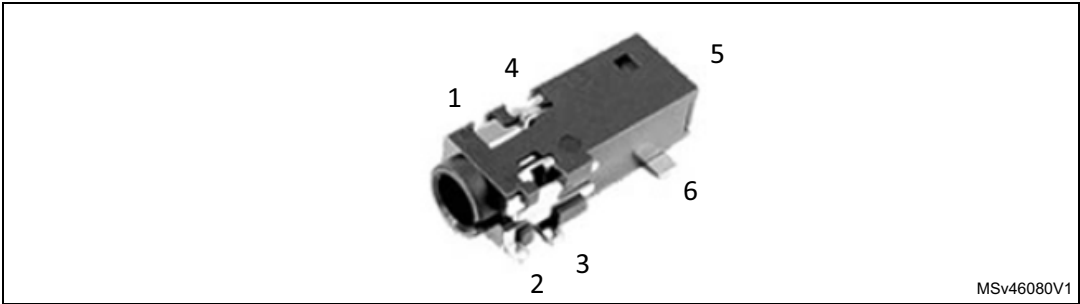


Table 28. Audio jack connector CN12

Pin number	Description	Stereo headset with microphone pinning	
6	OUT_Left	SPK_L (32 ohms typ.)	
4	OUT_Right	SPK_R (32 ohms typ.)	
3	GND	GND	
2	IN_Analog	Microphone	
5	NC	NA	
1	NC		

If a headset is plugged into CN12, the bias of the microphone is driven by the output MICBIAS1 of the codec and the analog audio enters into the codec by the pin AIN3A.

Appendix A GPIO assignment and sharing

Table 29. 32L4R9IDISCOVERY GPIO assignment and sharing

Pin	GPIO port	GPIO primary interface	STMod+ interface	PMOD interface	ARDUINO interface
K3	PA0	-	-	-	ARD_A4 (ADC1_IN5)
M1	PA1	-	-	-	ARD_D5 (TIM5_CH2)
N1	PA2	STLINK_USART2_TX	-	-	-
M2	PA3	STLINK_USART2_RX	-	-	-
N2	PA4	DCMI_HSYNC/DE	STMod+_ADC (ADC_1_IN9)	-	ARD_D7
L3	PA5	-	STMod+_PWM (TIM2_CH1)	-	ARD_A5 (ADC1_IN10)
L4	PA6	-	STMod+_SPI2_CS // STMod+_USART3_CTS ^(NU)	PMOD_SPI2_CS // PMOD_USART3_CTS ^(NU)	-
M4	PA7	-	-	-	ARD_A0 (ADC1_IN12)
E11	PA8	DCMI_CLK (MC0) // DSI_SWIRE ^(NU)	-	-	-
E12	PA9	V _{BUS}	-	-	-
D11	PA10	ID	-	-	-
E13	PA11	DM	-	-	-
D13	PA12	DP	-	-	-
A11	PA13	JTMS/SWDIO	-	-	-
A10	PA14	JTCK/SWCLK	-	-	-
A9	PA15	-	STMod+_USART3_RTS ^(NU)	PMOD_USART3_RTS ^(NU)	-
N4	PB0	DSI_USART3_CK ^(NU)	-	-	ARD_A3 (ADC1_IN15)
L5	PB1	DSI_BL_CTRL ^(NU) // DSI_SWIRE ^(NU)	-	-	-
N5	PB2	MFX_WAKEUP_OUT	-	-	-



Table 29. 32L4R9IDISCOVERY GPIO assignment and sharing (continued)

Pin	GPIO port	GPIO primary interface	STMod+ interface	PMOD interface	ARDUINO interface
A6	PB3	JTDO/TRACESWO	-	-	-
A5	PB4	-	-	-	ARD_D6 (TIM3_CH1)
B5	PB5	SAI1_SD_B	-	-	-
C5	PB6	I2C1_SCL	-	-	-
D5	PB7	PSRAM_NL (ADV)	-	-	-
C4	PB8	DCMI_D6	-	-	-
D4	PB9	SAI1_FS_A	-	-	-
N9	PB10	DSI_USART3_TX ^(NU)	STMod+_USART3_TX	PMOD_USART3_TX	-
H7	PB11	-	STMod+_USART3_RX	PMOD_USART3_RX	-
N12	PB12	DFSDM_1_DATIN1	STMod+_GPIO ^(NU)	-	-
N13	PB13	DSI_SPI2_SCK ^(NU)	STMod+_SPI2_SCK	PMOD_SPI2_SCK	ARD_D13 (SPI2_SCK)
M12	PB14	DSI_SPI_D/CX ^(NU)	STMod+_SPI2_MISO _p ^(NU)	PMOD_SPI2_MISO ^(NU)	ARD_D12 (SPI2_MISO)
L10	PB15	DSI_SPI2_MOSI ^(NU)	STMod+_SPI2_MOSI _p ^(NU)	PMOD_SPI2_MOSI ^(NU)	ARD_D11 (SPI2_MOSI_TIM3_CH2)
J2	PC0	-	-	-	ARD_D0 (LPUART1_RX)
J3	PC1	-	-	-	ARD_D1 (LPUART1_TX)
J4	PC2	DFSDM_1_CKOUT	STMod+_GPIO ^(NU)	-	-
K1	PC3	-	-	-	ARD_A2 (ADC1_IN4)
K4	PC4	-	-	-	ARD_A1 (ADC1_IN13)
F11	PC6	DCMI_D0	STMod+_INT	PMOD_INT	-
G11	PC7	DCMI_D1	STMod+_GPIO	-	-
F9	PC8	SDMMC_1_D0	-	-	-
G13	PC9	SDMMC_1_D1	-	-	-
D9	PC10	SDMMC_1_D2	-	-	-
E9	PC11	SDMMC_1_D3	-	-	-
F8	PC12	SDMMC_1_CK	-	-	-

Table 29. 32L4R9IDISCOVERY GPIO assignment and sharing (continued)

Pin	GPIO port	GPIO primary interface	STMod+ interface	PMOD interface	ARDUINO interface
E1	PC13	JOY_SEL // WAKEUP	-	-	-
F1	PC14-OSC32_IN	PC14-OSC32_IN	-	-	-
G1	PC15-OSC32_OUT	PC15-OSC32_OUT	-	-	-
B8	PD0	PSRAM_D2	-	-	-
C8	PD1	PSRAM_D3	-	-	-
D8	PD2	SDMMC_1_CMD	-	-	-
E8	PD3	PSRAM_CLK	-	-	-
C7	PD4	PSRAM_NOE	-	-	-
D7	PD5	PSRAM_NWE	-	-	-
E7	PD6	PSRAM_NWAIT	-	-	-
F7	PD7	PSRAM_NE1	-	-	-
K10	PD8	PSRAM_D13	-	-	-
K9	PD9	PSRAM_D14	-	-	-
J10	PD10	PSRAM_D15	-	-	-
J9	PD11	PSRAM_A16	-	-	-
J8	PD12	PSRAM_A17	-	-	-
H8	PD13	PSRAM_A18	-	-	-
H11	PD14	PSRAM_D0	-	-	-
H10	PD15	PSRAM_D1	-	-	-
A4	PE0	PSRAM_NBL0	-	-	-
B4	PE1	PSRAM_NBL1	-	-	-
D3	PE2	SAI1_MCLK_A	-	-	-
D2	PE3	PSRAM_A19	-	-	-
D1	PE4	DCMI_D4 // PSRAM_A20 (NU)	-	-	-



Table 29. 32L4R9IDISCOVERY GPIO assignment and sharing (continued)

Pin	GPIO port	GPIO primary interface	STMod+ interface	PMOD interface	ARDUINO interface
E4	PE5	SAI1_SCK_A	-	-	-
E3	PE6	SAI1_SD_A	-	-	-
L7	PE7	PSRAM_D4	-	-	-
K6	PE8	PSRAM_D5	-	-	-
J6	PE9	PSRAM_D6	-	-	-
H6	PE10	PSRAM_D7	-	-	-
N8	PE11	PSRAM_D8	-	-	-
M8	PE12	PSRAM_D9	-	-	-
L8	PE13	PSRAM_D10	-	-	-
K7	PE14	PSRAM_D11	-	-	-
J7	PE15	PSRAM_D12	-	-	-
F5	PF0	PSRAM_A0	-	-	-
F4	PF1	PSRAM_A1	-	-	-
F3	PF2	PSRAM_A2	-	-	-
G3	PF3	PSRAM_A3	-	-	-
G4	PF4	PSRAM_A4	-	-	-
G5	PF5	PSRAM_A5	-	-	-
H4	PF10	-	-	-	ARD_D3 (TIM15_CH2)
M5	PF11	DSI_TE	-	-	-
N6	PF12	PSRAM_A6	-	-	-
M6	PF13	PSRAM_A7	-	-	-
L6	PF14	PSRAM_A8	-	-	-
K5	PF15	PSRAM_A9	-	-	-
J5	PG0	PSRAM_A10	-	-	-
H5	PG1	PSRAM_A11	-	-	-

Table 29. 32L4R9IDISCOVERY GPIO assignment and sharing (continued)

Pin	GPIO port	GPIO primary interface	STMod+ interface	PMOD interface	ARDUINO interface
H9	PG2	PSRAM_A12	-	-	-
G8	PG3	PSRAM_A13	-	-	-
G7	PG4	PSRAM_A14	-	-	-
G9	PG5	PSRAM_A15	-	-	-
G12	PG6	-	-	-	ARD_D4
G10	PG7	-	STMod+_I2C3_SCL	-	ARD_D15 (I2C3_SCL)
F10	PG8	-	STMod+_I2C3_SDA	-	ARD_D14 (I2C3_SDA)
B7	PG9	OCTOSPIM_P2_IO6	-	-	-
D6	PG10	OCTOSPIM_P2_IO7	-	-	-
E6	PG11	-	-	-	ARD_D2
F6	PG12	OCTOSPIM_P2_NCS	-	-	-
G6	PG13	I2C1_SDA	-	-	-
C6	PG15	OCTOSPIM_P2_DQS	-	-	-
H1	PH0-OSC_IN	PH0-OSC_IN	-	-	-
J1	PH1-OSC_OUT	PH1-OSC_OUT	-	-	-
A2	PH2	MIC_VDD	-	-	-
E5	PH3-BOOT0	PH3-BOOT0	-	-	-
K8	PH4	LED_GREEN	-	-	-
L9	PH5	DCMI_PIXCLK/PDCK	-	-	-
N10	PH8	OCTOSPIM_P2_IO3	-	-	-
C11	PH9	OCTOSPIM_P2_IO4	-	-	-
M9	PH10	OCTOSPIM_P2_IO5	-	-	-
M10	PH11	DCMI_D2	-	-	-
B13	PH12	DCMI_D3	-	-	-
C9	PH13	-	-	-	ARD_D9 (TIM8_CH1N)



Table 29. 32L4R9IDISCOVERY GPIO assignment and sharing (continued)

Pin	GPIO port	GPIO primary interface	STMod+ interface	PMOD interface	ARDUINO interface
A13	PH14	DSI_SPI_USART_CS ^(NU)	-	-	-
B12	PH15	-	-	-	ARD_D8
A12	PI0	-	-	-	ARD_D10 (SPI2_NSS_TIM5_CH4)
B11	PI1	MFx_INT_IN	-	-	-
B10	PI2	-	STMod+_SPI2_MISOs	-	-
C10	PI3	-	STMod+_SPI2_MOSIs	-	-
D10	PI4	DCMI_D5	-	-	-
E10	PI5	DCMI_VSYNC/RDY	-	-	-
B9	PI6	OCTOSPIM_P2_CLK	-	-	-
B2	PI7	DCMI_D7	STMod+_RST	PMOD_RST	-
B1	PI9	OCTOSPIM_P2_IO2	-	-	-
A1	PI10	OCTOSPIM_P2_IO1	-	-	-
C3	PI11	OCTOSPIM_P2_IO0	-	-	-
Legend: or = Indicate shared or exclusive functions or interfaces on a GPIO port (NU) = Function mode which is not usable by default // = Highlights two exclusive functions available for one interface (xxx) = Name of the STM32L4R9AI GPIO Alternate function used on this interface					

Table 30. MFX_V3 GPIO assignment (LQFP48)

Pin	GPIO port	Implemented functions	Application function name
10	PA0-WKUP	-	-
11	PA1	MFX_aGPIO1	MFX_aGPIO1
12	PA2	MFX_aGPIO2	DSI_1V8_PWRON
13	PA3	-	-
14	PA4	Reserved DAC_Out1	SPARE
15	PA5	MFX_GPIO5	μSD_DETECT
16	PA6	MFX_GPIO6	STMOD+_SEL_0
17	PA7	MFX_GPIO7	STMOD+_SEL_1
29	PA8	MFX_GPIO8	DSI_3V3_PWRON
30	PA9	MFX_GPIO9	DSI_TOUCH_INT
31	PA10	MFX_GPIO10	DSI_RESET
32	PA11	MFX_GPIO11	EXT_RESET
33	PA12	MFX_GPIO12	DCMI_PWR_EN
34	PA13	MFX_SWDIO	MFX_SWDIO
37	PA14	MFX_SWCLK	MFX_SWCLK
38	PA15	MFX_IDD_SH3	SH3
18	PB0	MFX_GPIO0	LED_ORANGE
19	PB1	MFX_GPIO1	JOY_UP
20	PB2	MFX_GPIO2	JOY_DOWN
39	PB3	MFX_GPIO3	JOY_RIGHT
40	PB4	MFX_GPIO4	JOY_LEFT
41	PB5	MFX_IDD_VDD_MCU	IDD_VDD_MCU
42	PB6	MFX_I2C_SCL	I2C1_SCL from main MCU
43	PB7	MFX_I2C_SDA	I2C1_SDA from main MCU
45	PB8	MFX_I2C_ADDR	I2C_ADDR (external pull-down)

Table 30. MFX_V3 GPIO assignment (LQFP48) (continued)

Pin	GPIO port	Implemented functions	Application function name
46	PB9	MFX_IRQ_OUT	MFX_IRQ_OUT
21	PB10	-	-
22	PB11	-	-
25	PB12	MFX_IDD_MEAS	IDD_MEAS
26	PB13	MFX_GPIO13	USB_OTGFS_PPWR_EN
27	PB14	MFX_GPIO14	USB_OVER
28	PB15	MFX_GPIO15	AUDIO_Codec_RESET
2	PC13-ANTI_TAMP	MFX_WAKEUP	MFX_WAKEUP
3	PC14-OSC32_IN	MFX_IDD_CAL	CAL
4	PC15-OSC32_OUT	MFX_IDD_SH0	SH0
5	PH0-OSC_IN	MFX_IDD_SH1	SH1
6	PH1-OSC_OUT	MFX_IDD_SH2	SH2



Appendix B Solder bridges

Following [Table 31](#) describes each solder bridge. The default state is indicated in bold. ON state means a 0-ohm resistor is soldered. OFF state means SBxx is open.

Table 31. 32L4R9IDISCOVERY solder bridges

Solder bridges	State	Description
SB2 (ARD_D13 Green LED)	ON	Enables ARD Green LED control by ARD_D13
	OFF	Disables ARD Green LED
SB27 (ARD_AVDD on VREF+)	ON	Connects VREF+ from MCU to ARD_AVDD
	OFF	ARD_AVDD not connected
SB32, SB34 (I2C3 on ARD_A4/A5)	OFF	I2C3 disconnected from ARD_A4/A5, exclusive with SB33, SB35
SB33, SB35 (ADCs on ARD_A4/A5)	ON	ADCs inputs connected to ARD_A4/A5, exclusive with SB32, SB34
SB7, SB13 (USART3 on DSI display)	OFF	Disconnects USART3_CK/TX from pins 24/26 of DSI V3 connector, exclusive with SB6 and SB8
SB6, SB8 (SPI2 on DSI display)	ON	Connects SPI2_SCK/MOSI to pins 24/26 of DSI V3 connector, exclusive with SB7 and SB13
SB23 (VDD on OCTOSPI Flash)	ON	Connects OCTOSPI Flash power rails to VDD
	OFF	Disconnects VDD from OCTOSPI Flash
SB25 (OCTOSPI_ECS)	ON	ECS function active (need external pull-up)
	OFF	ECS function not active (no external pull-up)
SB24 (OCTOSPI_RESET)	ON	OCTOSPI Flash Reset is connected to General Reset of Board
	OFF	OCTOSPI Flash Reset not connected to General Reset of Board
SB1 (DFSDM_1_DATIN1)	ON	PB12 (DFSDM_1_DATIN1) is connected to Digital Microphones by default
	OFF	PB12 (DFSDM_1_DATIN1) is usable by STMod+ on pin 17
SB3 (RESERVED)	ON	Reserved, but removable if necessary (PSRAM_A20 to U6)
SB4 (RESERVED)	OFF	Reserved, do not modify (PSRAM_A20 to VDD)
SB16, SB17, SB18, SB19, SB20, SB21 (RESERVED)	OFF	Reserved, (STMod+/PMOD)
SB36 (RESERVED)	OFF	Reserved, (STLINK)

**Table 31. 32L4R9IDISCOVERY solder bridges (continued)**

Solder bridges	State	Description
SB5 (RESERVED)	ON	Reserved, do not modify (PSRAM)
SB14 (RESERVED)	ON	Reserved, do not modify (STLINK)
SB9, SB10, SB11, SB12 (RESERVED)	ON	Reserved, do not modify (display)
SB15 (RESERVED)	ON	Reserved, (USB OTG FS)
SB30 (RESERVED)	ON	Reserved, (Audio codec VL)
SB29 (RESERVED)	ON	Reserved, (Audio codec VD)
SB31 (RESERVED)	ON	Reserved, do not modify (MFX, IDD_VDD_MCU)
SB22 (RESERVED)	ON	Reserved, do not modify (STMod+/PMOD)
SB26 (RESERVED)	ON	Reserved, (OCTOSPI Flash)
SB37 (RESERVED)	ON	Reserved, (EXT_I2C)
SB28 (RESERVED)	OFF	Reserved, (MCO to HSE input)
SB38 (RESERVED)	ON	Reserved, (for U5 PSRAM)
SB39 (RESERVED)	OFF	Reserved, (for U6 PSRAM)

Appendix C STMod+ GPIO sharing and multiplexing

Table 32. STMod+ GPIO sharing and multiplexing

Shared or exclusive functions				STMod+ ⁽¹⁾							Shared or exclusive functions						
DSI	ARD	PMOD	Some other Alternate Functions ⁽²⁾	Basic	SB ⁽³⁾	Port	Pins	Port	SB	Basic	Some other Alternate Functions ⁽²⁾	PMOD	ARD	CAM	Dig Mic		
-	-	CTSS3 / CSN2	LCTS1 / T3.1 / T16.1 / [OP2_]+ / AD1.11]	CTSS3 / CSN2	-	PA6	1	-	11	PC6	-	INT	SA2.MCKA / DF1.C3 / T3.1 / T8.1	INT	-	D0	-
TXS3 MOSI2	MOSI2/T15.2	TXS3 MOSI2	LRX1 / T2.3 / SCL2 / SCL4 / DF1.D7 / [CP1_O] DF1.C2 / T1.3N / T8.3N / T15.2 / SA2.SDA / RTC_RFIN	TXS3 MOSI2	20 21	PB10 PB15	2		12	PI7	-	RST	T8.3	RST	-	D7	-
DC/X	MISO2	RXS3 MISO2	SDA2 / SDA4 / LTX1 / DF1.C7 / T2.4 / [CP2_O] SA2.MCKA / SDA2 / RTSS3 / DF1.D2 / T1.2N / T8.2N / T15.1	RXS3 MISO2	16 17	PB11 PB14	3		13	PA4	-	ADC	LT2.O / [AD1.9 / DAC1.1]	-	D7	HSYNC	-
SCK2	SCK2	RTSS3 SCK2	SA2.FSB / RXS2 / RTS4 / T2.1 / T2.E SCL2 / CTSS3 / LCTS1 / DF1.C1 / T1.1N / T15.1N / TXC2 / SA2.SCKA	RTSS3 SCK2	18 19	PA15 PB13	4		14	PA5	-	PWM	SCK1 / T2.1 / T8.1N / [AD1.10 / DAC1.2]	-	A5	-	-
-	-	-	-	GND	-	GND	5		15	+5V	-	+5V	-	-	-	-	-
-	-	-	-	+5V	-	+5V	6		16	GND	-	GND	-	-	-	-	-
-	SCL3	-	DF1.CO / LTX1	SCL3	-	PG7	7		17	PB12	-	GPIO	NSS2 / SA2.FSA / SMBA2 / CKS3 / LRTS1 / RXC2 / DF1.D1	-	-	-	DF1.D1
-	-	-	T8.E	MOSI2	-	PI3	8		18	PC2*	-	GPIO	DF1.CO / MISO2 / LT1.2 / [AD1.3]	-	-	-	DF1.CO
-	-	-	T8.4	MISO2	-	PI2	9		19	PC7	-	GPIO	T3.2 / T8.2 / DF1.D3	-	-	D1	-
-	SDA3	-	LRX1	SDA3	-	PG8	10		20	PC2*	-	GPIO	same as pin 18	-	-	-	DF1.CO
Legend: = DSI = Arduino Uno = Pmod = Alternate Functions = STMod+ = CAM = Digital Microphone = Supply = GND																	

- This [Table 32](#) gives description of the signals available on the STMod+ connector. It also shows which signal is shared with other board connector or function. In some boards, Solder bridges (SB) are present to manually select which function is wired by default (but here, refer to point (3) below). Analog signals are in brackets [xxx]. The I²C bus on pins 7 / 10 might be shared with built-in discovery slave devices. Check the slave address of your device when adding it to the bus.
- RTSS3 stands for USART3_RTS
 AD1.3 stands for ADC_1_IN3
 T1.3N stands for TIM_1_CH3N
 DAC1.1 stands for DAC_1_OUT1
 MOSI2 stands for SPI2_MOSI
 RST stands for RESET
 INT stands for INTERRUPT
 DF1.C3 stands for DF1.C3
 SDA3 stands for I2C3_SDA
 LTX1 stands for LP_UART1TX
 LT2.O stands for LPTIM2_OUT
 NSS2 stands for SPI2_NSS
 RXC1 stands for CAN_1_RX
 SA2.SCKA stands for SAI2_SCLK_A
- The solder bridges (SB) are available on PCB to select chosen Port, but they are not used by default: Instead of SB, an embedded SPDT quad switch is used to select Port. It is controlled by 2 GPIOs from the MFX_V3 Expander (STMOD+_SEL_0 and _1), refer to [Table 33](#) description below (Bold text is default configuration to support mikroBUS™ modules using MB1280 fan-out board)

Table 33. SPDT quad switch

	SPI	UART / SPI	UART	
STMOD+_SEL_0	0	1	1	STMOD+_SEL_0 is GPIO6 of MFX_V3
STMOD+_SEL_1	0	0	1	STMOD+_SEL_1 is GPIO7 of MFX_V3
pin 1	CSN2	CSN2	CTS3	pin 1 is connected directly to PA6
pin 2	MOSI2	TXS3	TXS3	
pin 3	MISO2	RXS3	RXS3	
pin 4	SCK2	SCK2	RTSS3	

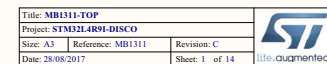
Appendix D Schematics

This section provides design schematics for the 32L4R9IDISCOVERY mainboard and design schematics of the round DSI display and fanout boards:

Appendix D contains the schematics diagrams listed below:

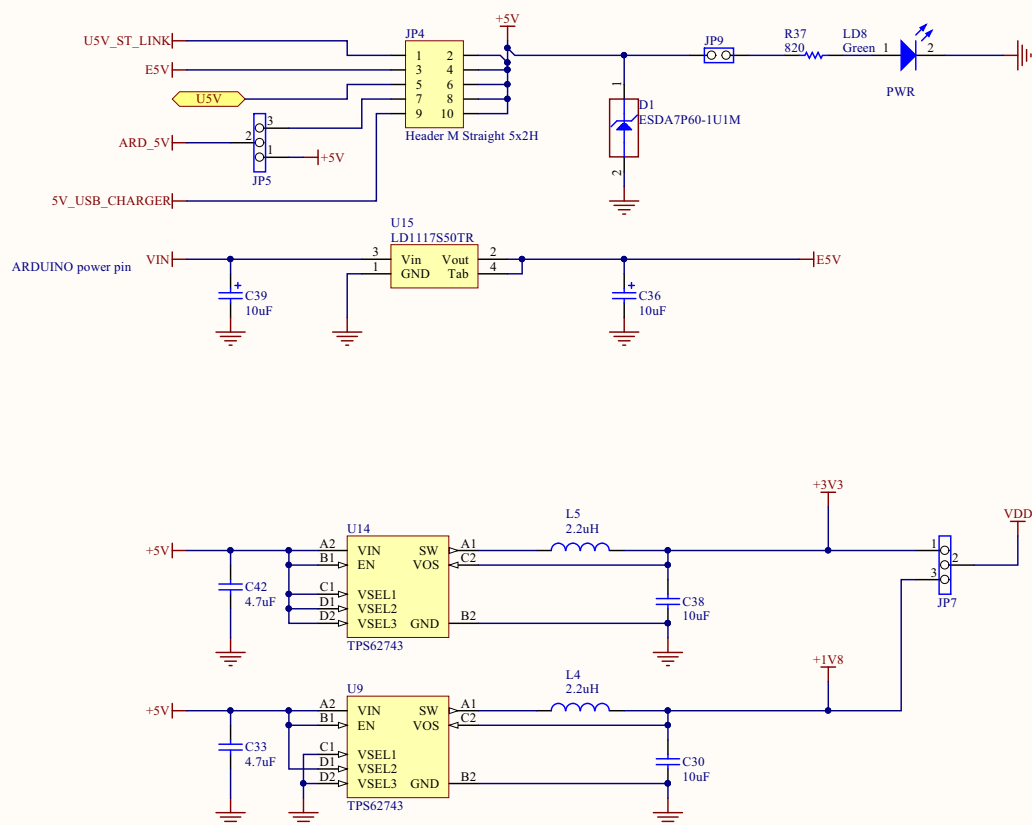
- [*Figure 20: 32L4R9IDISCOVERY board interconnections \(MB1311C\)*](#)
- [*Figure 21: 32L4R9IDISCOVERY power*](#)
- [*Figure 22: 32L4R9IDISCOVERY ARDUINO® Uno V3 connectors*](#)
- [*Figure 23: 32L4R9IDISCOVERY ST-LINK/V2-1*](#)
- [*Figure 24: 32L4R9IDISCOVERY Octo-SPI Flash memory*](#)
- [*Figure 25: 32L4R9IDISCOVERY peripherals*](#)
- [*Figure 26: 32L4R9IDISCOVERY USB OTG FS*](#)
- [*Figure 27: 32L4R9IDISCOVERY Round DSI display interface*](#)
- [*Figure 28: 32L4R9IDISCOVERY IDD measurement and Multi Function eXpander*](#)
- [*Figure 29: 32L4R9IDISCOVERY microcontroller*](#)
- [*Figure 30: 32L4R9IDISCOVERY PSRAM*](#)
- [*Figure 31: 32L4R9IDISCOVERY camera*](#)
- [*Figure 32: 32L4R9IDISCOVERY STMOD+ interface*](#)
- [*Figure 33: 32L4R9IDISCOVERY Audio and DFSDM*](#)
- [*Figure 34: Round DSI display board \(MB1314\)*](#)
- [*Figure 35: Fanout board \(MB1280\)*](#)

Schematics



UM2271

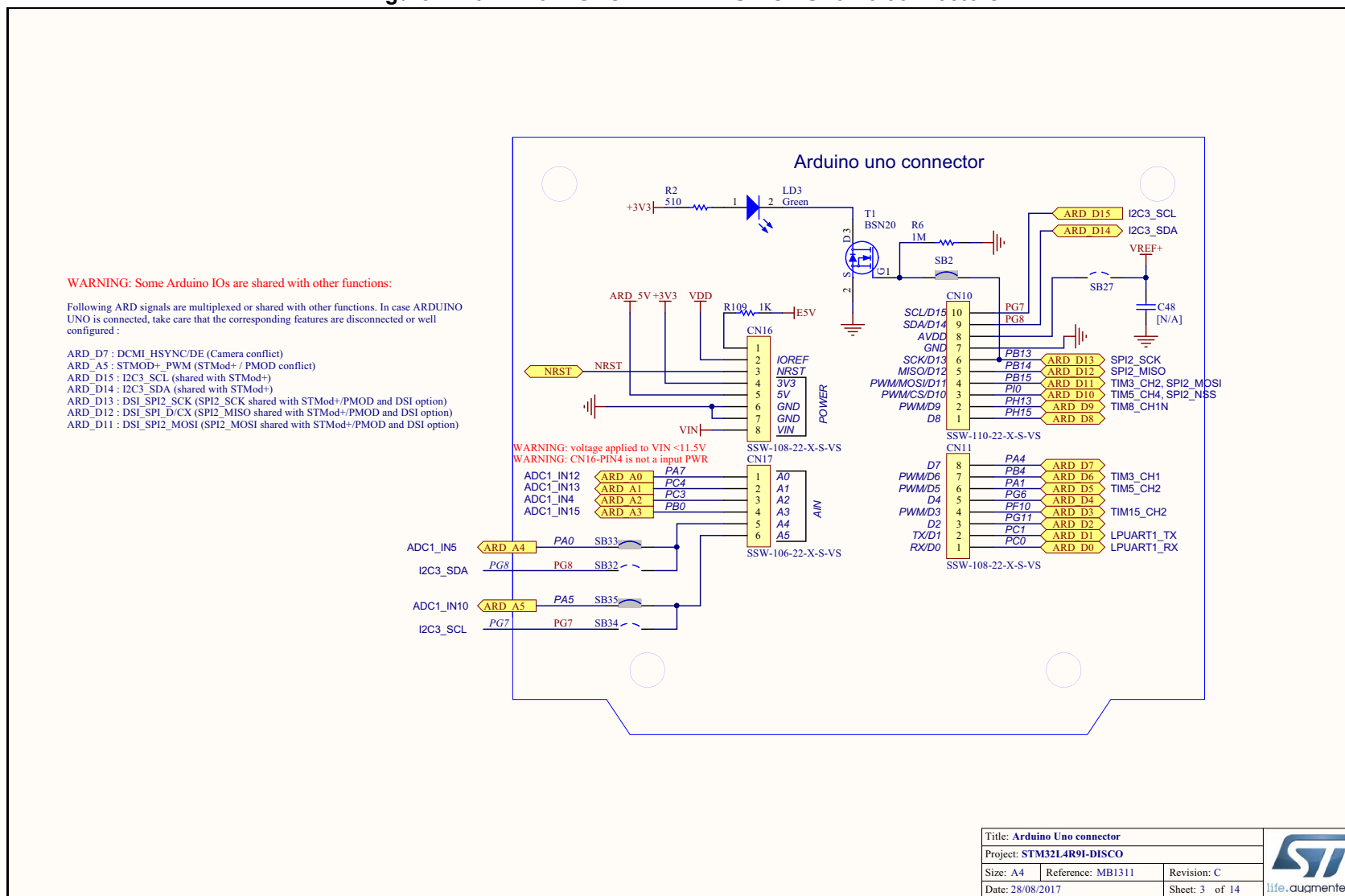
Figure 21. 32L4R9IDISCOVERY power



Title: Power			 life.augmented.com
Project: STM32L4R91-DISCO			
Size: A4	Reference: MBI311	Revision: C	
Date: 28/08/2017		Sheet: 2 of 14	

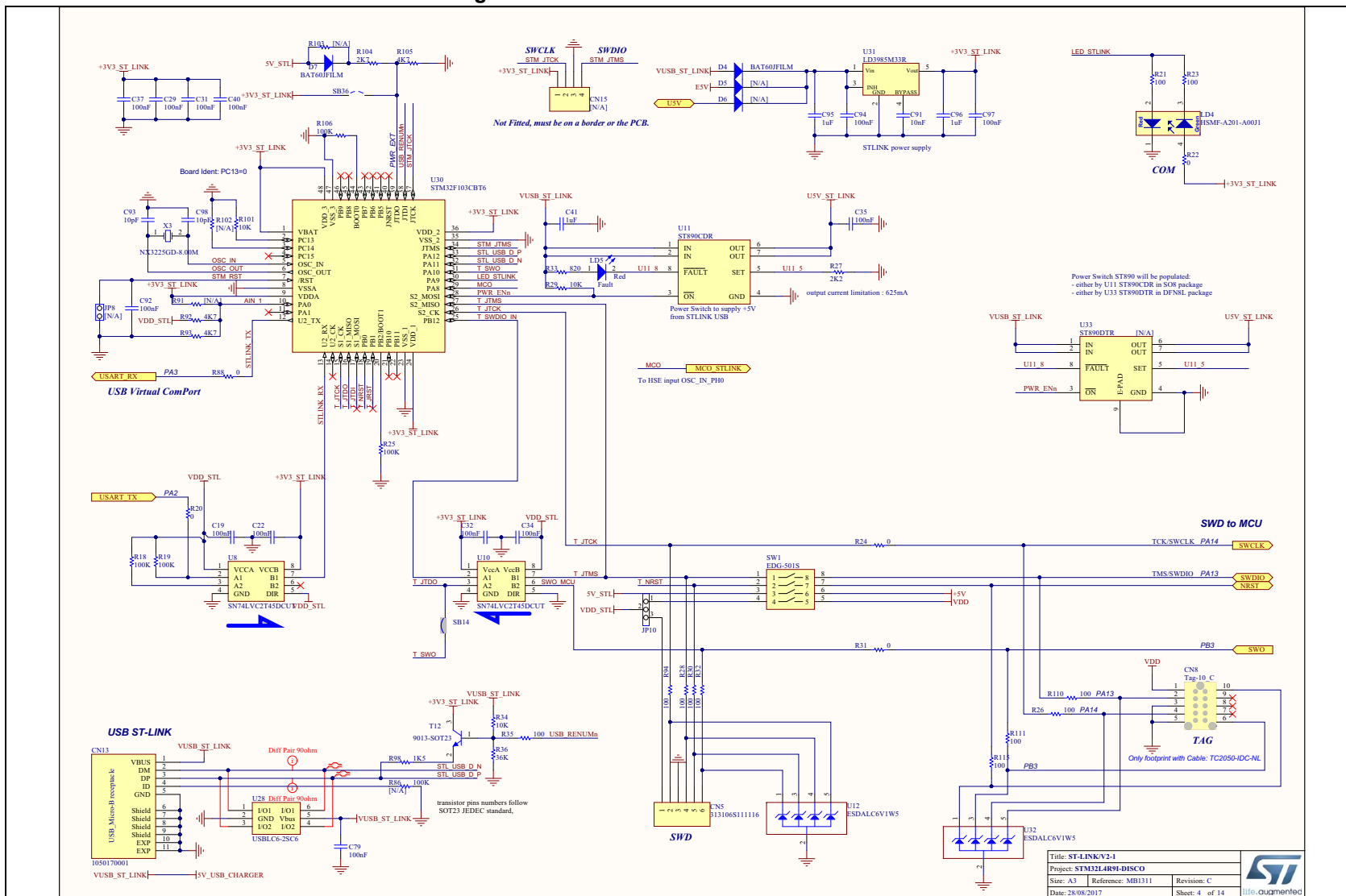
Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 22. 32L4R9IDISCOVERY ARDUINO® Uno V3 connectors



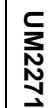
Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 23. 32L4R9IDISCOVERY ST-LINK/V2-1



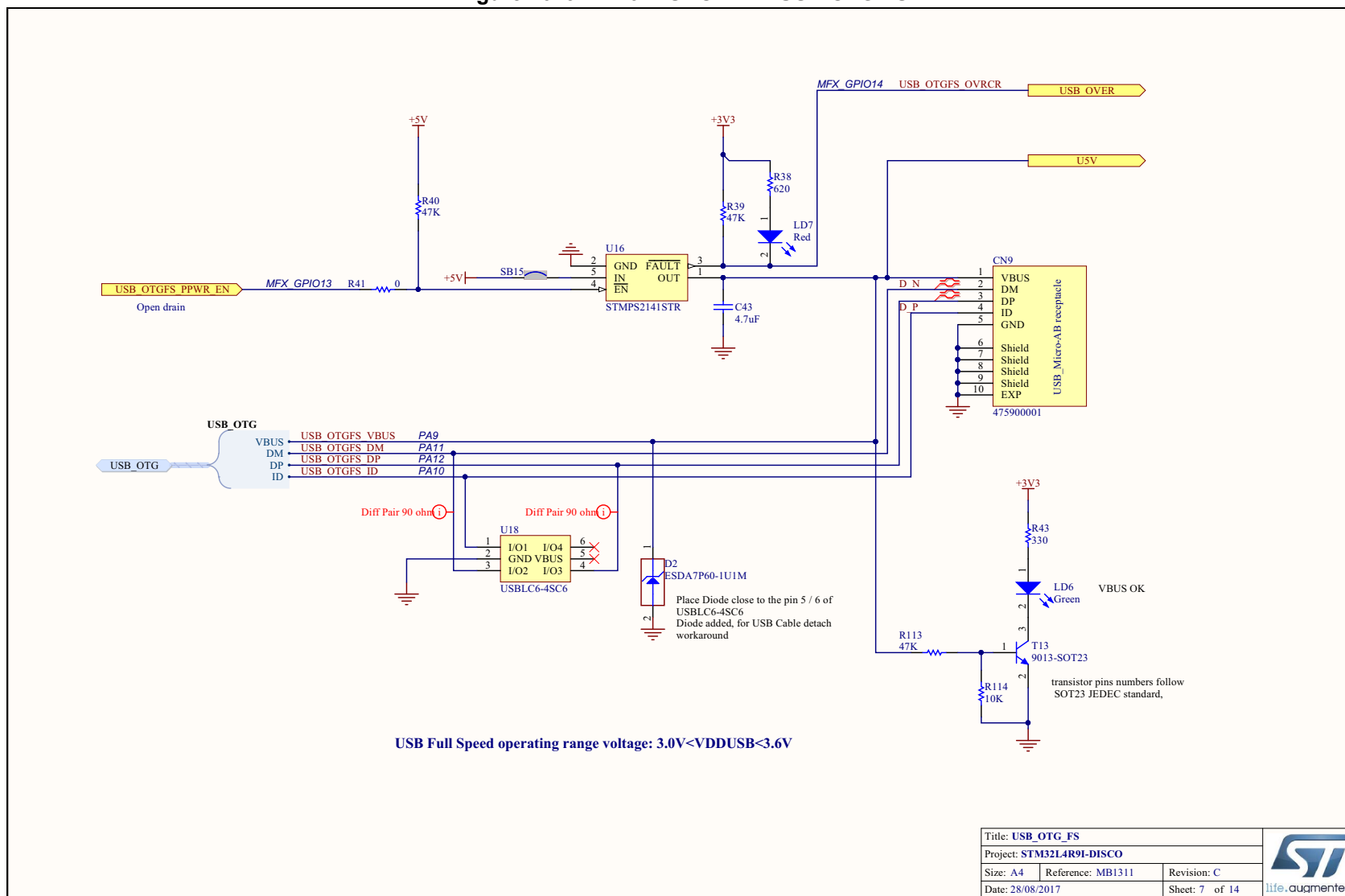
Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Schematics



Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 26. 32L4R9IDISCOVERY USB OTG FS



Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 27. 32L4R9IDISCOVERY Round DSI display interface

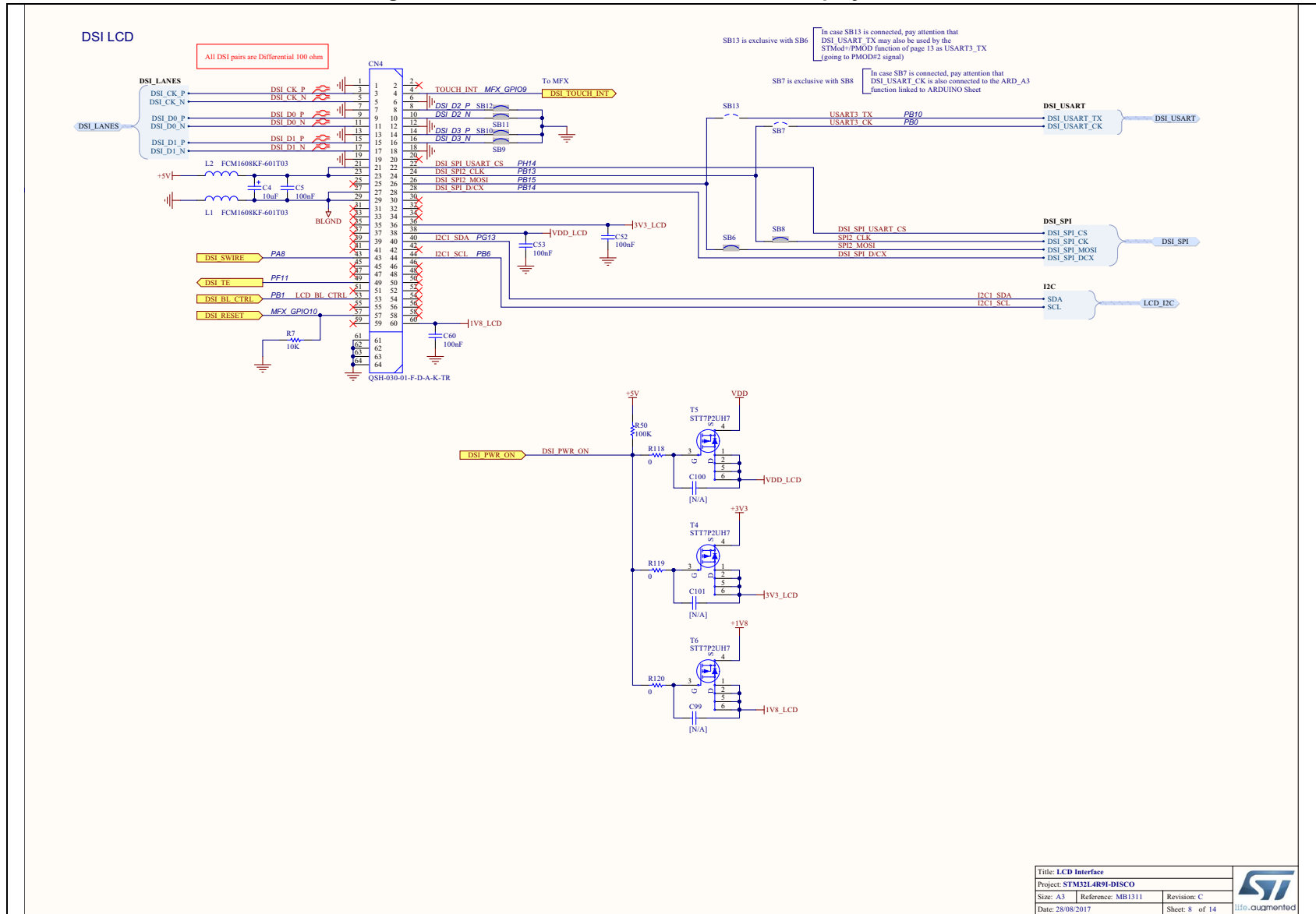
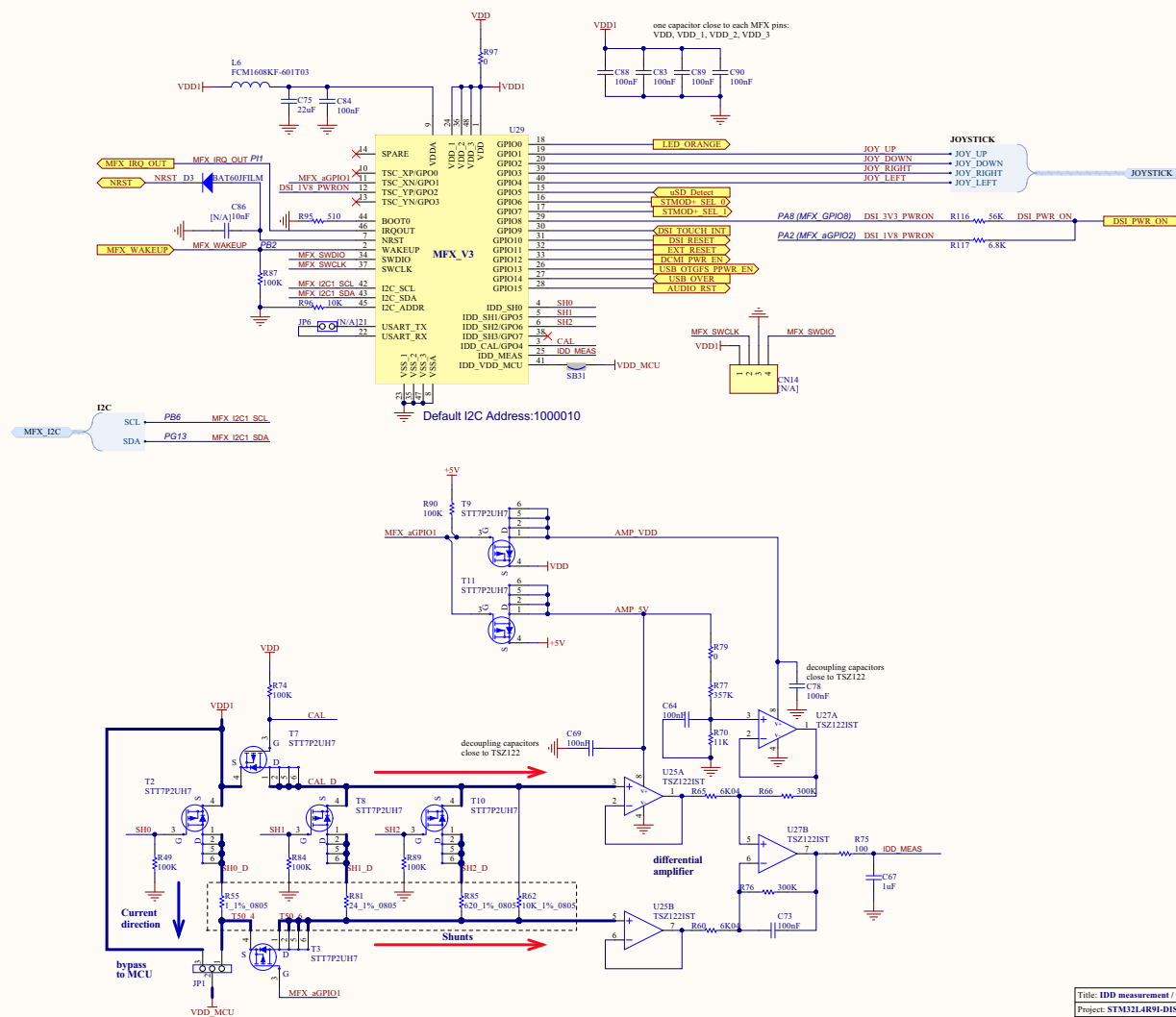


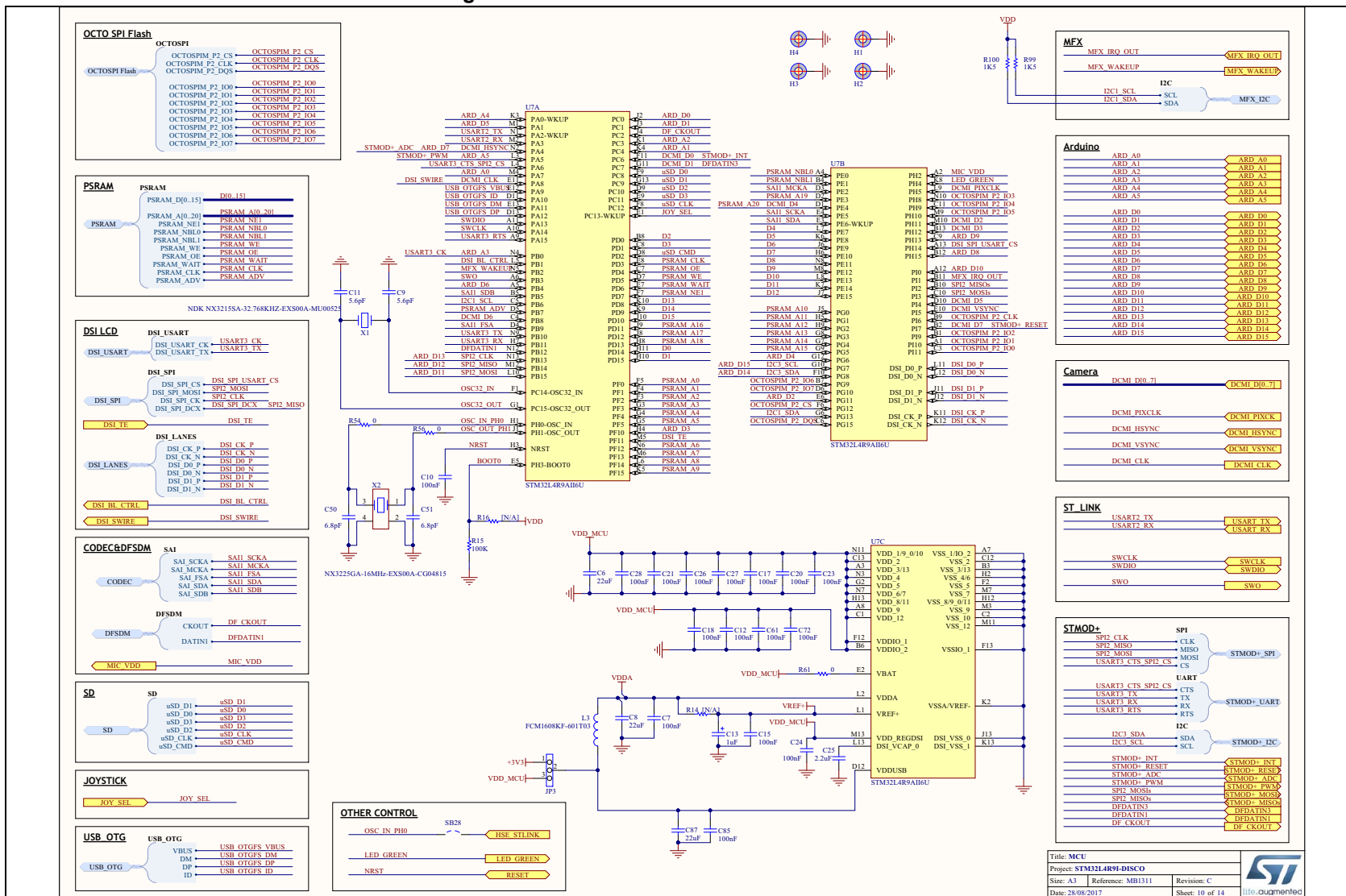
Figure 28. 32L4R9IDISCOVERY IDD measurement and Multi Function eXpander



Note:

The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 29. 32L4R9IDISCOVERY microcontroller



Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

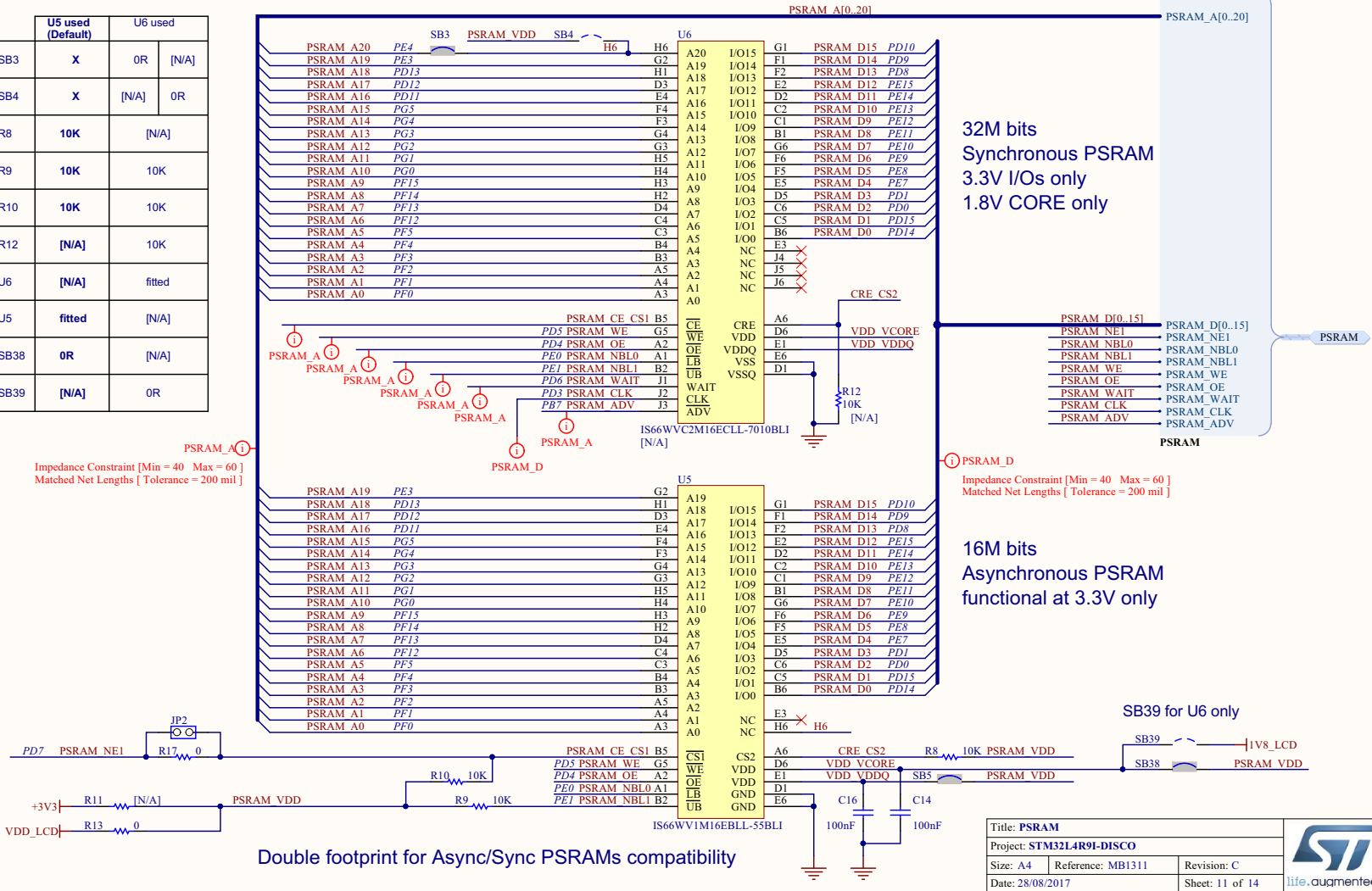


Figure 30. 32L4R9IDISCOVERY PSRAM

SB3 and SB4 are only useful for U6 : If SB3 is fitted, CAMERA and PSRAM functions are exclusives; if SB4 fitted, PSRAM usable memory density is reduced to 16M bits

	U5 used (Default)	U6 used	
SB3	X	0R	[N/A]
SB4	X	[N/A]	0R
R8	10K	[N/A]	
R9	10K	10K	
R10	10K	10K	
R12	[N/A]	10K	
U6	[N/A]	fitted	
U5	fitted	[N/A]	
SB38	0R	[N/A]	
SB39	[N/A]	0R	

PSRAM_A1
Impedance Constraint [Min = 40 Max = 60]
Matched Net Lengths [Tolerance = 200 mil]



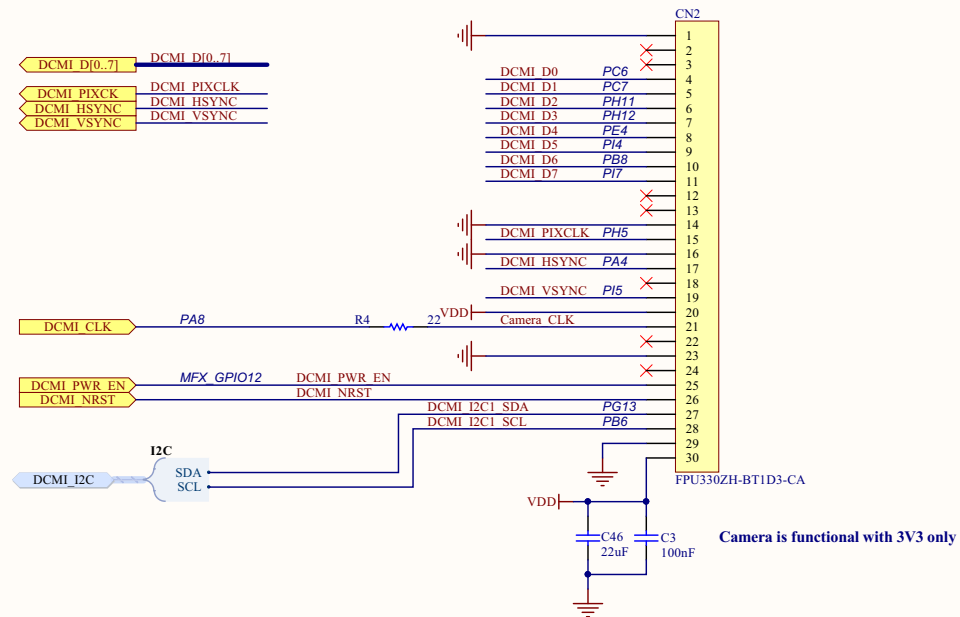
Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 31. 32L4R9IDISCOVERY camera

CAMERA is exclusive with some STMod+ , PMOD and ARDUINO signals

CAUTION : Following DCMI signals are multiplexed with other functions. In case CAMERA module is plugged, take care that the corresponding features are disconnected or well configured :

DCMI_D0 : STMod+ _INT
DCMI_D1 : DFDATIN3 (STMod+)
DCMI_D4 : PSRAM_A20 (only in case of U6 PSRAM is used)
DCMI_D6 : STMod+ _PWM
DCMI_D7 : STMod+ _RESET
DCMI_HSYNC/DE : STMod+ _ADC and ARD_D7



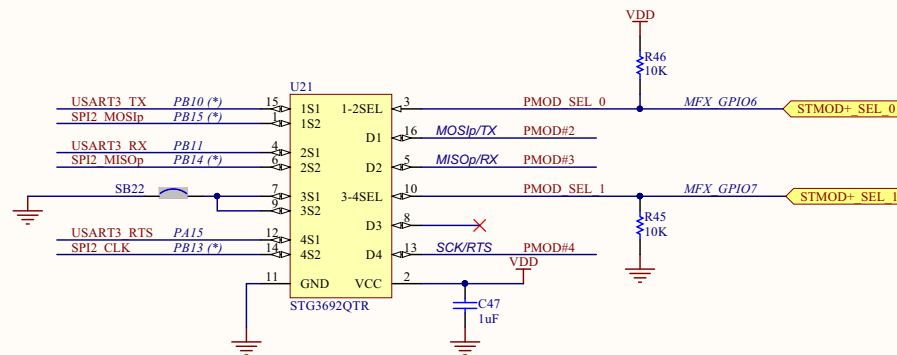
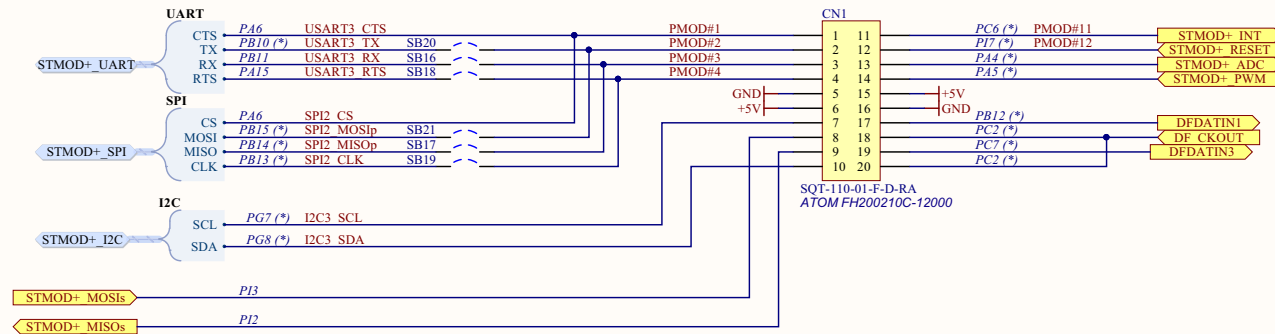
Title: Camera		
Project: STM32L4R9I-DISCO		
Size: A4	Reference: MB1311	Revision: C
Date: 28/08/2017	Sheet: 12 of 14	life.augmented


Figure 32. 32L4R9IDISCOVERY STMOD+ interface

CAUTION : Following STMod+/PMOD signals are multiplexed or shared with other functions. In case STMod+/PMOD module is plugged, take care that the corresponding features are disconnected or well configured :

(*)
 STMOD+/PMOD USART3_TX (PB10) may also use DSI_USART_TX option
 STMOD+/PMOD SPI2_MOSIp (PB15) shared with ARD_D11 and DSI_SPI2_MOSI option
 STMOD+/PMOD SPI2_MISO (PB14) shared with ARD_D12 and DSI_SPI2_DCX option
 STMOD+/PMOD SPI2_SCK (PB13) shared with ARD_D13 and DSI_SPI2_SCK option
 STMOD+ I2C3_SCL (PG7) shared with ARD_D15 (I2C3_SCL)
 STMOD+ I2C3_SDA (PG8) shared with ARD_D14 (I2C3_SDA)

(*)
 STMOD+ INT (PC6) in conflict with DCM1_D0 (Camera)
 STMOD+ RESET (PI7) in conflict with DCM1_D7 (Camera)
 STMOD+ ADC (PA4) in conflict with ARD_D7 and DCM1_HSYNC (Camera)
 STMOD+ PWM (PA5) in conflict with ARD_A5
 STMOD+ DFDATIN1 (PB12) in conflict with MEMs microphones (use SB1 in audio page)
 STMOD+ DF_CKOUT (PC2) in conflict with MEMs microphones
 DFDATIN3 (PC7) in conflict with DCM1_D1 (Camera)



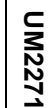
	SPI	UART/SPI	UART
STMOD+ SEL 0	0	1 (*)	1
STMOD+ SEL 1	0	0 (*)	1
PMOD#1 (PA6)	CS	CS	CTS
PMOD#2	MOSIp	TX	TX
PMOD#3	MISO	RX	RX
PMOD#4	SCK	SCK	RTS

(*) default configuration to support MikroBus modules using MB1280 fan-out board

Title: STMOD+ Interface		
Project: STM32L4R9I-DISCO		
Size: A4	Reference: MB1311	Revision: C
Date: 28/08/2017	Sheet: 13 of 14	life.augmented

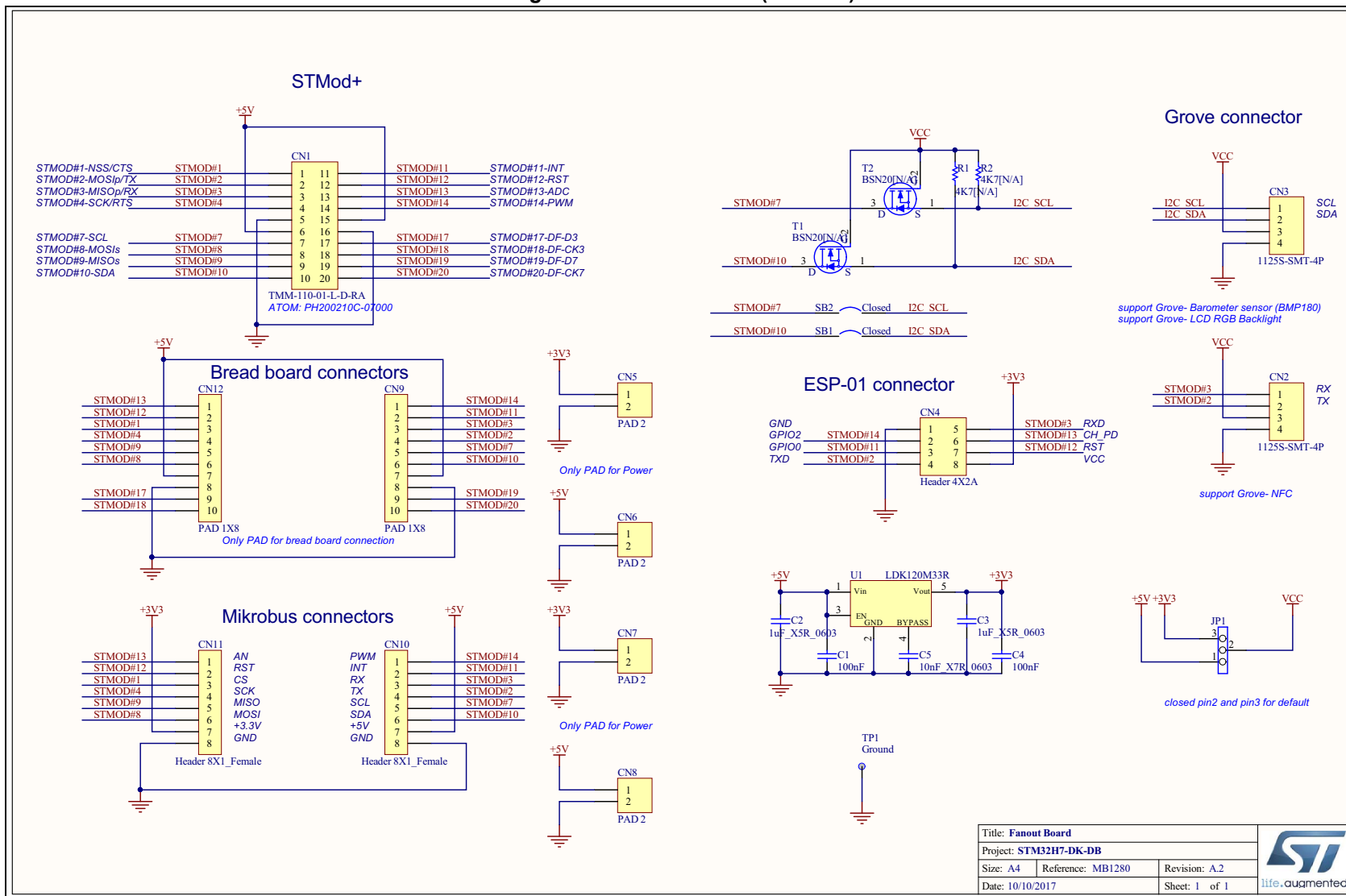
Note: The STM32L4R9I-DISCO may use a different MB1311 board revision than C-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Schematics



Note: The STM32L4R9I-DISCO may use a different MB1314 board revision than B-01. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

Figure 35. Fanout board (MB1280)



Note: The STM32L4R9I-DISCO may use a different MB1280 board revision than A-02. Refer to Hardware Resources of STM32L4R9I-DISCO available on www.st.com for relevant documentation.

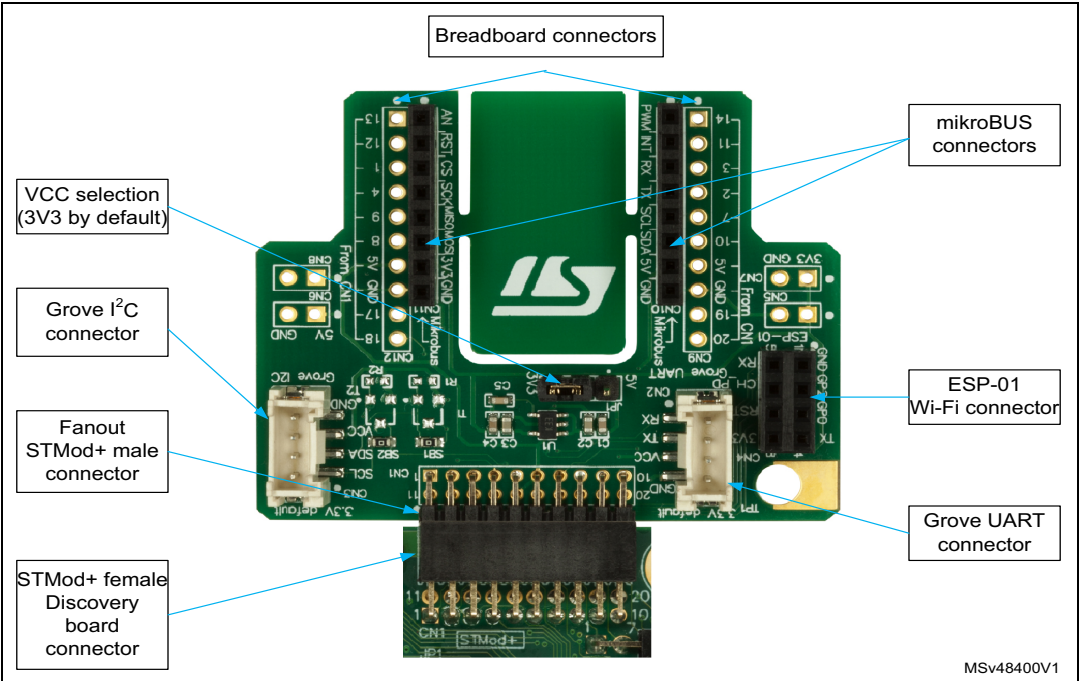
Appendix E Fanout board (MB1280)

The fanout board (Refer to [Figure 36](#)) is included in the 32L4R9IDISCOVERY kit. It is connectible to STMod+ connector (CN1) and it provides access to:

- MikroElektronika Click board compatible connectors (CN10 and CN11: two 1x8-pin female connectors)
- ESP-01 compatible connector (CN4: 2x4-pin female connector)
- Seeed Studio™ Grove compatible connectors (CN3 and CN2: two 1x4-pin male connectors)
- Reserved standard 2.54 mm pitch of STMod+ pin header for breadboard.

The main active component for this fanout board is the 3.3 V regulator U1 (200 mA).

Figure 36. STMod+ fanout module plugged into CN1 connector



E.1 MikroElektronika mikroBUS™ compatible connector (Fanout CN10 / CN11)

The mikroBUS™ compatible connector is 2.54 mm pitch with a pair of 1x8-pin female connectors. [Table 34](#) shows the definition of the pins.

Table 34. Description of the mikroBUS™ connectors (CN11 and CN10)⁽¹⁾

STMod+ connector CN11 number	Function of mikroBUS	Pin number	Pin number	Function of mikroBUS	STMod+ connector CN10 number
STMod+#13-ADC	AN	1	1	PWM	STMod+#14-PWM
STMod+#12-RST	RST	2	2	INT	STMod+#11-INT

Table 34. Description of the mikroBUS™ connectors (CN11 and CN10)⁽¹⁾ (continued)

STMod+ connector CN11 number	Function of mikroBUS	Pin number	Pin number	Function of mikroBUS	STMod+ connector CN10 number
STMod+#1-CS	CS	3	3	RX	STMod+#3-RX
STMod+#4-SCK	SCK	4	4	TX	STMod+#2-TX
STMod+#9-MISOs	MISO	5	5	SCL	STMod+#7-SCL
STMod+#8-MOSIs	MOSI	6	6	SDA	STMod+#10-SDA
-	+3.3 V	7	7	+5 V	STMod+#6#15 +5V
STMod+#5#16 GND	GND	8	8	GND	STMod+#5#16 GND

1. Refer to [Appendix C](#) to check STMod+ pin sharing with other functions of the 32L4R9IDISCOVERY

The mikroBUS™ pinout assignment is available at the: <http://mikroe.com> website.

E.2 ESP-01 Wi-Fi® board compatible connector

The ESP-01 Wi-Fi board connector is 2.54 mm pitch with 2x4-pin female connectors. [Table 35](#) shows the definition of the pins.

Table 35. Description of the ESP-01 Wi-Fi board connector pins⁽¹⁾

STMod+ connector number	Function of ESP-01	Pin number	Pin number	Function of ESP-01	STMod+ connector number
STMod+#5#16 GND	GND	1	8	TXD	STMod+#3-RX
STMod+#14	GPIO2	2	7	CH_PD	STMod+#13
STMod+#11	GPIO0	3	6	RST	STMod+#12-RST
STMod+#2-TX	RXD	4	5	VCC	-

1. Refer to [Appendix C](#) to check STMod+ pin sharing with other functions of the 32L4R9IDISCOVERY.

E.3 Compatible connectors for the Grove boards

The two connectors of the Grove board are 2.54 pitch with 1x4-pin male connectors, the part number is 1125S-SMT-4P.

E.3.1 Compatible connector for I²C Grove boards (Fanout CN3)

The CN3 connector is compatible with Grove- Barometer sensor (BMP180) and Grove-LCD RGB Backlight boards using a cable for connection. [Table 36](#) shows the definition of the pins.

Note the following limitations linked to Grove connector:

- MB1280A & MB1280B Grove connector does not support the 5V I²C interface.
- MB1280C can support the 5V I²C interface for the Grove connector, but users must solder the MOSFETs and related matched resistors by themselves.
- MB1280C board only supports 3V3 to 3V3 or 3V3 to 5V I²C interface. MB1280A & MB1280B Grove connector does not support the 5V I²C interface.

Table 36. Description of the I²C Grove board connector pins (CN3)⁽¹⁾

STMod+ connector NO.	Function of Grove CN3	Pin number
STMod+#7-SCL	SCL	1
STMod+#10-SDA	SDA	2
STMod+#6#15 +5 V	VCC	3
STMod+#5#16 GND	GND	4

1. Refer to [Appendix C](#) to check STMod+ pin sharing with other functions of the 32L4R9IDISCOVERY.

E.3.2 Compatible connector for UART Grove boards (Fanout CN2)

The CN2 connector is compatible with Grove-NFC boards using a cable for connection.

[Table 37](#) shows the definition of the pins.

Table 37. Description of the UART Grove board connector pins (CN2)⁽¹⁾

STMod+ connector	Function of Grove CN2	Pin number
STMod+#3-RX	RX (Grove TX)	1
STMod+#2-TX	TX (Grove RX)	2
STMod+#6#15 +5 V	VCC	3
STMod+#5#16 GND	GND	4

1. Refer to [Appendix C](#) to check STMod+ pin sharing with other functions of the 32L4R9IDISCOVERY.

Appendix F Federal Communications Commission (FCC) and Industry Canada (IC) Compliance

This kit is designed to allow:

1. Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and
2. Software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product does not cause harmful interference to licensed radio stations and that this product accepts harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of 47 CFR, Chapter I ("FCC Rules"), the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

Revision history

Table 38. Document revision history

Date	Revision	Changes
17-Oct-2017	1	Initial version
26-Oct-2017	2	Updated: – Chapter 10.6.1 : clarification on SW1 use – Table 4 : pin name ARD-5V – Table 5 : JP4 CHGR position description – Table 28 : Unused functions – Table 30 : Reserved solder bridges
4-Jan-2018	3	Updated: – Figure 4 : JP1 description – Section 8 : bootloader limitation – Section 10.5 and Table 3 : SW1 – Section 10.6.1 and Table 4 : ARD and JP1 – Section 10.9 : boot configuration – Table 12 , Table 27 , Table 28 – Appendix F Added: – Section 10.13.2 and Section 11.3 : limitation Removed: – Appendix G
12-Feb-2020	4	Reorganized the entire document: – Updated: Features , Ordering information , and Development toolchains – Added Codification Added: – Compatibility and limitations with Grove I ² C connector in Section E.3.1 – Notes under Figure 20 to Figure 35 schematics regarding latest versions available on www.st.com

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