

Discovery kit with STM32G474RE MCU

Introduction

The B-G474E-DPOW1 Discovery kit is a digital power solution and a complete demonstration and development platform for the STMicroelectronics Arm® Cortex®-M4 core-based STM32G474RET6 microcontroller. Leveraging the new HRTimer-oriented features, 96 Kbytes of embedded RAM, math accelerator functions, and USB PD3.0 offered by STM32G474RET6, the B-G474E-DPOW1 Discovery kit helps users prototype applications with digital power such as a buck-boost converter, RGB power LED lighting, or Class-D audio amplifier, based on the USB Type-C® 2.0 FS connector interface. The B-G474E-DPOW1 Discovery kit does not require any separate probe as it integrates the STLINK-V3E debugger and programmer.

The STM32G474RET6 microcontroller features FMAC and CORDIC mathematical hardware accelerator, five 12-bit ADCs (5 MSPS) up to 42 channels and with resolution up to 16-bit with hardware oversampling, seven 12-bit DAC channels, seven ultra-fast rail-to-rail analog comparators, six operational amplifiers with PGA mode, seventeen timers with various advanced functionalities, four I²C fast-mode plus, five USARTs, one LPUART, four SPIs, one SAI, three CAN-FD controllers, one USB 2.0 full-speed interface and a UCPD block allowing connection to USB Type-C® compatible with USB Power Delivery, a true random number generator, one FMC parallel synchronous interface, a Quad-SPI memory interface, and SWD and JTAG debugging support.

This Discovery kit offers everything required for users to start and develop applications. The hardware features on the board help to evaluate the following peripherals: USB Type-C[®] compatible with USB PD3.0, HRTimer evaluation, digital power for buck-boost application with Class-D audio amplifier and RGB power LED lighting. Thanks to its two 32-pin 2.54 mm pitch extension connectors, it also enables users to plug it into a breadboard for prototyping. The integrated STLINK-V3E provides an embedded in-circuit debugger and programmer for the STM32 MCU.

The B-G474E-DPOW1 Discovery kit comes with the STM32 comprehensive free software libraries and examples available with the STM32CubeG4 STM32Cube package.



Figure 1. B-G474E-DPOW1 top view

Figure 2. B-G474E-DPOW1 bottom view



Pictures are not contractual.



1 Features

- STM32G474RET6 Arm[®] Cortex[®]-M4 core-based microcontroller, featuring 512 Kbytes of flash memory and 128 Kbytes of SRAM, in an LQFP64 package
- USB Type-C[®] with USB 2.0 FS interface compatible with USB-PD 3.0
- RGB power LED for bright lighting
- · Digital power buck-boost converter with internal or external input voltage and onboard resistor loads
- Audio Class-D amplifier capable
- 4 user LEDs
- 3 LEDs for power and ST-LINK communication
- 4-direction joystick with a selection button
- Reset push-button
- · Board connectors:
 - USB Type-C[®]
 - USB Micro-B
 - 2 x 32-pin header, 2.54 mm pitch, daughterboard extension connector for breadboard connection
- Flexible power-supply options: ST-LINK USB V_{BUS} or USB Type-C[®] V_{BUS} or external source
- On-board STLINK-V3E debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeG4 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench[®], MDK-ARM, and STM32CubeIDE
- Handled by STM32CubeMonitor-UCPD (STM32CubeMonUCPD) software tool

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2 Ordering information

To order the B-G474E-DPOW1 Discovery kit, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board references	Target STM32
B-G474E-DPOW1	MB1428 ⁽¹⁾	STM32G474RET6

^{1.} Subsequently called main board in the rest of the documentation.

2.1 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

B-XXYYZ-TN	Description	Example: B-G474E-DPOW1
В	Discovery kit	Discovery kit
XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32G4 series
YY	MCU product line in the series	STM32G4x4 product line
Z	STM32 flash memory size: E for 512 Kbytes	512 Kbytes
-T	Dedicated to application	Control board for DPOW (digital power) application
N	Sequential number	First board version

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3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable (not included)
- USB Type-C[®] to USB Type-C[®] cable (included)

Note:

macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.

Linux[®] is a registered trademark of Linus Torvalds.

Windows is a trademark of the Microsoft group of companies.

3.2 Development toolchains

- IAR Systems® IAR Embedded Workbench®(1)
- Keil® MDK-ARM⁽¹⁾
- STMicroelectronics STM32CubeIDE
- 1. On Windows® only.

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from www.st.com.

3.4 CAD resources

All board design resources, including schematics, CAD databases, manufacturing files, and the bill of materials, are available from the B-G474E-DPOW1 product page at www.st.com.

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4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition	
Jumper JPx ON	Jumper fitted	
Jumper JPx OFF	Jumper not fitted	
Jumper JPx [1-2]	Jumper fitted between pin 1 and pin 2	
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor	
Solder bridge SBx OFF	SBx connections left open	
Resistor Rx ON	Resistor soldered	
Resistor Rx OFF	Resistor not soldered	
Capacitor Cx ON	Capacitor soldered	
Capacitor Cx OFF	Capacitor not soldered	

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5 Safety recommendations

5.1 Targeted audience

This product targets users with at least basic electronics or embedded software development knowledge such as engineers, technicians, or students. This board is not a toy and is not suited for use by children.

5.2 Handling the board

This product contains a bare printed circuit board and like all products of this type, the user must be careful about the following points:

- The connection pins on the board might be sharp. Be careful when handling the board to avoid hurting yourself
- This board contains static-sensitive devices. To avoid damaging it, handle the board in an ESD-proof
 environment.
- While powered, do not touch the electric connections on the board with your fingers or anything conductive.
 The board operates at a voltage level that is not dangerous, but components might be damaged when shorted.
- Do not put any liquid on the board and avoid operating the board close to water or at a high humidity level.
- Do not operate the board if dirty or dusty.

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6 Quick start

This section describes how to start development quickly using the STM32 Discovery board.

Before installing and using the product, accept the evaluation product license agreement from the www.st.com/epla webpage.

The Discovery board is a low-cost and easy-to-use development kit to evaluate quickly and start development with an STM32 microcontroller in an LQFP64 package. To start using this board, follow the steps below:

- 1. To correctly identify all device interfaces from the host PC, install the Discovery USB driver available on the B-G474E-DPOW1 webpage, before connecting the board.
- 2. Check that jumpers JP4 and JP7 are ON, JP5 is set on STLK, JP6 is OFF, the octal switch (SW1) is set to ALL ON (low physical position), and JP1 is set on VIN USBPD pins.
- 3. Connect a Type-A to Micro-B USB cable (not included) from the STM32G474 Discovery board (CN3) to a PC to power the board. The 3V3 (LD6), 5V (LD7), and COM (LD9) LEDs light up.
- 4. User LEDs (LD2, LD3, LD4, and LD5) scroll, indicating the demonstration application software startup.
- 5. The demo application software and its user manual, as well as other software examples for exploring STM32G4 features are available at B-G474E-DPOW1.
- 6. Develop an application using the available examples.

STLINK-V3E firmware upgrade

The STLINK-V3E embeds a firmware upgrade mechanism for an in-place upgrade through the USB port. The firmware might evolve during the lifetime of the STLINK-V3E product, with new functionalities, bug fixes, and support for new microcontroller families. It is therefore recommended that you visit the *www.st.com* website before using the B-G474E-DPOW1 Discovery kit, and periodically, to keep up to date with the latest firmware version.

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7 Hardware layout and configuration

The B-G474E-DPOW1 Discovery kit is designed around the STM32G474RET6 microcontroller, in a 64-pin LQFP package. The hardware block diagram (refer to Figure 3) illustrates the connection between the microcontroller and the peripherals (RGB power LED and buck LED, digital power buck-boost, 5 V converter, embedded STLINK-V3E, USB Type-C® 2.0 FS, four user LEDs and a joystick as user interfaces, and 2 x 32-pin extension connector headers). Figure 4 and Figure 5 help to locate these features on the B-G474E-DPOW1 board.

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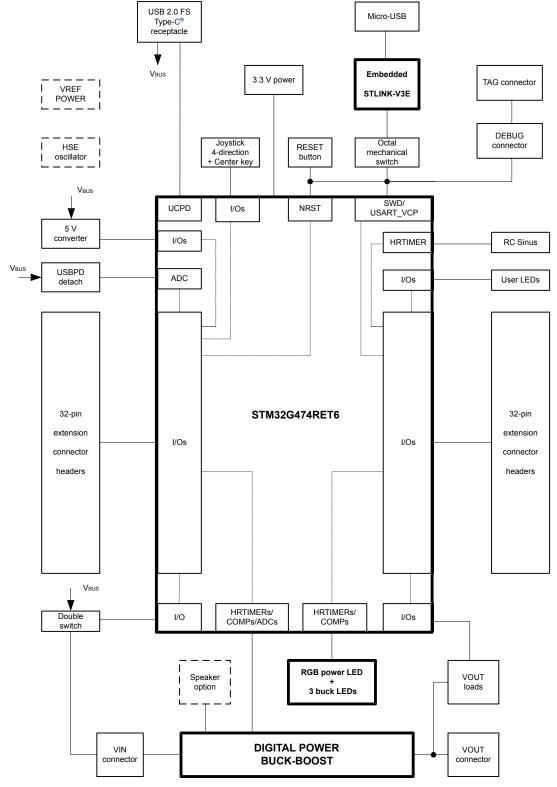


Figure 3. Hardware layout and configuration

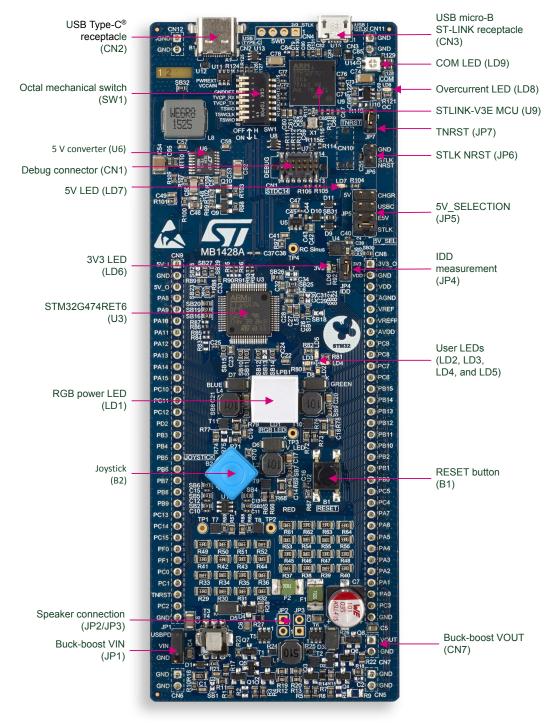
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7.1 Product layout (top and bottom)

Figure 4. B-G474E-DPOW1 top layout view

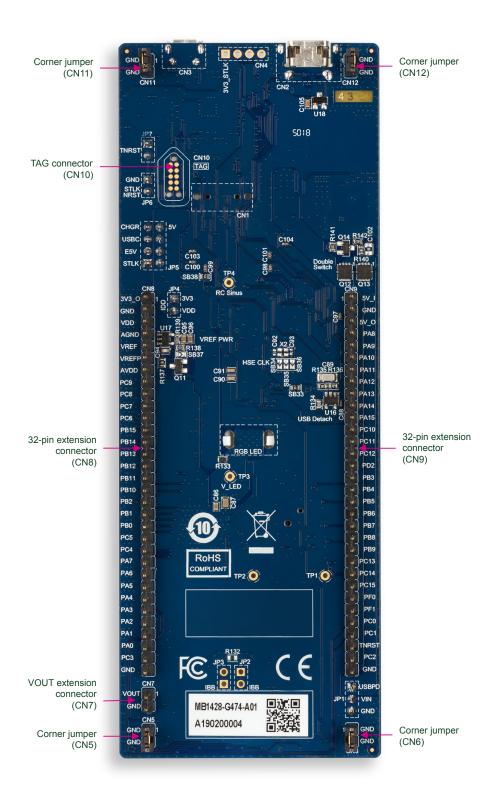


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Figure 5. B-G474E-DPOW1 bottom layout view



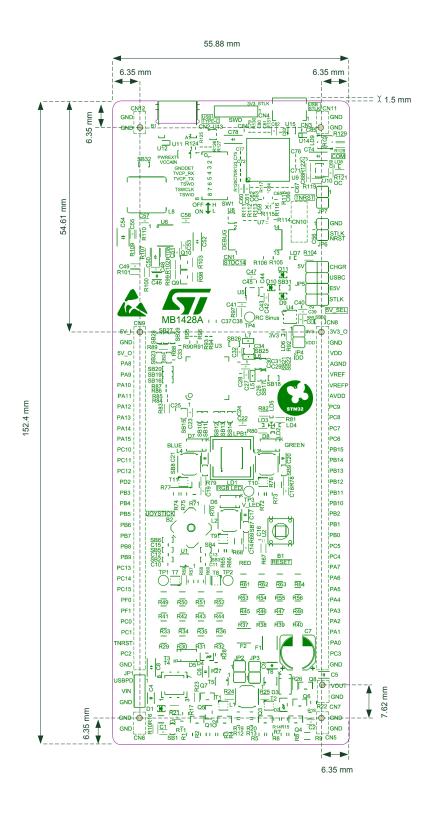
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7.2 Mechanical drawing

Figure 6. B-G474E-DPOW1 mechanical drawing



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8 Embedded STLINK-V3E

The new STLINK-V3E is the embedded version of the STLINK-V3 included in the design of the Discovery board. It allows access to the programming, debugging, and monitoring functions of the STM32 through the USB STLK connector (CN3).

To use the entire STLINK-V3E programming, debugging, and monitoring functions through the USB STLK connector (CN3), ensure that the following configuration is set on the STM32 target (refer to Figure 7):

- The octal mechanical switch (SW1) must be set to the ALL ON configuration: all the 1.27 mm pitch switches must be in a low physical position.
- The JP7 header must be equipped with a 2.54 mm jumper to connect the output reset from STLINK-V3E to the TNRST reset input of the STM32G474RET6.
- The JP6 header must be OFF to set STLINK-V3E in the Active mode.
- The JP4 header must be ON to power the STM32.
- The JP5 header must be ON (Power source selected and relevant power input connected as described in Section 9.2).
- The debug and TAG connectors (CN1 and CN10) are not used.

USB micro-B ST-LINK receptacle (CN3) Octal mechanical switch (SW1) **TNRST** (JP7) STLK NRST Debug connector (JP6) (CN1) 5V_SELECTION (JP5) IDD measurement (JP4)

Figure 7. Configuration to use STLINK-V3E

The B-G474E-DPOW1 product can be powered from the ST-LINK USB STLK connector (CN3), but the host PC only provides 100 mA to the ST-LINK circuit until the end of the USB enumeration. Then, the B-G474E-DPOW1 product asks for 500 mA of current to the host PC.

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If the host PC can provide the required power, the enumeration finishes with a *SetConfiguration* command. Then, the power switch is turned ON, after which the B-G474E-DPOW1 product can draw a current of 500 mA. At this step, the PC can rely on the power switch overcurrent protection at 700 mA. In the case of overcurrent detection, the FAULT pin is asserted which lights on the red OC LED (LD8).

If the host PC cannot provide the requested current, the enumeration fails. Therefore, the power switch remains OFF and the 5V power reference of the board is OFF. The 5V green LED (LD7) is turned OFF.

The green LED (LD7) is turned ON when the B-G474E-DPOW1 product is correctly powered by 5V. The COM LED (LD9) indicates the STLINK-V3E communication status with the host. Refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

Note:

If the board is powered by a USB wall charger on CN3 with JP5 on STLK, there is no USB enumeration. So, the COM LED (LD9) remains OFF, but the power switch is activated and the board is powered up, with 700 mA current protection.

8.1 STLINK-V3E deactivation (Reset mode)

It is simple to deactivate the STLINK-V3E function, by adding a jumper on JP6 to connect STLK NRST to GND, as shown in Figure 8 and Table 4. Programming, debugging, and monitoring through ST-LINK are impossible in this Reset state, where all STLINK-V3E PIOs are in high impedance.

The Reset state is useful to connect an external probe to the debug or TAG connectors (CN1 or CN10) for embedded STM32 debug.

In this Reset state, if JP7 is OFF, the 5V selection JP5 CHGR source can power the board without current protection, but the 5V selection JP5 STLK is not functional.

Figure 8. STLK NRST default configuration (JP6)



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Table 4. STLK NRST configuration (JP6)

Reference	Jumper ⁽¹⁾	Function	Comment
JP6 ⁽²⁾	OFF	STLINK-V3E active	STLINK-V3E detects USBSTLK plug on CN3.
JF0 ⁽⁻⁾	ON	STLINK-V3E Reset state	Set STLINK-V3E in Reset mode (all I/Os in high impedance).

- 1. The default setting is in bold.
- 2. In the case JP6 is ON, JP7 must be OFF.

8.2 STLINK-V3E physical disconnection

It is possible to isolate partially or completely the STLINK-V3E signals from the rest of the STM32 board by disconnecting part of the physical signals or all of them:

- By default, STLINK-V3E is physically connected to STM32: SW1 is in ALL ON low physical position, and JP7 is ON, to enable the use of STLINK-V3E in Program/Debug/Monitoring modes. Refer to Figure 9, Table 5, and Table 6 for a detailed description.
- For complete physical isolation, the octal mechanical switch (SW1) must be set in ALL OFF and JP7 OFF. The STLINK-V3E connector (CN3) behaves like an external power supply with the 5V selection coming from either the CHGR or STLK source. Program/Debug/Monitoring through ST-LINK is not possible.
- For partial signal connection, ensure the ST-LINK firmware and STM32 target software are compatible with your selected SW1/JP7 configuration.

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Figure 9. TNRST default configurations (SW1/JP7)





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Table 5. SW1 configuration

Pin number	Function	STLINK-V3E description	State ⁽¹⁾	Comment
1	PWREXT	T_PWR_EXT (PB1)	ON or OFF	Connect or isolate STLINK-V3E from the general 5V power presence indicator
2	VCCAIN	T_VCC_AIN (PA0)	ON or OFF	Connect or isolate STLINK-V3E from the general 3V3 power presence indicator
3	GNDDET	GND detection (PG5)	ON or OFF	Connect or isolate STLINK-V3E from debug connector
4	TVCP_RX	STLK_VCP_TX (PG14)	ON or OFF	Connect or isolate STLINK-V3E from STM32
5	TVCP_TX	STLK_VCP_RX (PG9)	ON or OFF	Connect or isolate STLINK-V3E from STM32
6	TSWO	T_SWO (PD2)	ON or OFF	Connect or isolate STLINK-V3E from STM32
7	TSWCLK	T_SWCLK (PH6)	ON or OFF	Connect or isolate STLINK-V3E from STM32
8	TSWIO	T_SWDIO_IN (PH7)/ T_SWDIO_OUT (PF9)	ON or OFF	Connect or isolate STLINK-V3E from STM32

^{1.} ON (default setting) means that the switch is in the low physical position (L marking onboard). OFF means that the switch is in the high physical position (H marking onboard)

Table 6. TNRST configuration (JP7)

Reference	Jumper ⁽¹⁾	Function	Comment
JP7 TNRST ⁽²⁾	ON	T NRST (PA6)	STLINK-V3E output reset connected to T_NRST of STM32
JPT INRST	OFF	I_NRSI (PAO)	STLINK-V3E output reset isolated from T_NRST of STM32

^{1.} The default setting is in bold.

In case the USB Type- C^{\otimes} connector is used to power the board (JP5 USBC setting), it is also possible to disconnect the STLINK-V3E power, unsoldering the SB31 solder bridge. In that case, ensure that all signals are previously disconnected (SW1 in ALL OFF position, and JP7 OFF).

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^{2.} In the case JP7 is ON, JP6 must be OFF.



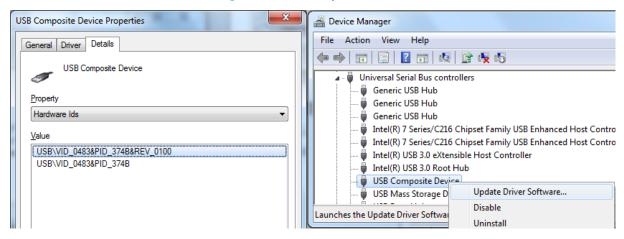
8.3 STLINK-V3E drivers

Before connecting the Discovery board to a Windows PC via USB, a driver for the STLINK-V3E must be installed. It is available on the *www.st.com* website.

In case the Discovery board is connected to the PC before the driver is installed, some Discovery board interfaces might be declared as *Unknown* in the PC device manager. In this case, the user must install the driver files, and update the driver of the connected device from the device manager. Refer to Figure 10.

Note: Prefer using the USB Composite Device handle for a full recovery.

Figure 10. USB composite device



8.4 STLINK-V3E VCP configuration

STLINK-V3E supports the Virtual COM port (VCP) by default. To disable this function, the relevant SW1 switches linked to the VCP function can be set to the OFF state. Refer to Table 5.

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9 Power supply

9.1 Power diagram

The following diagram describes the power architecture and the maximum voltage and current limits, under which functions can be safely used on the B-G474E-DPOW1 product. In any case, ensure the total power budget of the application always conforms to the selected 5V power source mode, if not malfunction can occur. For detailed configuration, refer to the relevant function description and technical application notes.

Note:

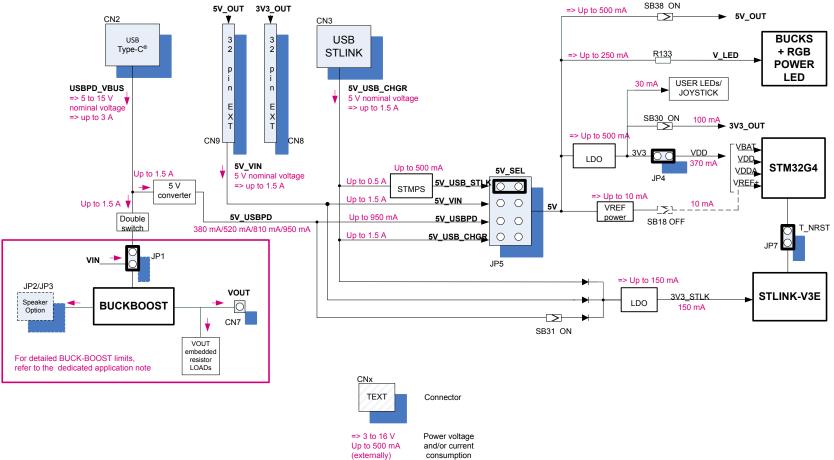
When using 5V_VOUT and 3V3_OUT to power external functions on 32-pin extension connectors, it can be necessary to use one of the two following power sources, depending on the application power budget:

- 5V_USB_CHGR, up to 1.5 A
- 5V_VIN, up to 1.5 A

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POWER DIAGRAM



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9.2 Power source selection

The B-G474E-DPOW1 product is designed to be powered by a 5 V DC power supply. It is possible to configure the Discovery board with JP5 header to use any of the four sources described in Table 7 for the 5 V DC power supply.

Reference	Jumper ⁽¹⁾	Function	Comment
	STLK	5V is supplied by USB STLK (CN3).	 5 V (+/- 5%) 700 mA embedded overcurrent protection Up to 500 mA capable
	CHGR 5V is supplied by USB STLK (CN3).		 5 V (+/- 5%) No embedded current protection Up to 1.5 A current
JP5	USBC	5V is supplied by a 5 V converter. The power source is connected to the USB Type-C [®] connector (CN2).	5 V (+/- 3%) Embedded selectable current protection: - Up to 950 mA on 5 V - Up to 1.5 A from USB Type-C® V _{BUS} USB Type-C® V _{BUS} nominal voltage from 5 to 15 V ⁽²⁾
	E5V	5V is supplied by the 5V_I pin of the extension connector (CN9).	 5 V (+/- 5%) No embedded current protection Up to 1.5 A current

Table 7. 5V_SEL configuration (JP5)

In all below four power source configurations, the 5V (LD7) and 3V3 (LD6) LEDs must be lit when the B-G474E-DPOW1 product is correctly powered by the 5 V.

9.2.1 STLK

Figure 12 shows the selection of 5V from STLK on JP5, with a power source connected to USB ST-LINK (CN3). It is the default setting.

The STLK ST-LINK USB connector (CN3) can power the B-G474E-DPOW1 Discovery kit, but the host PC only provides 100 mA to the ST-LINK circuit until the end of the USB enumeration. At the end of the USB enumeration, the B-G474E-DPOW1 Discovery kit asks for a 500 mA current to the host PC.

If the USB enumeration succeeds, a power switch powers the board with a current of up to 500 mA. This power switch also features a 700 mA current limitation to protect the PC in case of overcurrent on the board.

Note:

In this mode, if a wall charger powers the board, there is no USB enumeration. Therefore, the COM LED (LD9) remains OFF permanently, but the 700 mA protection is still active on the powered board.

Figure 12. JP5 (STLK) from USB STLK (CN3)





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^{1.} The default setting is in bold

^{2.} The software Demo mode integrated by default supports only a 5 V VBUS nominal voltage for the BuckBoost function.



9.2.2 CHGR

Figure 13 shows 5 V DC power from CHGR on JP5, with a power source connected to USB ST-LINK (CN3) and without current protection. Thus, if the B-G474E-DPOW1 Discovery kit is powered by a USB PC port, debug features are available, but with the risk of damaging the PC. If a silent USB wall charger powers the B-G474E-DPOW1 Discovery kit, the debug features are unavailable. CHGR pin can draw a 1.5 A maximum recommended current.

Figure 13. JP5 (CHGR) from USB STLK (CN3)





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9.2.3 USBC

Figure 14 shows the selection of 5 V DC power from USBC on JP5, with a power source connected to USB Type-C[®] connector (CN2). The 5 V converter (U6) provides the 5 V regulated voltage, from the USB Type-C[®] connector (CN2).

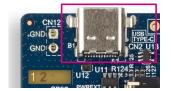
By default, the USB Type- C^{\otimes} V_{BUS} nominal voltage must be in the 5 V to 15 V range. Nevertheless, some exceptions might apply, so refer to the dedicated application note.

The default input current protection set on USB Type-C® CN2 implies the following constraints on USB host types to be used:

- Low-power USB hosts are not supported, and permanent damage can occur.
- USB 2.0 or USB 3.x legacy high-power hosts are not recommended in this configuration, because of the 100 mA current limit before enumeration, which is not sufficient to start the product.
- Any other USB Host can supply and start the B-G474E-DPOW1 board, like a silent USB wall charger, a
 USB battery charging 1.2 Host, or a USB Type-C[®] Host.

Figure 14. JP5 (USBC) from USB Type-C®(CN2)





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9.2.4 E5V

Figure 15 shows the selection of 5 V DC power from E5V on JP5. The power source is connected to external 5V_VIN on CN9 pin 1 (5V_I on the silkscreen) and GND on CN9 pin 2. Note that GND is also available on other pins of extension connectors (CN8 and CN9). Refer to Section 12.5 for details.

Note:

In this case, the B-G474E-DPOW1 product must be powered by a power supply unit or by auxiliary equipment complying with the EN 62368-1:2014+A11:2017 standard and must be safety extralow voltage (SELV) with limited power capability.

Note that there is no input current protection in this configuration. The recommended maximum current to be drawn from this E5V pin is 1.5 A.

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Figure 15. JP5 (E5V) from 5V I/GND (CN9)





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9.3 Microcontroller power

By default, the STM32G474RET6 microcontroller power supplies are all connected to the VDD power supply. In case the user wants to test any other power supply configuration, a few solder bridges can be modified (refer to Section 14.2).

VDD power supply is connected in the design to 3V3, 3.3 V-regulated output, which can draw a current up to 500 mA. An LDO regulator provides the VDD power supply from the 5 V general power supply. As soon as VDD is available, the 3V3 green LED (LD6) is lit.

A jumper is fitted on the JP4 header to connect the LDO-regulated output to the VDD power supply rail. An ammeter can replace this jumper for IDD measurement. Refer to Figure 16 and Table 8.

Figure 16. IDD default configuration (JP4)



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Table 8. IDD configuration (JP4)

Reference	Jumper ⁽¹⁾	Function	Comment
JP4	ON	3V3 connected to VDD	3V3 powers VDD. The current measurement is impossible.
JF4	OFF	3V3 not connected to VDD	VDD is not powered. Add an ammeter to measure the current.

1. The default setting is in bold.

By default, analog ground VSSA and general ground VSS are connected at one point of the design, thanks to SR25

VREF+ is the STM32G474RET6 input reference voltage for ADCs and DACs. It has different possible configurations:

- Connected to VDD (Default setting)
- Connected to an embedded VREF PWR block function. It provides an accurate and low noise VREF reference voltage, set at a 3.25 V default value. This block is based on the TL1431 programmable voltage reference.
- Connected to the output of the STM32G474RET6 internal voltage reference buffer when enabled.

When using a VREF+ configuration different from the default one, the user must take care, and alternatively needs to adapt the design parts using ADCs or DACs.

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10 Clock sources

The B-G474E-DPOW1 Discovery kit uses the internal HSI clock reference.

In case the user wants to apply external clock sources, there are three possible options:

- X2, 24 MHz oscillator footprint (not fitted by default)
- MCO clock source coming from STLINK-V3E (not connected by default)
- External clock source from extension connector (on PF0, pin 26 of CN9)

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11 Boot options

By default, the B-G474E-DPOW1 boots on the STM32G474RET6 internal flash memory, thanks to the nSWBOOT0 option bit set to 0. The hardware configuration of the B-G474E-DPOW1 product (BOOT0 pin not used, PB8 available for users) implies changing the default MCU option bytes settings. This ensures that the software Demo mode programmed into the main flash memory is executed directly after the startup sequence. Refer to the reference manual *STM32G4 series advanced Arm®-based 32-bit MCUs* (RM0440) for detailed boot configuration and option bytes settings. Thus, by default, the software completely manages the boot procedure. But, as the PB8 pin of the STM32G474RET6 is also free for use by default, the user can choose any boot mechanism based on the BOOT0 pin function. In that case, do not forget to set correctly the relevant option bytes linked to the booting procedure:

- Use PB8 as the BOOT0 pin and fit pull-down R83,
- Or use PB8 as the BOOT0 pin and add any pull-down or pull-up resistor connected to pin 21 of the extension connector (CN9).

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12 Board functions

This chapter explains all the functions, peripherals, and interfaces of the board (Refer to Section 1: Features, Section 7: Hardware layout and configuration, Figure 4. B-G474E-DPOW1 top layout view, and Figure 5. B-G474E-DPOW1 bottom layout view).

12.1 USB Type-C®

The B-G474E-DPOW1 product supports a USB FS 2.0 interface on a USB Type-C[®] receptacle connector (CN2). The B-G474E-DPOW1 product offers compatibility with USB Type-C[®] revision 1.3, USB PD3.0, and with USB battery charging 1.2.

Caution:

The B-G474E-DPOW1 Discovery kit does not support the connection of low-power USB hosts on the USB Type-C® connector (CN2). As required by the USB Type-C® specification, the B-G474E-DPOW1 product can interface on CN2 with USB2.0 and USB3.x legacy high-power hosts supporting USB full-speed data link, but some feature restrictions apply:

- JP5 must not be set on USBC.
- SB31 must be removed.

 This ensures that the USB Type-C® connector (CN2) can only power the digital power buck-boost feature of the Discovery board.

Caution:

The total drawn current on USB Type-C® V_{BUS} must not exceed 3 A in any application.

CubeMonitor-UCPD tool, available on www.st.com, can be used to modify the desired allowed voltages, but the user must not use the CubeMonitor-UCPD tool to add 5 A PDOs.

Note that the B-G474E-DPOW1 Discovery kit offers also the possibility to connect any external display compatible with a 3 V I²C interface: PB8 and PB9 PIOs are free to use on the extension connector (CN9) and they offer access to I2C1 SCL and I2C1 SDA alternate functions.

The USB Type-C® connector (CN2) can be used to demonstrate different features of the B-G474E-DPOW1.

- 1. Power the Discovery board with a 5 V regulated power supply source, thanks to the 5 V converter.
- 2. Power the digital power buck-boost VIN input voltage.
- 3. Power the audio Class-D amplifier feature.

12.1.1 Power the 5V general supply

The USB Type-C[®] connector (CN2) can power the Discovery board with a 5 V regulated power supply source thanks to the 5 V converter (U6). Refer to Section 9.1: Power diagram.

A jumper must be set on JP5 to select a USBC configuration. In this mode, USBPD_VBUS nominal voltage must not exceed the 5 to 15 V range. Even if the 5 V converter can withstand a USBPD_VBUS nominal voltage of 20 V, the digital power buck-boost feature supports only a USBPD_VBUS nominal voltage of 15 V maximum.

In this mode, note the USB low-power hosts and USB 2.0 or USB 3.x hosts are not supported.

Thanks to the UCPD controller of the STM32G474RET6, and as the UCPD_CC1 and UCPD_CC2 inputs are respectively connected to the UCPD_DBCC1 and UCPD_DBCC2 inputs, the USB Type- C^{\otimes} allows direct power-up of the Discovery board with a 5 V V_{BUS} nominal voltage. The current protection is managed thanks to two I/Os controlled by the STM32G474RET6 microcontroller: they are driving the 5 V converter maximum allowable output current, up to 950 mA typical.

These two I/Os are named USBPD_550mA_PROTECT (PD2) and 5V_USBPD_1A_PROTECT (PC12) in schematics. By default, the two I/Os are deactivated, and the current protection on the 5V general supply is fixed at 380 mA typical, thanks to R101.

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Table 9. P	D2 and	PC12	function
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Command	Logic state ⁽¹⁾	Description
USBPD 550mA PROTECT (PD2)	0	Deactivated
USBFD_SSUIIA_FROTECT (FD2)	1	Connects R99 in parallel to R101
5V USBPD PROTECT 1A (PC12)	0	Deactivated
3V_03BFD_FR01E01_1A (F012)	1	Connects R102 in parallel to R101

^{1.} The default setting is in bold.

It is possible to increase the default current limitation set on the 5V_USBPD supply with the settings shown in Table 10.

Table 10. Typical current protection on 5V_USBPD

Mode	5V_USBPD_PROTECT_1A (PC12) ⁽¹⁾	USBPD_550mA_PROTECT (PD2) ⁽¹⁾	5V_USBPD typical protection
Default	0	0	380 mA
Mode 1	0	1	520 mA
Mode 2	1	0	810 mA
Mode 3	1	1	950 mA

^{1.} The default setting is in bold.

Note that the current protection set on the 5V_USBPD might include the current drawn by the 3V3_STLK power supply at the start. This additional current depends on the 5V_USBPD, the 5V_USB_CHGR, and the 5V_VIN voltages of the board. It can reach 150 mA maximum and can be suppressed by removing SB31. Note also that removing SB31 might bring a behavior constraint: upon USB STLK insertion, the board is reset unless JP7 is removed.

In case of overcurrent detected on 5V_USBPD, the 5 V converter progressively lowers the 5V_USBPD voltage and might reset the Discovery board. The LD7 and LD6 LEDs might indicate such a 5V power decrease. By shutting down the 5V_USBPD voltage, the current on USB Type- C^{\otimes} V_{BUS} of CN2 decreases, protecting the USB Host from overcurrent.

The current protection set on the 5V_USBPD supply leads to the corresponding current protection on USBPD_VBUS of the USB Type-C® connector (CN2). Table 11 gives typical figures for two use cases.

Table 11. Typical current protection on CN2

Mode	5 V USBPD_VBUS nominal voltage ⁽¹⁾	15 V USBPD_VBUS nominal voltage
Default	0.45 A	0.15 A
Mode 1	0.7 A	0.23 A
Mode 2	1.2 A	0.4 A
Mode 3	1.5 A	0.45 A

^{1.} The default setting is in bold.

A USBPD_Detach function is designed to be able to monitor the USBPD_VBUS voltage on an STM32G474RET6 microcontroller ADC. It is used by the USB software stack to get a USBPD_VBUS voltage status close to the USB Type-C® connector and manage the unplugging procedure.

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12.1.2 Power input to the digital power buck-boost feature

The USB Type-C[®] connector (CN2) can also be used as a power input to demonstrate the digital power buck-boost converter feature of the B-G474E-DPOW1 product (Refer to Section 12.2: Digital power buck-boost converter):

By default, ensure that the JP5 is not set on the USBC position. Nevertheless, some exceptions might apply, so refer to the dedicated application note on this digital power buck-boost function.

In this mode, the USBPD_VBUS nominal voltage must not exceed 15 V. A jumper must be set on JP1 to connect VIN to USBPD. Based on Q12 and Q13 transistors, the double switch function connects or isolates USBPD_VBUS and digital power buck-boost VIN input. The double switch is controlled with the BUCKBOOST_USBPD_EN signal (PC3) respecting the USB standard constraints.

The current protection is implemented to limit the current drawn from VIN. This protection is managed thanks to a current sensing function connected to BUCKBOOST I IN AVG (PA2) for ADC conversion.

12.1.3 Power and data input to the audio Class-D amplifier feature

The USB Type-C® connector (CN2) can also be used as a power and data input to demonstrate the audio Class-D amplifier feature of the B-G474E-DPOW1 product (Refer to Section 12.3: Audio Class-D amplifier).

The audio Class-D amplifier uses the digital power buck-boost feature of the Discovery board. Audio data are sent from the USB host through the USB 2.0 FS interface of the CN2 connector. Then, the STM32G474RET6 microcontroller converts these audio data into HRTimer controls to output audio sound on a speaker connected to JP2/JP3 footprints.

In this mode, the USBPD_VBUS nominal voltage must not exceed 12 V. A jumper must be set on JP1 to connect VIN to USBPD.

Based on Q12 and Q13 transistors, the double switch function connects or isolates USBPD_VBUS to/from digital power buck-boost VIN input. The double switch is controlled with the BUCKBOOST_USBPD_EN signal (PC3) respecting the USB standard constraints.

The current protection is implemented to limit the current drawn from VIN. This protection is managed thanks to a current sensing function connected to BUCKBOOST I IN AVG (PA2) for ADC conversion.

12.2 Digital power buck-boost converter

The B-G474E-DPOW1 includes a digital power buck-boost converter feature with two embedded resistor load networks on VOUT.

Attention:

The digital power buck-boost converter feature might not support the JP5 setting on USBC. Refer to the dedicated application note for additional specific conditions.

Caution:

Check that the following default rules are applied, or permanent damage can occur:

- The VIN input voltage source must not exceed 16 V.
- When powered from the USB Type-C® connector (CN2), the buck-boost converter must not consume a current higher than 1.5 A.
- The VOUT output voltage must not exceed 16 V.
- For thermal and safety reasons, each VOUT embedded resistor load network is protected against current higher than 400 mA. Do not shunt the PTC fuse components.

The digital power buck-boost converter is composed of the following block functions:

- The buck-boost converter function, which is based on HRTimers with advanced control, input/output
 voltage regulation, and input current regulation optionally.
- The double switch function, which isolates or connects the USB Type-C[®] V_{BUS} to the buck-boost converter input VIN.
- The VIN header (JP1), which selects the input power source of the buck-boost converter (external VIN or VIN from USB Type-C[®] V_{BUS}).
- The VOUT embedded resistor loads to demonstrate buck-boost behavior with static and dynamic loads.
- The VOUT connector (CN7), which can be connected to a breadboard for direct access to an external application.

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PA6 PC15 PA5 PA4 Embedded PF0 PF1 D PA3 **VOUT** resistor PA2 PC0 loads PC1 PA1 NRST 6 PA0 O PC3 PC2 Headers GND (JP2/JP3) VOUT/GND VIN selection TUOV VIN (JP1) 0 (CN7)

Figure 17. Digital power buck-boost converter

The buck-boost converter function is composed of symmetrical half-bridge topology and works in either Buck, Boost, or Buck-boost mode. It leverages advanced HRTimers, FMAC, and digital slope compensation management. It integrates a current regulation in Buck mode and can measure average and instantaneous currents at buck-boost converter input (thanks to ADC and internal comparator). Input and output voltage regulations are managed thanks to the ADC channel usage. A current sensing function allows the implementation of the current protection at the digital buck-boost converter input VIN.

By default, the **double switch function** isolates USB Type-C[®] V_{BUS} from the buck-boost converter input. The activation of BUCKBOOST_USBPD_EN (PC3) controls the double switch. Activation of this double switch connects the USBPD VBUS to bring power to the buck-boost converter input VIN if JP1 is set correctly.

By default, **the VIN header (JP1)** selects the power source from USBPD_VBUS of the USB Type-C[®] connector (CN3), with a closing jumper to connect USBPD and VIN [1-2]. The users might also want to use an external VIN. In that case, they must connect an external power supply to the VIN and GND pins of the JP1 header, and the JP1 jumper must be removed.

Figure 18. VIN default configuration (JP1)



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Ensure to use always a closed jumper type on JP1 to avoid any unwanted short-circuit damage to the USB Host V_{BUS} .

Table 12. VIN configuration (JP1)

Reference	Jumper ⁽¹⁾	Function	Comment
JP1	[1-2]	VIN connected to USBPD	This connects a buck-boost VIN to the V_{BUS} from USB Type- C^{\circledR} when the double switch is activated
	OFF	VIN is free for use	This enables the use of an external power supply as a buck-boost VIN input voltage
	[2-3]	VIN connected to GND	This deactivates the buck-boost function. VIN is not accessible

1. The default setting is in bold.

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The VOUT embedded resistor load function is based on two independent and identical resistor networks, each of them being controlled by the STM32G474RET6 microcontroller. Each network presents an equivalent resistor of 33 Ω and has a fuse, which activates current protection. The minimum current that transitions the fuse from low resistance to high resistance is 400 mA at 23°C. The buck-boost converter output can be loaded with 50 or 100% of these resistor loads, with BUCKBOOST_LOAD_50% (PC14) and BUCKBOOST_100%_LOAD (PC15), which can be activated in any order. The maximum current, which each resistor load network passes without interruption at +23°C still air, is 200 mA. For a higher output current capability on VOUT, the external load can be used on the VOUT connector (CN7).

The VOUT connector (CN7) is placed on the bottom side of the Discovery board to allow the easy use of additional external resistor loads on a breadboard.

Note:

If the user wants to exercise the I/Os used by the digital power buck-boost converter for another application, it is very important to disconnect those I/Os from the buck-boost converter, to avoid permanent damage. Serial resistors are available for this purpose.

12.3 Audio Class-D amplifier

The Discovery board can be used to demonstrate the audio Class-D amplifier application, based on the digital power buck-boost feature. The JP2/JP3 4-pole connector is used to connect external stereo speakers of 8 Ω total equivalent impedance. This application requires specific hardware and software configuration, refer to the dedicated application note to achieve the best possible performance.

By default, the JP1 VIN header selects the power source from USBPD_VBUS of the USB Type-C[®] connector (CN2), with a closing jumper on the JP1 header to connect USBPD and VIN [1-2]. The users might also want to use an external VIN. In that case, they must connect an external power supply to the VIN and GND pins of the JP1 header, and the JP1 jumper must be OFF. Refer to Table 12.

12.4 RGB power LED

Attention:

According to the photobiological safety of lamps and lamp systems (IEC62471), the B-G474E-DPOW1 product is rated risk 1 in its default configuration (low risk). The most restrictive optical radiation is the retinal blue light hazard 300 to 400 nm. Associated technical reports with exposure hazard values and exposure distance are deliverable on demand.

Caution:

In case of any modifications of this function, it is the user's responsibility to ensure safe conditions. Do not remove the LPB1 diffuser/protection placed over the RGB power LED (LD1), or else users might be exposed to higher hazard values. It is also recommended to keep unchanged the RGB LED current limit examples set in the software Demo mode.

Attention:

In case the user wants to use the DRIVE or SENSE controls of any RGB LED for another application, it is very important to disconnect those controls from the buck-LED converters. Serial resistors can be removed for that purpose (Refer to schematics, Table 17, and Table 18). The user might also alternatively remove the SB7, SB8, or SB9 solder bridge to disconnect the onboard RGB LED, if sufficient in its application.

The RGB power LED feature is designed with the following elements:

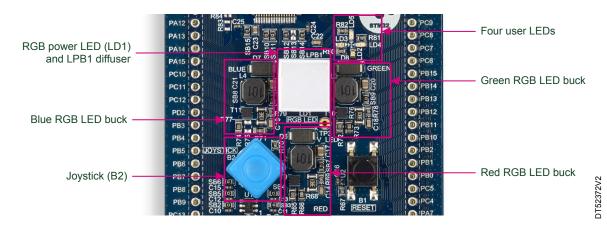
- RGB high brightness LED
- Squared pipe bar and diffuser
- 3 step-down inverted buck converters, each one driving a color LED (red, green, or blue)
- 4-way joystick plus selection key managing the color selection and luminous intensity dimming
- 4 user LEDs as status indicators

The joystick and user LEDs give full control of the RGB power LED function selection and management. For more details about the RGB LED function management, refer to the application note *High-brightness RGB LED control using the B-G474E-DPOW1 Discovery kit* (AN5345).

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Figure 19. RGB power LED function



The inverted buck topology is used to reduce the number of components for this discrete application. Each buck-LED converter is controlled with an HRTimer as the DRIVE command and has a current regulation on a SENSE comparator input.

The STM32G474RET6 microcontroller manages each color LED individually, which enables the following features:

- Single color LED or mixed color LED pattern selection, including white-colored LED.
- Manual or automatic dimming for luminance selection.

By default, the 5 V general supply of the board is used as a power supply for the three buck-LED converters. The total current needed to run this function is quite low, about 250 mA for white color at its recommended maximum luminance. Thus, any of the JP5 power sources can be used to demonstrate the RGB power LED.

In case the user wants to use any other power supply, it is possible to bring it on TP3 and disconnect R133.

12.5 Extension connector headers

Caution:

Before using the extension connector pin to control an external application, check that the PIOs to use are not already used in the design, otherwise permanent damage can occur. Every PIO of the extension connector might be used externally, providing it is isolated from the features integrated into the Discovery board. Serial resistors or solder bridges are available to disconnect most of them. Refer to Section 13.4: Extension connector (CN9) and Section 13.5: Extension connector (CN8).

Caution:

When the B-G474E-DPOW1 Discovery board is used standalone, take care to put it on a nonconductive material to avoid short circuits on all bottom side connectors or permanent damage can occur.

The two extension connector headers (CN8 and CN9), placed on both-hand sides of the board, are 32-pin 2.54 mm pitch standard connectors. Connector spacing is $(17 \times 2.54) \times 43.18 \text{ mm}$. They offer easy access to signal pins on the bottom and top sides of the Discovery board.

Thus, the B-G474E-DPOW1 product is compatible with standard breadboards for prototyping. To allow a complete board connection, the GND corner headers (CN5, CN6, CN11, and CN12), and the VOUT/GND connector (CN7) are also compatible with the 2.54 mm pitch grid. Refer to Figure 6. B-G474E-DPOW1 mechanical drawing for details.

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(IGND (D) VDD 5V_0 0 PAS PAS (2) AGNI O VREF PA10 1 VREF PA11 (2) @ AVDD D PC9 PA13 | 1 PC8 PA14 O PC7 PA15 (1 PC6 PC10 (1) O PB15 PC11 0 PB14PB13 Extension PC12 Extension PD2 D PB12 connector connector PB3 **(**)
PB4 **(**) PB11 (CN9) (CN8) (PB10 PB5 O PB2 PB6 O PB1 **○** PB0 0 PB8 PC5 PC4 PB9 O PA7 PC13 PC14 0 PA6 PA5PA4 PC15 PF0 D PA3 PF1 PA2 PC0 | PA1 PC1 PA0 TNRST 🗑 D PC3 PC2 I GND

Figure 20. Extension connectors (CN8 and CN9)

All the power supplies and all the PIOs from the STM32G474RET6 microcontroller are available on these extension connectors. Analog and general grounds are also available.

Furthermore, to ease prototyping, 5V_OUT and 3V_OUT power supplies, coming respectively from the general 5V and the 3V3 of the Discovery board, are also available on the extension connectors (CN8 and CN9). Pay attention that the currents drawn on the 5V_OUT and 3V3_OUT power supplies do not exceed the maximum recommended values. Refer to Section 9.1: Power diagram for details.

A 5V_IN pin is available to power the Discovery board from an external power supply. Refer to Section 9: Power supply.

12.6 RC sinus function

The RC sinus function is used to demonstrate HRTimer output capability.

The principle is to generate a triangle waveform, to show the accuracy of the HRTimer on the ramp-down compared to a standard PWM on the ramp-up. The signal might be filtered with a low-pass filter to get a sine-wave shape.

The generated signal is available for probing on the TP4 test point.

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12.7 Joystick function

The B2 joystick, with four directions and a selection key, is located on top. It is used to switch between different modes of demonstration software. It is also used to dim the luminance and select the color of the RGB power LED. The selection key can be used as a wake-up key. Through their interrupt feature, five PIOs manage this joystick. All keys are active low.

12.8 Reset button function

The B1 reset button located on top activates the STM32G474RET6 microcontroller PG10-NRST pin (T_NRST signal tied to GND). It resets the board with a low logical level.

The board reset is also accessible on the extension connector (JP9), on the header (JP7), and on the debug connector (CN1).

During reset activation, the blue user LED (LD2) is lit at low luminance. PA15 has an internal pull-up during the reset and it drives this LD2 with a low current.

12.9 Buttons and LEDs function

Table 13 summarizes the different buttons and LEDs of the B-G474E-DPOW1 Discovery kit and their function:

Reference Function Color Comment В1 Black RESET button (T_NRST) Reset the board JOYSTICK SELECT PC13 **PB10** JOYSTICK_UP B2 Blue JOYSTICK_DOWN PC5 JOYSTICK_RIGHT PB2 JOYSTICK_LEFT PC4 RGB power LED for lighting LD1 Red, green, or blue Lighting application User LED, PA15 (lit during LD2 LED_DOWN_BLUE Blue reset) LD3 LED_LEFT_ORANGE User LED, PB1 Orange LD4 Green LED RIGHT GREEN User LED, PB7 LD5 LED_UP_RED User LED, PB5 Red lit when 3V3 is ON LD6 Green 3V3 power LD7 Green 5V power lit when 5V is ON lit when STLK overcurrent LD8 Red ST-LINK Overcurrent (OC) detected lit according to ST-LINK LD9 Red, green, or orange ST-LINK COM status

Table 13. Buttons and LEDs

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13 Connectors

Eleven connectors are implemented on the B-G474E-DPOW1 product:

CN3: USB Micro-B
 CN2: USB Type-C[®]
 CN1: Debug connector
 CN10: TAG connector

CN8 and CN9: Extension connector headers

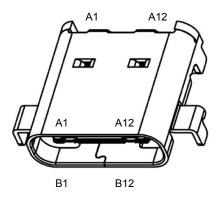
CN7: VOUT connector header

CN5, CN6, CN11, and CN12: GND connector headers

13.1 USB Type-C® receptacle connector (CN2)

CN2 is a 24-pin double-row midmount connector compatible with USB Type- C^{\otimes} specifications and shown in Figure 21. It is compatible with V_{BUS} current up to 3 A.

Figure 21. USB Type-C® receptacle connector upper front view (CN2)



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The related pinout for the USB Type-C® connector is listed in Table 14.

Table 14. USB Type-C® receptacle connector (CN2)

Pin number	Description	Signal assignment	Pin number	Description	Signal assignment	
B12	GND	GND	A1	GND	GND	
B11	RX1_P	-	A2	TX1_P	-	
B10	RX1_N	-	A3	TX1_N	-	
В9	V_{BUS}	USBPD_VBUS	A4	V_{BUS}	USBPD_VBUS	
B8	SBU2	-	A5	CC1	USBPD_CC1	
B7	DM2	USBPD_FS_DM	A6	DP1	USBPD_FS_DP	
B6	DP2	USBPD_FS_DP	A7	DM1	USBPD_FS_DM	
B5	CC2	USBPD_CC2	A8	SBU1	-	
B4	V _{BUS}	USBPD_VBUS	A9	V _{BUS}	USBPD_VBUS	
В3	TX2_N	-	A10	RX2_N	-	
B2	TX2_P	-	A11	RX2_P	-	
B1	GND	GND	A12	GND	GND	

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13.2 Debug connector (CN1)

The STDC14 debug connector is implemented to program and debug the STM32G474RET6 microcontroller. The SWD protocol must be used by default.

To use the STDC14 connector to debug STM32G474RET6, it is mandatory to place a jumper on JP6 to connect STLK NRST to GND. This sets the STLINK-V3E MCU in a high-impedance state.

In case the user wants to isolate completely the STDC14 debug connector from the STLINK-V3E MCU, the octal mechanical switch (SW1) must be set accordingly, and JP7 must be removed. This also disconnects the STM32G474RET6 microcontroller from STLINK-V3E.

1

Figure 22. STDC14 debug connector (CN1)

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If needed, a MIPI10 female connector can be plugged into the STDC14 connector (CN1), if pins 1, 2, 13, and 14 are bent or cut. Alternatively, a MIPI10 connector can be soldered on the footprint (CN1) in place of STDC14.

Pin Pin Description **Assignment** Description **Assignment** number number 1 2 3 3V3 4 SWDIO/JTMS 3V3 power T_SWDIO (PA13) 5 **GND GND** SWCLK/JTCK T SWCLK (PA14) 6 SWO/JTDO 7 **KEY GND** 8 T_SWO (PB3) 10 JTDI T_JTDI (PA15) 9 11 **GNDDetect** 100 Ω pull-down 12 RESET/JTRST T_NRST (PG10) 13 Tx T_VCP_RX (PC11) 14 T_VCP_TX (PC10) Rx

Table 15. STDC14 connector

Note:

4-wire and 5-wire JTAG debug modes are not supported by default. The 4-wire JTAG mode might be used but might require deactivating the USB Type-C[®] feature in hardware and software, to connect JTDI with the SB28 solder bridge and disconnect the R89 resistor.

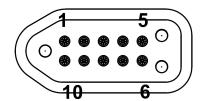
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13.3 TAG connector (CN10)

The TAG connector footprint is implemented on the bottom side of B-G474E-DPOW1.

Figure 23. TAG connector (CN10)



To use the TAG connector footprint to debug STM32G474RET6, it is mandatory to place a jumper on JP6 to connect STLK NRST to GND. This puts the STLINK-V3E MCU in a high-impedance state.

In case the user wants to isolate completely the TAG connector from the STLINK-V3E MCU, the mechanical octal switch (SW1) must be set accordingly, and the JP7 jumper must be removed.

Using the TAG connector is exclusive to using the debug connector.

Table 16. TAG connector (CN10)

Pin number	Description	Assignment	Pin number	Description	Assignment
1	VDD	3V3	10	NRST	T_NRST (PG10)
2	SWDIO	T_SWDIO (PA13)	9	NA	-
3	GND	GND	8	NA	-
4	SWCLK	T_SWCLK (PA14)	7	NA	-
5	GND	-	6	SWO	T_SWO (PB3)

13.4 Extension connector (CN9)

The 32-pin extension connector (CN9) is accessible on the left-hand side on top of the B-G474E-DPOW1, or the right-hand side of its bottom. It provides access to some PIOs of STM32G474RET6 and most of the Discovery board power supplies. It can be plugged into a breadboard for prototyping (2.54 mm pitch). All pins remain accessible on the top side for probing.

Table 17. Extension connector (CN9)

Pin number	Description	Main function	Signal assignment	Optional modification ⁽¹⁾
1	5V_I	Power	5V_IN	-
2	GND	Power	GND	-
3	5V_O	Power	5V_OUT	-
4	PA8	RGB LED	BUCK_BLUE_DRIVE	Remove R74
5	PA9	USBPD	USBPD_DBCC1	Remove R94
6	PA10	USBPD	USBPD_DBCC2	Remove R93
7	PA11	USBPD	USBPD_FS_DM	Remove R96 and connect R91
8	PA12	USBPD	USBPD_FS_DP	Remove R95 and connect R90
9	PA13	STLINK	T_SWDIO	Remove SB6

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Pin	Description	Main function	Signal assignment	Optional modification ⁽¹⁾
number	Description	Main failetion	Oignal assignment	Optional modification 7
10	PA14	STLINK	T_SWCLK	Remove SB4
11	PA15	RGB LED	LED_DOWN_BLUE (T_JTDI)	Remove R89 (SB28)
12	PC10	STLINK	T_VCP_TX	Remove SB24
13	PC11	STLINK	T_VCP_RX	Remove SB23
14	PC12	USBPD	5V_USBPD_1A_PROTECT	Remove SB20
15	PD2	USBPD	USBPD_550mA_PROTECT	Remove SB19
16	PB3	STLINK	SWO	Remove SB16
17	PB4	USBPD	USBPD_CC2	Remove R86 and connect R87
18	PB5	USER LED	LED_UP_RED	Remove R82
19	PB6	USBPD	USBPD_CC1	Remove R85 and connect R84
20	PB7	USER LED	LED_RIGHT_GREEN	Remove R81
21	PB8-BOOT0	-	PB8 (Free)	-
22	PB9	-	PB9 (Free)	-
23	PC13	JOYSTICK	JOYSTICK_SELECT	Remove SB5
24	PC14	BUCK-BOOST	BUCKBOOST_LOAD 50%	Remove R58
25	PC15	BUCK-BOOST	BUCKBOOST_LOAD 100%	Remove R57
26	PF0	-	PF0 (Free)	-
27	PF1	-	PF1 (Free)	-
28	PC0	-	PC0 (Free)	-
29	PC1	-	PC1 (Free)	-
30	PG10-NRST	STLINK	T NRST	-
31	PC2	USBPD	USBPD_VIN	Remove SB33
32	GND	Power	GND	-

^{1.} To use PIOs to drive an external function plugged into CN9, optional modification might be necessary to disconnect PIOs from the onboard main function. In that case, take care to keep hardware coherency in the design and adapt the software accordingly.

13.5 Extension connector (CN8)

The 32-pin extension connector (CN8) is accessible on the right-hand side on top of the B-G474E-DPOW1, or the left-hand side of its bottom. It provides access to some PIOs of STM32G474RET6 and some Discovery board power supplies. It can be plugged into a breadboard for prototyping (2.54 mm pitch). All pins remain accessible on the top side for probing.

Table 18. Extension connector (CN8)

Pin number	Description	Main function	Signal assignment	Optional modification ⁽¹⁾
1	3V3_O	Power	3V3_OUT	-
2	GND	Power	GND	-
3	VDD	Power	VDD	-
4	AGND	Power	AGND	-
5	VREF	Power	VREF	-
6	VREFP	Power	VREFP	-

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Pin number	Description	Main function	Signal assignment	Optional modification ⁽¹⁾
7	AVDD	Power	AVDD	-
8	PC9	-	PC9 (Free)	-
9	PC8	RGB LED	BUCK_GREEN_DRIVE	Remove R72
10	PC7	RC sinus	RC-sinus function	Remove R97
11	PC6	RGB LED	BUCK_RED_DRIVE	Remove R65
12	PB15	BUCK-BOOST	BUCKBOOST_P2_DRIVE	Remove R6, R5
13	PB14	BUCK-BOOST	BUCKBOOST_N2_DRIVE	Remove R20
14	PB13	BUCK-BOOST	BUCKBOOST_N1_DRIVE	Remove R19
15	PB12	BUCK-BOOST	BUCKBOOST_P1_DRIVE	Remove R3, R4
16	PB11	BUCK-BOOST	BUCKBOOST_I_IN_SENSE	Remove SB26
17	PC5	JOYSTICK	JOYSTICK_DOWN	Remove SB6
18	PB10	JOYSTICK	JOYSTICK_UP	Remove SB4
19	PB1	USER LED	LED_LEFT_ORANGE	Remove R80
20	PB0	RGB LED	BUCK_BLUE_SENSE	Remove R79, C19, and C91
21	PB2	JOYSTICK	JOYSTICK_RIGHT	Remove SB3
22	PC4	JOYSTICK	JOYSTICK_LEFT	Remove SB2
23	PA7	RGB LED	BUCK_RED_SENSE	Remove R69, C14, and C90
24	PA6	-	PA6 (Free)	-
25	PA5	-	PA5 (Free)	-
26	PA4	-	PA4 (Free)	-
27	PA3	BUCK-BOOST	BUCKBOOST_VOUT	Remove R18 and R22
28	PA2	BUCK-BOOST	BUCKBOOST_I_IN_AVG	Remove SB14
29	PA1	BUCK-BOOST	BUCKBOOST_VIN	Remove R11, R17, and C3
30	PA0	RGB LED	BUCK_GREEN_SENSE	Remove R78, C18, and C22
31	PC3	BUCK-BOOST	BUCKBOOST_USBPD_EN	Remove SB12
32	GND	Power	GND	-

To use PIOs to drive an external function plugged into CN8, optional modification might be necessary to disconnect PIOs
from the onboard main function. In that case, take care to keep hardware coherency in the design and adapt the software
accordingly.

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13.6 VOUT extension connector (CN7)

The VOUT extension connector (CN7) is accessible on the right-hand side on top of the B-G474E-DPOW1, or the left-hand side of its bottom. It provides access to VOUT, buck-boost output voltage, and GND. It can be plugged into a breadboard for prototyping (2.54 mm pitch). VOUT and GND remain accessible on the top side for probing.

Table 19. VOUT extension connector (CN7)

Pin number	Description	Main function	Signal assignment
1	VOUT	BUCK-BOOST	VOUT
2	GND	BUCK-BOOST	GND

13.7 GND extension connectors (CN5, CN6, CN11, and CN12)

The GND extension connectors are accessible on each of the four corners of the B-G474E-DPOW1. They provide access to GND. They can be plugged into a breadboard for prototyping (2.54 mm pitch). GND remains accessible on the top side for probing.

Table 20. GND extension connectors (CN5, CN6, CN11, and CN12)

Pin number	Description	Main function	Signal assignment
1	GND	Power	GND
2	GND	Power	GND

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14 Jumpers and solder bridges

14.1 Jumpers

The jumper functions and their default status are described in Table 21.

Table 21. Jumper configuration

Reference	Jumper ⁽¹⁾	Function	Comment
	[1-2]	VIN connected to USBPD	Connect the buck-boost VIN to the V_{BUS} from USB Type- $C^{\textcircled{®}}$ when the double switch is activated.
JP1	OFF	VIN is free for use	Enable the use of an external power supply as a buck-boost VIN input voltage.
	[2-3]	VIN connected to GND	Deactivate buck-boost function, VIN not accessible.
ID4	ON	3V3 connected to VDD	3.3 V powers VDD. It is impossible to measure the current.
JP4	OFF	3V3 not connected to VDD	VDD is not powered. Add an ammeter to measure the current.
	STLK	5 V is supplied by USB STLK (CN3).	 5 V (+/- 5%), 700 mA embedded overcurrent protection Up to 500 mA capable
	CHGR	5 V is supplied by USB STLK (CN3).	 5 V (+/- 5%) No embedded current protection Up to 1.5 A current recommended
JP5	USBC	5 V is supplied by the 5 V converter. The power source is connected to the USB Type-C® connector (CN2).	5 V (+/- 3%) Embedded selectable current protection (up to 950 mA on 5 V, up to 1.5 A on USB Type-C® V _{BUS}) USB Type-C® V _{BUS} nominal voltage 5-15 V
	E5V	5 V is supplied by the 5V_I pin of the extension connector (CN9).	 5 V (+/- 5%) No embedded current protection Up to 1.5 A current recommended
	OFF	STLINK-V3E Active state	STLINK-V3E detects USBSTLK plug on CN3.
JP6 ⁽²⁾	ON	STLINK-V3E Reset state	Set STLINK-V3E in Reset mode (all input/outputs in high impedance).
JP7 ⁽²⁾	ON	T NRST (PA6)	STLINK-V3E output reset connected to T_NRST of STM32
JF/	OFF	I_NNST (FAU)	STLINK-V3E output reset isolated from T_NRST of STM32

^{1.} The default setting is in bold.

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^{2.} JP6 and JP7 must not be ON together



14.2 Solder bridges

The jumper functions and their default status are described in Table 22.

Table 22. Solder bridge configuration

SB name	Status ⁽¹⁾	Function	Comment
	ON	AGND to GND connection near the	Connect AGND to the GND plane near T3.
SB1	OFF	digital power buck-boost for analog measurements	Isolate AGND from the GND plane near T3.
	ON		Connect the PC4 of STM32 to the joystick.
SB2	OFF	PC4 connection to JOYSTICK_LEFT	Isolate PC4 from the joystick. PC4 can be used for any other application at the extension connector (CN8).
	ON		Connect PB2 of STM32 to the joystick.
SB3	OFF	PB2 connection to JOYSTICK_RIGHT	Isolate PB2 from the joystick. PB2 can be used for any other application at the extension connector (CN8).
	ON		Connect PB10 of STM32 to the joystick.
SB4	OFF	PB10 connection to JOYSTICK_UP	Isolate PB10 from the joystick. PB10 can be used for any other application at the extension connector (CN8).
	ON		Connect PC13 to JOYSTICK.
SB5	OFF	PC13 connection to JOYSTICK_SELECT	Isolate PC13 from JOYSTICK. PC13 can be used for any other application at the extension connector (CN9).
	ON		Connect PC5 of STM32 to JOYSTICK.
SB6	OFF	PC5 connection to JOYSTICK_DOWN	Isolate PC5 from JOYSTICK. PC5 can be used for any other application at the extension connector (CN9).
SB7	ON	Red power LED (LD1) cathode	Connect the red power LED to the inverted Buck.
357	OFF	connection	Isolate the red power LED from the inverted Buck.
SB8	ON	Blue power LED (LD1) cathode	Connect the blue power LED to the inverted Buck.
ОБО	OFF	connection	Isolate the blue power LED from the inverted Buck.
SB9	ON	Green power LED (LD1) cathode	Connect the green power LED to the inverted Buck.
020	OFF	connection	Isolate the green power LED from the inverted Buck.
SB10	ON	PF0 connection to the extension	Connect PF0 to the extension connector (CN9).
0210	OFF	connector (CN9)	Isolate PF0 from the extension connector (CN9).
SB11	ON	PF1 connection to the extension	Connect PF1 to the extension connector (CN9).
OBTI	OFF	connector (CN9)	Isolate PF1 from the extension connector (CN9).
	ON		Connect PC3 to BUCKBOOST_USBPD_EN.
SB12	OFF	PC3 connection to BUCKBOOST_USBPD_EN	Isolate PC3 from BUCKBOOST_USBPD_EN. PC3 can be used for any other applications at the extension connector (CN8).
SB13	ON	PA0 secondary connection	RESERVED
3013	OFF	(RESERVED)	Isolate PA0 from BUCKBOOST_I_IN_SENSE.
	ON		Connect PA2 to BUCKBOOST_I_IN_AVG.
SB14	OFF	PA2 connection to BUCKBOOST_I_IN_AVG	Isolate PA2 from BUCKBOOST_I_IN_AVG. PA2 can be used for any other applications at the extension connector (CN8).
SB15	ON	VBAT connection to VDD	Connect VBAT to VDD.
0010	OFF	VDAT CONTINUOUS (IO VDD	Isolate VBAT from VDD.

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SB name	Status ⁽¹⁾	Function	Comment
	ON		Connect PB3 to T_SWO.
SB16	OFF	PB3 connection to T_SWO	Isolate PB3 from T_SWO. PB3 can be used for any other applications at the extension connector (CN9).
CD47	ON	VREF+/VREFP connection to VDDA/	Connect VREF+/VREFP to VDDA/AVDD.
SB17	OFF	AVDD	Isolate VREF+/VREFP from VDDA/AVDD.
07.40	ON	VREF+/VREFP connection to VREF	Connect VREF+/VREFP to VREF PWR.
SB18	OFF	PWR	Isolate VREF+/VREFP from VREF PWR.
	ON		Connect PD2 to USBPD_550mA_PROTECT.
SB19	OFF	PD2 connection to USBPD_550mA_PROTECT	Isolate PD2 from USBPD_550mA_PROTECT. PD2 can be used for any other applications at the extension connector (CN9).
	ON		Connect PC12 to 5V_USBPD_1A_PROTECT.
SB20	OFF	PC12 connection to 5V_USBPD_1A_PROTECT	Isolate PC12 from 5V_USBPD_1A_PROTECT. PC12 can be used for any other applications at the extension connector (CN9).
SD21	ON OFF	VDDA/AVDD connection to VDD	Connect VDDA/AVDD to VDD.
3621	OFF	VDDA/AVDD connection to VDD	Isolate VDDA/AVDD from VDD.
SB22	ON	VDDA/AVDD connection to 3V3	Connect VDDA/AVDD to 3V3.
3022	OFF	VDDA/AVDD connection to 3V3	Isolate VDDA/AVDD from 3V3.
	ON		Connect PC11 to T_VCP_RX.
SB23	OFF	PC11 connection to T_VCP_RX	Isolate PC11 from T_VCP_RX. PC11 can be used for any other applications at the extension connector (CN9).
	ON		Connect PC10 to T_VCP_TX.
SB24	OFF	PC10 connection to T_VCP_TX	Isolate PC10 from T_VCP_TX. PC10 can be used for any other applications at the extension connector (CN9).
CDOF	ON	AGND to GND connection close to	Connect AGND to GND plane near STM32.
SB25	OFF	STM32	Isolate AGND from the GND plane near STM32.
	ON		Connect PB11 to BUCKBOOST_I_IN_SENSE.
SB26	OFF	PB11 connection to BUCKBOOST_I_IN_SENSE	Isolate PB11 from BUCKBOOST_I_IN_SENSE. PB11 can be used for any other applications at the extension connector (CN8).
	ON		Connect PA14 to T_SWCLK.
SB27	OFF	PA14 connection to T_SWCLK	Isolate PA14 from T_SWCLK. PA14 can be used for any other applications at the extension connector (CN9).
	ON		Connect PA15 to T_JTDI.
SB28	OFF	PA15 connection to T_JTDI	Isolate PA15 from T_JTDI. PA15 can be used for any other applications at the extension connector (CN9). Remove R89 if necessary.
	ON		Connect PA13 to T_SWDIO.
SB29	OFF	PA13 connection to T_SWDIO	Isolate PA13 from T_SWDIO. PA13 can be used for any other applications at the extension connector (CN9).
SB30	ON	3V3 connection to 3V3_OUT	Connect 3V3 to 3V3_OUT on the extension connector (CN8).
3830	OFF	5 V 5 551116581011 10 5 V 5_0 0 1	3V3_OUT is not powered on the extension connector (CN8).

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SB name	Status ⁽¹⁾	Function	Comment
SB31	ON	Power 3V3 STLK from 5V USBPD	Power 3V3_STLK from 5V_USBPD when USB Type- $C^{\text{\tiny{\$}}}$ is plugged
2831	OFF	Fower 3V3_31LK Holli 3V_U3BPD	No power on 3V3_STLK from 5V_USBPD when USB Type-C® is plugged
SB32	ON	5 V converter automatic Burst/PWM	Automatic Burst/PWM mode is activated.
3632	OFF	mode control	RESERVED
	ON		Connect PC2 to USBPD_VIN.
SB33	OFF	PC2 connection to USBPD_VIN	Isolate PC2 from USBPD_VIN. PC2 can be used for any other applications at the extension connector (CN9).
SB34	ON	PF1 connection to the extension HSE	Connect PF1 to HSE CLK footprint.
SB34	OFF	CLK footprint (OSC_IN)	Isolate PF1 from the HSE CLK footprint.
SB35	ON	PF0 connection to HSE CLK footprint	Connect PF0 to the HSE CLK footprint.
3533	OFF	(OSC_OUT)	Isolate PF0 from the HSE CLK footprint.
SB36	ON	PF0 connection to MCO of ST-LINKV3E	Connect PF0 to STL-LINK/V3E MCO.
3530	OFF	PFO CONNECTION to IVICO OF ST-LINKV3E	Isolate PF0 from STL-LINK/V3E MCO.
SB37	ON	VDEE manual vallence reference chains	VREF is set at 2.5 V. Remove R138.
SB37	OFF	VREF power voltage reference choice	VREF is set at 3.25 V.
CD20	ON	EV connection to EV OUT	This connects 5V to 5V_OUT on the extension connector (CN9).
SB38	OFF	5V connection to 5V_OUT	5V_OUT is not powered on the extension connector (CN9).

^{1.} Default configuration in bold.

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15 STM32G474RET6 GPIO and pin assignment

Table 23. STM32G474RET6 GPIO and pin assignment

Pin number	Pin name	Signal assignment	Main function		connector umber
Hullibel				CN9	CN8
1	VBAT	VDD	MCU power	-	-
2	PC13	JOYSTICK_SELECT	Joystick	23	-
3	PC14-OSC32_IN	BUCKBOOST_LOAD_50%	Buck-boost	24	-
4	PC15- OSC32_OUT	BUCKBOOST_LOAD_100%	Buck-boost	25	-
5	PF0-OSC_IN	PF0 (Free)	-	26	-
6	PF1-OSC_OUT	PF1 (Free)	-	27	-
7	PG10-NRST	T_NRST	STLINK	30	-
8	PC0	PC0 (Free)	-	28	-
9	PC1	PC1 (Free)	-	29	-
10	PC2	USBPD_VIN	USBPD	31	-
11	PC3	BUCKBOOST_USBPD_EN	Buck-boost	-	31
12	PA0	BUCK_GREEN_SENSE	RGB LED	-	30
13	PA1	BUCKBOOST_VIN	Buck-boost	-	29
14	PA2	BUCKBOOST_I_IN_AVG	Buck-boost	-	28
15	VSS	GND	MCU power	2/32	2/32
16	VDD	VDD	MCU power	-	3
17	PA3	BUCKBOOST_VOUT	Buck-boost	-	27
18	PA4	PA4 (Free)	-	-	26
19	PA5	PA5 (Free)	-	-	25
20	PA6	PA6 (Free)	-	-	24
21	PA7	BUCK_RED_SENSE	RGB LED	-	23
22	PC4	JOYSTICK_LEFT	Joystick	-	22
23	PB2	JOYSTICK_RIGHT	Joystick	-	21
24	PB0	BUCK_BLUE_SENSE	RGB LED	-	20
25	PB1	LED_LEFT_ORANGE	User LED	-	19
26	PB10	JOYSTICK_UP	Joystick	-	18
27	VSSA	AGND	MCU power	-	4
28	VREF+	VREFP	MCU power	-	6
29	VDDA	AVDD	MCU power	-	7
30	PC5	JOYSTICK_DOWN	Joystick	-	17
31	VSS	GND	MCU power	2/32	2/32
32	VDD	VDD	MCU power	-	3
33	PB11	BUCKBOOST_I_IN_SENSE	Buck-boost	-	16
34	PB12	BUCKBOOST_P1_DRIVE	Buck-boost	-	15
35	PB13	BUCKBOOST_N1_DRIVE	Buck-boost	-	14

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Div.				Extension	connector
Pin number	Pin name	Signal assignment	Main function	Pin n	umber
				CN9	CN8
36	PB14	BUCKBOOST_N2_DRIVE	Buck-boost	-	13
37	PB15	BUCKBOOST_P2_DRIVE	Buck-boost	-	12
38	PC6	BUCK_RED_DRIVE	RGB LED	-	11
39	PC7	RC sinus function	RC sinus	-	10
40	PC8	BUCK_GREEN_DRIVE	RGB LED	-	9
41	PC9	PC9 (Free)	-	-	8
42	PA8	BUCK_BLUE_DRIVE	RGB LED	4	-
43	PA9	USBPD_DBCC1	USBPD	5	-
44	PA10	USBPD_DBCC2	USBPD	6	-
45	PA11	USBPD_FS_DM	USBPD	7	-
46	PA12	USBPD_FS_DP	USBPD	8	-
47	VSS	GND	MCU power	2/32	2/32
48	VDD	VDD	MCU power	-	3
49	PA13	T_SWDIO	STLINK	9	-
50	PA14	T_SWCLK	STLINK	10	-
51	PA15	LED_DOWN_BLUE/T_JTDI	User LED/JTAG	11	-
52	PC10	T_VCP_TX	STLINK	12	-
53	PC11	T_VCP_RX	STLINK	13	-
54	PC12	5V_USBPD_1A_PROTECT	USBPD	14	-
55	PD2	USBPD_550mA_PROTECT	USBPD	15	-
56	PB3	T_SWO	STLINK	16	-
57	PB4	USBPD_CC2	USBPD	17	-
58	PB5	LED_UP_RED	User LED	18	-
59	PB6	USBPD_CC1	USBPD	19	-
60	PB7	LED_RIGHT_GREEN	User LED	20	-
61	PB8-BOOT0	PB8 (Free)	-	21	-
62	PB9	PB9 (Free)	-	22	-
63	VSS	GND	MCU power	2/32	2/32
64	VDD	VDD	MCU power	-	3

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16 B-G474E-DPOW1 product information

16.1 Product marking

The product and each board composing the product are identified with one or several stickers. The stickers, located on the top or bottom side of each PCB, provide product information:

 Main board featuring the target device: product order code, product identification, serial number, and board reference with revision

Single-sticker example:

Product order code Product identification syywwxxxx MBxxxx-Variant-yzz



Dual-sticker example:

Product order code Product identification

and

MBxxxx-Variant-yzz syywwxxxxx



Other boards if any: board reference with revision and serial number.

Examples:



MBxxxx-Variant-yzz syywwxxxxx



or 🖁

or



On the main board sticker, the first line provides the product order code, and the second line the product identification.

On all board stickers, the line formatted as "MBxxxx-Variant-yzz" shows the board reference "MBxxxx", the mounting variant "Variant" when several exist (optional), the PCB revision "y", and the assembly revision "zz", for example B01. The other line shows the board serial number used for traceability.

Products and parts labeled as "ES" or "E" are not yet qualified or feature devices that are not yet qualified. STMicroelectronics disclaims any responsibility for consequences arising from their use. Under no circumstances will STMicroelectronics be liable for the customer's use of these engineering samples. Before deciding to use these engineering samples for qualification activities, contact STMicroelectronics' quality department.

"ES" or "E" marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the ordering part number of the evaluation tool that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

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16.2 B-G474E-DPOW1 product history

Table 24. Product history

Order code	Product identification	Product details	Product change description	Product limitations
B-G474E-DPOW1	BG474EDPOW1\$AT1	MCU: STM32G474RET6 silicon revision "Z" MCU errata sheet: STM32G471xx/473xx/ 474xx/483xx/484xx device errata (ES0430) Board:	Initial revision	No limitation
	BG474EDPOW1\$AT3	MB1428-G474RE-B01 (main board) MCU: STM32G474RET6 silicon revision "X" MCU errata sheet: STM32G471xx/473xx/	MCU silicon revision changed	No limitation
		#74xx/483xx/484xx device errata (ES0430) Board: MB1428-G474RE-B01 (main board)		
	BG474EDPOW1\$AT4	MCU: STM32G474RET6 silicon revision "X" MCU errata sheet: STM32G471xx/473xx/ 474xx/483xx/484xx device errata (ES0430) Board:	New revision based on new packaging/labeling	No limitation
		• MB1428-G474RE-B01 (main board)		

16.3 Board revision history

Table 25. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB1428 (main board)	G474RE-B01	Initial revision	No limitation

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17 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

17.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15 21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible Party – U.S. Contact Information:

Francesco Doddo STMicroelectronics, Inc. 200 Summit Drive | Suite 405 | Burlington, MA 01803 USA

Telephone: +1 781-472-9634

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17.2 ISED Compliance Statement

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (B) / NMB-3 (B).

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES-3 (B) / NMB-3 (B).

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18 Product disposal

Disposal of this product: WEEE (Waste Electrical and Electronic Equipment)

(Applicable in Europe)



This symbol on the product, accessories, or accompanying documents indicates that the product and its electronic accessories should not be disposed of with household waste at the end of their working life.

To prevent possible harm to the environment and human health from uncontrolled waste disposal, please separate these items from other type of waste and recycle them responsibly to the designated collection point to promote the sustainable reuse of material resources.

Household users:

You should contact either the retailer where you buy the product or your local authority for further details of your nearest designated collection point.

Business users:

You should contact your dealer or supplier for further information.

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Revision history

Table 26. Document revision history

Date	Revision	Changes
12-Jul-2019	1	Initial release.
08-Sep-2020	2	Added: Section 6.2 Debug connector configuration Updated: Section 14.2 CN1 debug connector split in STDC14 and MIPI10 sections Appendix A Federal Communications Commission (FCC) and Innovation, Science and Economic Development Canada (ISED) Compliance Statements Class B compliance
06-Feb-2025	3	Added: Note to Table 7 regarding software Demo mode limitation B-G474E-DPOW1 product information with Product marking, Product history, and Board revision history Safety recommendations and Product disposal Updated: Section 11 Boot option clarified to indicate option bytes are changed from MCU default value
		 Section 13.2: Debug connector (CN1) simplification Figure 3 to Figure 5, Figure 7, Figure 11, Figure 17, Figure 19, and Figure 20 with standard component designation Removed Limitations section.

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