
Evaluation board for TDA7803A and TDA7808 power amplifiers in PSO package

Introduction

Scope of this document is to describe the EVAL-7803APSO-SA standalone demo module.

It contains the module description, the schematic, the bill of materials and the board layout of the following modules:
6038-469.18 v1.0

In the following chapters it will be referred as 469 module.

1 Hardware description

1.1 Board description

This board is based for TDA7803A and TDA7808 in PSO36 package. It is designed to provide 4 x 27 W on 4 Ω load.

Figure 1. EVAL-7803APSO-SA board Top view

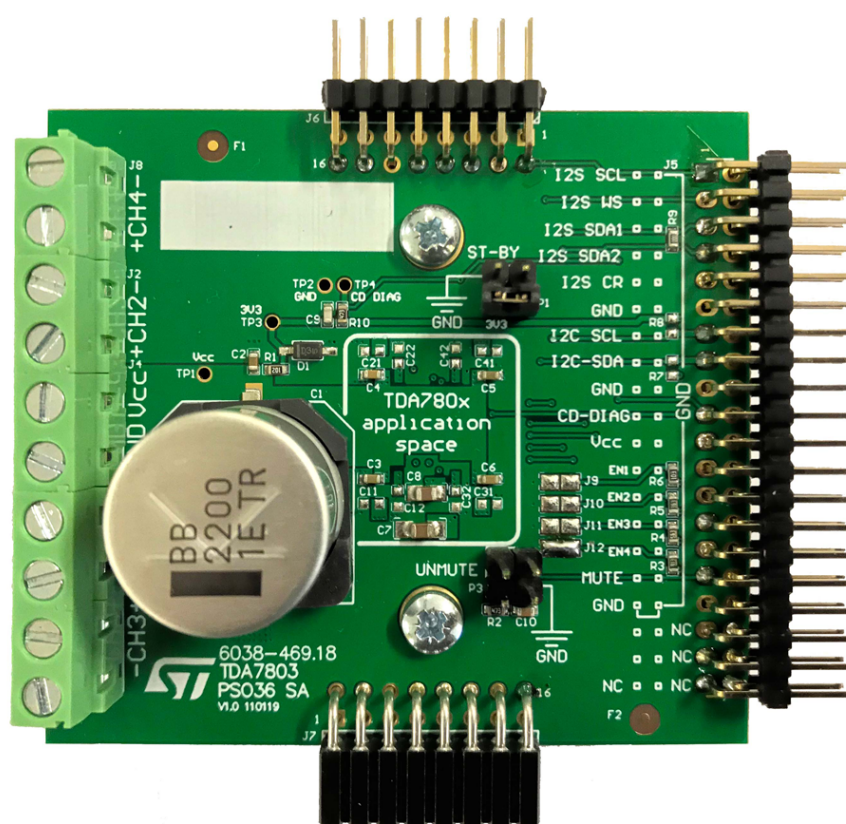
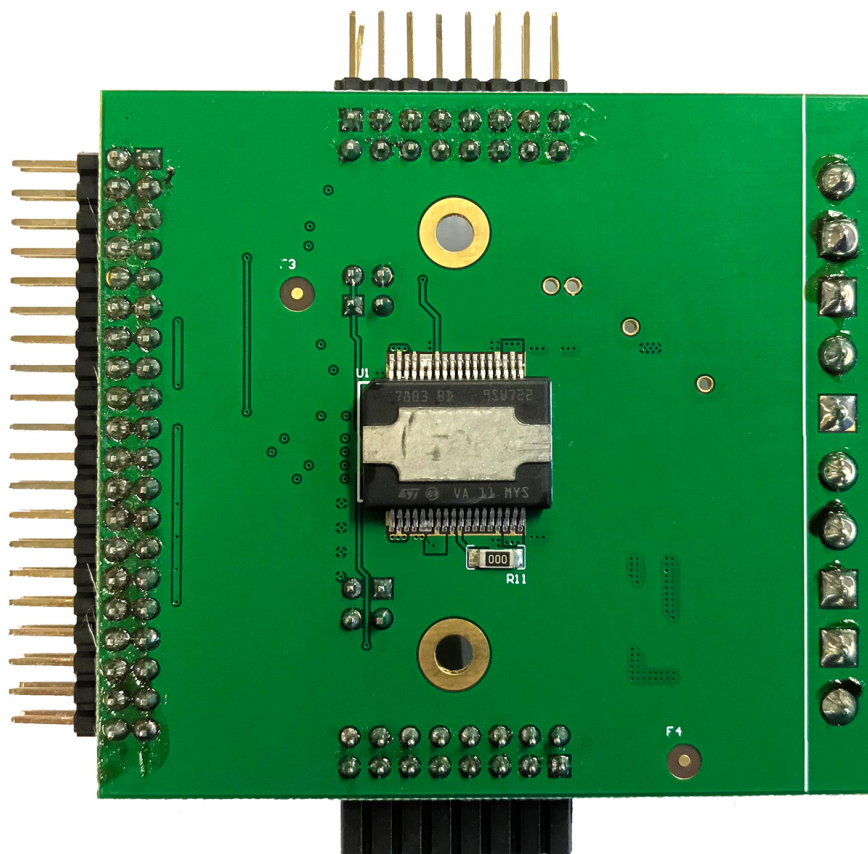


Figure 2. EVAL-7803APSO-SA board Bottom view



Note:

- Demo board are designed with scope to show typical device performance in standard application. Furthermore, some components mounted on PCB could result downsized for satisfy a full performance operation. Adequate heat dissipation must be provided for optimal performance: heatsink provided with demo board ensures optimal dissipation when device is supplied with 14 V supply and a 4 Ω load is connected to its outputs. For further information about high power measurements please contact ST application team.
- The Figure 2 is taken without heatsink which is listed in the BOM reported in the Table 1.

1.2 Connector and connections

Power supply

The power supply, ranging from 4.5 V to 18.5 V, can be connected on J4 screw terminal following the labels.

Outputs

The amplifier outputs are present on J1, J2, J3, J8 screw terminal. The output assigned to each connection is written nearby the connector

Input control signal

On J5 terminal is possible to find the I²C and I²S inputs. Additional control/monitor signals are available on this connector: please refer to [Section 1.3 Board option](#).

Board cascading

To test multiple device systems, is possible to connect more than one 469 modules together by means of J6 and J7. Plugging J6 of one board to J7 of another, the I²C and I²S bus will be shared allowing to control the system by means of one I²C interface and feed the same audio.

In order to command each device independently from each other, different addresses must be used on each 469 board. The number of 469 modules is limited by the maximum number of address that can be set.

1.3 Board option

Address selection

Proper I²C address for 469 module could be set by shorting with a 0 Ω resistor (or tin drop) one resistor from J9 to J12. Please refer to TDA7901 datasheet for list of available addresses.

3.3 V voltage reference

On board 3.3 V reference (made by R1 and D1) is used for pull-up resistor of digital lines. When accurate current measurement is needed (i.e. efficiency measurements) voltage reference should be disabled: in this case an external 3.3v reference must be provided for 3V3 line.

STBY function

Stand by function can be hardware controlled by jumper P1 (3V3 → Device ON or GND → Device standby).

UNMUTE

Hardware unmute function is controlled by P3 (GND → device mute). By default these jumpers are left open (device internal pull-up). P3 jumper allows also to remote control UNMUTE function through J10 connector (PIN 31, MUTE).

CD/DIAG

CD/DIAG function can be monitored through J10 connector, pin 19.

I²S data line pairing

If only one I²S data line is needed, SDA1 and SDA2 could be shorted through R9 with a 0 Ω (or tin drop).

1.4 Parallelized channels

TDA7803 provides the possibility to parallelize the channels to increase the output current capability. During this operation one of the two channels in the parallel configuration will become the "Master" channel, the other one will be the "Slave" channel.

The possible configurations are:

- CH1 and CH2 in parallel: CH1 is the master, CH2 is the slave
- CH3 and CH4 in parallel: CH3 is the master, CH4 is the slave

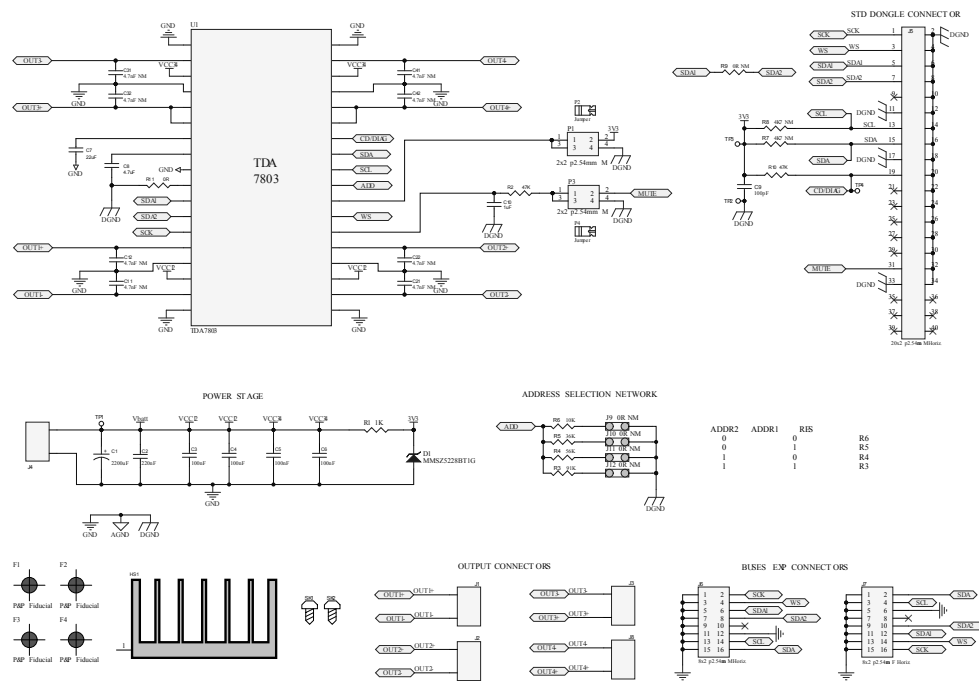
To use parallel configuration connect the two channels outputs close to the load, respecting output polarities.

Important:

When channels are parallelized, pay attention to the device's configuration. Play signal with parallelized channels when the device is configured for single output channels can lead to improper functioning

1.5 Board schematic

Figure 3. EVAL-7803APSO-SA board schematic



1.6 Bill of materials

Table 1. Bill of materials

Quantity	Designator	Description	Value	Rated V	Package
1	C1	SMD Electrolytic Capacitor	2200 uF	25 V	19x19 d18 mm
1	C2	SMD MLCC X7R Capacitor	220 nF	25 V	0603
4	C3, C4, C5, C6	SMD MLCC X7R Capacitor	100 nF	25 V	0603
1	C7	SMD MLCC X7R Capacitor	22 uF	6.3 V	1206
1	C8	SMD MLCC X7R Capacitor	4.7 µF	10 V	0805
1	C9	SMD MLCC X7R Capacitor	100 pF	16 V	0603
1	C10	SMD MLCC X7R Capacitor	1 µF	25 V	0805
8	C11, C12, C21, C22, C31, C32, C41, C42	SMD MLCC X7R Capacitor	4 n7	25 V	0603
1	D1	3.9V Zener DIODE	-	3.9 V	SOD-123
1	HS1	HEATSINK	-	-	-
5	J1, J2, J3, J4, J8	Terminal Block 2position p5.08mm	-	-	p5.08 mm
1	J5	Header, 40-Pin, Dual row, TH, Right Angle, Male	-	-	p2.54 mm
1	J6	Header, 8-Pin, Dual row, TH, Right Angle, Male	-	-	p2.54 mm
1	J7	Header, 8-Pin, Dual row, TH, Right Angle, Female	-	-	p2.54 mm
4	J9, J10, J11, J12	Solder Jumper 0805	-	-	0805
2	P1, P3	Header, 2-Pin, Dual row, TH, Straight, Male	-	-	p2.54 mm
2	P2, P4	Jumper shunt p2.54mm	-	-	p2.54 mm
1	R1	Surface mount chip resistor	1 KΩ	75 V	0603
1	R2	Surface mount chip resistor	47 KΩ	75 V	0603
1	R3	Surface mount chip resistor	91 KΩ	75 V	0603
1	R4	Surface mount chip resistor	56 KΩ	75 V	0603
1	R5	Surface mount chip resistor	36 KΩ	75 V	0603
1	R6	Surface mount chip resistor	10 KΩ	75 V	0603
2	R7, R8	Surface mount chip resistor	4.7 KΩ	75 V	0603
1	R9	Surface mount chip resistor	0 Ω	75 V	0603
1	R10	Surface mount chip resistor	47 KΩ	75 V	0603
1	R11	Surface mount chip resistor	0 Ω	200 V	1206
2	SK1, SK2	M3 Fastener	-	-	-
1	U1	4 Channel Class AB Amplifier	-	-	PSO36

1.7 Board layout

Figure 4. Assembly top

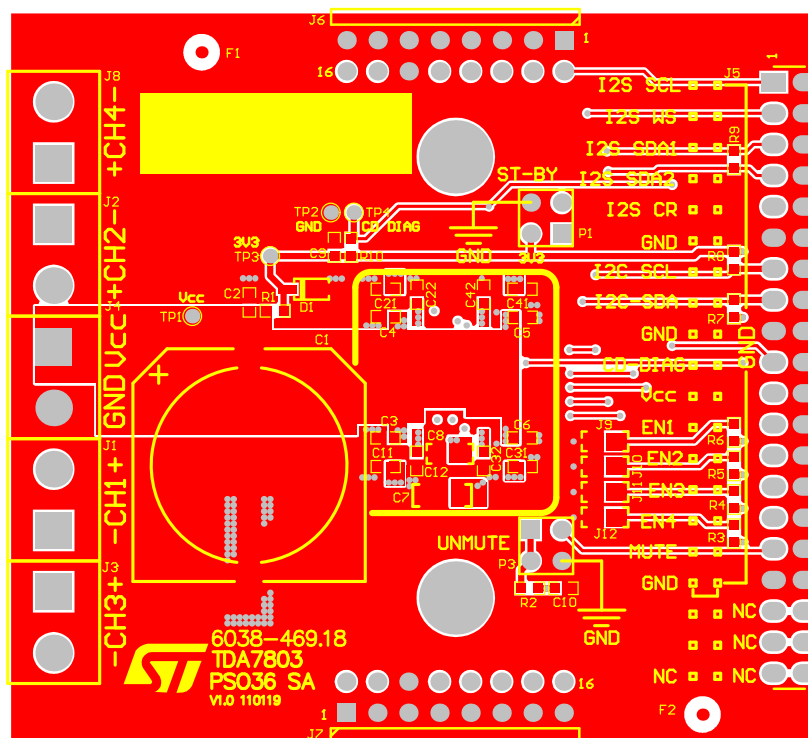


Figure 5. Inner 1

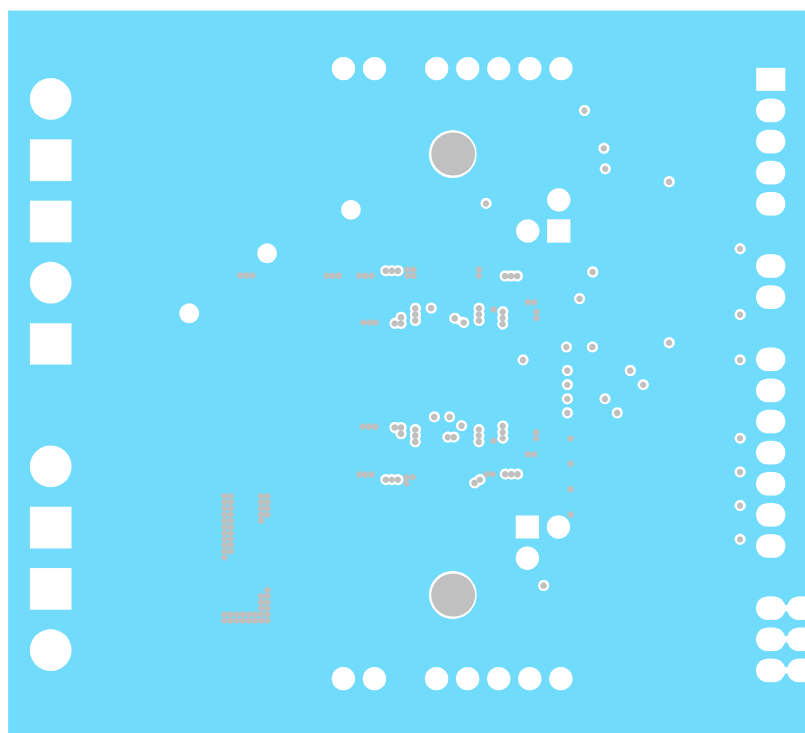


Figure 6. inner 2

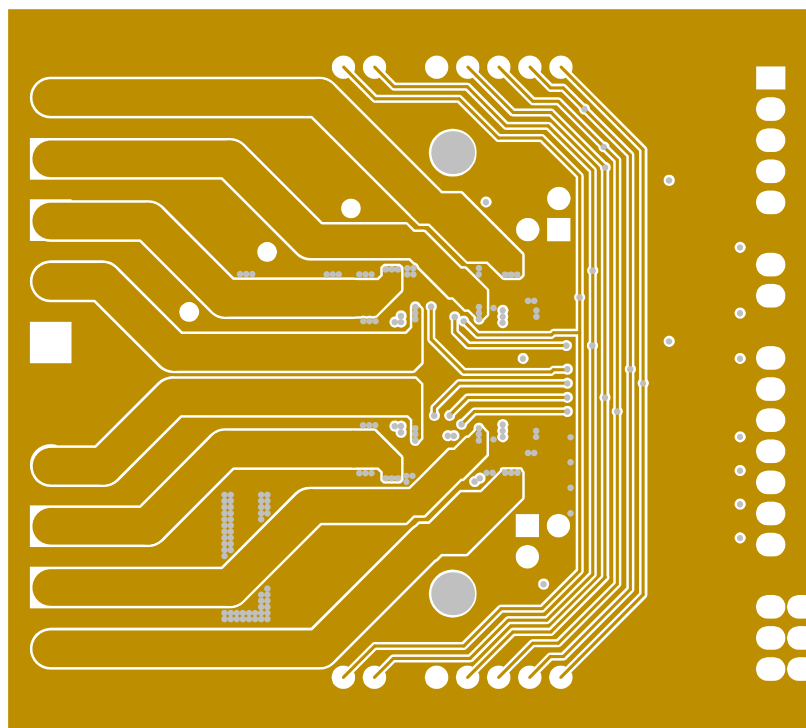
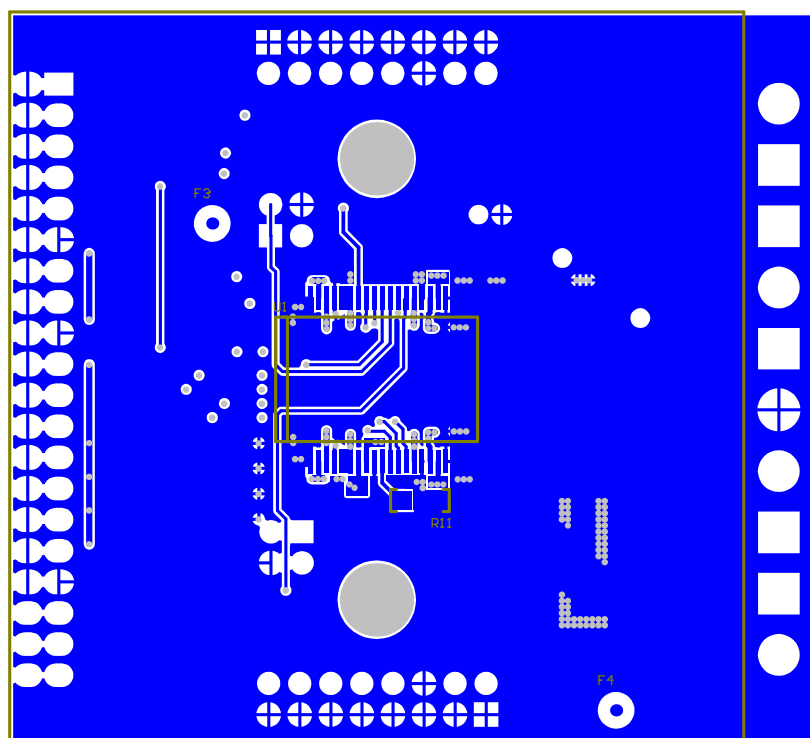


Figure 7. Assembly bottom



2 Information on board use

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Revision history

Table 2. Document revision history

Date	Version	Changes
05-Aug-2020	1	Initial release.

Contents

1	Hardware description	2
1.1	Board description	2
1.2	Connector and connections	4
1.3	Board option	4
1.4	Parallelized channels	4
1.5	Board schematic	5
1.6	Bill of materials	6
1.7	Board layout	7
2	Information on board use	9
	Revision history	10

List of figures

Figure 1.	EVAL-7803APSO-SA board Top view	2
Figure 2.	EVAL-7803APSO-SA board Bottom view	3
Figure 3.	EVAL-7803APSO-SA board schematic	5
Figure 4.	Assembly top	7
Figure 5.	Inner 1.	7
Figure 6.	inner 2.	8
Figure 7.	Assembly bottom	8

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