UM0212
User manual

STOTG04 USB OTG full-speed transceiver demonstration board

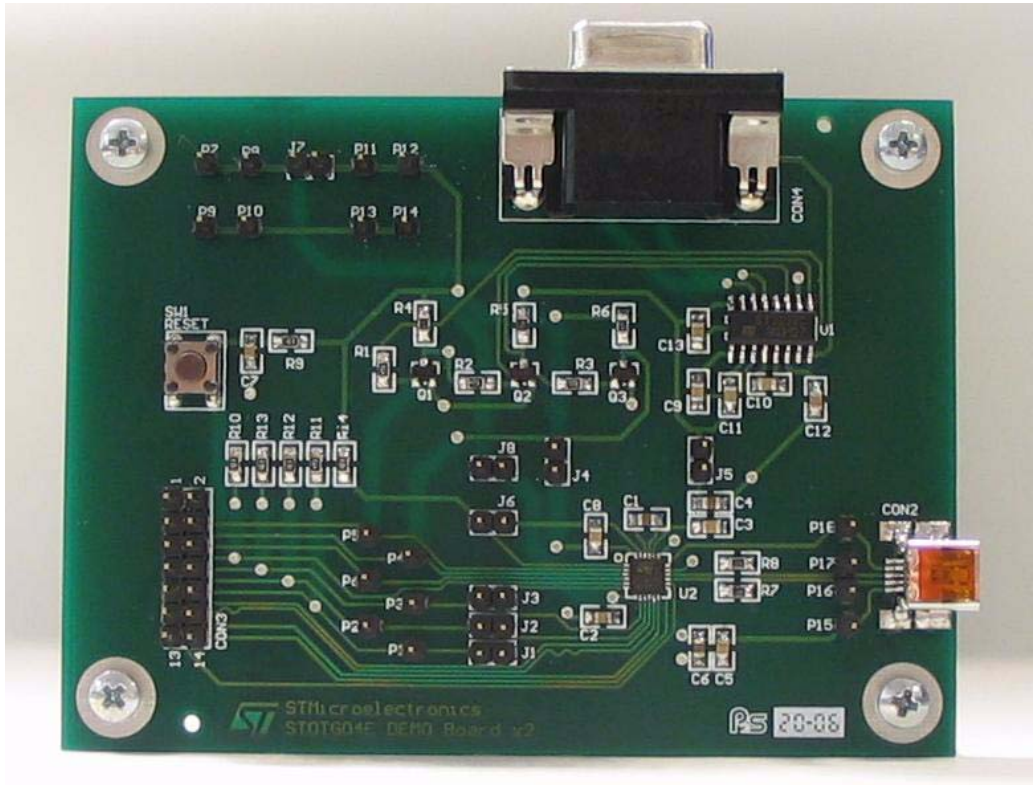
Introduction

This manual explains how to use and take full advantage of the STOTG04 universal serial bus (USB) on-the-go (OTG) full-speed transceiver demonstration board, which is designed to help users evaluate their USB OTG applications. The PC board (PCB) connections make it possible to test the STOTG04 transceiver while it is connected to the USB OTG controller. Without the controller, the STOTG04 is configurable through the I^2C interface.

The STOTG04 is fully compliant with the USB v2.0 specification and the on-the-go supplement to this specification (see http://www.usb.org for details). It provides a complete physical layer (PHY) solution for any USB OTG device. When the STOTG04 is connected to a USB OTG controller, it is ideal for use with several mobile applications (such as cell phones, digital cameras, printers and PDAs).

The STOTG04 transceiver is controlled by the "USB OTG Demo" software that runs on Microsoft Windows operating systems. This software enables designers to configure and monitor the transceiver's internal registers.

Figure 1. STOTG04 demonstration board



Contents

1 STOTG04 demonstration board hardware

The demonstration board consists of six main parts (see *Figure 2* and *Figure 3*).

- Power supply pins (V_{BAT} and V_{IF})
- Level shifters
- The STOTG04 full-speed transceiver
- Configuration jumpers
- A USB OTG controller connector
- A reset switch (see *Section 1.5*).

The STOTG04 needs two types of power supply voltages to function (see *Section 1.1*). The battery supply voltage (V_{BAT}) supplies power to the analog functions, and the digital interface voltage (V_{IF}) supplies power to the digital interface. These supply voltages are connected to the demonstration board through the power pins.

The board can also be controlled by a PC serial port (see *Section 1.2*). The RS-232C PC signal levels are converted to I^2C levels by the level shifter block.

The jumpers allow users to test and measure the STOTG04 characteristics without a USB OTG controller (see *Section 1.3*).

The USB OTG controller header connector enables the user to connect a USB OTG controller (see *CON3 pin*) or any digital control system to the demonstration board. USB or USB OTG devices can be connected via the mini-AB connector (see *Appendix A: STOTG04 demonstration board schematics*).

Figure 2. STOTG04 demonstration board block diagram

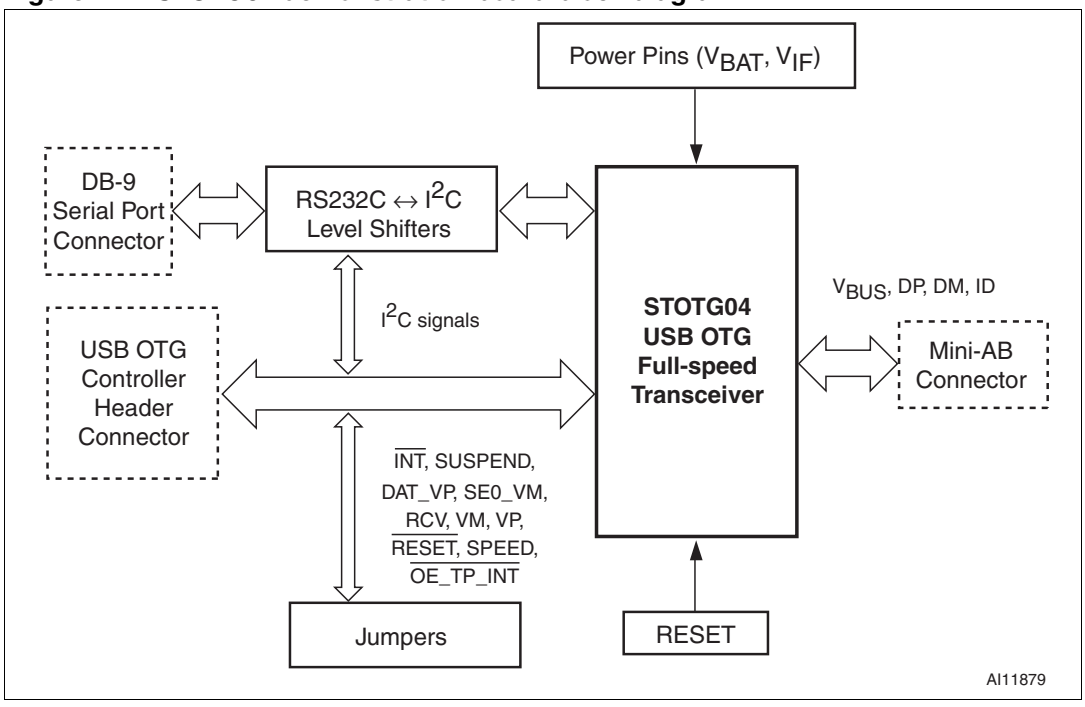


Figure 3. Assembled demonstration board PCB

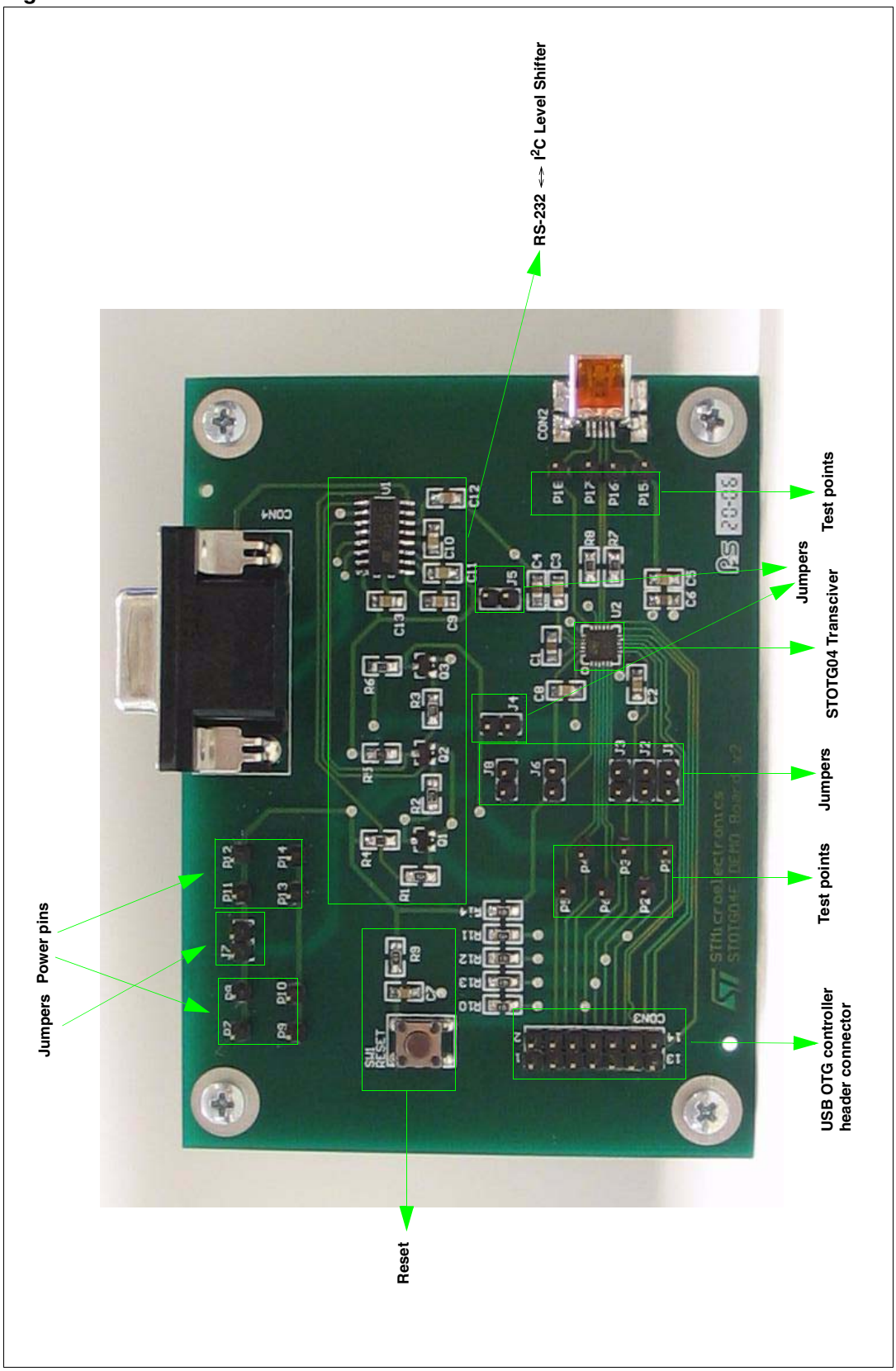
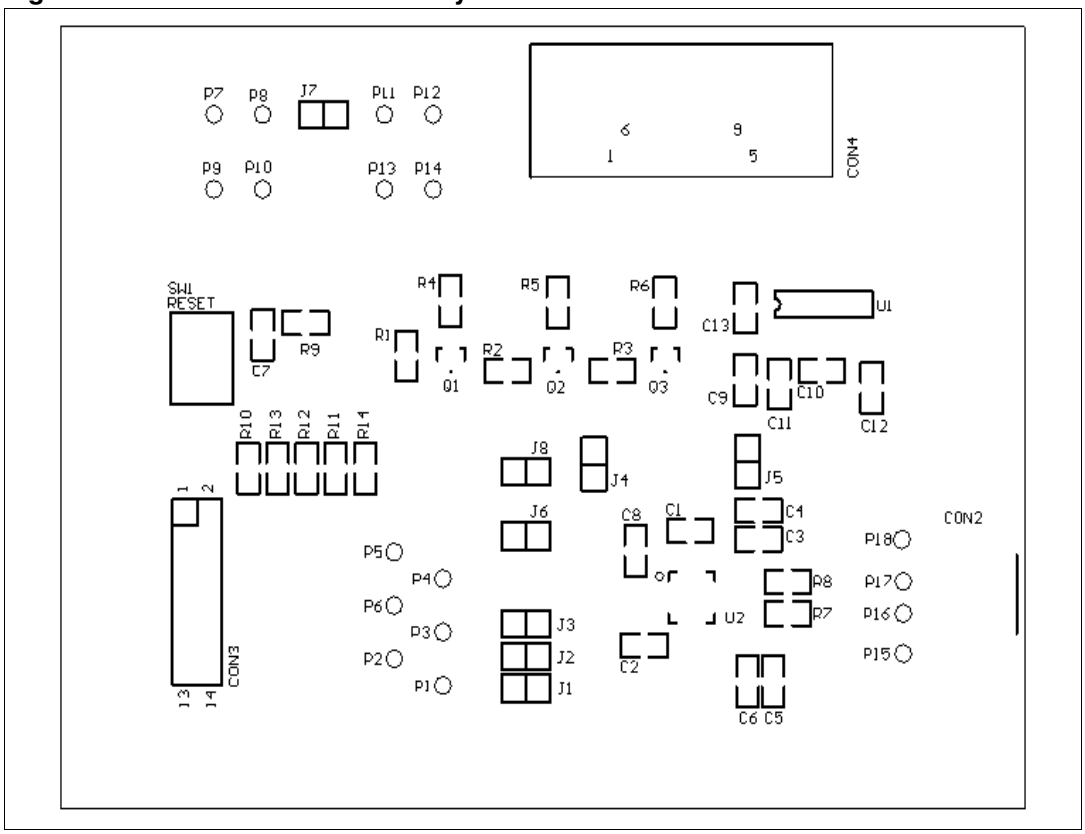


Figure 4. Demonstration board layout



1.1 STOTG04 power requirements

The recommended supply voltages of the transceiver are:

- V_{IF} = 1.6 V to 3.6 V (V_{IF} = 1.8 V, typ)
- V_{BAT} = 2.7 V to 5.5 V (V_{BAT} = 3.3 V, typ).

The demonstration board was designed for these same voltage ranges. However, the board does not contain any voltage regulators, so if only one common supply voltage is used, the following range is recommended:

V_{COMMON} = 2.7 V to 3.6 V

Note: Jumper J7 connecting the V_{BAT} and V_{IF} power supply pins has to be shorted (see Table 1).

1.2 Connecting to a PC

The STOTG04 demonstration board must be connected to the PC serial port via a non-crossed serial cable. The PC serial port can be selected in the USB OTG demonstration board software (see *Chapter 2*).

1.3 Jumper assignments

Table 1. Demonstration board jumper assignments(1)

Jumper	Related pin (s)	Function	
J1	$\overline{\text{OE\_TP\_INT}}$	Short	Enables the differential driver or I^2C mode (when TRANSP_EN Bit = 1)
		Open	Interrupt output when SUSPEND = 0 (J2) and SUSPEND Bit = 1
J2	SUSPEND	Short	Disables power-down mode when SUSPEND Bit = 1
		Open	Enables power-down mode when SUSPEND Bit = 1
J3	SPEED	Short	Enables low-speed mode operation
		Open	Enables full-speed mode operation
J4	V_{IF}	Short	Provides power to the V_{IF} pin. Can be used for current consumption measurement
		Open	V_{IF} pin is left floating
J5	V_{BAT}	Short	Provides power to the V_{BAT} pin. Can be used for current consumption measurement
		Open	V_{BAT} pin is left floating
J6	ADR	Short	The lsb of the I^2C address is '0'
		Open	The lsb of the I^2C address is '1'
J7	V_{BAT}, V_{IF}	Short	$V_{BAT} = V_{IF}$ (V_{COMMON} must be 3.0 V - 3.6 V)
		Open	$V_{BAT} \neq V_{IF}$ (use recommended V_{BAT} and V_{IF})
J8	V_{TRM}, V_{BAT}	Short	Internal LDO regulator bypassed (usable only when the V_{BAT} supply voltage is between 3.0 V and 3.6 V)
		Open	Internal LDO regulator operational

1. See *Figure 4*.

1.4 Connector assignments

Table 2. Demonstration board connectors(1)

Connector	Descriptions
CON1	Power supply pins (P7-P14): V_{BAT}, V_{IF}, and GND
CON2	USB Mini-AB connector for USB/USB OTG devices
CON3	Header connector for the USB OTG controller via the serial interface engine (SIE) signals (see *Section 1.4.1*)
CON4	DSUB-9 connector for the PC serial port used to control the transceiver through the I^2C bus

1. See *Figure 4*.

1.4.1 CON3 pin

The USB OTG controller accesses the USBOTG04's SIE through the CON3 connector and controls the following signals (see *Table 3*):

- DAT_VP
- SE0_VM
- RCV
- $\overline{\text{OE\_TP\_INT}}$
- I^2C bus, and
- other main signals used by most types of OTG controllers.

Warning: The Q1 and Q3 transistor bases **MUST** be connected to GND **BEFORE** the demonstration board is connected to the USB OTG controller. The Q1 and Q3 bases are connected to the R1 and R3 resistors (see *Appendix A: STOTG04 demonstration board schematics*).

Table 3. CON3 pin assignments

Pin No.	Description	Pin no.	Description
1	GND	8	SPEED
2	Not connected	9	VM
3	SCL (I^2C clock signal)	10	$\overline{\text{OE\_TP\_INT}}$
4	SDA (I^2C data signal)	11	RVC
5	$\overline{\text{INT}}$	12	VP
6	$\overline{\text{RESET}}$	13	DAT_VP
7	SUSPEND	14	SE0_VM

1.5 Reset switch (SW1)

The Reset switch (see *Figure 3* and *Figure 4*) can be used to manually reset the STOTG04 hardware. The reset pulse can also be generated by the USB OTG controller via the CON3 $\overline{\text{RESET}}$ pin (see *Table 3*).

2 USB OTG demonstration software

The "USB OTG Demo" software controls the STOTG04 full-speed transceiver. The application requires a PC with at least one serial port, and any Windows® operating system.

Note: This software has been tested on Windows XP.

The software configures and monitors the STOTG04's internal registers. It sends and receives I^2C signals with RS-232C voltage levels via the serial port. The RS-232C PC signal levels are converted to the proper I^2C signal levels by the demonstration board's level shifter (see *Chapter 1*).

2.1 Launching the software

The USB OTG demonstration program does not require any installation.

1. Copy the "demo.exe" file to a destination folder or *C:\temp* directory
2. Double-click on the "demo.exe" file to launch the PC-to-demonstration board interface window
3. Use the RS-232C cable to connect the board to the PC (or confirm this connection if it is already set-up)
4. Select the correct PC serial port in the interface window (for example COM1, COM2, COM3 or COM4)
5. Select the STOTG04 address in the interface window (for example 2Ch or 2Dh). The default address is "2Dh", which is equivalent to open jumper J6 (see *Section 1.3: Jumper assignments*)
6. Select the correct device version (STOTG04E or STOTG04ES)
7. Connect the correct supply voltage to the demonstration board.

2.2 PC-to-demonstration board communication

Communication is controlled by two programming buttons (see *Figure 5*, bottom-right):

- Read all
- Write all.

These buttons enable READs or WRITEs to all of the STOTG04 registers, otherwise the program cannot communicate with the STOTG04.

Note: For correct use of the application and to prevent any anomalous behavior, it is important to understand the STOTG04 registers as well as the READ/WRITE sequence of the USB OTG demonstration program when multiple registers are changing at the same time.

2.3 STOTG04 registers

The STOTG04 has four types of registers (see *Figure 5*).

- Control registers
- Interrupt registers (source, latch, and falling/rising edges)
- Information registers (vendor ID and product ID)
- STOTG04 device address (2Ch or 2Dh) registers.

Having a general knowledge of the registers may prevent certain anomalies. For example, if the J1 jumper is shorted and the "TRANSP_EN" bit has been set by mistake, the STOTG04 stops I^2C communication with the board because it is now in "Transparent I^2C" mode. The communication can be reinstated by opening J1. Knowing the READ and WRITE sequence is important for using the interrupt registers, especially when multiple registers are changing at the same time. In these cases, the interrupt's "falling edge" and "rising edge" registers have the highest priority. For example, to monitor the VBUS_VLD interrupt (this is usually done when the charge pump is switched ON):

1. set the VBUS_VLD bit in the "rising edge" register and the VBUS_DRV bit in "Control Register2"
2. Click on the "Write All" button

   The register WRITE order (priority) is:

   – "Write [Rising Edge (VBUS_VLD)]" **THEN**

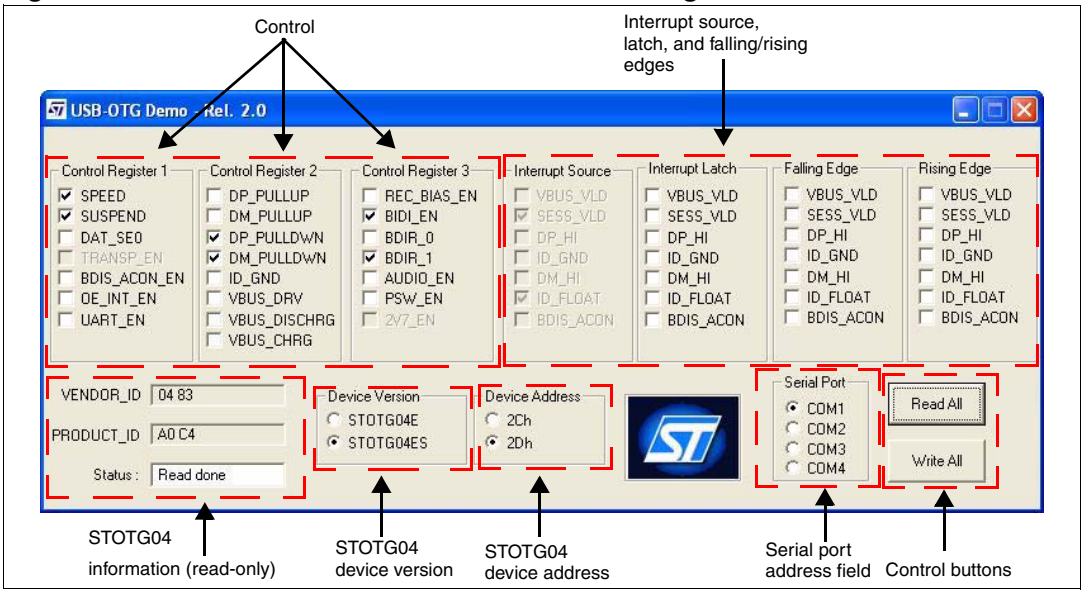
   – "Write [Control Register 2 (VBUS_DRV)]".

The user should always monitor the "Status" field to see if READ or WRITE operations are successful.

Note that the TRANSP_EN bit in the control register 1 and the 2V7_EN bit in the control register 3 are enabled only when the STOTG04E device version is selected. The "VendorID" and "ProductID" registers are read-only and provide the STOTG04's identity.

Note: See the STOTG04 USB OTG full-speed transceiver datasheet for details.

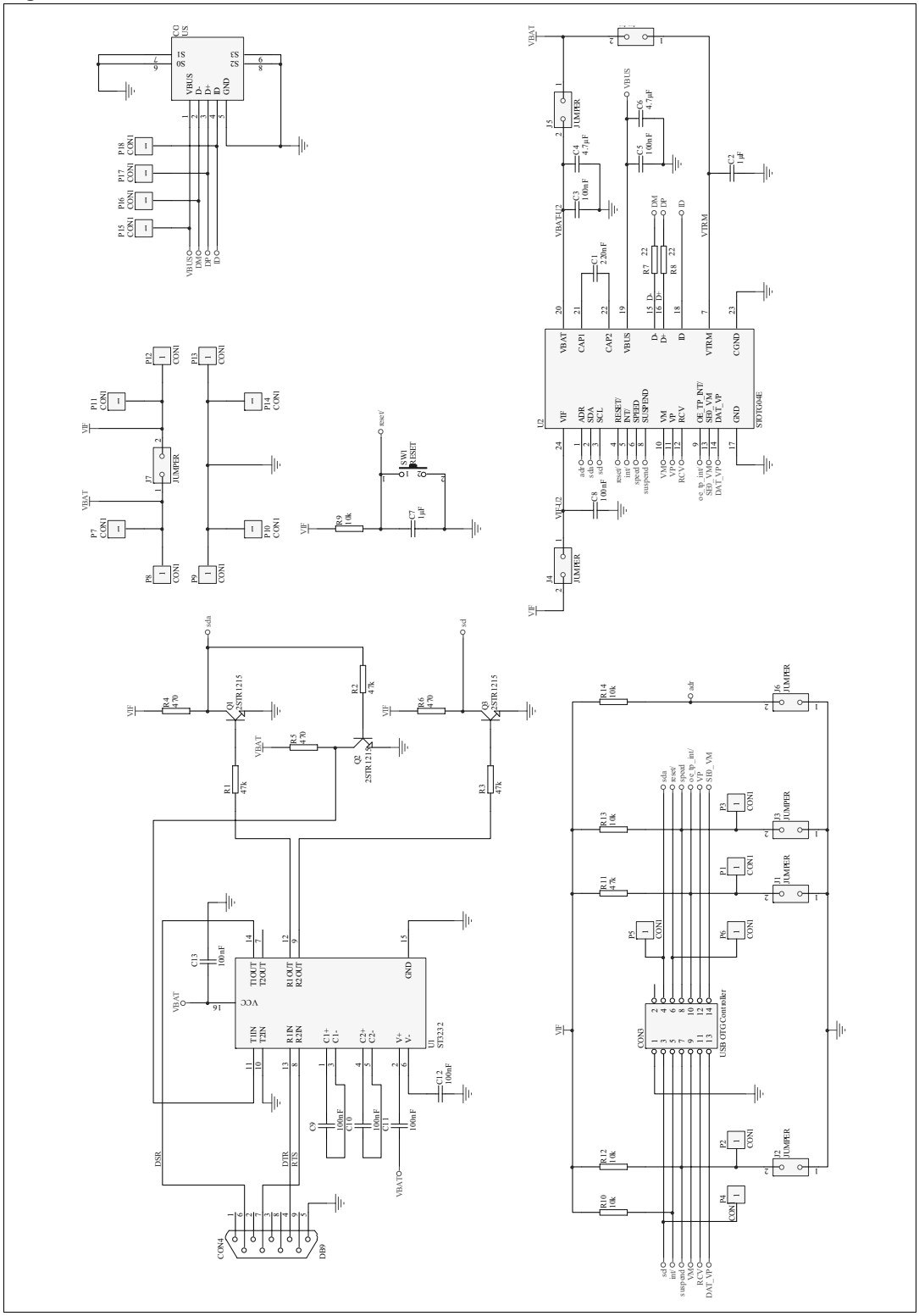
Figure 5. USB OTG demonstration user interface registers



Note: These are STOTG04 register settings after the first "Read All" instruction.

Appendix A STOTG04 demonstration board schematics

Figure 6. STOTG04 demonstration board schematics



Appendix B STOTG04 demonstration board bill of materials

Table 4. STOTG04 bill of materials

Part type	Qty	Designator	Footprint
ST3232	1	U1	SO-16
STOTG04	1	U2	QFN-24
100 nF ±10%	8	C3, C5, C8, C9, C10, C11, C12, C13	0805
1 µF ±10%/16 V/X7R (high cap ceramic)	2	C2, C7	0805
220 nF ±10%/25 V/X7R	1	C1	0805
4,7 µF ±10%/6.3 V/X5R (high cap ceramic)	2	C4, C6	0805
47 kΩ ±5%	4	R1, R2, R3, R11	0805
470 Ω ±5%	3	R4, R5, R6	0805
22 Ω ±5%	2	R7, R8	0805
10 kΩ ±5%	5	R9, R10, R12, R13, R14	0805
Jumper	6	J1, J2, J3, J6, J7, J8	Thru-hole
Header 1	18	P1-P18	Thru-hole
Header 7x2	1	CON3	Thru-hole
DSUB-9 (male)	1	CON4	Thru-hole
Switch	1	SW1	Thru-hole
MINI USB-AB receptacle	1	CON2	USB mini A-B
2STR1215	3	Q1, Q2, Q3	SOT-23

Revision history

Table 5. Document revision history

Date	Revision	Changes
22-Jun-2006	1	Initial release
19-Nov-2008	2	Modified: *Figure 5*