

## Introduction

The STEVAL-ISB032V1 is a product evaluation board based on the STNS01, which is a linear charger for single cell Li-Ion batteries integrating an LDO regulator and several battery protection functions.

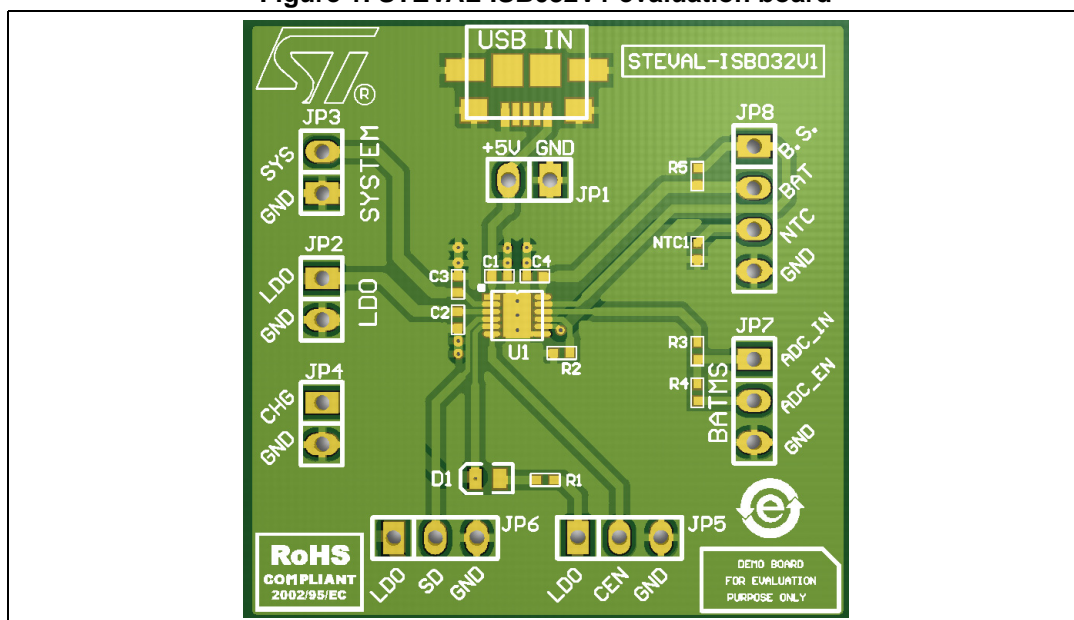
The device uses a CC/CV algorithm to charge the battery; the fast-charge current can be programmed using an external resistor. Precharge current and termination current are scaled accordingly. The floating voltage value is 4.2 V.

The input supply voltage is normally used to charge the battery and provide power to the LDO regulator; when a valid input voltage is not present and the battery is not empty, the device automatically switches to battery power.

The STNS01 integrates overcharge, overdischarge and overcurrent protection circuitry to prevent the battery from being damaged under fault conditions; it also features a charger enable input to stop the charging process when a battery overtemperature is detected by external circuitry.

When the shutdown mode is activated the battery power consumption is reduced to less than 500 nA to maximize battery life during shelf time.

**Figure 1. STEVAL-ISB032V1 evaluation board**

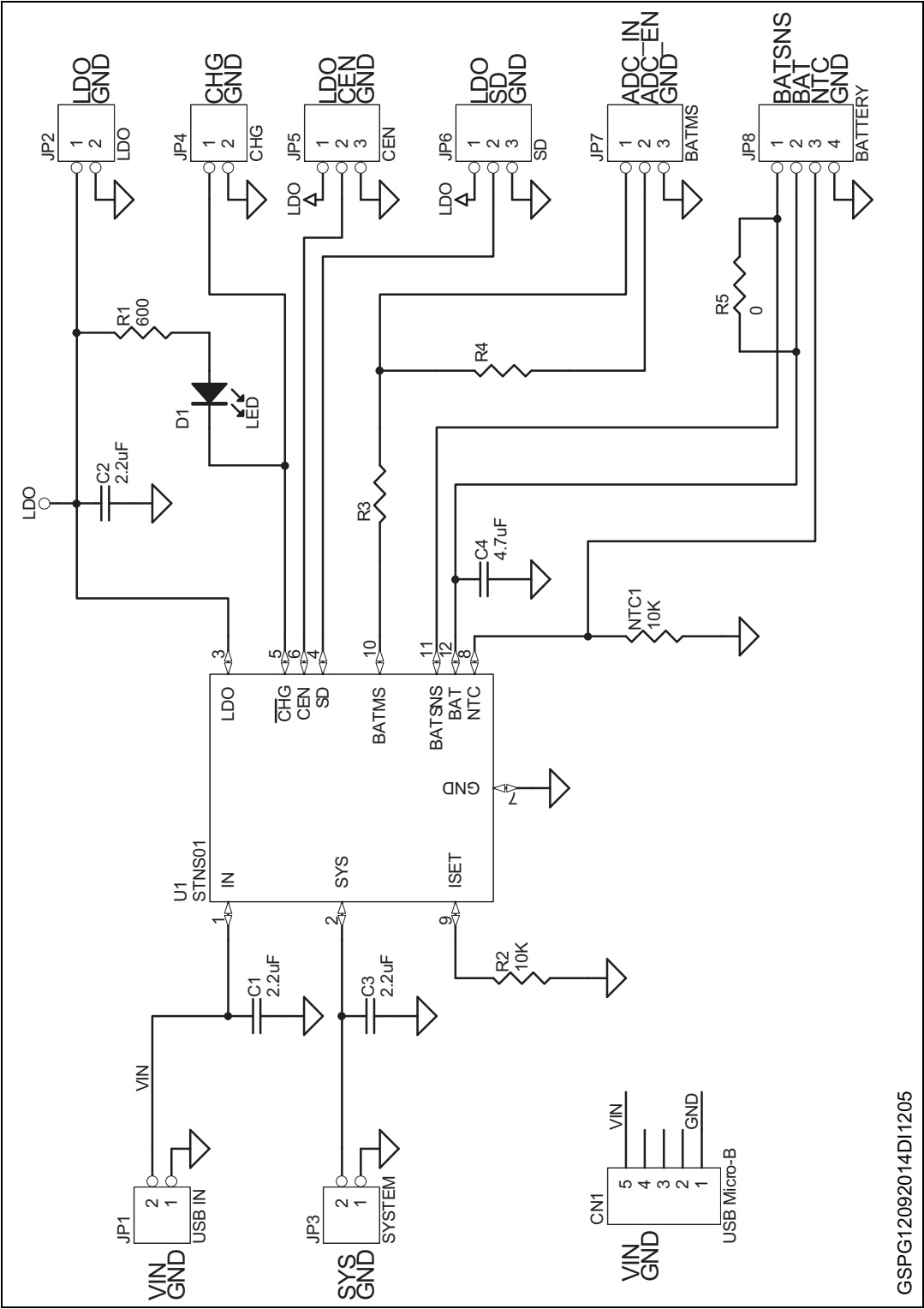


# 1      **General features**

- Charges single-cell Li-Ion batteries with CC-CV algorithm and charge termination
- Charge current programmable up to 400 mA
- 1% accuracy on floating voltage (4.2 V)
- Integrated 3.1 V LDO regulator
- Automatic power path management
- Battery overcharge protection
- Battery overdischarge protection
- Battery overcurrent protection
- Charging timeout
- Very low battery leakage in overdischarge/shutdown mode
- Low quiescent current
- Charge/fault status output
- Charger enable input

2 Schematic diagram

Figure 2. STEVAL-USB032V1 circuit schematic



GSPG12092014DI1205

Table 1. Bill of material (BOM)

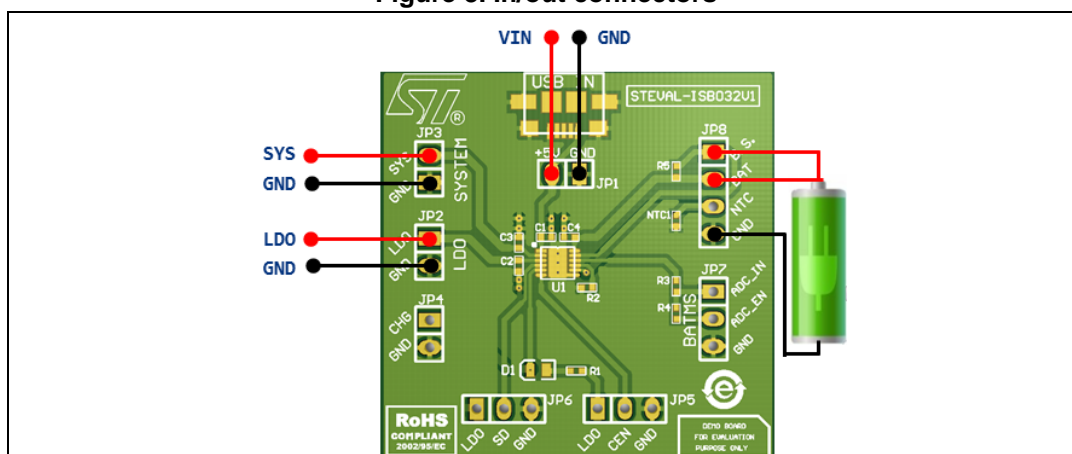
Component	Manufacturer	Part number / Description	Value	Size
C <sub>1</sub>	Murata	GRM188R71A225KE15D	2.2 $\mu$ F	0603
C <sub>3</sub>	Murata	GRM188R71A225KE15D	2.2 $\mu$ F	0603
C <sub>2</sub>	Murata	GRM188R71A225KE15D	2.2 $\mu$ F	0603
C <sub>4</sub>	Murata	GRM188R61A475KE15D	4.7 $\mu$ F	0603
R <sub>2</sub>	Any	Resistor	1 K $\Omega$ - 13 K $\Omega$	0603
R <sub>1</sub>	Any	Resistor	600 $\Omega$	0603
R <sub>5</sub>	Any	Resistor	0 $\Omega$	0603
R <sub>NTC1</sub>	Any	Resistor	10 k $\Omega$	0603
R <sub>3</sub> , R <sub>4</sub>	Any	Depending on the BATMS status		0603
D1	Any	Diode Led		0603

### 3 Input/output connections

**Table 2. Input and output connections**

Reference Designator	Name	Description
JP1	VIN	<ul style="list-style-type: none"> <li>– JP1_1: GND power</li> <li>– JP1_2: VIN power</li> </ul>
JP2	LDO	<ul style="list-style-type: none"> <li>– JP2_1: LDO pin</li> <li>– JP2_2: GND</li> </ul>
JP3	SYS	<ul style="list-style-type: none"> <li>– JP3_1: GND</li> <li>– JP3_2: SYS pin</li> </ul>
JP4	CHG	<ul style="list-style-type: none"> <li>– JP4_1: CHG pin</li> <li>– JP4_2: GND</li> </ul>
JP5	CEN	<ul style="list-style-type: none"> <li>– JP5_1: LDO</li> <li>– JP5_2: CEN pin</li> <li>– JP5_3: GND</li> </ul>
JP6	SD	<ul style="list-style-type: none"> <li>– JP6_1: LDO</li> <li>– JP6_2: SD pin</li> <li>– JP6_3: GND</li> </ul>
JP7	BATMS	<ul style="list-style-type: none"> <li>– JP7_1: ADC_IN</li> <li>– JP7_2: ADC_EN</li> <li>– JP7_3: GND</li> </ul>
JP8	BATTERY	<ul style="list-style-type: none"> <li>– JP8_1: BATSNS pin</li> <li>– JP8_2: BAT pin</li> <li>– JP8_3: NTC pin</li> <li>– JP8_4: GND</li> </ul>
CN1	USB Micro	<ul style="list-style-type: none"> <li>– CN1_1: GND</li> <li>– CN1_2: NC</li> <li>– CN1_3: NC</li> <li>– CN1_4: NC</li> <li>– CN1_5: VIN</li> </ul>

Figure 3. In/out connectors



1. Connect a power supply source between VIN power (JP1\_2) and GND power (JP1\_1) and battery between BAT (JP8\_2) and GND (JP8\_4). The EWM charging the battery at the current value set by R2.
2. Connect a battery between BAT (JP8\_2) and GND (JP8\_4).
3. Connect a multimeter between BATSNS (JP8\_1) and GND (JP8\_4) for a precise battery output voltage sensing.
4. Connect a multimeter between SYS (JP3\_2) and GND (JP3\_1) for a precise SYS voltage sensing. This pin outputs a 3.1 V regulated voltage and can supply up to 100mA
5. Connect a multimeter between LDO (JP2\_2) and GND (JP2\_1) for a precise LDO voltage sensing. This pin can be used to supply up to 100 mA to external devices
6. JP5 - Charger enable: A logic low level on this pin disables the battery charger. A transition from high to low and then back to high restarts the charger when the charge cycle has been stopped for one of the following reasons:
  - Charging timeout (precharge, fast-charge)
  - Battery voltage below VPRE after the fast charge has already started
  - End of charge
  - The CEN pin has no effect if the charge cycle has been stopped for a battery overcharge condition.
7. The CEN pin has no effect if the charge cycle has been stopped for a battery overcharge condition.
8. JP6 - Shutdown input: A logic high level on this pin when the input voltage ( $V_{IN}$ ) is not valid makes the device enter shutdown mode. In this mode the battery drain is reduced to less than 500 nA and the SYS and LDO voltages are not present. Connecting a valid input voltage ( $V_{UVLO} < V_{IN} < V_{INOV}$ ) restores normal operating conditions if the battery voltage is higher than 3 V ( $V_{ODCR}$ , battery voltage overdischarge).
9. JP7 - Battery voltage measurement: This pin is internally shorted to the BATSNS pin during normal operating conditions to monitor the battery voltage. The BATMS pin is disconnected from the battery if the LDO output voltage drops to zero (battery discharge overcurrent, battery overdischarge, shutdown mode, short-circuit on SYS or LDO). By calculating appropriate values of R3 and R4 is possible to obtain a voltage divider of battery voltage to be read with an ADC converter.

## 4 Application information

### Operation description

The STNS01 is a power management IC integrating a battery charger with power path function, battery protection circuitry, battery temperature monitoring and a 3.1 V 100 mA LDO.

When a valid input voltage ( $V_{IN}$ ) is present on the IN pin, after security checks are performed, the battery charger starts charging the battery using a constant current /constant voltage charging algorithm.

The input voltage ( $V_{IN}$ ) is considered to be valid if it is higher than  $V_{UVLO}$  and lower than  $V_{INOV}$ .

The power path architecture allows charging the battery and supplying the system at the same time. When the input voltage is not valid, the LDO (and every external IC connected to SYS) is supplied by the battery through a low resistance path.

The device also provides protection to the battery against the following fault conditions:

- overcharge
- overdischarge
- charge overcurrent
- discharge overcurrent

If a fault condition is detected while the input voltage is valid ( $V_{UVLO} < V_{IN} < V_{INOV}$ ), the CHG pin starts toggling to inform the control logic that an error occurred.

The device can also be put in reduced battery drain mode (shutdown,  $I_{BAT} < 500$  nA) to maximize battery life during end-product shipping and shelf time.

### Programming the output current

Connect a resistor ( $R_{ISET}$ ) to ground to set the fastcharge current ( $I_{FAST}$ ) according to the following equation:

$$I_{FAST} = V_{ISET} / R_{ISET} * K$$

Where  $V_{ISET} = 1$  V and  $K = 200$ . Fast charge currents ranging from 15 mA to 200 mA can be programmed. Precharge current and end of charge current are scaled accordingly.

Charging currents higher than 200 mA can be programmed but the increased voltage drop over internal MOSFETs can limit the minimum input voltage ( $V_{IN}$ ) needed to obtain full charge.

### Battery charge

The charging process starts if the battery voltage is higher than  $V_{BATMIN}$ . If the battery is deeply discharged (the battery voltage is lower than  $V_{PRE}$  and higher than  $V_{BATMIN}$ ) the charger enters the pre-charge phase and starts charging in constant-current mode using a low current ( $I_{PRE} = 20\% I_{FAST}$ ). If the battery voltage does not reach the  $V_{PRE}$  threshold within  $t_{PRE}$ , the charging process is stopped and a fault is signaled. When the battery voltage reaches the  $V_{PRE}$  threshold, the constant-current fast-charge phase is entered and the charging current is increased to  $I_{FAST}$ . The value of  $I_{FAST}$  can be programmed from 15 mA to 200 mA.

Once the fast charge phase has started, if the battery voltage decreases again below  $V_{PRE}$ , the charging process is stopped and a fault is signaled. The constant current fast charge phase lasts as long as the battery voltage is lower than  $V_{FLOAT}$ . When  $V_{BAT}$  reaches  $V_{FLOAT}$ , the charging algorithm switches to constant-voltage (CV) mode. During the CV mode the battery voltage is regulated to  $V_{FLOAT}$  and the charging current starts decreasing. When the charging current reaches the  $I_{END}$  threshold ( $I_{END} = 10\%I_{FAST}$ ), the charging process is stopped and the CHG pin is put in high impedance. If the fast charge phase is not terminated within  $t_{FAST}$ , the charging process is stopped and a fault is signaled.

Figure 4. CC-CV Charging profile (not to scale)

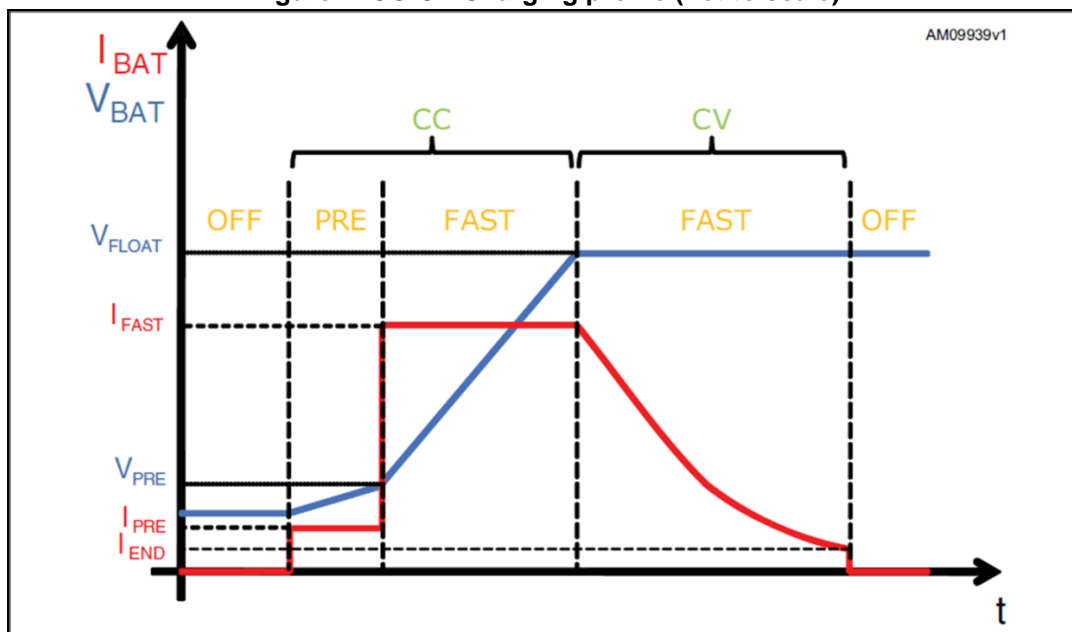
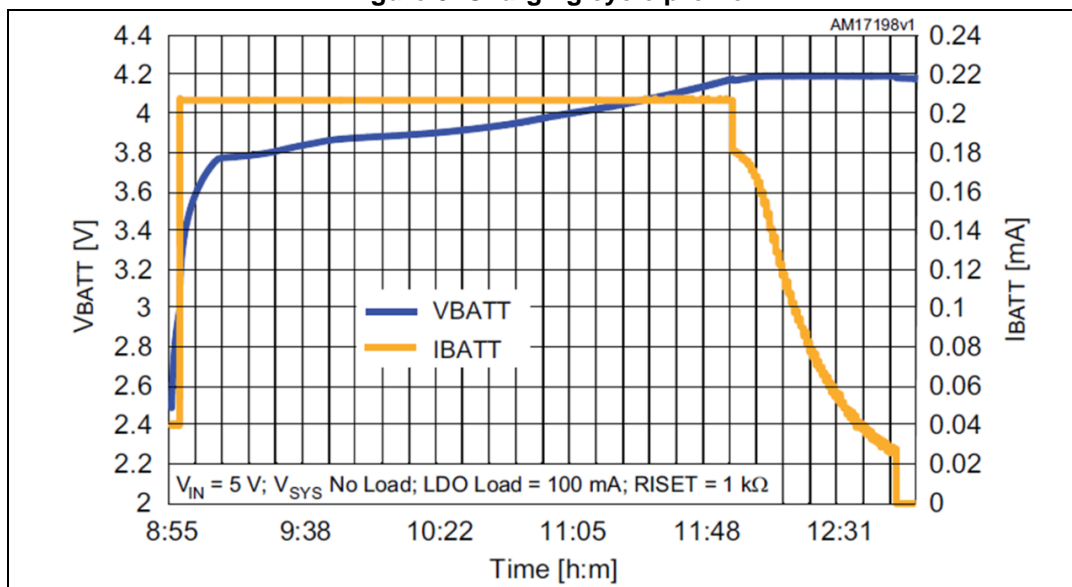


Figure 5. Charging cycle profile





**SYS pin**

LDO input voltage. This pin can be used to supply up to 100 mA to external devices. The voltage source of this pin can be either IN or BAT depending on the operating conditions.

**LDO pin**

LDO output voltage. This pin outputs a 3.1 V regulated voltage and can supply up to 100 mA.

**Table 3. SYS/LDO pin voltage**

$V_{IN}$	$V_{BAT}$	$V_{SYS}$	LDO
$> V_{UVLO} \ \& \ < V_{INOVP}$	x (don't care)	$V_{IN}^{(1)}$	ON
$< V_{UVLO}$	$< V_{ODC}^{(2)}$	Not powered	OFF
$< V_{UVLO}$	$> V_{ODC}^{(2)}$	$V_{BAT}^{(1)}$	ON
$> V_{INOVP}$	$< V_{ODC}^{(2)}$	Not powered	OFF
$> V_{INOVP}$	$> V_{ODC}^{(2)}$	$V_{BAT}^{(1)}$	ON

1. Voltage drop over internal MOSFETs not included.

2.  $V_{ODCR}$  if shutdown mode or overdischarge protection have been previously activated.

## 5 Board layout

Figure 6. Assembly layer

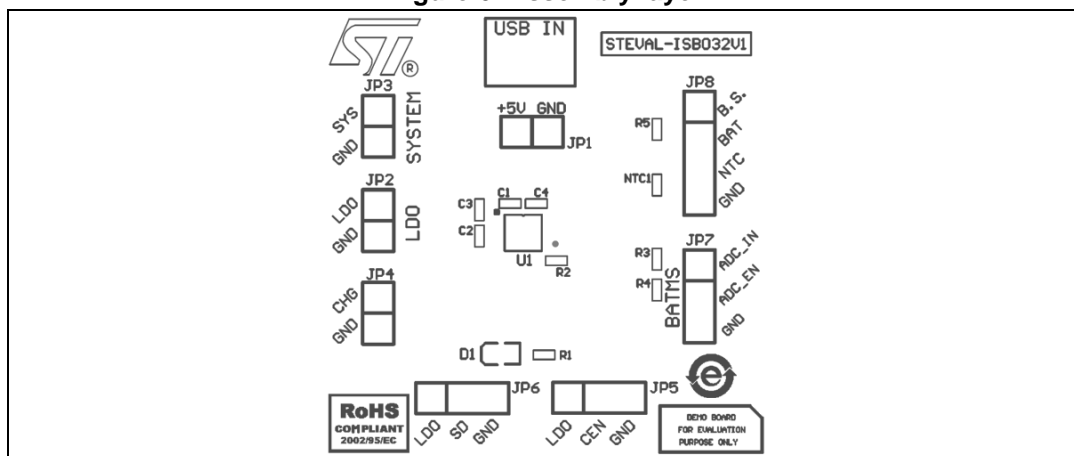


Figure 7. Top layer

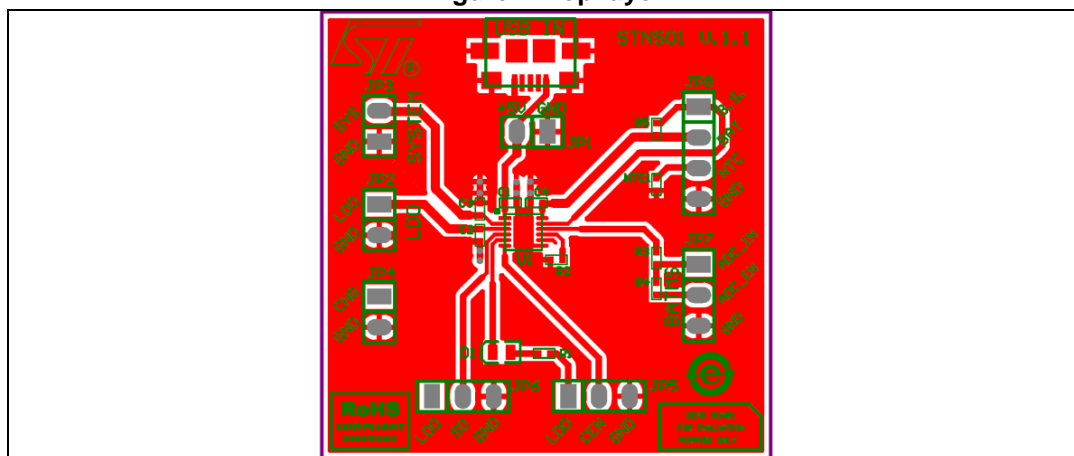
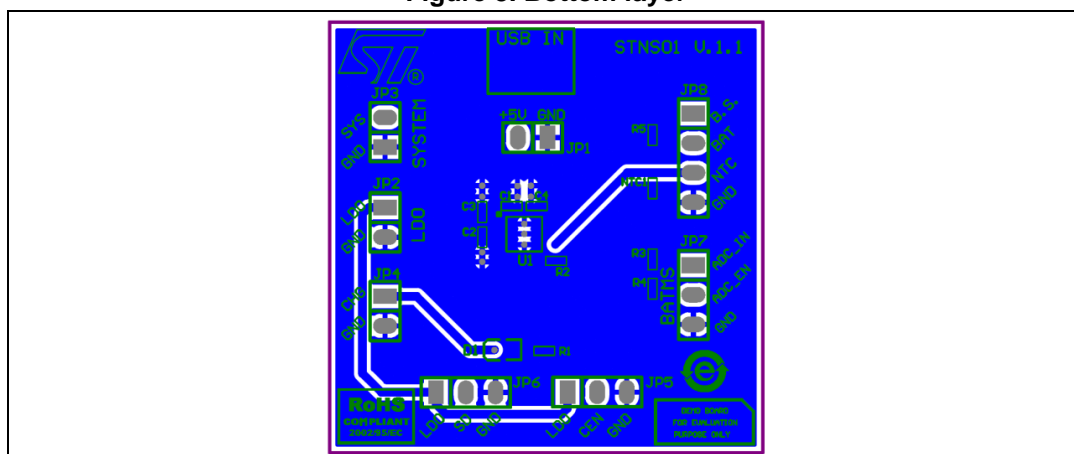


Figure 8. Bottom layer



## 6 Revision history

**Table 4. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
11-Nov-2014	1	Initial release.

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