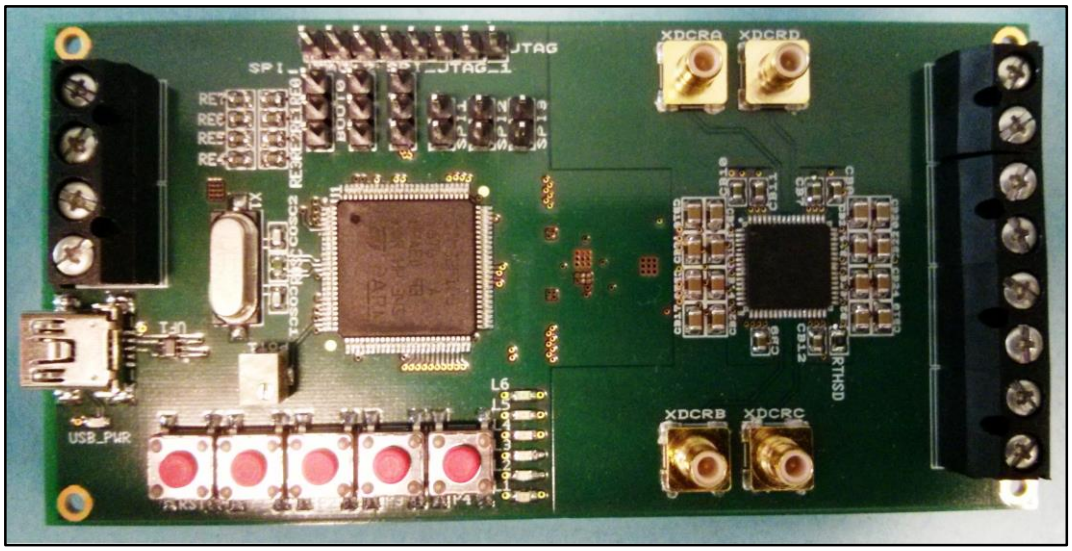
UM1957
User manual

STEVAL-IME011V1 evaluation board based on the STHV748 ultrasound pulser

Introduction

The STEVAL-IME011V1 is an evaluation board designed around the STHV748 ultrasound pulser IC, a state of the art product in ultrasound imaging applications. The system drives four transducers as 4-channel transmitters, and can output waveforms directly to an oscilloscope by connecting the scope probe on the relative BNCs. Four preset waveforms are available to test the HV pulser under different conditions.

Figure 1: STEVAL-IME011V1 evaluation board



Contents

1 Board features

- Suitable for ultrasound imaging applications
- 4 monolithic channels, 5 level high voltage pulser
- Integrated T/R switch
- On-board equivalent piezoelectric load implemented through an R/C equivalent network
- USB interface available for uploading customized output waveforms
- Embedded Microcontroller Flash memory available for storing customized waveforms
- High voltage screw connectors to power the STHV748
- Automatic lockout overvoltage protection
- 7 LEDs to signal EVAL BOARD status and proper operation
- Human Machine Interface to select, start and stop the stored output waveforms

2 Getting starting

The STEVAL-IME011V1 is shipped by STMicroelectronics ready to use. The user only needs to:

1. Plug the right power supply to the board (see *Section 1: "Board features"* for further details)
2. Connect the BNC to the oscilloscope
3. Check that LED PROGRAM 1 (LD1) turns on
4. Select the waveform with the PROGRAM button. The corresponding PROGRAM LED (LD1-LD4) turns on
5. Press the START button to run the selected program; the START LED L5 turns on. When the program ends, the microcontroller returns to the IDLE state (LED L5 off)
6. If a continuous wave program is selected, the STOP button must be pressed to stop program execution. The microcontroller returns to the IDLE state and the STOP led (L5) turns off
7. To run the same program again, restart from step 5. To run another program, restart from step 4
8. An overvoltage protection mechanism suspends pattern generation if the HV supply exceeds 90 V and the red L6 LED switches on. Pattern generation will restart once the HV supply voltage falls back into the allowed range.

3 Hardware layout and configuration

The STEVAL-IME011V1 evaluation board is designed around the STHV748. The hardware block diagram below illustrates the main connection between STHV748 and the STM32F4. *Figure 3: "STEVAL-IME003V1 board layout"* will help you to locate connectors, LEDs and features on the board.

Figure 2: Hardware block diagram

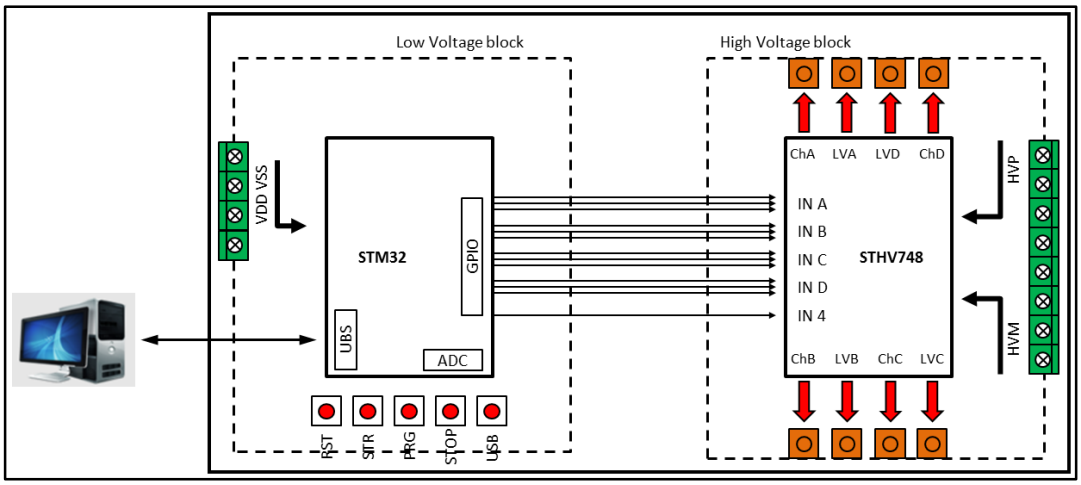
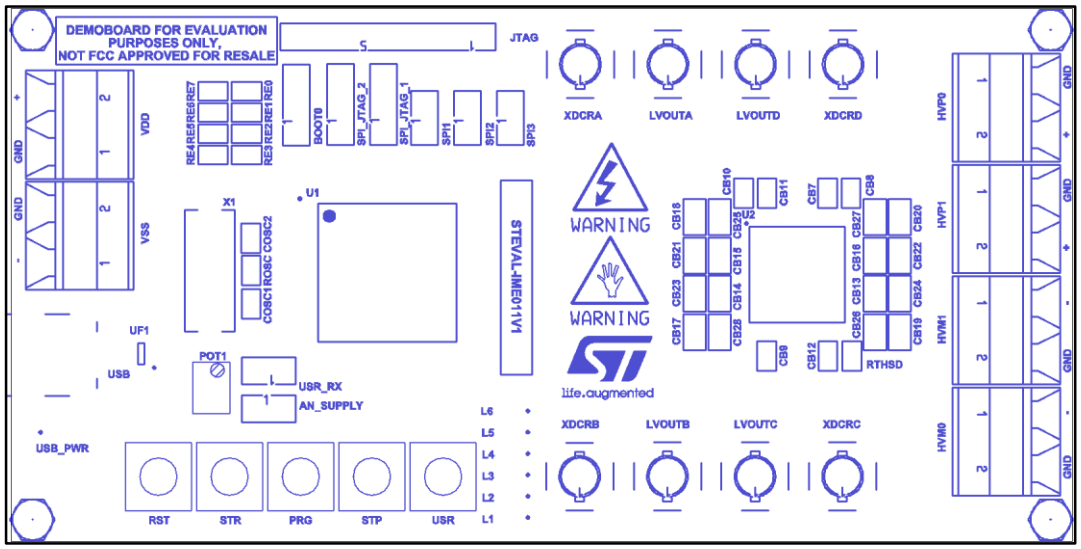


Figure 3: STEVAL-IME003V1 board layout



3.1 Power supply

The low voltage block of the STEVAL-IME011V1 board is designed to be powered:

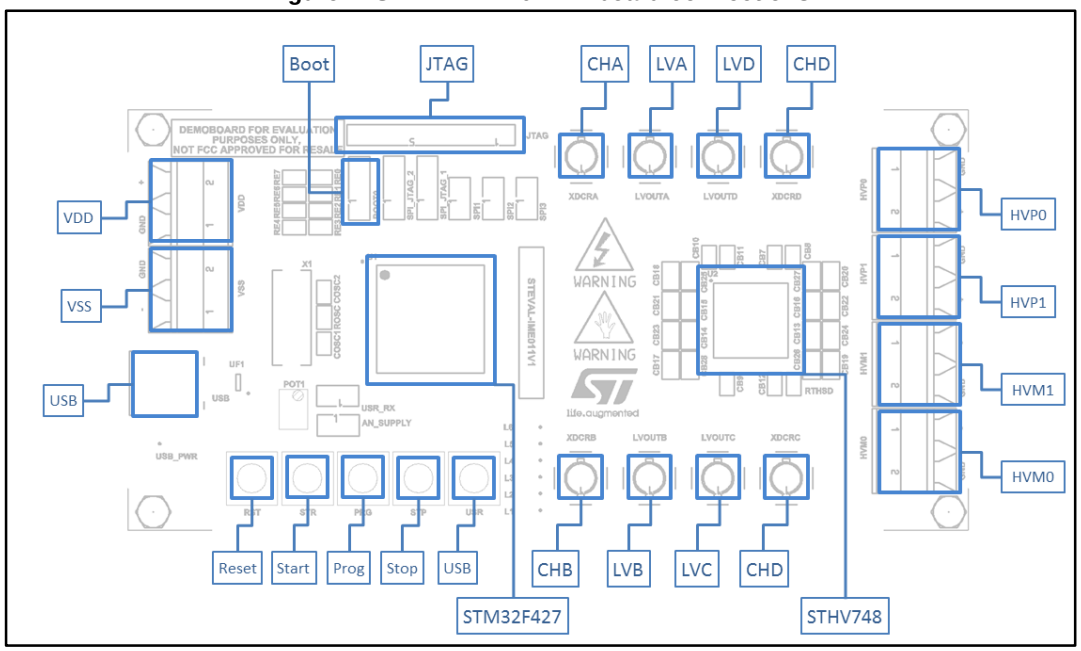
- during programming and when the board is connected to the PC:
  - 5V DC through USB Mini B connector to supply the STM32F4
- During pattern generation and when high voltage is powered on:
  - 5V DC connected to VDD to supply STM32F4 and STHV748 through an LDO
  - -5V DC connected to VSS to supply STHV748 through an LDO

the USB link must be removed when high voltage is connected to the board

The high voltage block of the STEVAL-IME011V1 is designed to be powered:

- VDD: Positive supply voltage, 5 V (2 - VDD conn.)
- GND: Ground (1 – VDD conn. And 2 – VSS conn)
- VSS: Negative supply voltage 5 V (1 - VSS conn.)
- GND: Ground (1 – HVP0 conn.)
- HVP0: TX0 High voltage positive supply (2 - HVP0 conn.)
- GND: Ground (1 – HVP1 conn.)
- HVP1: TX1 High voltage positive supply (2 - HVP1 conn.)
- HVM1: TX1 high voltage negative supply (1 - HVM1 conn.)
- GND: Ground (2 - HVM1 conn.)
- HVM0: TX0 high voltage negative supply (1 - HVM0 conn.)
- GND: Ground (2 – HVM0 conn.)

Figure 4: STEVAL-IME011V1 board connections



3.2 MCU

The STM32F427 is fully dedicated to generating the bitstream on its GPIO pins to drive the pulser's output channels. It is already pre-programmed as a DFU (device firmware upgrade) device with the ability to upgrade internal FLASH memory. The STM32F427 manages all the DFU operations, such as the authentication of product identifier, vendor identifier and Firmware version. The MCU drives the pulser channels through the use of different General Purpose IO (GPIO) pins. You can simulataneously drive from 1 to 16 different pins by simply writing a 16-bit word into the GPIO Output Data Register (ODR). The board can be connected to a PC via USB. The required pattern is sent as a sequence of states for each pulser channel and of durations for each state. Here, all durations are expressed in units of MCU system clock cycles. Once the information is received, the channel states are converted into 16-bit words for the GPIO peripheral and they are stored in the embedded Flash, together with the timing information. After programming, the PC is

no longer required, so the board can act as a stand-alone device. Different patterns can be stored and the user can select which one to use at run-time. The same MCU can implement two different solutions for real-time execution.

The first solution involves the use of the STM32 Direct Memory Access (DMA) peripheral. The DMA is able to transfer data from memory to any peripheral register, GPIO included, without the intervention of the MCU core.

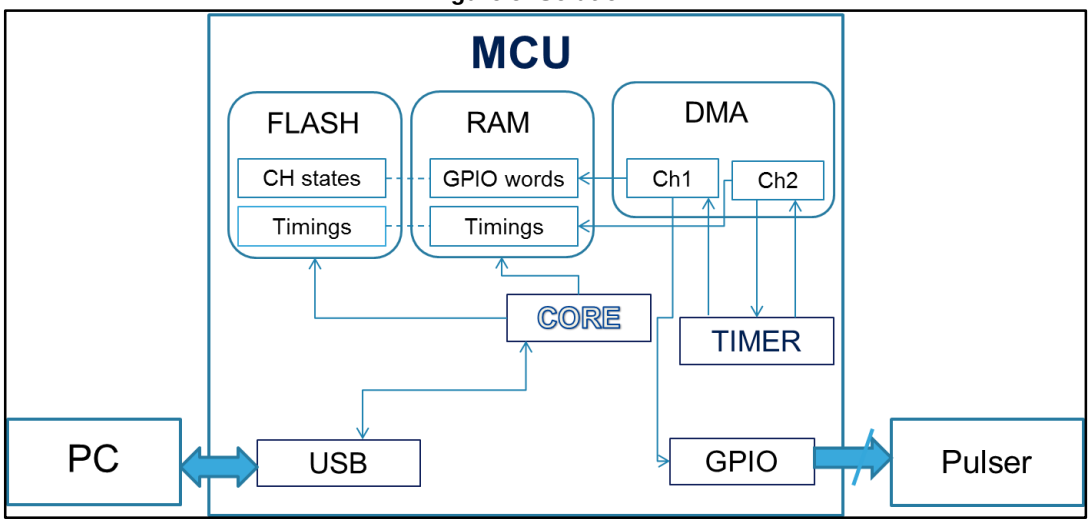
To trigger DMA transfer, a general purpose TIMER is used. The timer works at the system clock frequency and basically acts as a counter and the reload value (the value at which the counter returns to zero) is stored in the Auto Reload Register (ARR). The timer triggers two different DMA channels in two different moments:

- the first channel is triggered at each reload event and transfers the new GPIO word into the ODR;
- the second is triggered at a constant time after reload and transfers the new duration information into the ARR

The timer preload feature is enabled, so that the new ARR value is effective only at the next reload. Since the time needed by the first DMA channel to update the ODR is a constant, considering the reload trigger as the starting point, the time between two different GPIO updates is simply given by the ARR value. The Circular buffer feature of the DMA can be enabled to allow the automatic regeneration of the same pattern at each end. This solution has the advantage of being fully managed by hardware. The MCU core is completely free for any user requirement.

The main drawback is that each timing value between two subsequent states cannot be lower than a minimum value in order to guarantee enough time for both DMA channels to perform their transfers.

Figure 5: Solution 1



The second solution is designed to overcome the minimum duration requirement of the DMA solution and involves the MCU core directly.

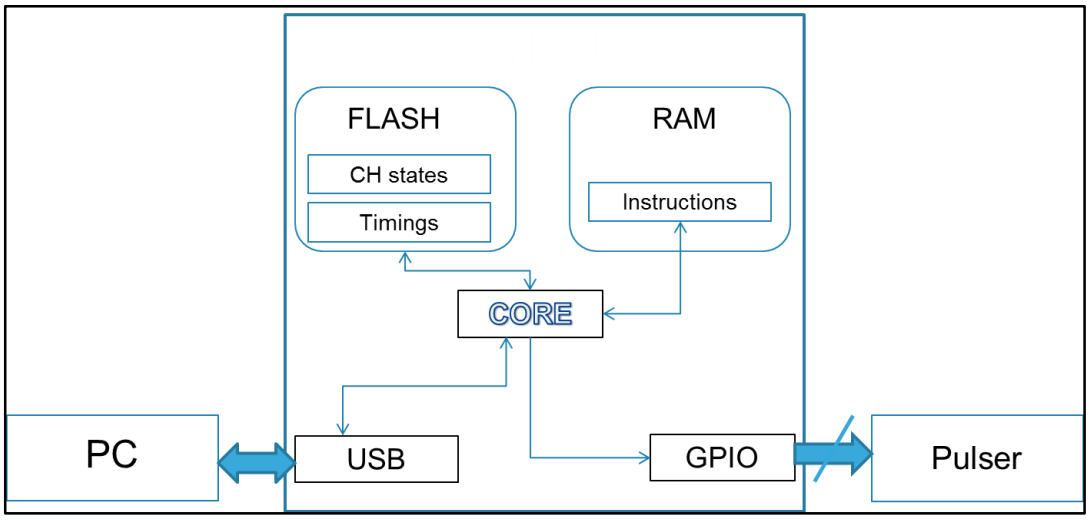
- During run-time, the core generates the binary assembly code it needs to load and store each word in the ODR. Any unnecessary instructions like control loops are avoided; the code is only a succession of simple load/store instructions.
- To adapt the timing to the pattern needs, dummy instructions are inserted in the assembly code. To avoid wasting time to load each word from memory, the word is inserted as a literal in the assembly instruction itself, which means that a 32-bit instruction is needed instead of a 16-bit equivalent.

- In order to avoid any latency due to the instruction fetch from Flash, the code is executed from the embedded RAM. Moreover, the RAM is configured to be accessed by the core through a different bus to the one used to access the ODR.

Thanks to all these solutions, it is possible to achieve a minimum time of two system clock cycles before two updates and maintain a one system clock cycle resolution. For instance, if you consider a STM32F4 clocked at 168 MHz, the minimum timing you can achieve is 12 ns and you can set the duration of each state with a resolution of 6 ns. For a repetitive pattern, a branch instruction is added at the end of the routine to restart the pattern generation. In this case, the clock cycles needed for the branch instruction has to be considered for the last state.

The main drawback of this solution is that the MCU core is 100% involved in the pattern generation even though it can still be called by peripheral interrupts and stop pattern generation to perform other tasks.

Figure 6: Solution 2



3.3 Stored patterns

The STEVAL-IME011V1 can memorize four patterns in the MCU FLASH memory in order to demonstrate the achievable performance at the pulser outputs. Four selectable patterns already stored into STM32 flash memory form the default set which is available and ready to use. A detailed description of the programs is listed below.

Programmed waveform description, flagged by LED L1 to L4.

Program “1” (see *Figure 7: "Scheme of program “1”"*)

- XDCR_A: Pulse Wave mode, TX0 switching, 5 pulses, time-period TP=400ns and PRF=150µs
- XDCR_B: Pulse Wave mode, TX0 switching, 5 pulses in counter phase respect to XDCR_A, time-period TP=400ns and PRF=150µs
- XDCR_C: Pulse Wave mode, TX1 switching, 5 pulses, time-period TP=200ns and PRF=150µs
- XDCR_D: Pulse Wave mode, TX1 switching, 5 pulses in counter phase respect to XDCR_C, time-period TP=200ns and PRF=150µs

TX0 means H-Bridge supplied by HVP/M0, while TX1 means H-Bridge supplied by HVP/M1.

Figure 7: Scheme of program "1"

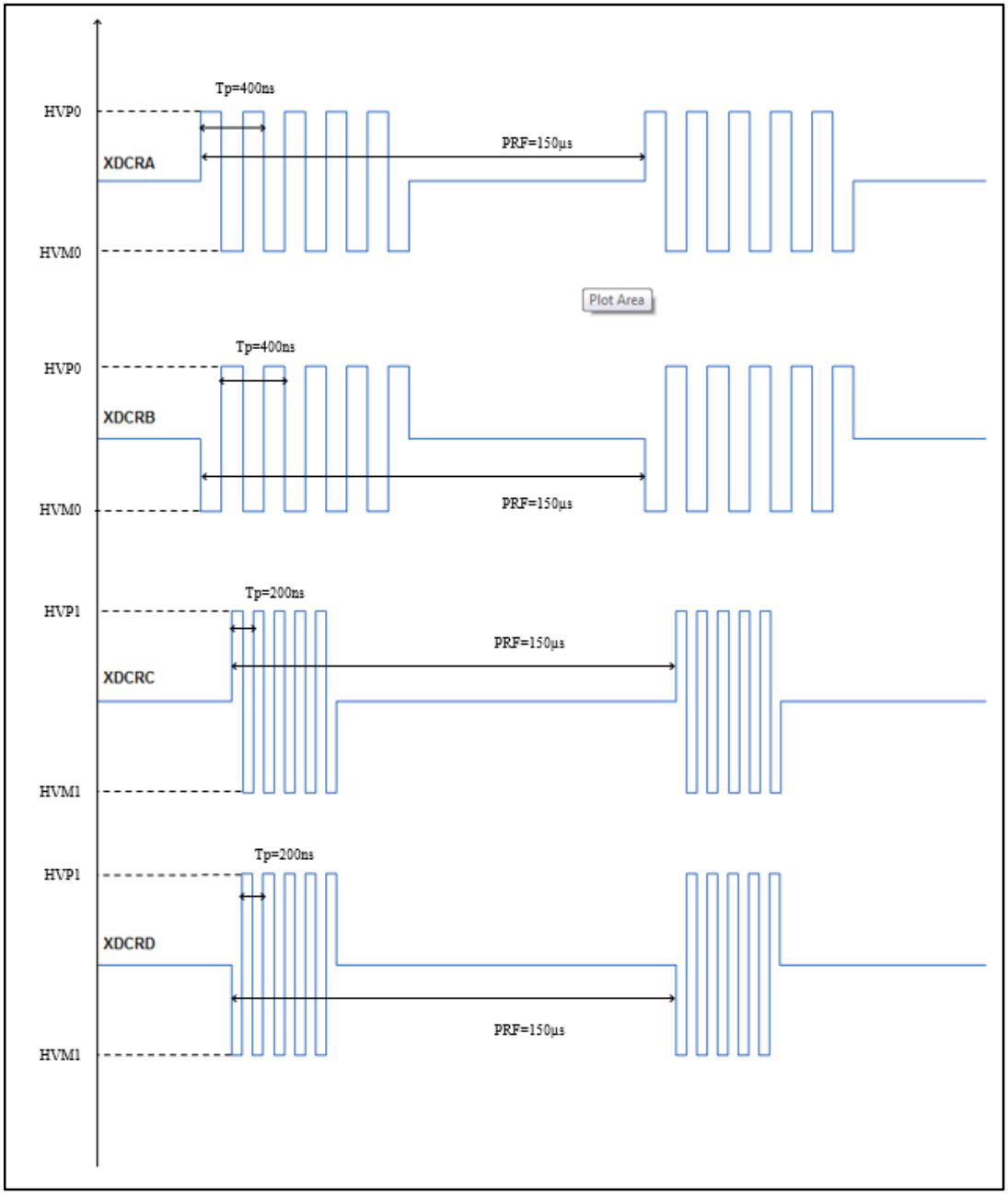
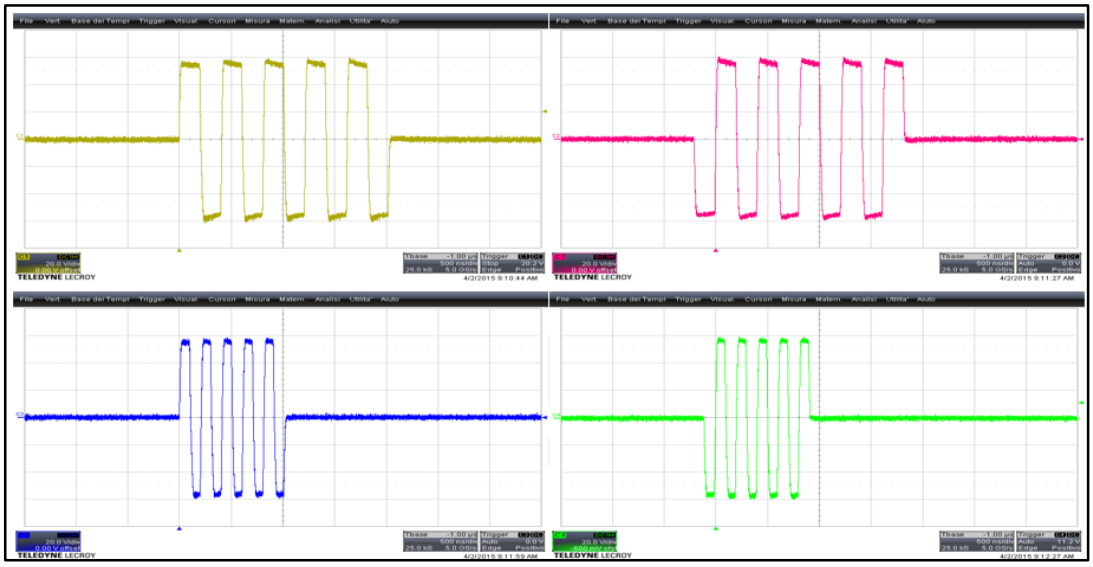


Table 1: Program "1"

PW 5pulses - HV0/1=±60 V; LOAD: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	2.5	5	positive	TX0	150 µs
Ch B	PW	2.5	5	negative	TX0	150 µs
Ch C	PW	5	5	positive	TX1	150 µs
Ch D	PW	5	5	negative	TX1	150 µs

Figure 8: Acquisition by Program “1”



Program "2" (see *Figure 9: "Scheme of program “2”"*)

- XDCR_A: Pulse Wave mode, TX0 switching, 5 pulses, time-period TP=200ns and PRF=150 µs
- XDCR_B: Pulse Wave mode, TX0 switching, 5 pulses in counter phase respect to XDCR_A, time-period TP=200ns and PRF=150 µs
- XDCR_C: Pulse Wave mode, TX1 switching, 5 pulses, time-period TP=100ns and PRF=150 µs
- XDCR_D: Pulse Wave mode, TX1 switching, 5 pulses in counter phase respect to XDCR_C, time-period TP=100ns and PRF=150 µs

Figure 9: Scheme of program "2"

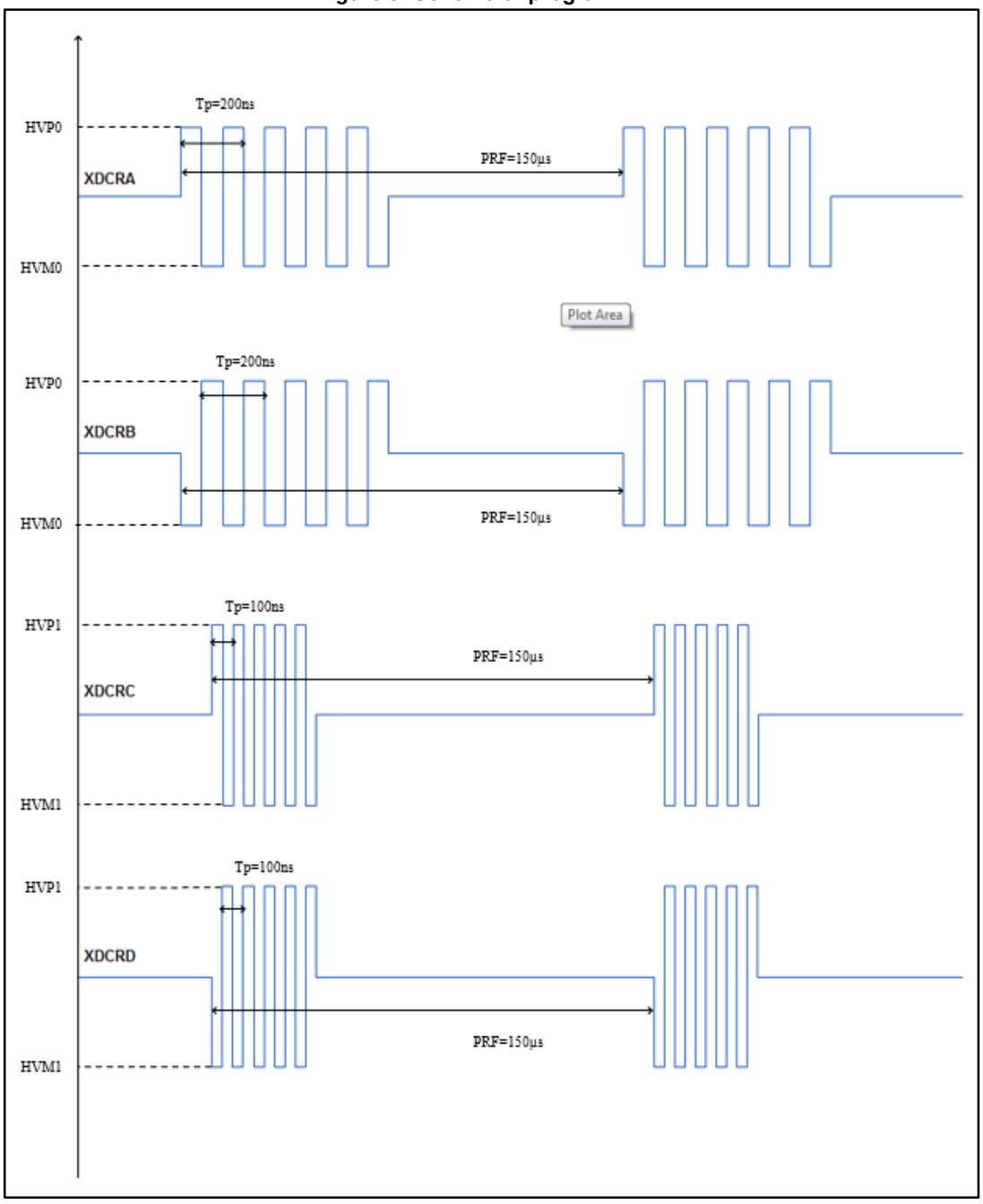
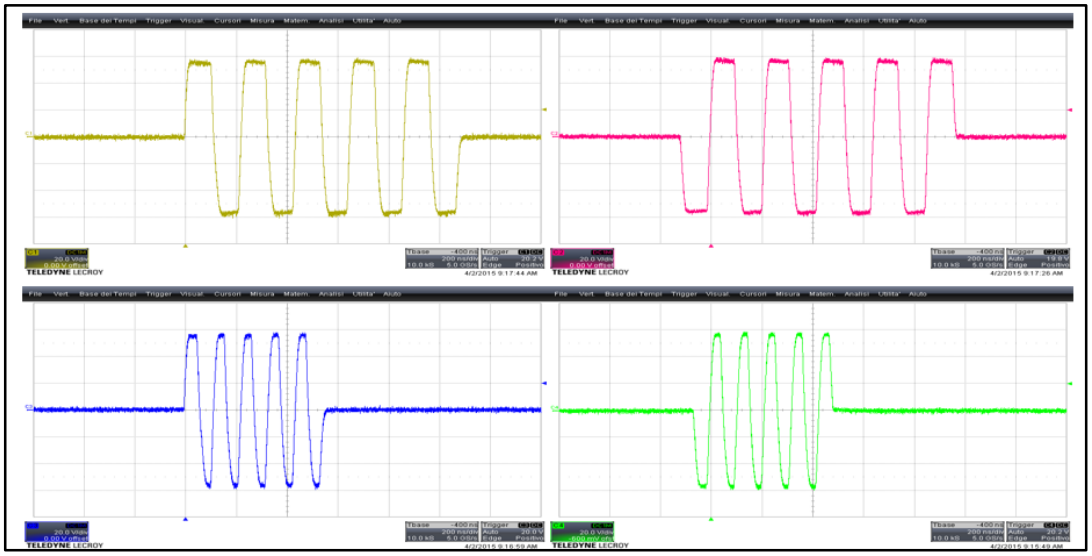


Table 2: Program "2"

PW TX0&TX1 5pulses - HV0/1=±60 V; LOAD: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	5	5	positive	TX0 & TX1	150 µs
Ch B	PW	5	5	negative	TX0 & TX1	150 µs
Ch C	PW	10	5	positive	TX0 & TX1	150 µs
Ch D	PW	10	5	negative	TX0 & TX1	150 µs

Figure 10: Acquisition by Program "2"



Program "3" (see *Figure 11: "Scheme of program "3""* **)**

- XDCR_A: Continuous Wave mode, TX-CW switching, time-period TP=400 ns
- XDCR_B: Continuous Wave mode, TX-CW switching in counter-phase respect to XDCR_A, time-period TP=400 ns
- XDCR_C: Continuous Wave mode, TX-CW switching, time-period TP=200 ns
- XDCR_D: Continuous Wave mode, TX-CW switching in counter-phase respect to XDCR_C, time-period TP=200 ns

Figure 11: Scheme of program "3"

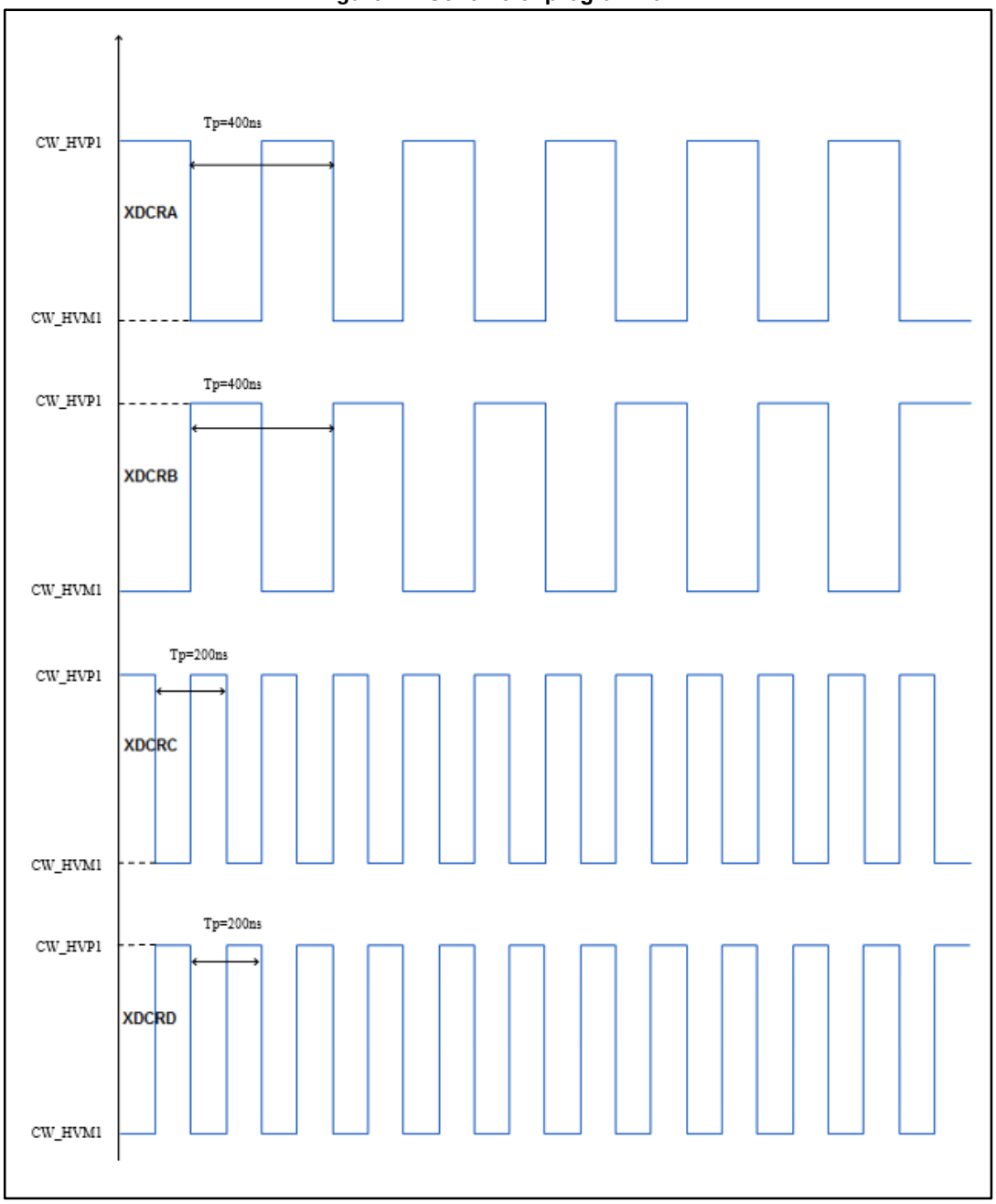
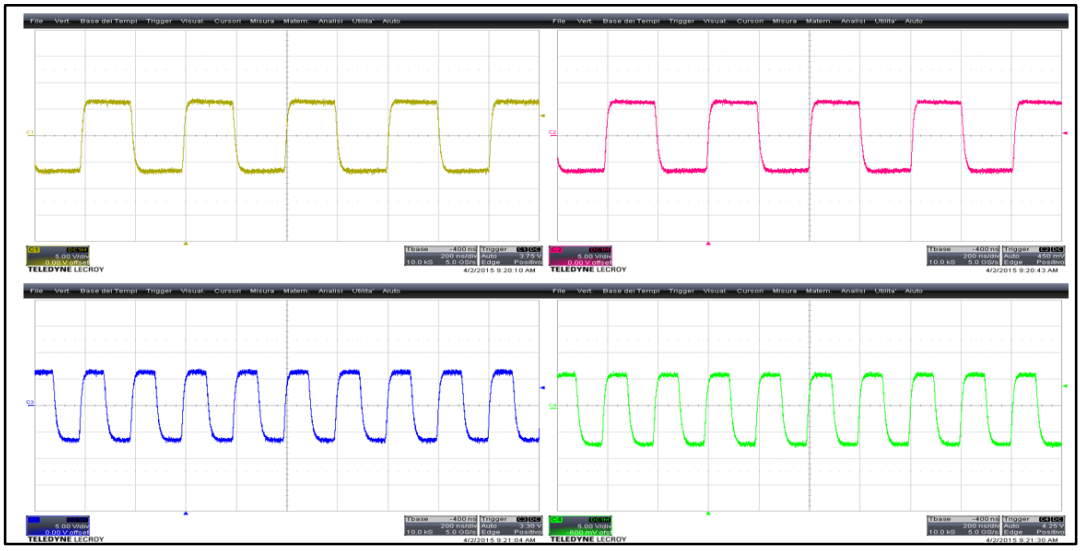


Table 3: Program "3"

Continuous Wave - HV1=±10V; LOAD: 270 pF//100 Ω					
	mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-Bridge**
Ch A	CW	2.5	continuous wave	positive	TX-CW
Ch B	CW	2.5	continuous wave	negative	TX-CW
Ch C	CW	5	continuous wave	positive	TX-CW
Ch D	CW	5	continuous wave	negative	TX-CW

Figure 12: Acquisition by Program "3"



Program "4" (see *Figure 13: "Scheme of program "4""*)

- XDCR_A: Pulse Wave mode, TX0 switching, 1.5 pulses, time-period TP=400 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs
- XDCR_B: Pulse Wave mode, TX0 switching, 1.5 pulses, time-period TP=400 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs
- XDCR_C: Pulse Wave mode, TX0 switching, 1.5 pulses, time-period TP=200 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs
- XDCR_D: Pulse Wave mode, TX0 switching, 1.5 pulses, time-period TP=200 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs

Figure 13: Scheme of program "4"

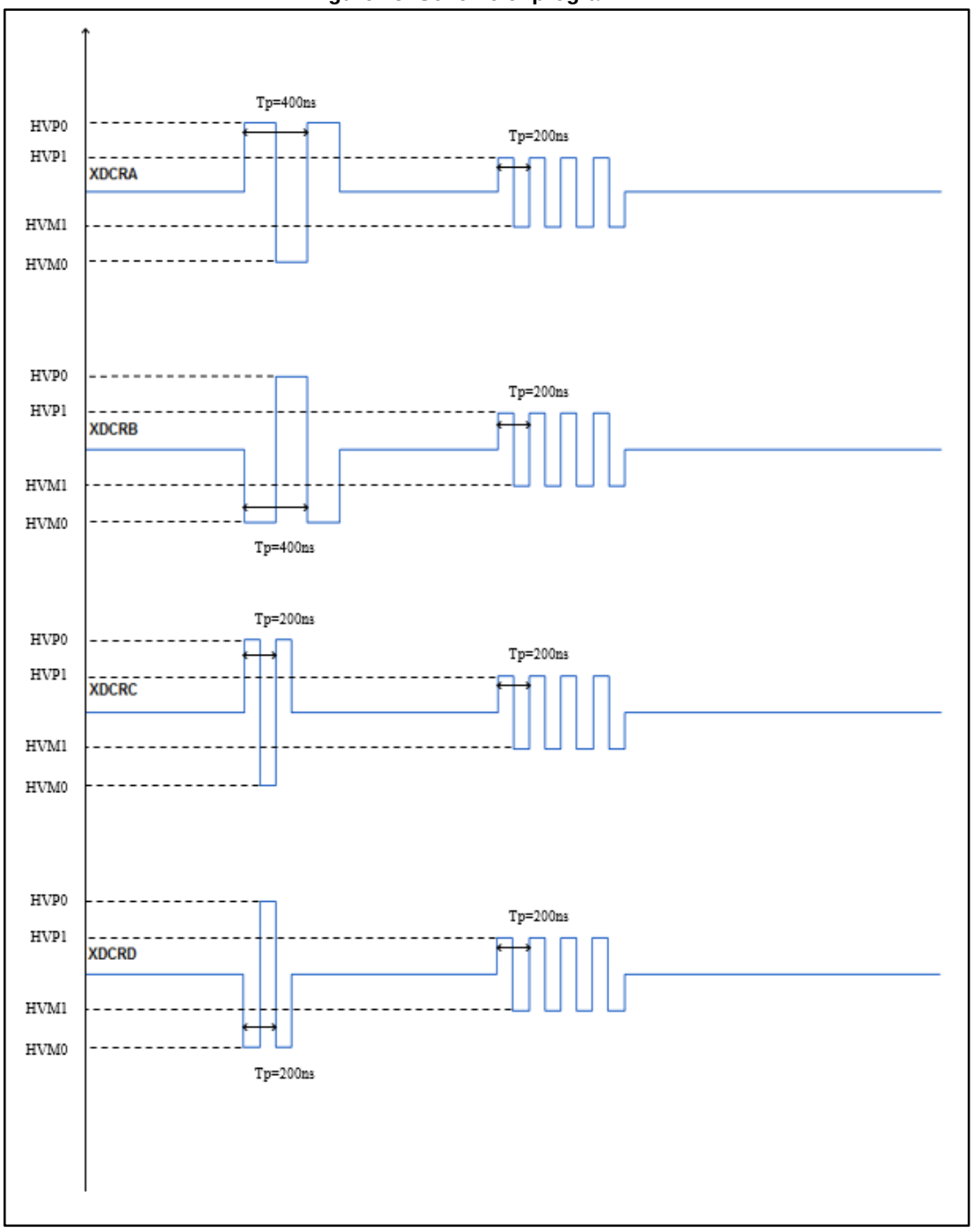
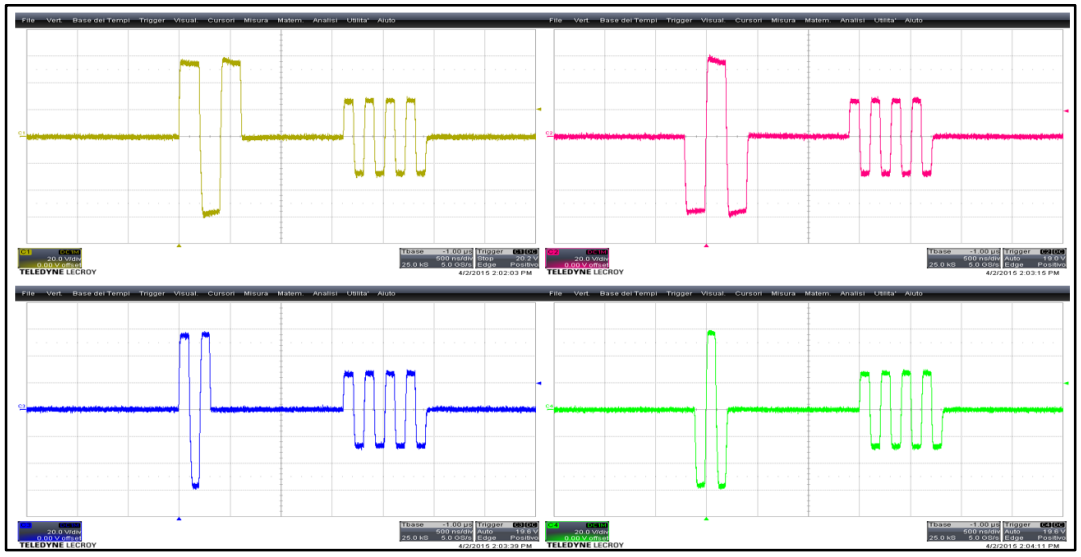


Table 4: Program "4"

Pulse Cancellation - HV0/1=±60 V; LOAD: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-bridge**	**PRF**
Ch A	PW	2.5 - 5	3 half pulse then 4 pulse	positive	TX0 then TX1	150 µs
Ch B	PW	2.5 - 5	3 half pulse then 4 pulse	negative	TX0 then TX1	150 µs
Ch C	PW	5	3 half pulse then 4 pulse	positive	TX0 then TX1	150 µs
Ch D	PW	5	3 half pulse then 4 pulse	negative	TX0 then TX1	150 µs

Figure 14: Acquisition by Program "4"



The board can be connected to a PC via USB cable and patterns can be edited by means of a user interface.

the USB link must be removed when a high voltage is connected to the board

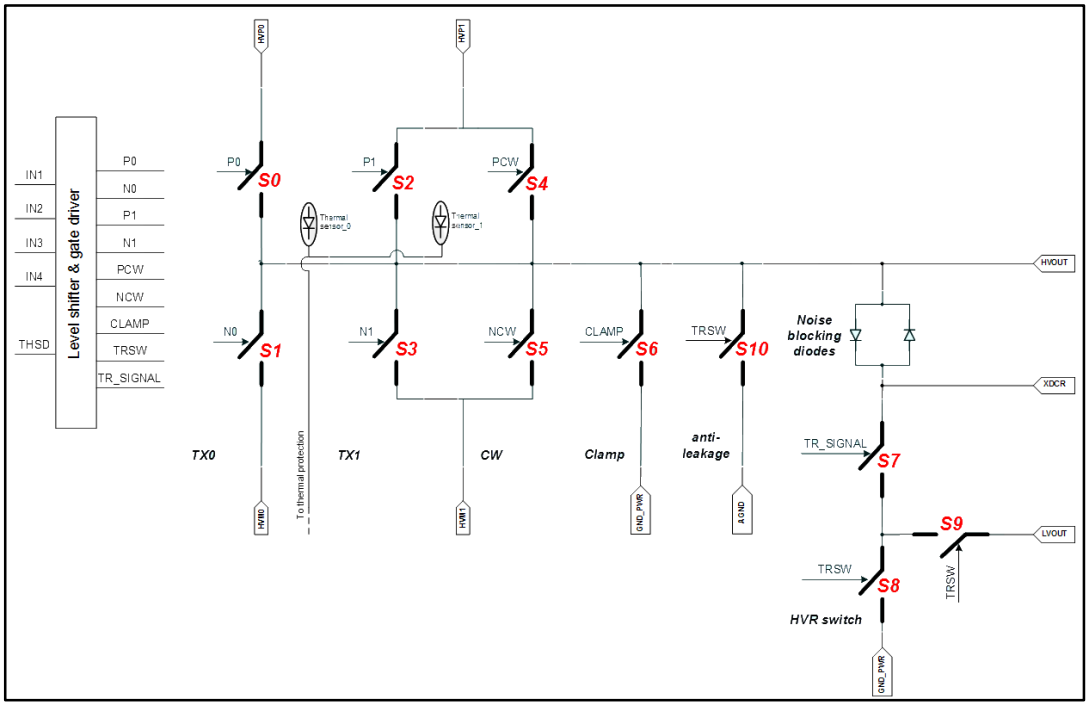
3.4 STHV748 stage

The STHV748 high-voltage, high-speed ultrasound pulser IC features four independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive, or MEMS transducers. The device contains a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes, and high-power P-channel and N-channel MOSFETs as output stages for each channel. There is also clamping-to-ground circuitry, anti-leakage, an anti-memory effect block, a thermal sensor, and a HV receiver switch (HVR_SW), which guarantees strong decoupling during the transmission phase. Moreover, the STHV748 includes self-biasing and thermal

shutdown blocks (see *Figure 15: "STHV748 single channel block diagram"*). Each channel can support up to five active output levels with two half bridges. The output stage of each channel is able to provide a ±2 A peak output current. In order to reduce power dissipation during continuous wave mode, the peak current is limited to 0.6 A (a dedicated half bridge is used).

For further information, please refer to the STHV748 datasheet.

Figure 15: STHV748 single channel block diagram



The STHV748 output waveforms can be displayed directly for each channel Ch A/B/C/D using an oscilloscope by connecting the scope probe to the XDCRA, XDCRB, XDCRC, and XDCRD SMB connectors. Moreover, the pulser outputs are connected to the onboard equivalent load, a 270 pF 200 V capacitor paralleled with a 100 Ω, 2 W resistor. A coaxial cable can also be used to easily connect the user transducer; in this case, the equivalent load should be removed from the board. Furthermore, four low voltage outputs are available to receive the echo traduced signal coming from the piezo-element through HVR_SW (LVOUTA, LVOUTB, LVOUTC, LVOUTD).

The main issues in this PCB design are the capacitance values necessary to ensure good filtering and the effective decoupling between the low voltage inputs (IN1, IN2, IN3, IN4, and EN for each channel) and the HV switching signals (XDCR, HVOUT, etc.,), which is ensured by the implemented layer separation.

3.5 Operating supply conditions

Table 5: DC working supply conditions

Operating supply voltages					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Value**
V_{DD}	Positive supply voltage	5	6	10	V
V_{SS}	Negative supply voltage	-5	6	-10	V
HVP0	TX0 high voltage positive supply			95	V
HVP1	TX1 high voltage positive supply			95	V
HVM0	TX0 high voltage negative supply	-95			V
HVM1	TX1 high voltage negative supply	-95			V

The high voltage pins must be HVP0 ≥ HVP1 and HVM1 ≥ HVM0

4 Connectors

4.1 Power supply

The STEVAL-IME011V1 board is powered through the screw connectors as shown in the following figures.

Figure 16: Power supply connector VDD (+5V - GND)

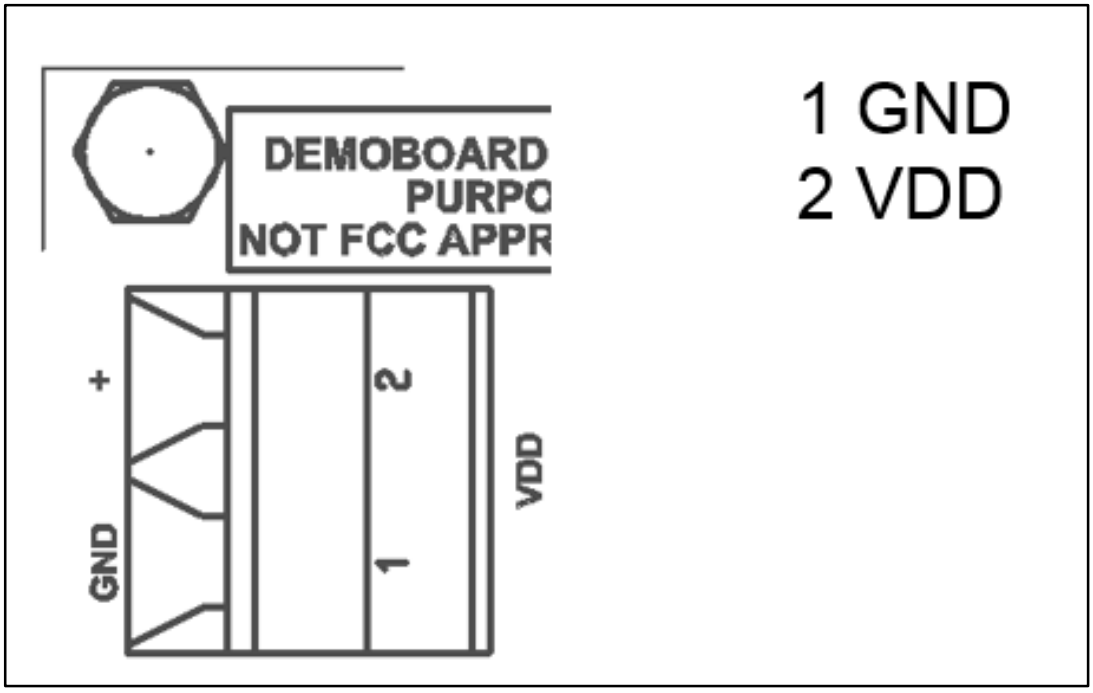


Figure 17: Power supply connector VSS (GND - -5V)

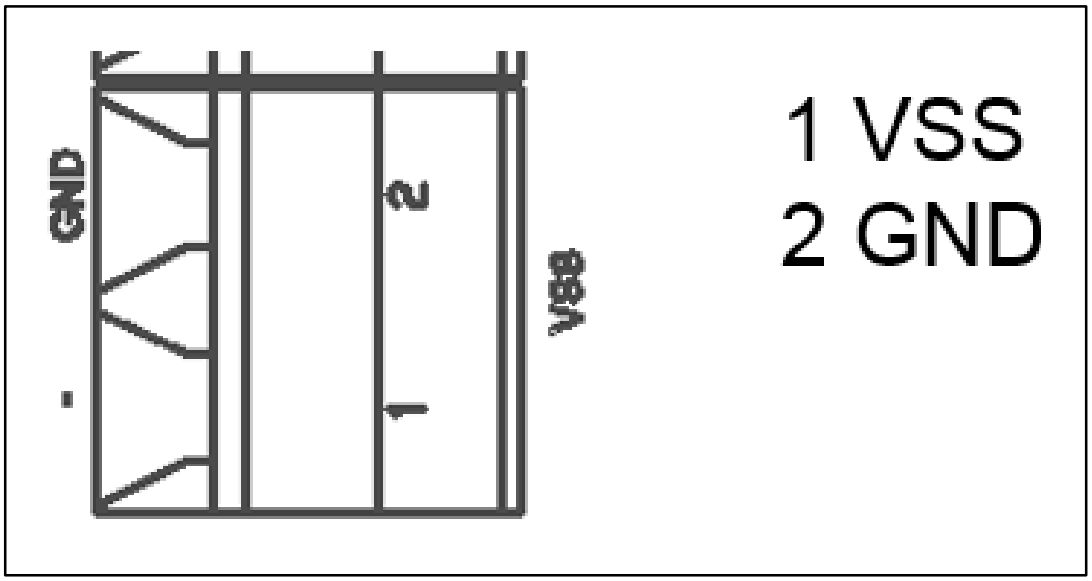
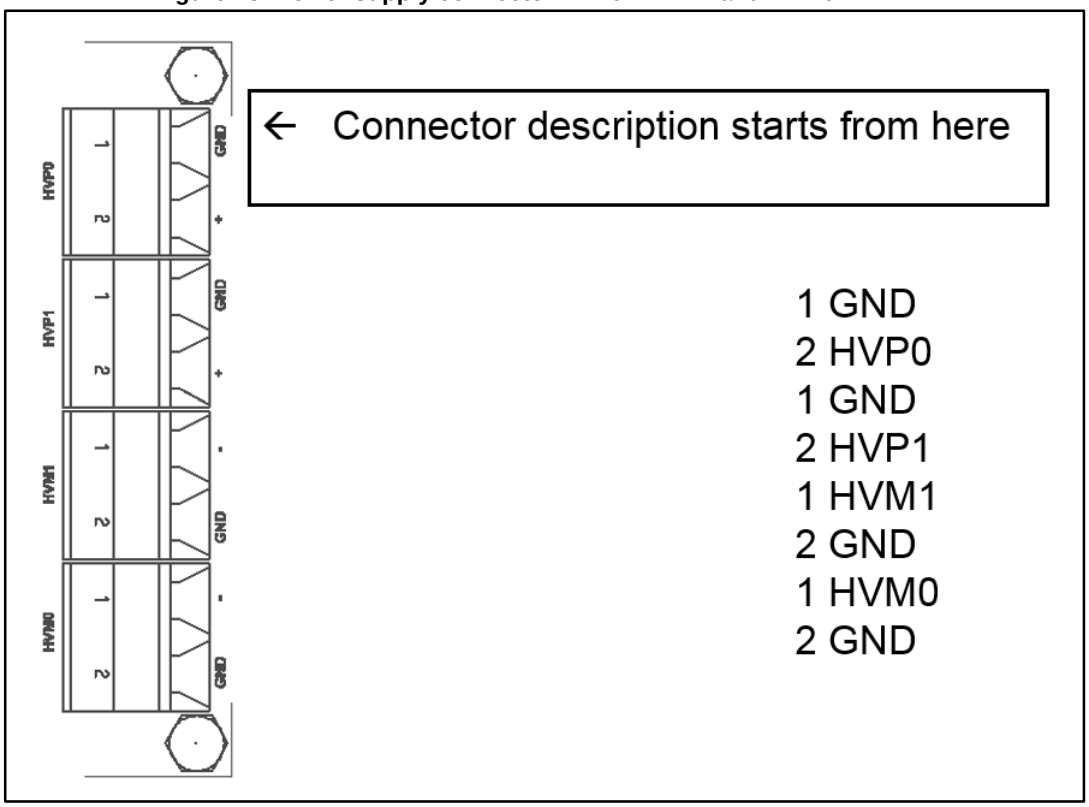


Figure 18: Power supply connector HVP0 – HVP1 and HVM0 – HVM1



4.2 MCU

Figure 19: USB mini-B connector (CN1)

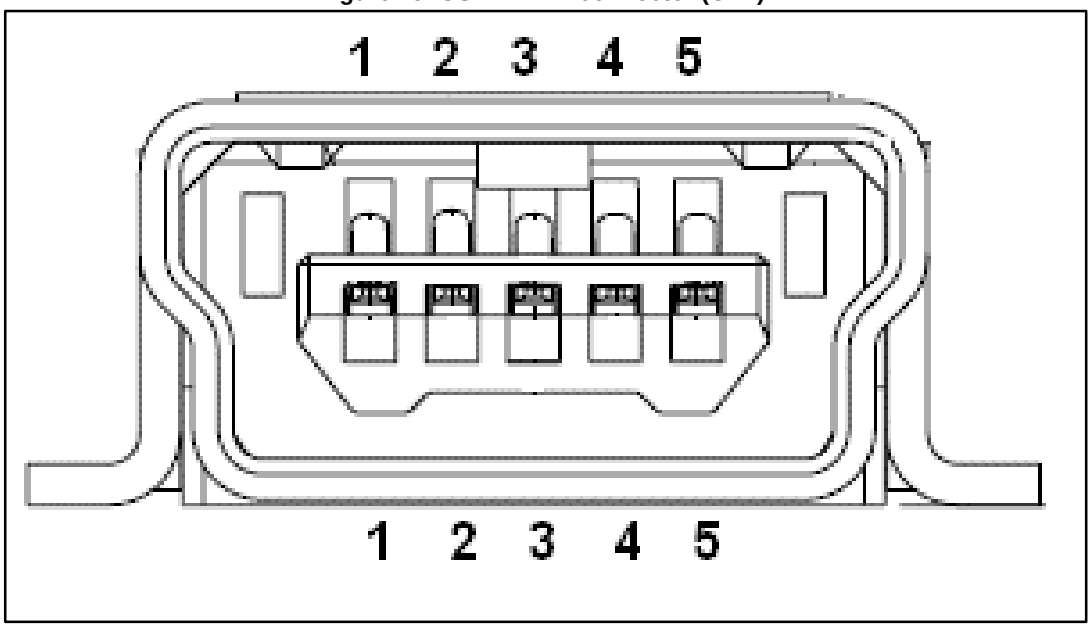


Table 6: USB mini B connector pin out

Pin number	Description
1	Vbus (power)
2	DM (STM32 PA11)
3	DP (STM32 PA12)
4	N.C.
5	Ground

Figure 20: JTAG connector

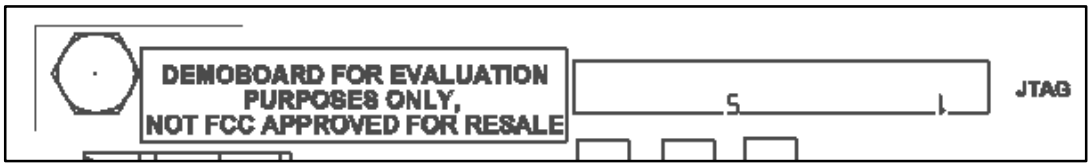


Table 7: JTAG connector

1	DVDD
2	JTDI
3	JTMS
4	JTCK
5	JTDO
6	JRST
7	GND
8	NRST

Figure 21: Boot connector

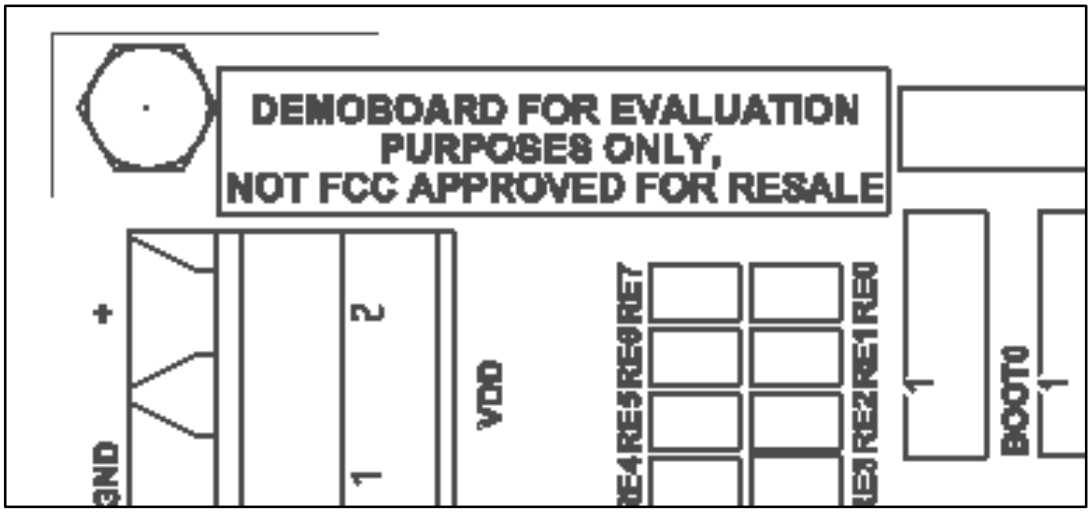
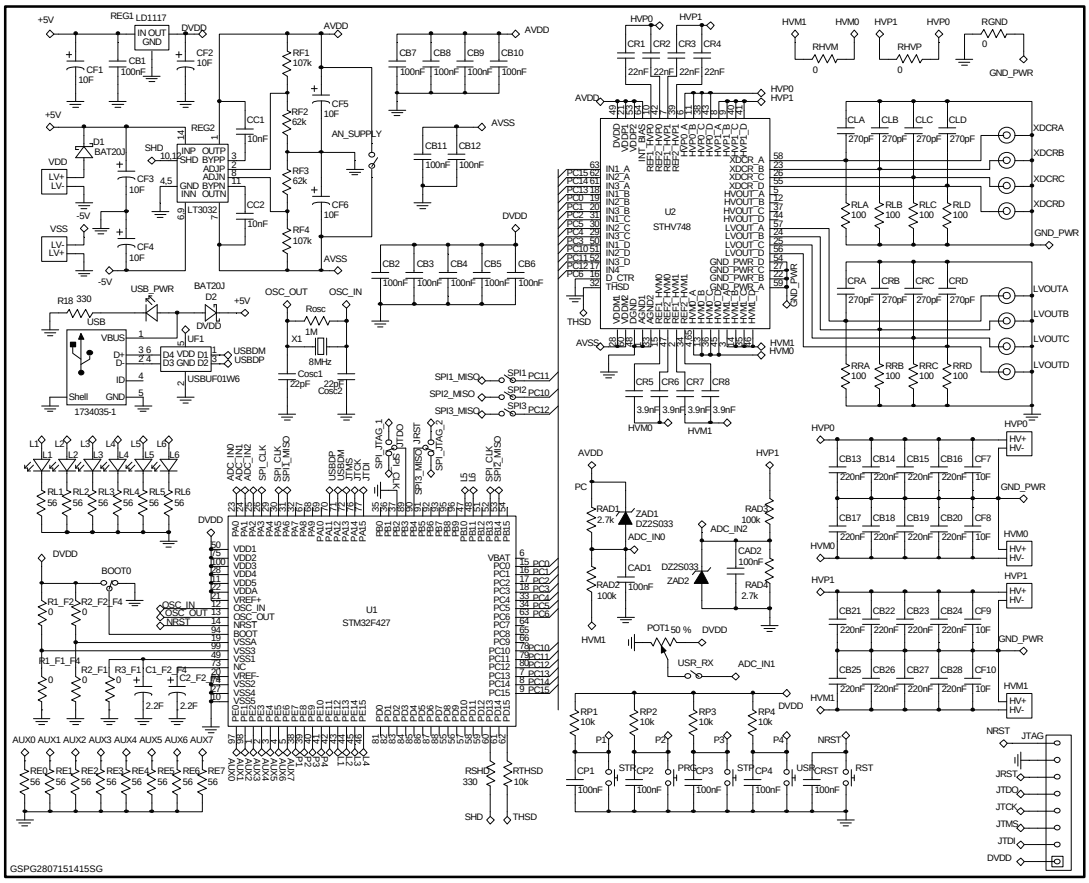


Table 8: Boot connector

1	GND
2	BOOT0 (boot from flash memory)
3	DVDD (DFU mode)

5 Schematic

Figure 22: STEVAL-IME011V1 circuit schematic



6 PCB layout

Figure 23: Top layer

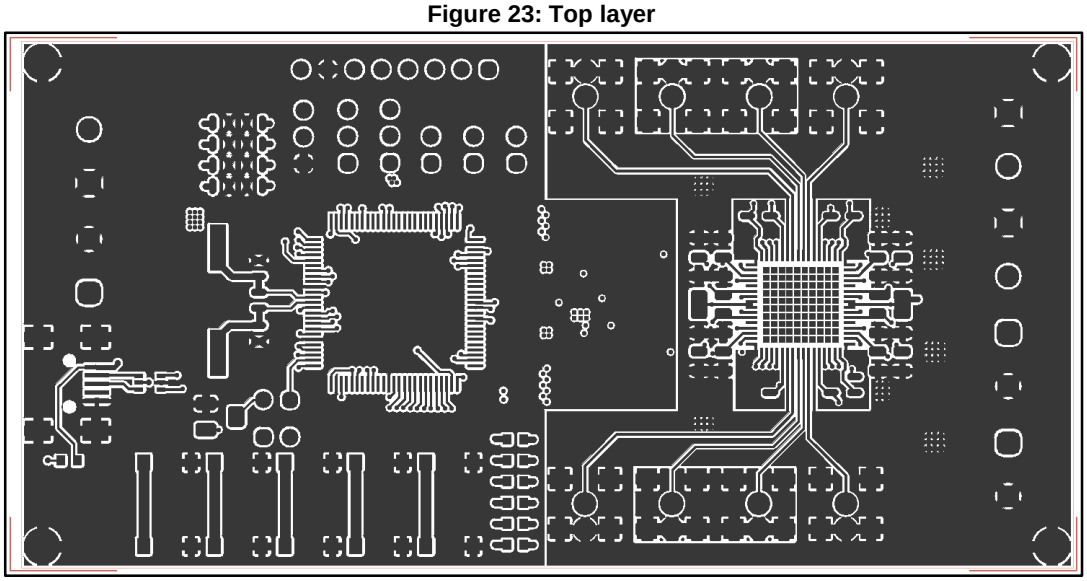


Figure 24: Inner 1

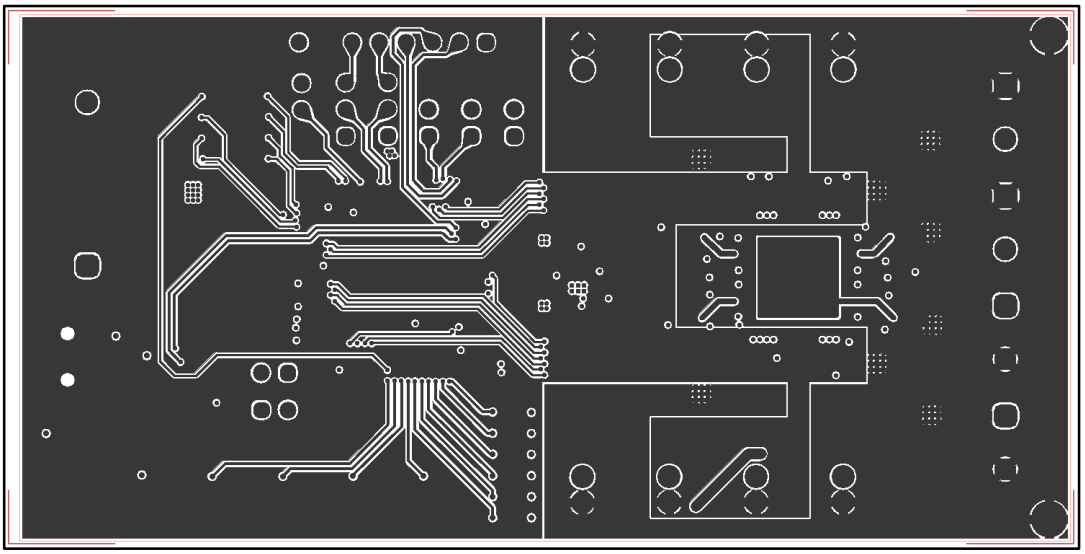


Figure 25: Inner 2

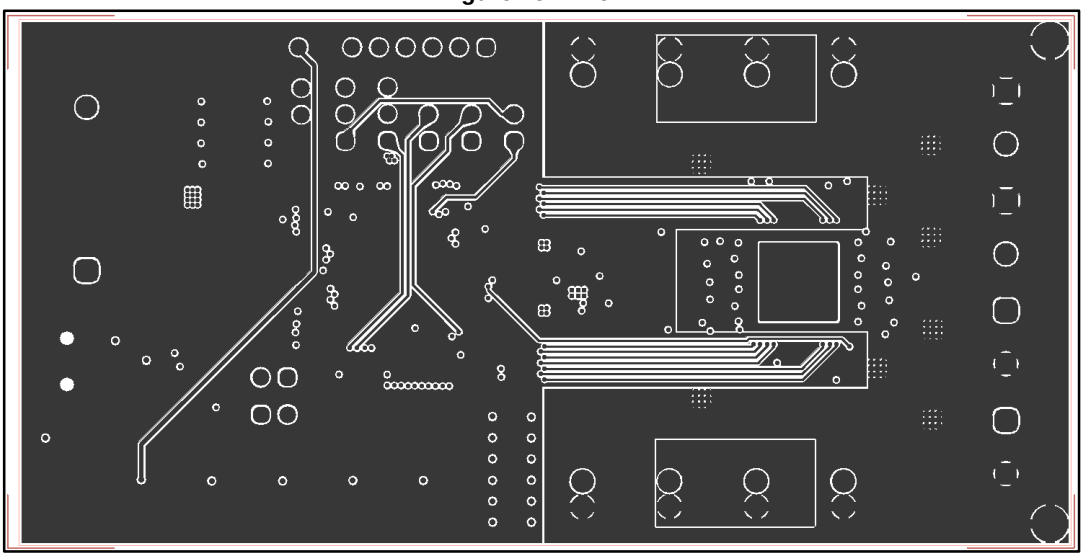


Figure 26: Inner 3

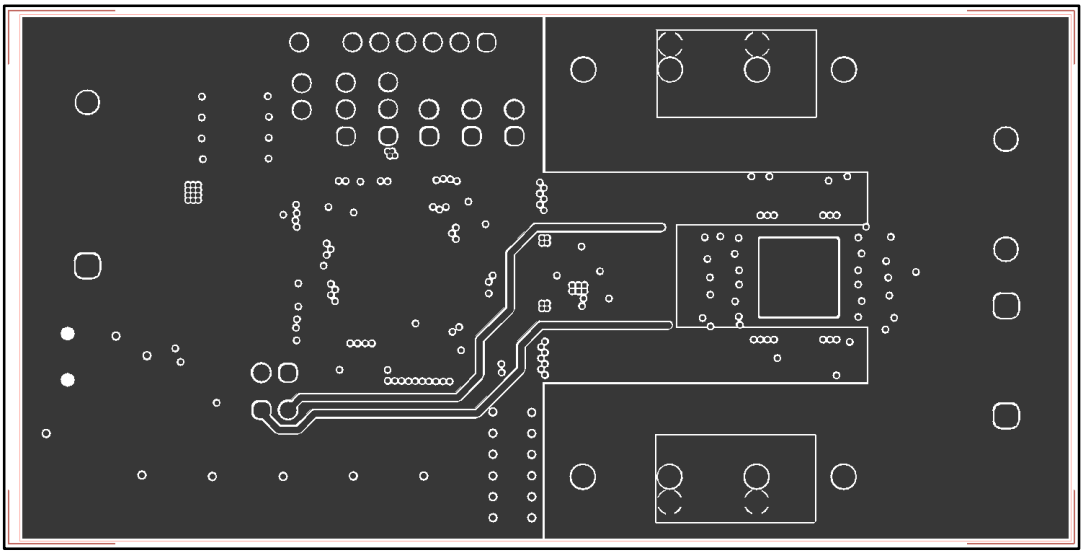


Figure 27: Inner 4

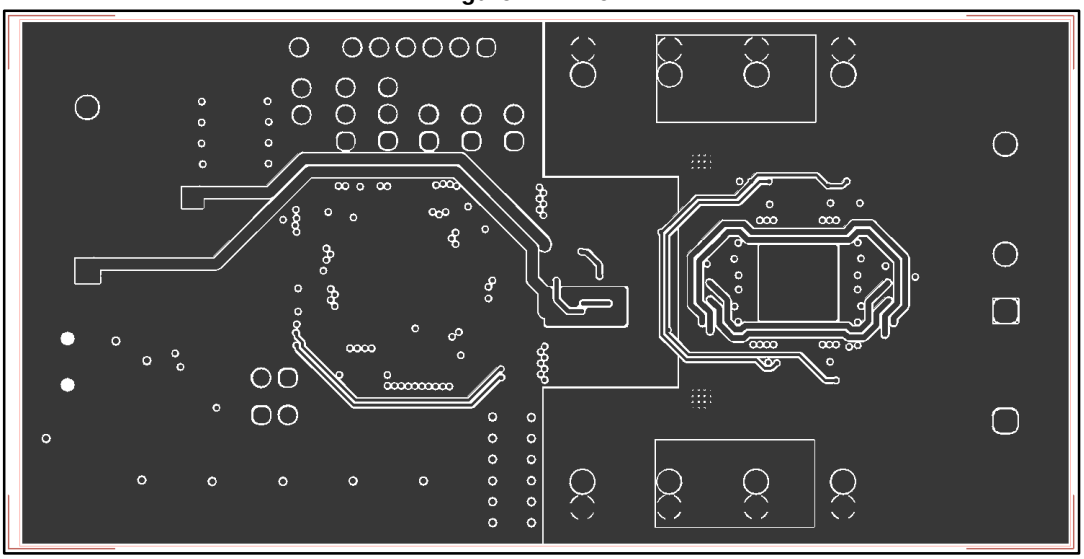
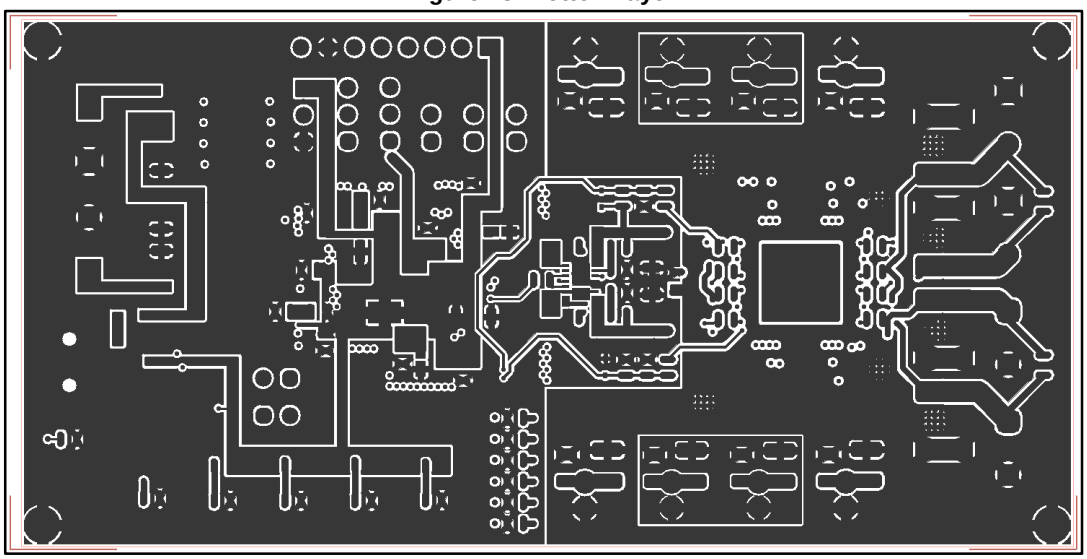


Figure 28: Bottom layer



7 Revision history

Table 9: Document revision history

Date	Version	Changes
26-Nov-2015	1	Initial release.

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