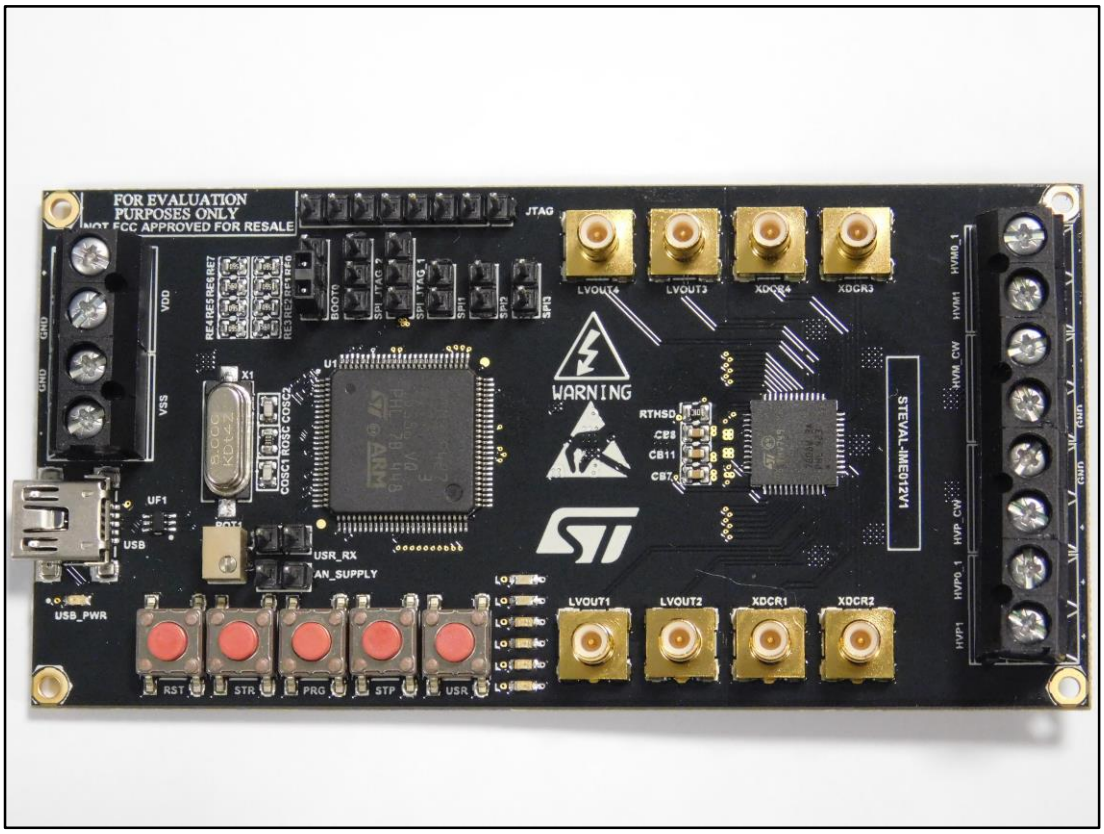
UM1961
User manual

STEVAL-IME012V1 evaluation board based on the STHV749 ultrasound pulser

Introduction

The STEVAL-IME012V1 is an evaluation board designed around the STHV749 ultrasound pulser IC, a state-of-the-art device for ultrasound imaging applications. The system can drive four transducers as 4-channel transmitters, and the output waveforms can be displayed directly on an oscilloscope by connecting the scope probe to the relative BNCs. Four preset waveforms are available to test the HV pulser under different conditions.

Figure 1: STEVAL-IME012V1 evaluation board



Contents

1 Board features

- Suitable for ultrasound imaging applications
- 4 output channels, up to 7 levels
- 8 monolithic channels, 5 level high voltage pulser
- Integrated T/R switch
- On-board equivalent piezoelectric load implemented by means of R/C equivalent network
- USB interface available to upload customized output waveforms
- Built-in microcontroller Flash memory available for storing customized waveforms
- High voltage screw connectors to power the STHV749
- Automatic lockout overvoltage protection
- 7 LEDs to check evaluation board status and proper operation
- Human machine interface to select, start and stop the stored output waveforms

2 Getting started

The STEVAL-IME012V1 is shipped by STMicroelectronics ready to use. The user only needs to:

1. Plug the right power supply to the board (see for further details)
2. Connect the BNC to the oscilloscope
3. Check that the LED PROGRAM 1 (LD1) turns on
4. Select the waveform with the Program button. The corresponding program LED (LD1-LD4) will turn on
5. Press the Start button to run the selected program; the Start LED L5 turns on. After the program ends, the microcontroller returns to the idle state (LED L5 is off)
6. If a continuous wave program has been selected, the Stop button must be pressed to halt program execution. The microcontroller returns to the idle state and the Stop LED (L5) turns off
7. To run the same program again, restart from Step 5. To run another program, restart from Step 4
8. Overvoltage protection will suspend pattern generation if the HV supply exceeds 90 V and the red LED L6 switches on. Pattern generation will restart after the HV supply voltage returns within the allowed range.

3 Hardware layout and configuration

The STEVAL-IME012V1 evaluation board is designed around the STHV749. The hardware block diagram below illustrates the main connection between the STHV749 and the STM32F4. Please see the board layout diagram to locate connectors, LEDs and features on the board.

Figure 2: Hardware block diagram

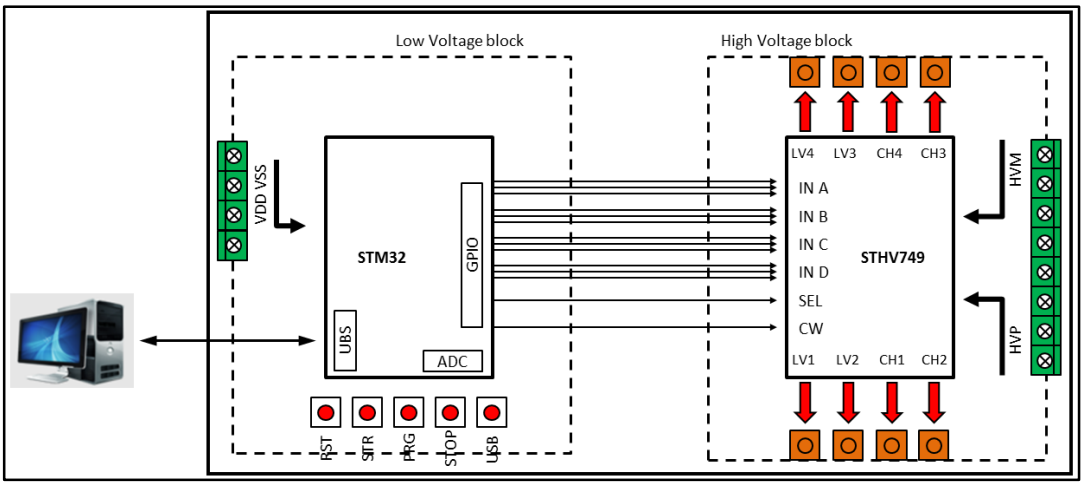
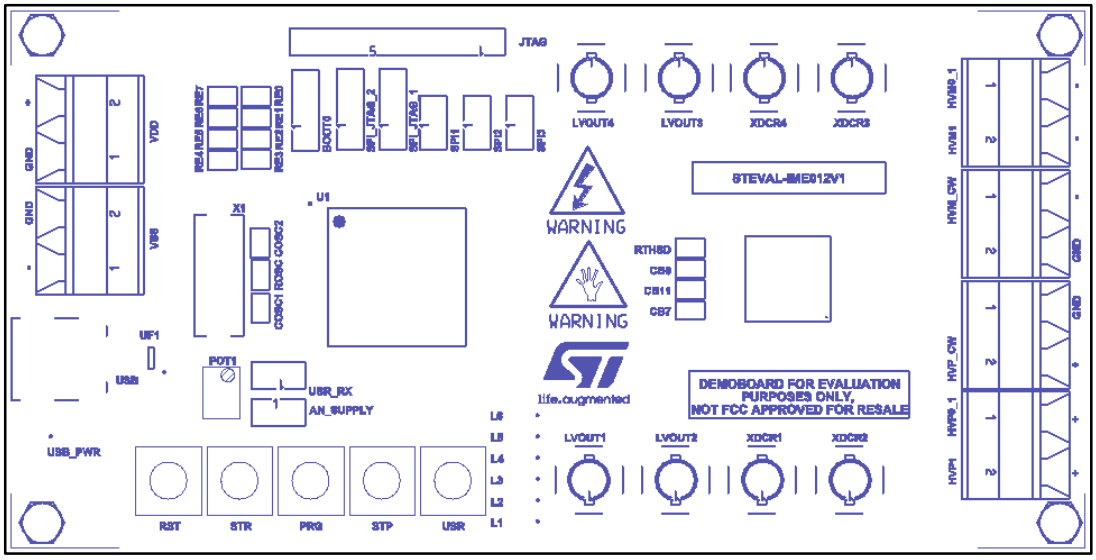


Figure 3: STEVAL-IME012V1 board layout



3.1 Power supply

The low voltage block of the STEVAL-IME012V1 board is designed to be powered by:

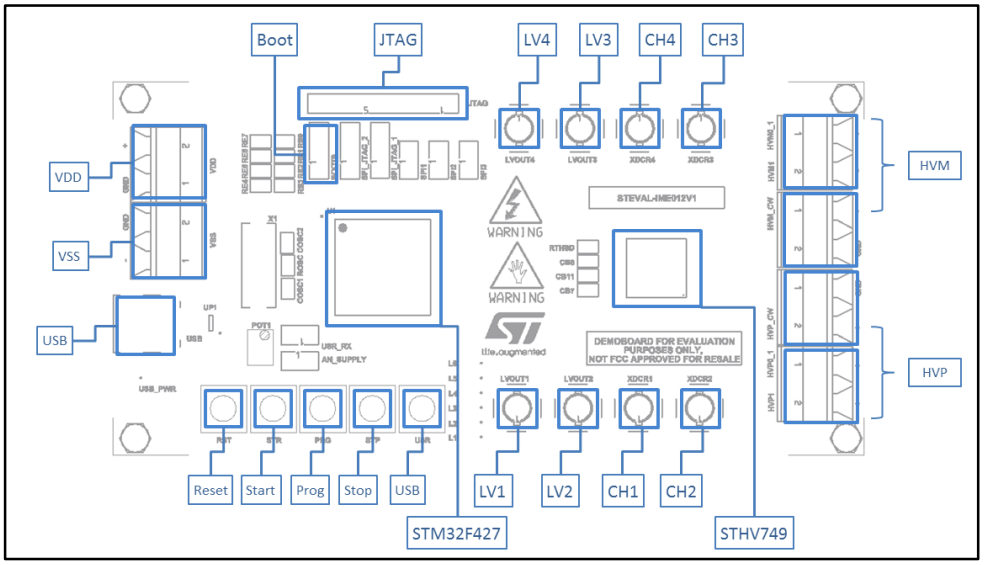
- During programming and when the board is connected to the PC
  - 5 V DC through USB Mini B connector to supply the STM32F4
- During pattern generation and when high voltage is powered on
  - 5 V DC connected to VDD to supply STM32F4 and STHV749 through a LDO
  - -5 V DC connected to VSS to supply STHV749 through a LDO

USB link must be removed when high voltage is connected to the board

The high voltage block of the STEVAL-IME012V1 is designed to be powered by:

- VDD: Positive supply voltage, 5 V (2 - VDD conn.)
- GND: Ground (1 – VDD conn. And 2 – VSS conn.)
- VSS: Negative supply voltage -5 V (1 - VSS conn.)
- HVM0: TX0 high voltage negative supply
- HVM1: TX1 high voltage negative supply
- HVM_CW: Continuous high voltage negative supply
- GND: Ground
- HVP_CW: Continuous high voltage positive supply
- HVP0: TX0 High voltage positive supply
- HVP1: TX1 High voltage positive supply

Figure 4: STEVAL-IME012V1 board connections



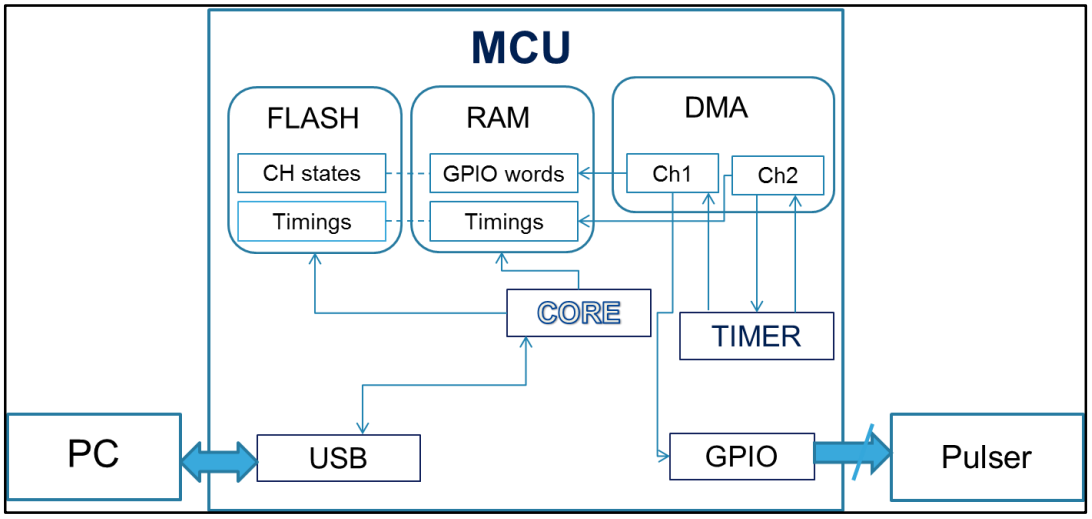
3.2 MCU

The STM32F427 is fully dedicated to generate the bitstream on its GPIO pins to drive the pulser's output channels. It is already pre-programmed as a DFU (device firmware upgrade) device and has the ability to upgrade internal Flash memory. The STM32F427 manages all DFU operations, such as the authentication of product identifier, vendor identifier, and firmware version. The MCU drives the pulser channels through the use of different general purpose IO (GPIO) pins. It is possible to drive simultaneously from 1 to 16 different pins simply by writing a 16-bit word into the GPIO output data register (ODR). The board can be connected to a PC through USB. The required pattern is sent as a sequence of states for each pulser channel and of durations for each state. Here, all durations are expressed in units of MCU system clock cycles. Once the information is received, the channel states are converted into 16-bit words for the GPIO peripheral and they are stored in the embedded Flash together with the timing information. After programming, the PC connection is no longer needed, so the board can act as a stand-alone device. Different patterns can be stored and the user can select which one to use at runtime. The same MCU can perform two different solutions to guarantee a real-time execution.

1. The first solution involves the use of the STM32 direct memory access (DMA) peripheral. The DMA is able to transfer data from memory to any peripheral register, GPIO included, without taking into account the MCU core. To trigger the DMA transfer, a general purpose

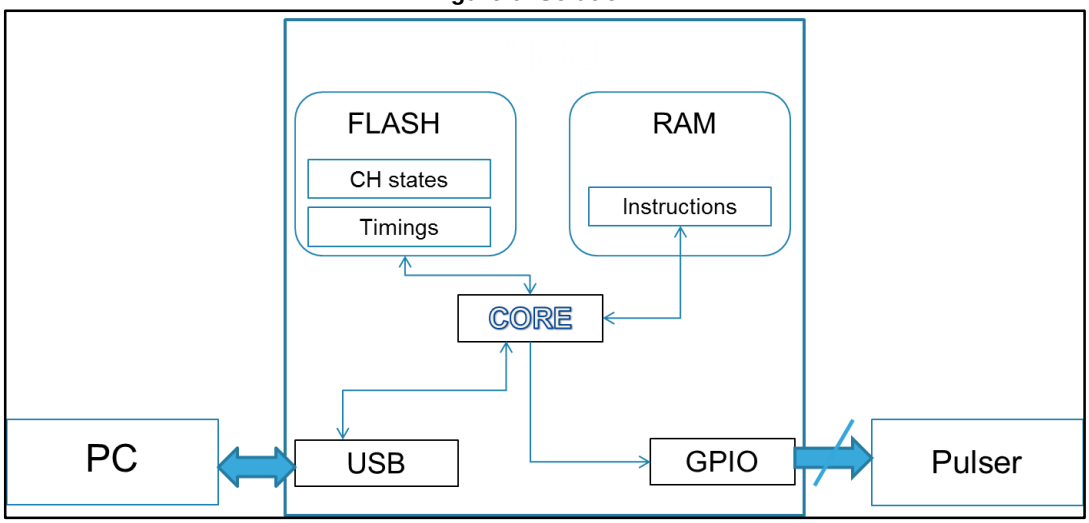
timer is used. The timer works at the system clock frequency. Basically, it acts as a counter and the reload value (the value at which the counter returns to zero) is stored in the auto reload register (ARR). The timer triggers two different DMA channels at two different moments: the first channel is triggered at each reload event, while the second is triggered at a constant time after reload. Once the first trigger is received, the first channel transfers the new GPIO word into the ODR. At the second trigger, the second channel transfers the new duration information into the ARR. The timer preload feature is enabled, so that the new ARR value is effective only at the next reload. Since the time needed by the first DMA channel to update the ODR is a constant, considering the reload trigger as the starting point, the time that elapses between two different GPIO updates is simply given by the ARR value. The circular buffer feature of the DMA can be enabled to allow an automatic regeneration of the same pattern at each end. This solution has the advantage of being fully managed by hardware. The MCU core is completely free for any user needs. The main drawback is that each timing value between two subsequent states cannot be lower than a minimum value, in order to guarantee enough time for both of the two DMA channels to perform their transfers.

Figure 5: Solution 1



2. The second solution was designed to overcome the minimum duration requirement of the DMA solution and involves the MCU core directly. During runtime, the core generates the binary assembly code it needs to load and store each word in the ODR. Any unnecessary instructions, like control loops or similar, are avoided. The code is only a succession of simple load/store instructions. To adapt the timing to the pattern needs, dummy instructions are inserted in the assembly code. To avoid wasting time to load each word from memory, the word is inserted as a literal in the assembly instruction itself. This means that a 32-bit instruction is needed instead of a 16-bit equivalent. In order to avoid any latency due to the instruction fetch from Flash, the code is executed from the embedded RAM. Moreover, the RAM is configured to be accessed by the core through a bus different from the bus used to access the ODR. Thanks to this, it is possible to achieve a minimum time of 2 system clock cycles before two updates and still a 1 system clock cycle resolution. For instance, if you consider a STM32F4 clocked at 168 MHz, the minimum timing you can achieve is 12 ns and you can set the duration of each state with a resolution of 6 ns. If there is a repetitive pattern, a branch instruction is added at the end of the routine to restart the pattern generation. In this case, the clock cycles needed for the branch instruction has to be considered for the last state. The main drawback of this solution is that the MCU core is 100% involved in the pattern generation. However, it can still be woken up by peripheral interrupts and the pattern generation stopped to perform other tasks.

Figure 6: Solution 2



3.3 Stored patterns

The STEVAL-IME012V1 offers the capability to memorize 4 patterns into the MCU Flash memory in order to demonstrate the performance achievable by the pulser outputs. Four selectable patterns already stored in the STM32 Flash memory are the default set available and ready for use. A detailed description of the programs is listed below.

Programming waveform description, flagged by LED L1 to L4.

Program “1”, SEL=0 (3-level output), CW=0

- XDCR_A: Pulse Wave mode, TX0 switching, 5 pulses, time-period T_P=400 ns and PRF=150 µs
- XDCR_B: Pulse Wave mode, TX0 switching, 5 pulses in counter phase respect to XDCR_A, time-period T_P=400ns and PRF=150 µs
- XDCR_C: Pulse Wave mode, TX1 switching, 5 pulses, time-period T_P=200ns and PRF=150 µs
- XDCR_D: Pulse Wave mode, TX1 switching, 5 pulses in counter phase respect to XDCR_C, time-period T_P=200ns and PRF=150 µs

TX0 means H-Bridge supplied by HVP/M0, while TX1 means H-Bridge supplied by HVP/M1

Figure 7: Scheme of program "1"

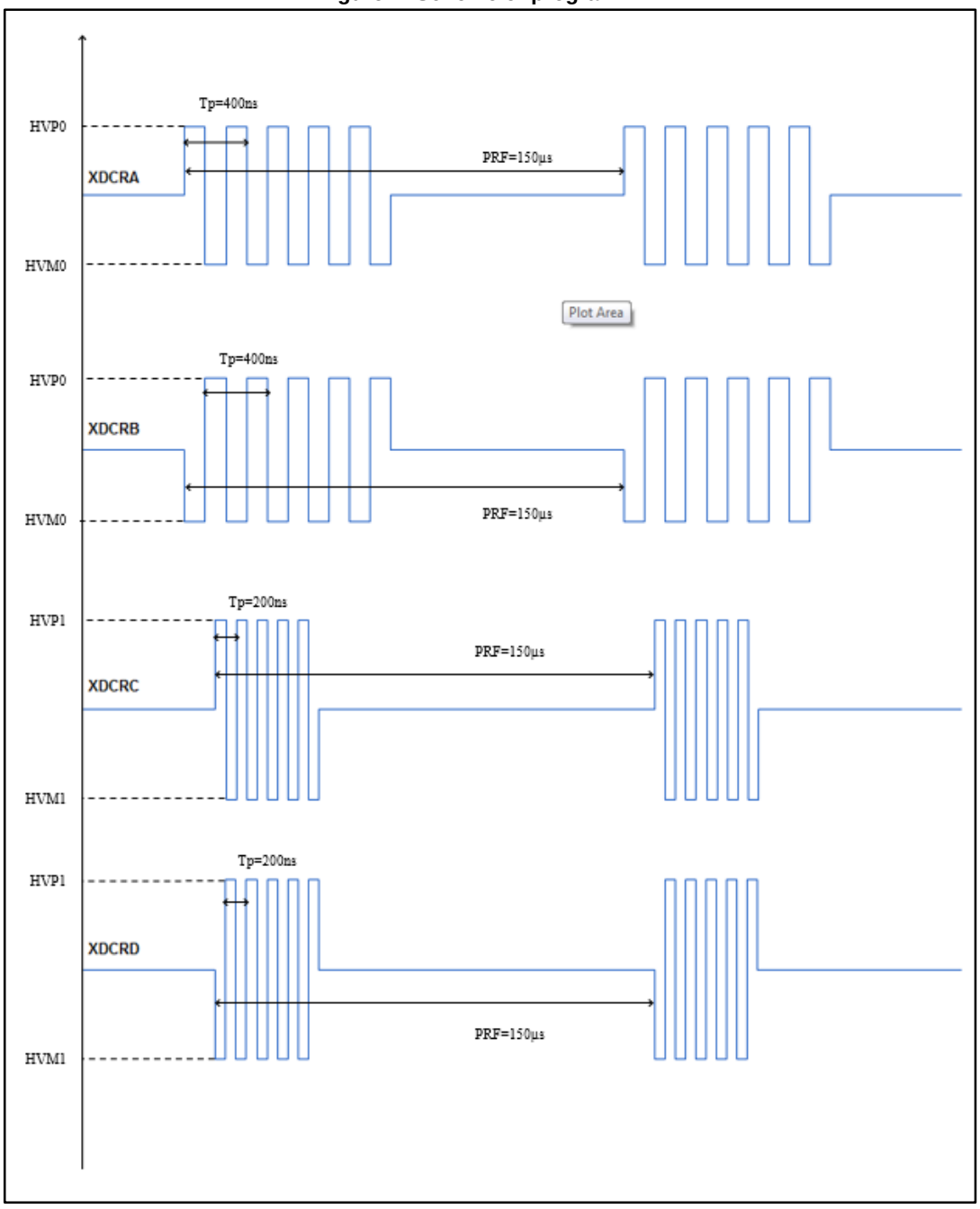
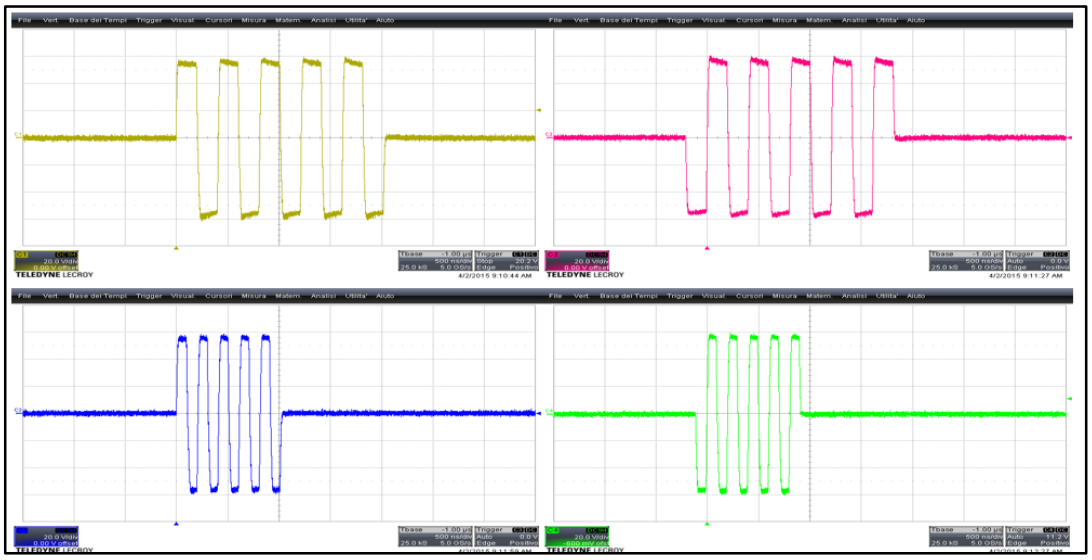


Table 1: Program "1"

PW 5pulses - HV0/1=±60 V; load: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-Bridge**	**PRF**
Ch A	PW	2.5	5	positive	TX0	150 µs
Ch B	PW	2.5	5	negative	TX0	150 µs
Ch C	PW	5	5	positive	TX1	150 µs
Ch D	PW	5	5	negative	TX1	150 µs

Figure 8: Acquisition by program "1"



Program “2” SEL=0 (3-level output), CW=0, see *Figure 9: "Scheme of program "2""*

- XDCR_A: Pulse Wave mode, TX0 switching, 5 pulses, time-period T_P=200ns and PRF=150 µs
- XDCR_B: Pulse Wave mode, TX0 switching, 5 pulses in counter phase respect to XDCR_A, time-period T_P=200ns and PRF=150 µs
- XDCR_C: Pulse Wave mode, TX1 switching, 5 pulses, time-period T_P=100ns and PRF=150 µs
- XDCR_D: Pulse Wave mode, TX1 switching, 5 pulses in counter phase respect to XDCR_C, time-period T_P=100ns and PRF=150 µs

Figure 9: Scheme of program "2"

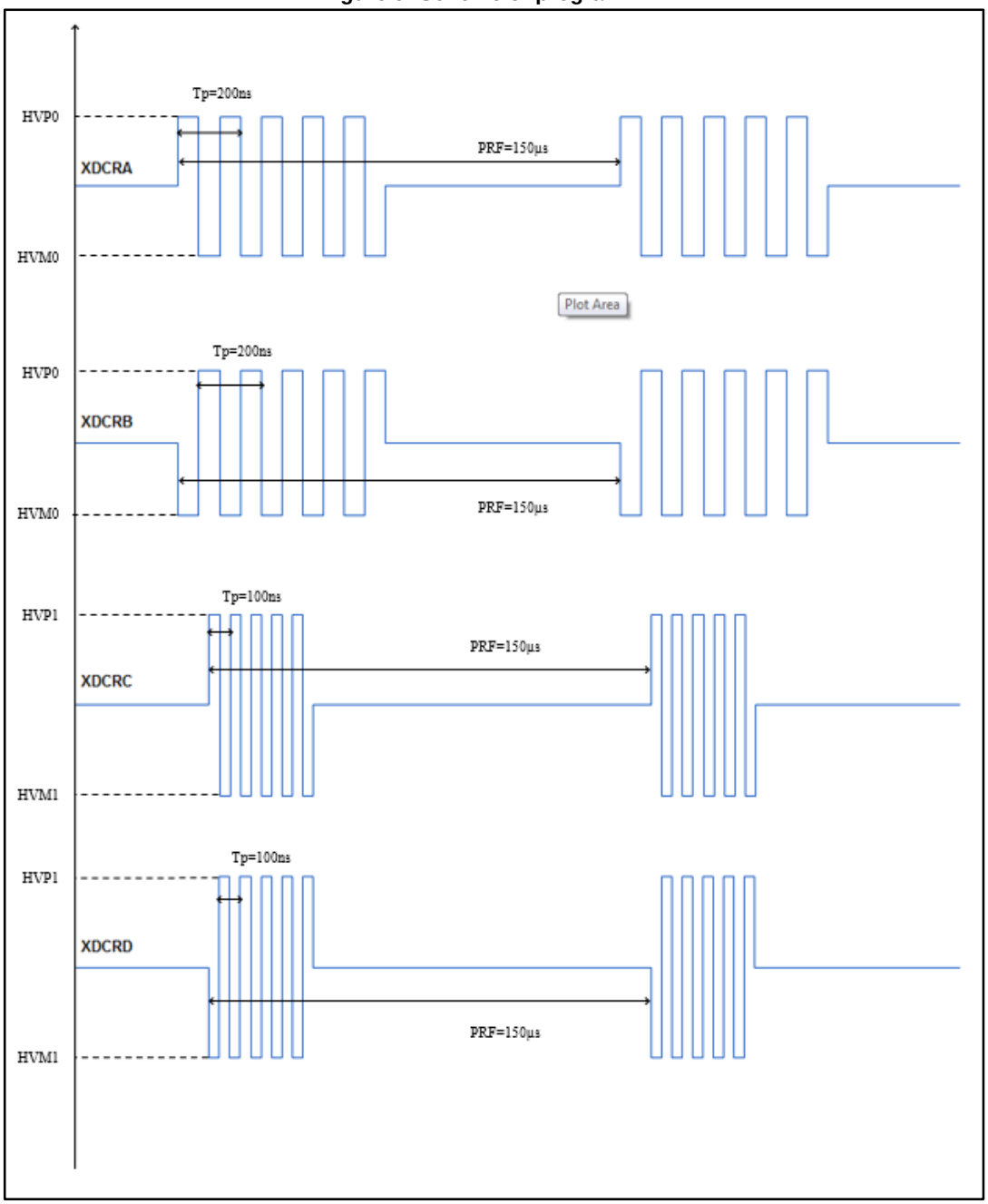
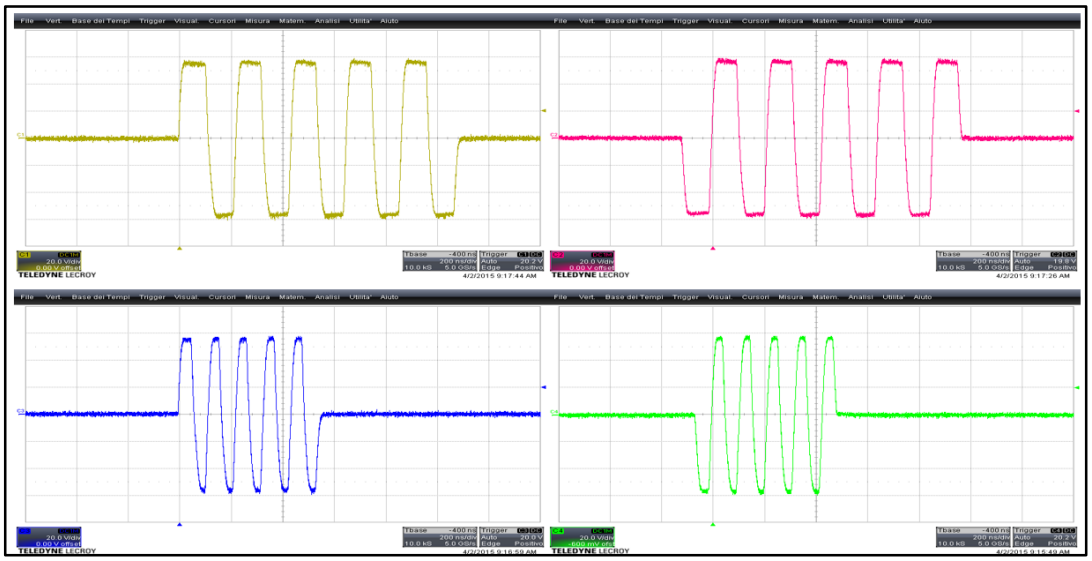


Table 2: Program "2"

PW TX0&TX1 5pulses - HV0/1= ±60 V; load: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-Bridge**	**PRF**
Ch A	PW	5	5	positive	TX0 & TX1	150 µs
Ch B	PW	5	5	negative	TX0 & TX1	150 µs
Ch C	PW	10	5	positive	TX0 & TX1	150 µs
Ch D	PW	10	5	negative	TX0 & TX1	150 µs

Figure 10: Acquisition by program "2"



Program “3” SEL=don’t care, CW=1, see *Figure 11: "Scheme of program "3"*

- XDCR_A: Continuous Wave mode, TX-CW switching, time-period T_P=400 ns
- XDCR_B: Continuous Wave mode, TX-CW switching in counter-phase respect to XDCR_A, time-period T_P=400 ns
- XDCR_C: Continuous Wave mode, TX-CW switching, time-period T_P=200 ns
- XDCR_D: Continuous Wave mode, TX-CW switching in counter-phase respect to XDCR_C, time-period T_P=200 ns

Figure 11: Scheme of program "3"

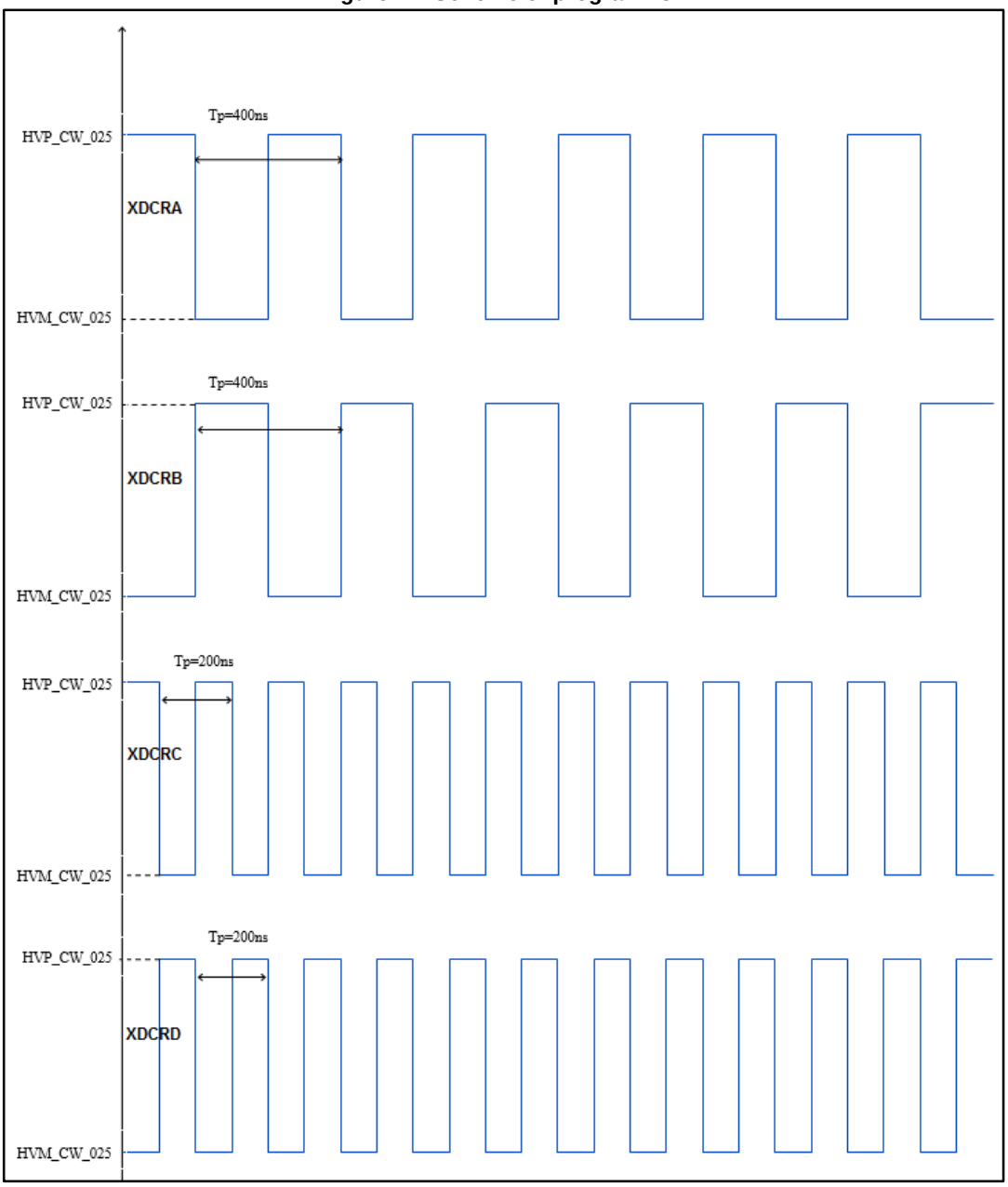
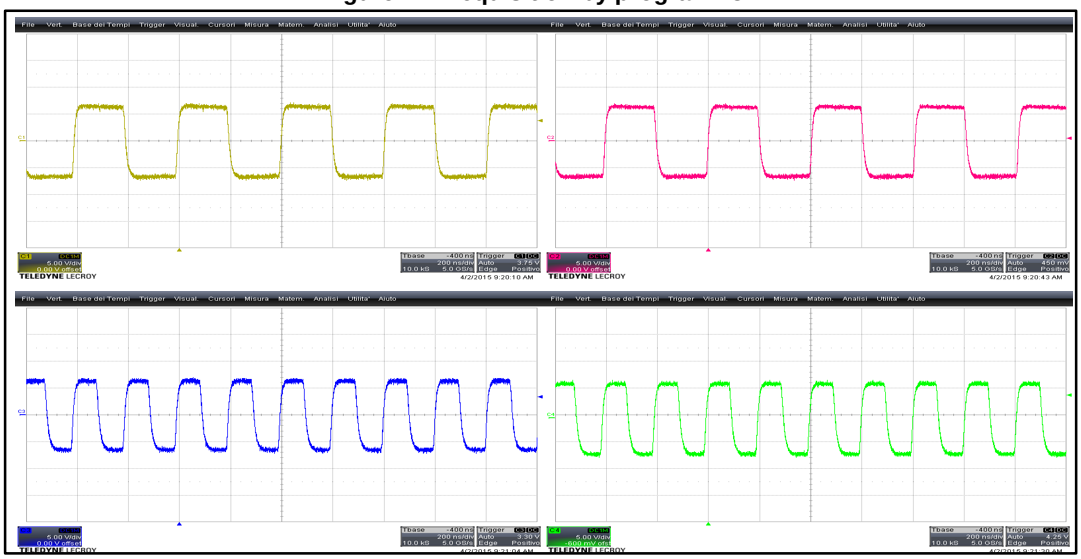


Table 3: Program "3"

Continuous wave - HV1= ±10 V; load: 270 pF//100 Ω					
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-Bridge**
Ch A	CW	2.5	Continuous wave	Positive	TX-CW
Ch B	CW	2.5	Continuous wave	Negative	TX-CW
Ch C	CW	5	Continuous wave	Positive	TX-CW
Ch D	CW	5	Continuous wave	Negative	TX-CW

Figure 12: Acquisition by program "3"



Program “4” SEL=1 (5-level output), CW=0

- XDCR_A: Pulse wave mode, TX0 switching, 1.5 pulses, time-period T_P=400 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs
- XDCR_B: Pulse wave mode, TX0 switching, 1.5 pulses, time-period T_P=400 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs
- XDCR_C: Pulse wave mode, TX0 switching, 1.5 pulses, time-period T_P=200 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs
- XDCR_D: Pulse wave mode, TX0 switching, 1.5 pulses, time-period T_P=200 ns and consequently TX1 switching, 5 pulses, time-period=200 ns and PRF=150 µs

Figure 13: Scheme of program "4"

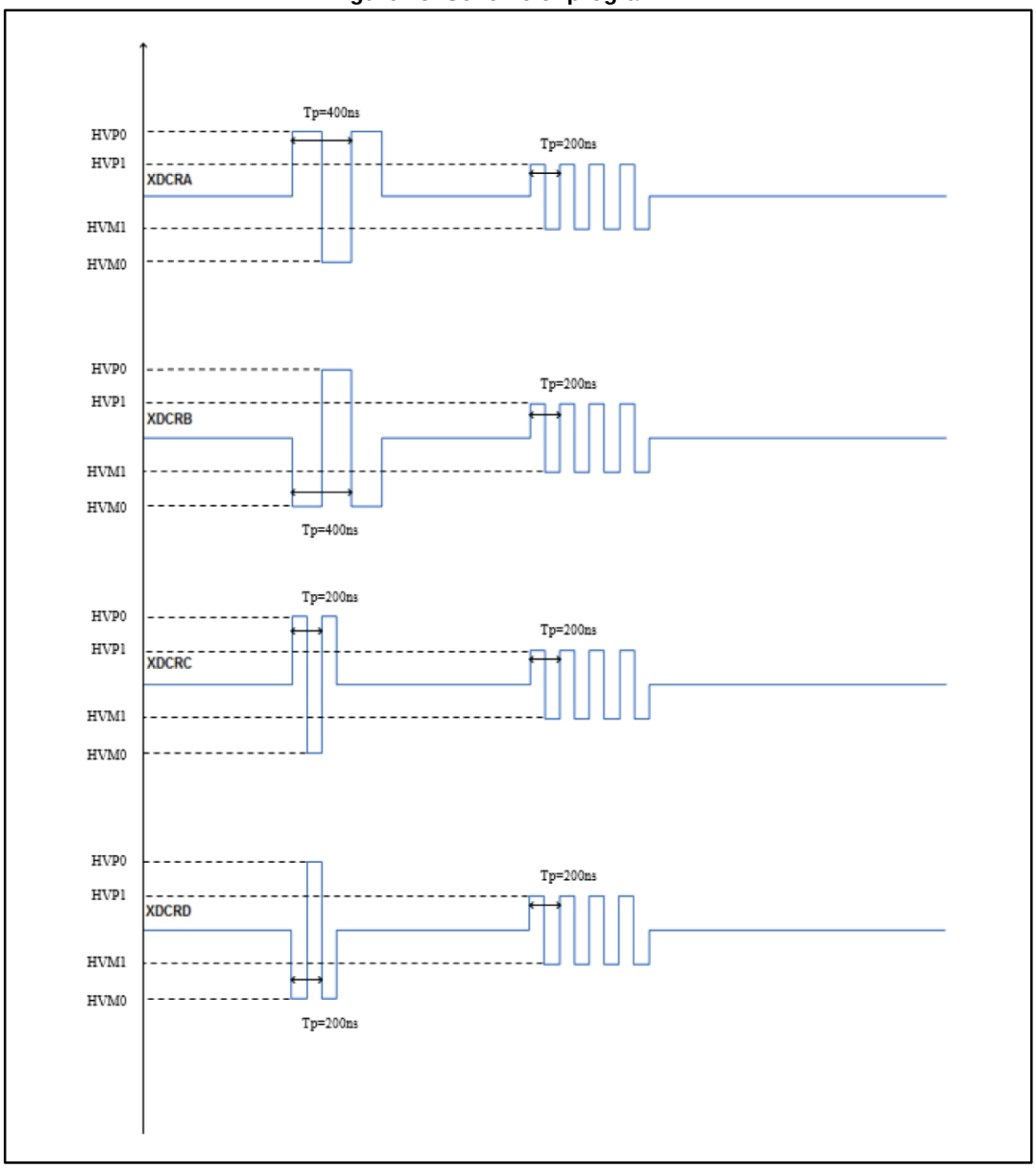
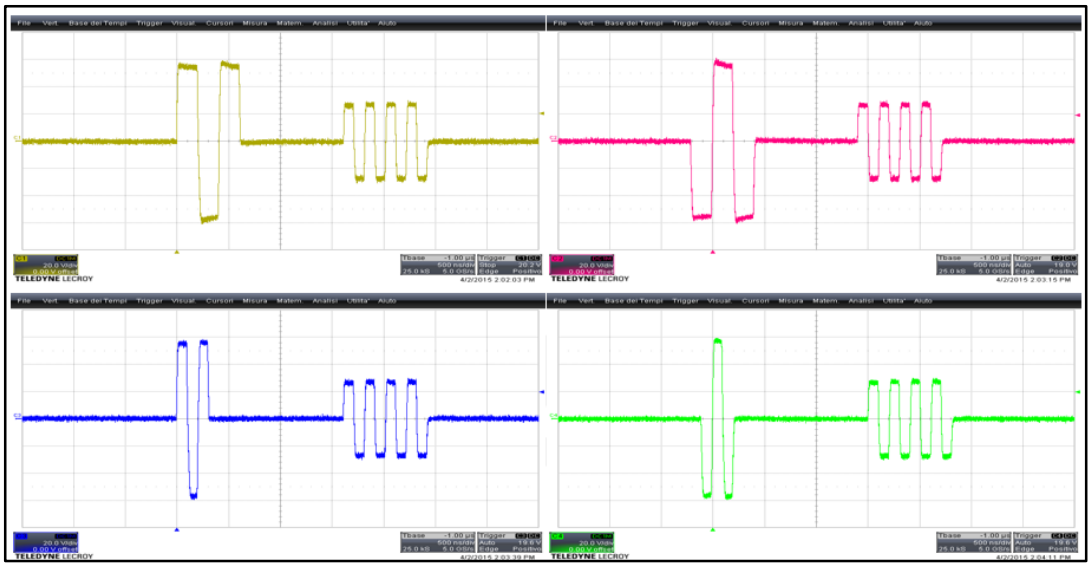


Table 4: Program "4"

PW - HV0= ±60 V – HV1= ±30 V; load: 270 pF//100 Ω						
	Mode	**Frequency (MHz)**	**Number of pulses**	**Initial pulse**	**H-Bridge**	**PRF**
Ch A	PW	2.5 - 5	3 half pulse then 4 pulse	positive	TX0 then TX1	150 µs
Ch B	PW	2.5 - 5	3 half pulse then 4 pulse	negative	TX0 then TX1	150 µs
Ch C	PW	5	3 half pulse then 4 pulse	positive	TX0 then TX1	150 µs
Ch D	PW	5	3 half pulse then 4 pulse	negative	TX0 then TX1	150 µs

Figure 14: Acquisition by program "4"



Board can be connected to a PC via USB cable and patterns can be edited by means of a user interface.

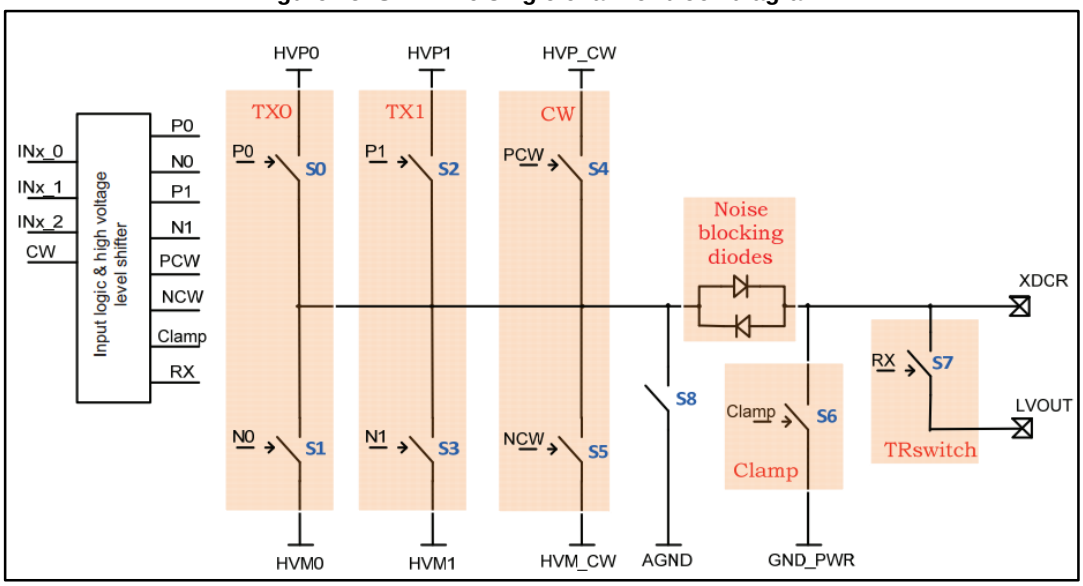
USB link must be removed when high voltage is connected to the board.

3.4 STHV749 stage

The STHV749 high voltage, high speed ultrasound pulser generator features four independent channels. It is designed for medical ultrasound applications, but can also be used for other piezoelectric, capacitive, or MEMS transducers. The device contains a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes, and high-power P-channel and N-channel MOSFETs as output stages for each channel. There is also clamping-to-ground circuitry, anti-leakage, an anti-memory effect block, a thermal sensor, and an HV receiver switch (HVR_SW) to ensure strong decoupling during the transmission phase. The STHV749 also includes self-biasing and thermal shutdown blocks. Each channel can support up to five active output levels with two main half bridges. It consists of three independently supplied output stages: two (TX0 and TX1) used for pulsed wave (PW) and one for continuous wave (CW) operations. TX0 and TX1 are able to provide up to ± 2 A peak output current each while, to reduce power dissipation and jitter in continuous wave mode, the fully optimized CW output stage delivers up to ± 0.3 A. The current capability for CW mode can also be set to 0.6 A. The device can also be configured to operate as a 3-output-level, ± 4 A, 40 MHz pulser. This mode can be selected via a dedicated input pin (SEL). In this configuration, the TX0 and TX1 half bridges are paralleled in order to provide higher peak current and shorter pulse waveforms, thus providing a higher output frequency.

For further information, please refer to the STHV749 datasheet.

Figure 15: STHV749 single channel block diagram



3.5 Operating supply conditions

Table 5: DC working supply conditions

Operating supply voltages					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Value**
V_{DD}	Positive supply voltage	5	6	10	V
V_{SS}	Negative supply voltage	-5	6	-10	V
HVP0	TX0 high voltage positive supply			95	V
HVP1	TX1 high voltage positive supply			95	V
HVM0	TX0 high voltage negative supply	-95			V
HVM1	TX1 high voltage negative supply	-95			V
HVP_CW	CW high voltage positive supply			95	V
HVM_CW	CW high voltage negative supply	-95			V

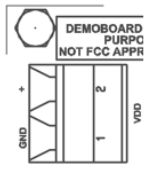
HVM0 / HVM1 /HVM_CW and HVP0 / HVP1 /HVP_CW are fully independent on the board.

4 Connectors

4.1 Power supply

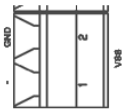
The STEVAL-IME011V1 board must be powered by screw connectors, as shown in following illustrations.

Figure 16: Power supply connector VDD (+5 V - GND)



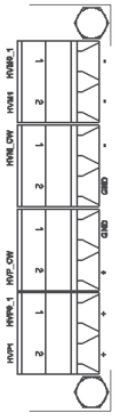
1	GND
2	VDD

Figure 17: Power supply connector VSS (GND - -5 V)



1	VSS
2	GND

Figure 18: Power supply connector HVP0 – HVP1 and HVM0 – HVM1



1	HVM0
2	HVM1
1	HVM_CW
2	GND
1	GND
2	HVP_CW
1	HVP0
2	HVP1

4.2 Power-up sequence

1	VDD
2	VSS

The recommendation for powering up the board is for the low voltages shown above in the table above. Other voltages are fully power-up/power-down free, meaning that there is no recommended sequence to follow.

4.3 MCU

Figure 19: USB mini-B connector (CN1)

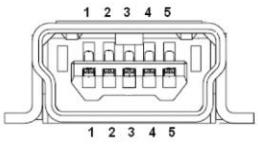
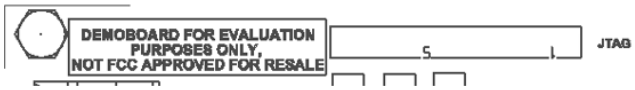


Table 6: USB mini B connector pinout

PIN Number	Description
1	Vbus (power)
2	DM (STM32 PA11)
3	DP (STM32 PA12)

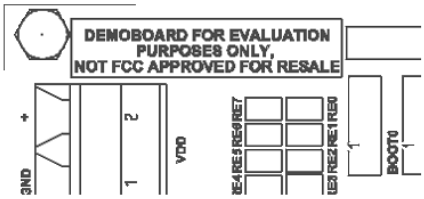
PIN Number	Description
4	N.C.
5	Ground

Figure 20: JTAG connector



1	DVDD
2	JTDI
3	JTMS
4	JTCK
5	JTDO
6	JRST
7	GND
8	NRST

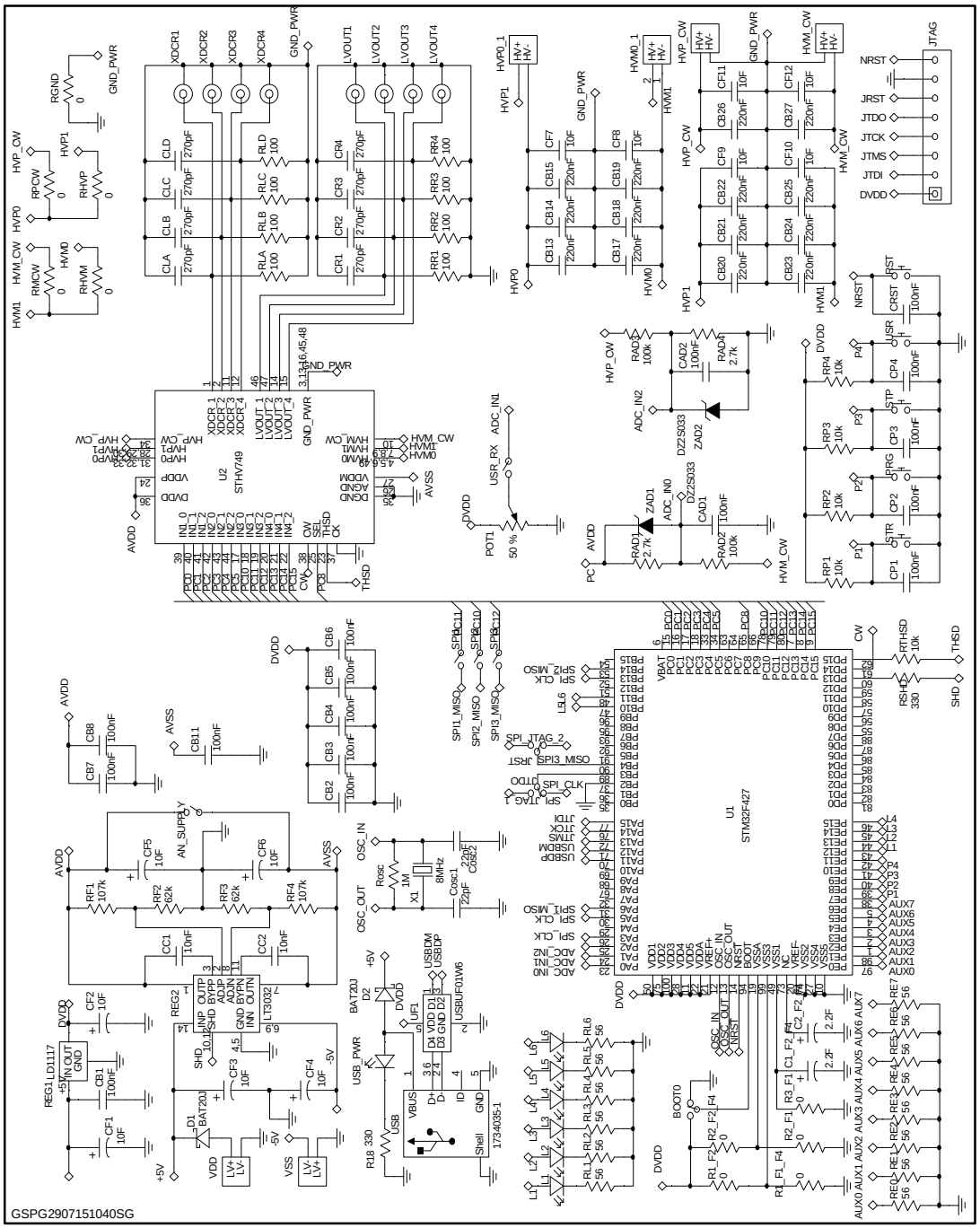
Figure 21: Boot connector



1	GND
2	BOOT0 (boot from flash memory)
3	DVDD (DFU mode)

5 Schematic diagram

Figure 22: STEVAL-IME012V1 circuit schematic



6 PCB layout

Figure 23: Top layer

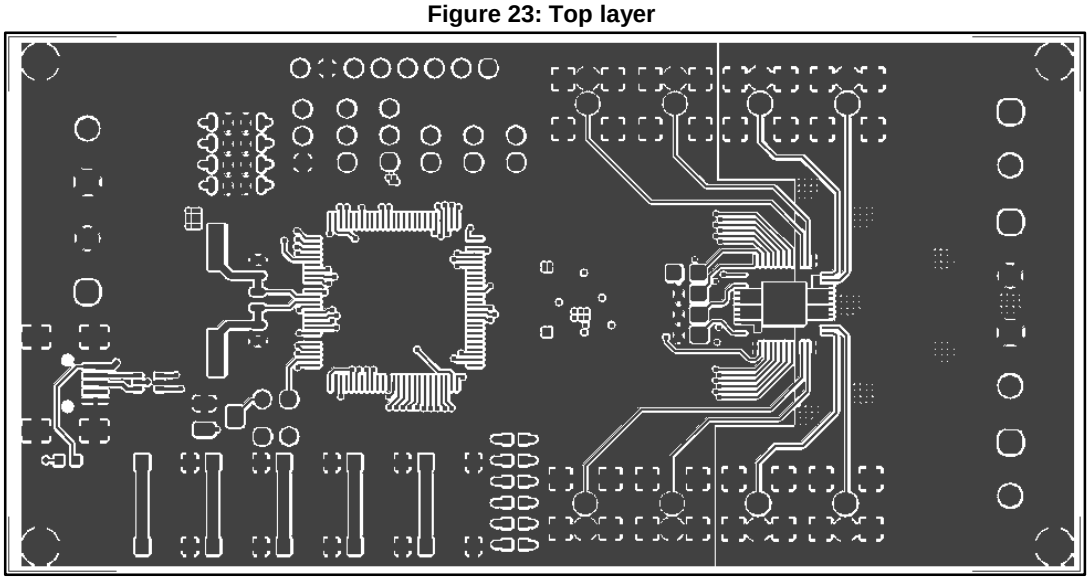


Figure 24: Inner layer 1

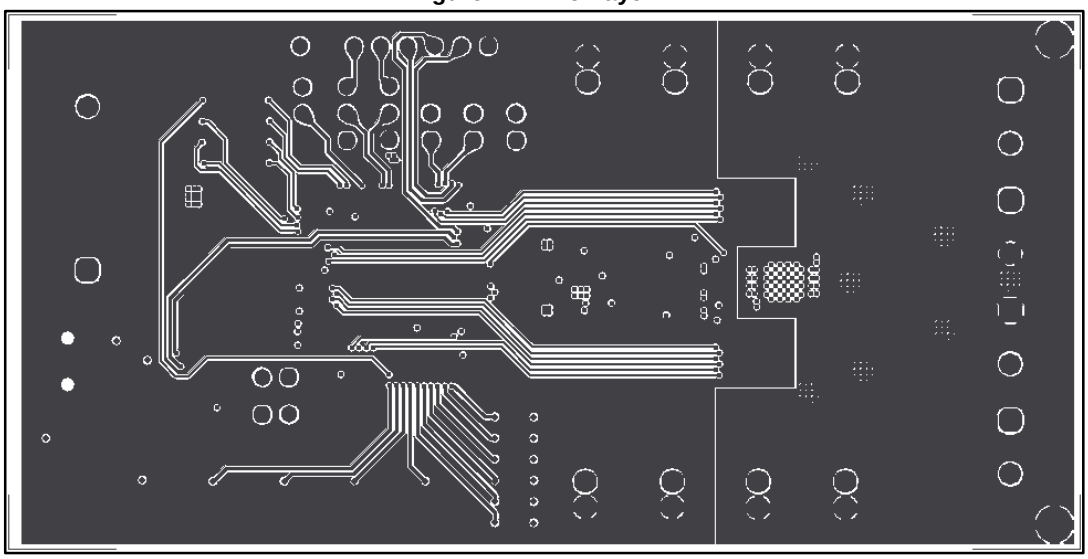


Figure 25: Inner layer 2

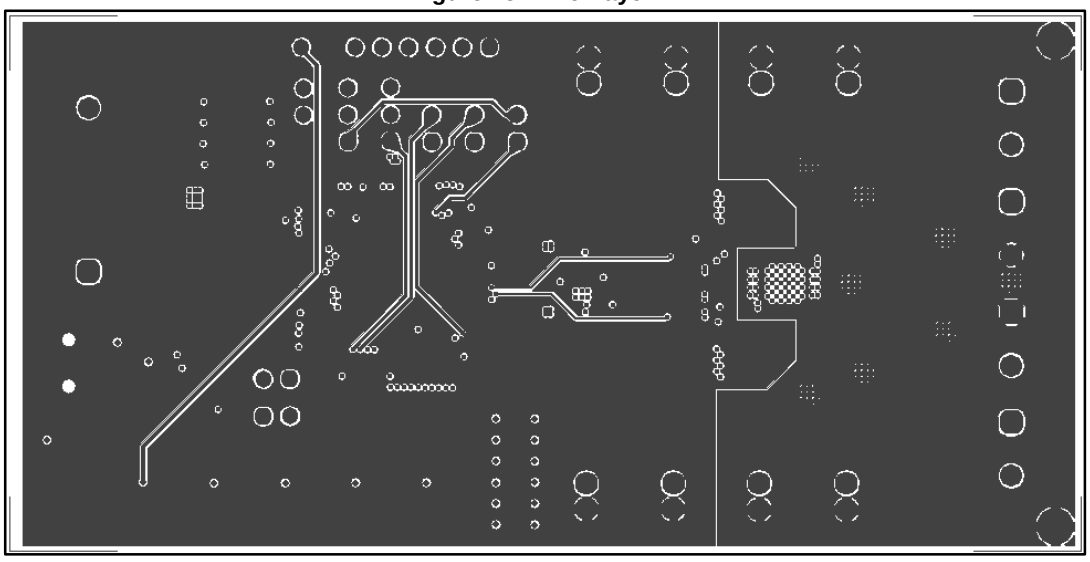


Figure 26: Inner layer 3

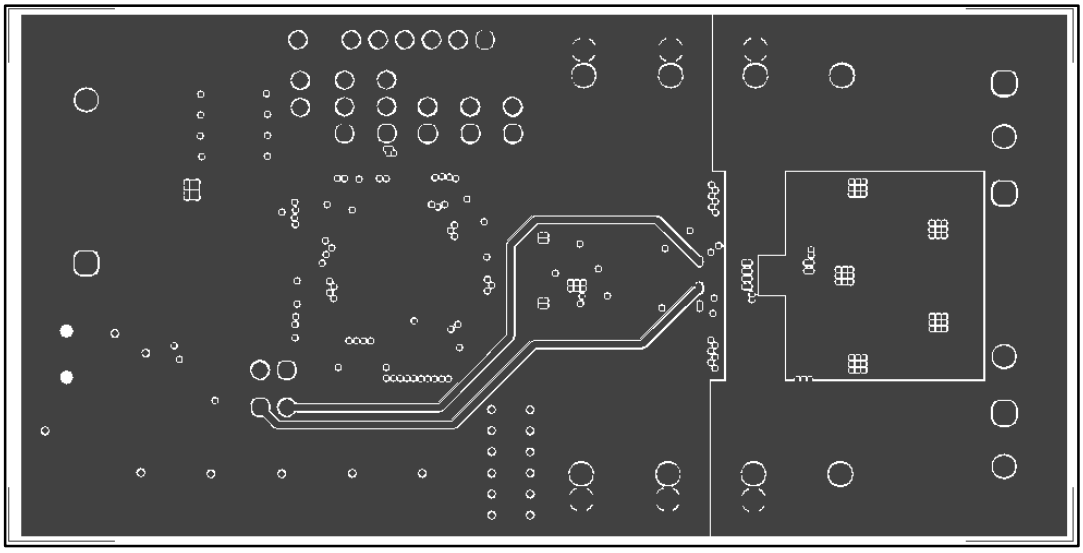


Figure 27: Inner layer 4

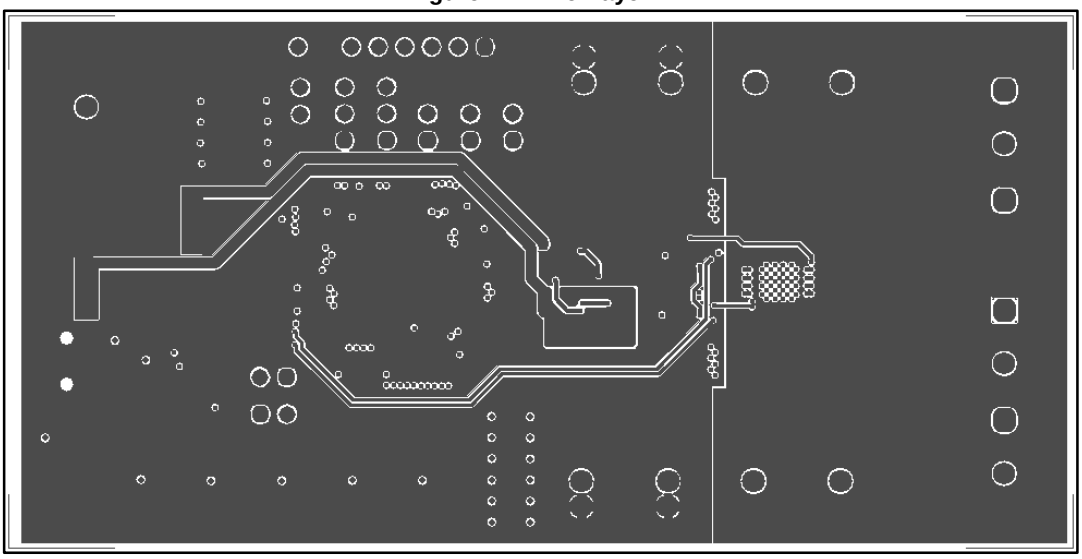
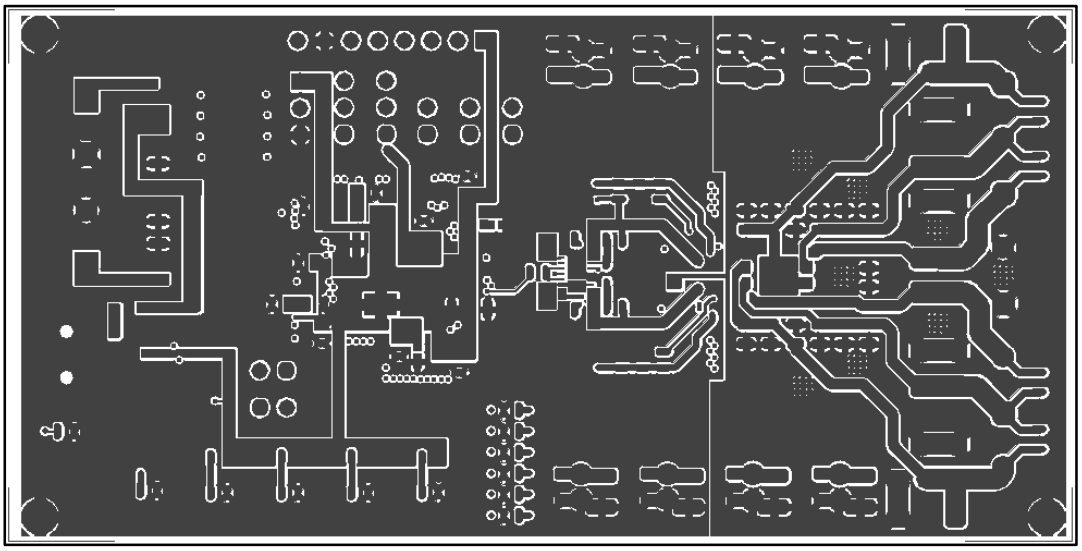


Figure 28: Bottom layer



7 Revision history

Table 7: Document revision history

Date	Version	Changes
05-Nov-2015	1	Initial release.

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