

## Discovery kit for the ST25R3911B high performance HF reader / NFC initiator

### Introduction

The ST25R3911B-DISCO is a ready-to-use development kit to evaluate the functions of the high performance HF reader / NFC initiator ST25R3911B in Reader mode for contactless applications.

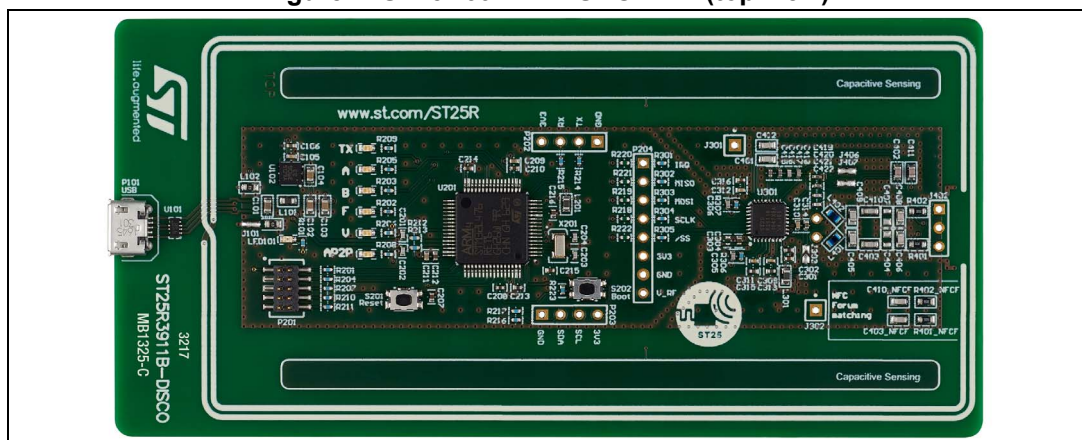
The ST25R3911B-DISCO kit supports

- ISO 18092 (NFCIP-1) active P2P
- ISO 14443A and ISO14443B
- ISO 15693
- FeliCa™
- VHBR, with 6.8 Mbit/s PCD to PICC framing and 3.4 Mbit/s PICC to PCD framing
- Up to 1.4 W output power with differential antenna
- Possibility of driving two antennas in single ended mode, with automatic antenna tuning (AAT) system
- Inductive and capacitive Wake-up
- User selectable and automatic gain control
- Transparent and Stream modes to implement MIFARE® Classic compliant or other custom protocols

The evaluation kit includes

- the STM32L476RET6, a 32-bit microcontroller with 512 KB of Flash memory
- a 105 mm x 52 mm, two turns antenna etched on the PCB, and its VHBR tuning circuit
- a Micro-USB connector for communication with the host PC and board powering
- six LEDs indicating the presence of the RF field and of the protocol used to communicate.

Figure 1. ST25R3911B-DISCO PCB (top view)



# Contents

- 1 Quick start ..... 5**
  - 1.1 Getting started ..... 5
  - 1.2 System requirements ..... 5
  
- 2 Hardware ..... 6**
  - 2.1 Block diagram ..... 6
  - 2.2 Schematics ..... 6
    - 2.2.1 USB connectivity and power supply ..... 7
    - 2.2.2 STM32L4 MCU ..... 7
    - 2.2.3 ST25R3911B ..... 7
    - 2.2.4 Antenna and matching network components ..... 8
  - 2.3 PCB layout ..... 14
    - 2.3.1 PCB overview ..... 14
    - 2.3.2 PCB layers ..... 14
  
- 3 Antenna matching ..... 20**
  
- 4 Federal Communications Commission (FCC) and Industry Canada (IC) compliance statements ..... 22**
  - 4.1 FCC Compliance Statement ..... 22
    - 4.1.1 Part 15.19 ..... 22
    - 4.1.2 Part 15.21 ..... 22
    - 4.1.3 Part 15.105 ..... 22
    - 4.1.4 FCC ID ..... 22
  - 4.2 Formal notices required by the Industry Canada (“IC”) ..... 22
    - 4.2.1 Compliance Statement ..... 22
    - 4.2.2 Declaration de Conformité ..... 23
    - 4.2.3 IC ID ..... 23
  
- 5 Revision history ..... 24**

## List of tables

Table 1. NFC Forum matching alternatives ..... 21  
Table 2. Document revision history ..... 24

## List of figures

Figure 1.	ST25R3911B-DISCO PCB (top view) . . . . .	1
Figure 2.	Functional block diagram . . . . .	6
Figure 3.	Schematics overview . . . . .	9
Figure 4.	USB interface . . . . .	10
Figure 5.	STM32L476 schematics . . . . .	11
Figure 6.	ST25R3911B schematics . . . . .	12
Figure 7.	Antenna and matching network schematics . . . . .	13
Figure 8.	PCB overview . . . . .	14
Figure 9.	PCB layout, top layer . . . . .	16
Figure 10.	PCB layout, mid layer 1 . . . . .	17
Figure 11.	PCB layout, mid layer 2 . . . . .	18
Figure 12.	PCB layout, bottom layer . . . . .	19
Figure 13.	VHBR matching with an AAT setting of 8 . . . . .	20
Figure 14.	NFC Forum matching with an AAT setting of 11 . . . . .	21

# 1 Quick start

The ST25R3911B-DISCO is connected to a PC via USB to show the features of the ST25R3911B chip. To do so, use the software STSW-ST25R001 to control all the functions of the discovery kit.

## 1.1 Getting started

Connect the discovery kit to a PC using a micro USB cable. The USB port of the PC must be capable of delivering at least 250 mA at 5 Volt supply.

To control the board, download the software STSW-ST25R001 from [www.st.com](http://www.st.com) and install it. Further information on how to operate the software can be found in the user manual UM2177 "PC software for the ST25R3911B-DISCO kit", available on [www.st.com](http://www.st.com).

## 1.2 System requirements

- Windows® PC (Windows 7 recommended)
- USB port, capable of delivering at least 250 mA at 5 V supply (1.25 W)
- Unit must be supplied by a Safety Extra Low Voltage (SELV) limited power source through the USB port, the source should not exceed 60 V<sub>DC</sub> / 8 A / 100 VA
- Micro-USB cable

## 2 Hardware

The PCB (Printed Circuit Board) is connected via USB to the PC. The STSW-ST25R001 PC software controls the STM32 MCU located on the PCB. The STM32 MCU (based on Arm<sup>®</sup> core) then operates the ST25R3911B via SPI.

**arm**

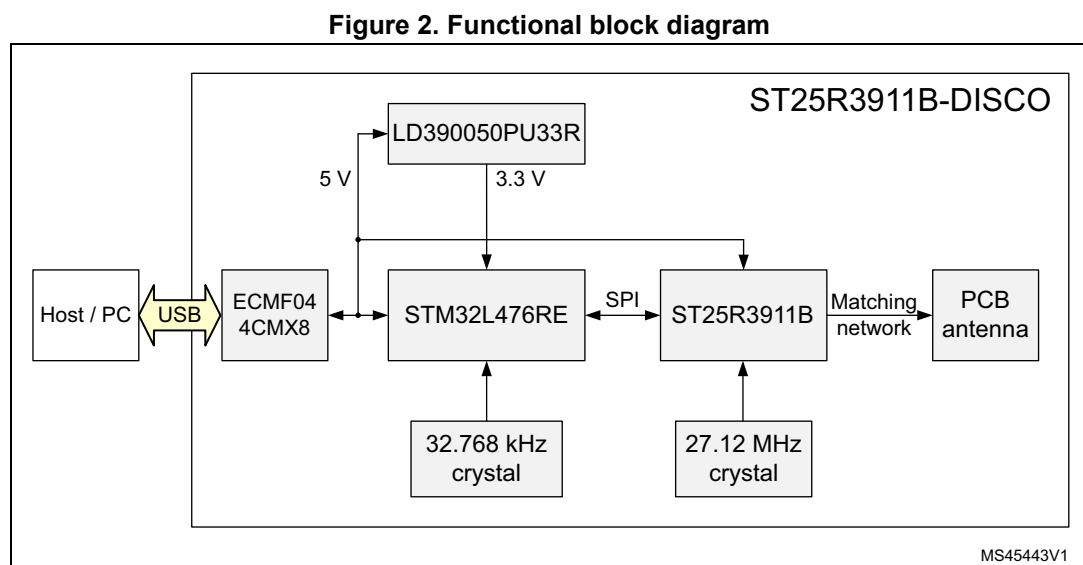
The ST25R3911B is connected directly to the 5 V supply of the USB bus. An LDO converts this voltage down to 3.3 V, to supply the microcontroller.

A green LED close to the USB plug indicates if the board is powered. Six blue LEDs indicate the mode of operation (transmit / receive) and which technologies are in use.

The antenna runs along the PCB perimeter.

### 2.1 Block diagram

*Figure 2* shows the functional block diagram of the board.



### 2.2 Schematics

As indicated in *Figure 3*, the schematics can be split into four main parts

- USB connectivity and power supply (*Figure 4*)
- STM32 MCU (*Figure 5*)
- ST25R3911B (*Figure 6*)
- Antenna and matching network components (*Figure 7*)

### 2.2.1 USB connectivity and power supply

The ST25R3911B-DISCO board can be connected via USB to a host device.

Right behind the Micro-USB plug, an ECMF02 common mode filter with ESD protection for USB 2.0 interface is placed. The common mode filter is connected to VBUS and to the D+/D- data lines of the USB. All the USB terminals are ESD-protected by the built-in ESD diodes of the ECMF02.

Additionally, the power supply filter for the 5 V supplies the 3.3 V LDO, which, in turn, supplies the microcontroller.

A green LED is connected to the USB VBUS supply and shows the USB-power status.

### 2.2.2 STM32L4 MCU

This schematic includes the microcontroller needed to operate the NFC reader IC.

The MCU is clocked by a 32.768 kHz crystal. The MCU uses an internal PLL to generate the 48 MHz USB clock and the 80 MHz core clock from the provided 32.768 kHz.

Connector P201 is a JTAG/SWD interface to assist in software development. It can be connected to an external ST-LINK/V2 device using a 9-pin Cortex<sup>®</sup>-M adapter.

The six blue LEDs (LED201 to LED206) show the current mode of communication. If multiple protocols are active at the same time, then all corresponding LEDs are turned on.

The five resistors (R218 to R222) can be used to disconnect the MCU from SPI interface header P204. This SPI cross-connect mode can be used to operate the ST25R3911B with a different MCU PCB by cross connecting the ST25R3911B SPI to the second MCU PCB.

Connectors P202 and P203 can be used to connect an external UART or I2C host device to the MCU.

### 2.2.3 ST25R3911B

The ST25R3911B is directly connected to the filtered 5 V USB supply, and there are additional supply filtering components placed close to it. The jumper JP301 can be used to measure the supply current of the chip. If this measurement is performed, the ferrite bead L301 has to be removed.

Capacitors C301 to C304 provide additional filtering. All decoupling capacitors have been placed as close as possible to the ST25R3911B. Special care has been taken for C310, C302, C314 and C301, as they are the decoupling capacitors for the high power driver stage.

In order to demonstrate the capacitive wake-up feature, two capacitive electrodes are placed on the PCB. Additional electrodes can be connected using UFL connectors on P301 and P302.

For SPI cross-connecting to another reader PCB, the resistors R301 to R305 can be removed. Then the STM32L4 MCU SPI can be connected to the ST25R3911B on any customer PCB via header P204.

Thanks to J303 it is possible to bypass the internal VSP\_RF regulator, this is required in case output currents higher than 200 mA need to be supplied.

## 2.2.4 Antenna and matching network components

This schematic contains the matching network and the automatic antenna tuning capacitors, as well as the alternative NFC Forum matching components. In the default configuration, the ST25R3911B-DISCO is populated with a VHBR matching, with communication speeds up to 3.4 Mbps.

To support VHBR, the antenna is matched to a system Q-Factor of 8. By switching to the NFC Forum matching components the system Q-Factor is increased to 16. This can increase the read range up to 20%, depending on the used communication technology, but limits the maximum supported communication bit rate to 848 kbps. Additional details about antenna matching can be found on [www.st.com/st25r](http://www.st.com/st25r).



Figure 3. Schematics overview

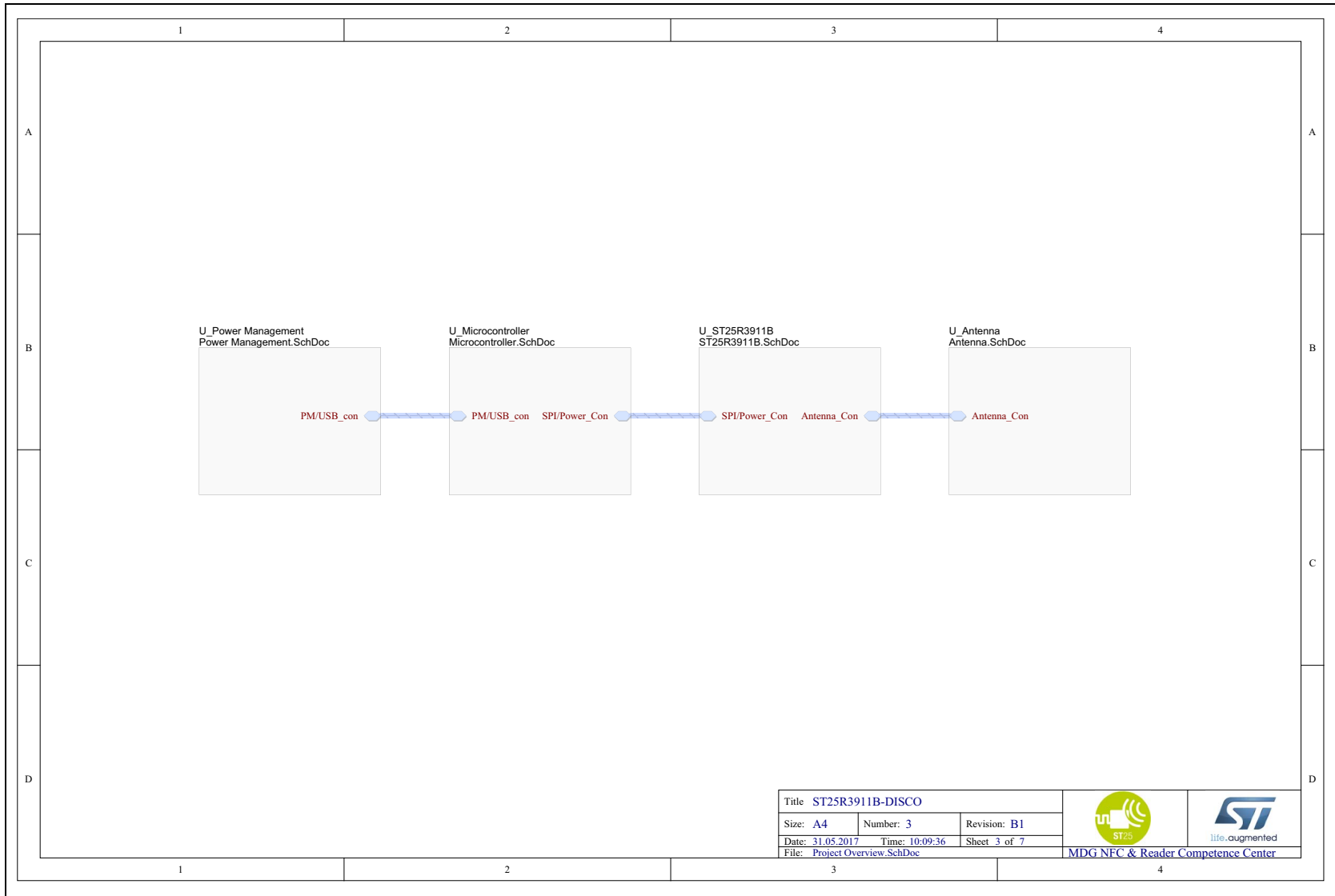
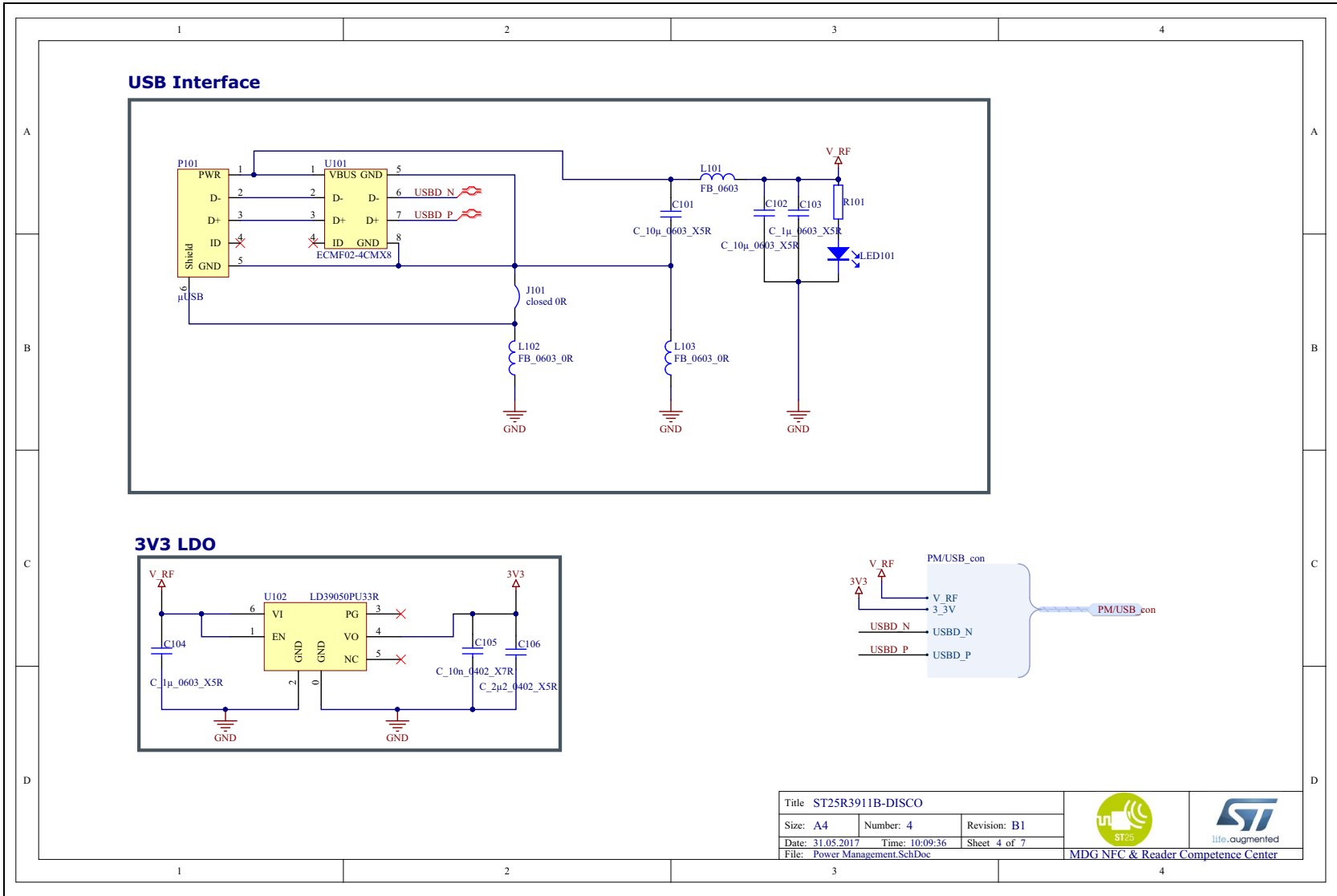




Figure 4. USB interface



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File: Power Management.SchDoc				

Figure 5. STM32L476 schematics

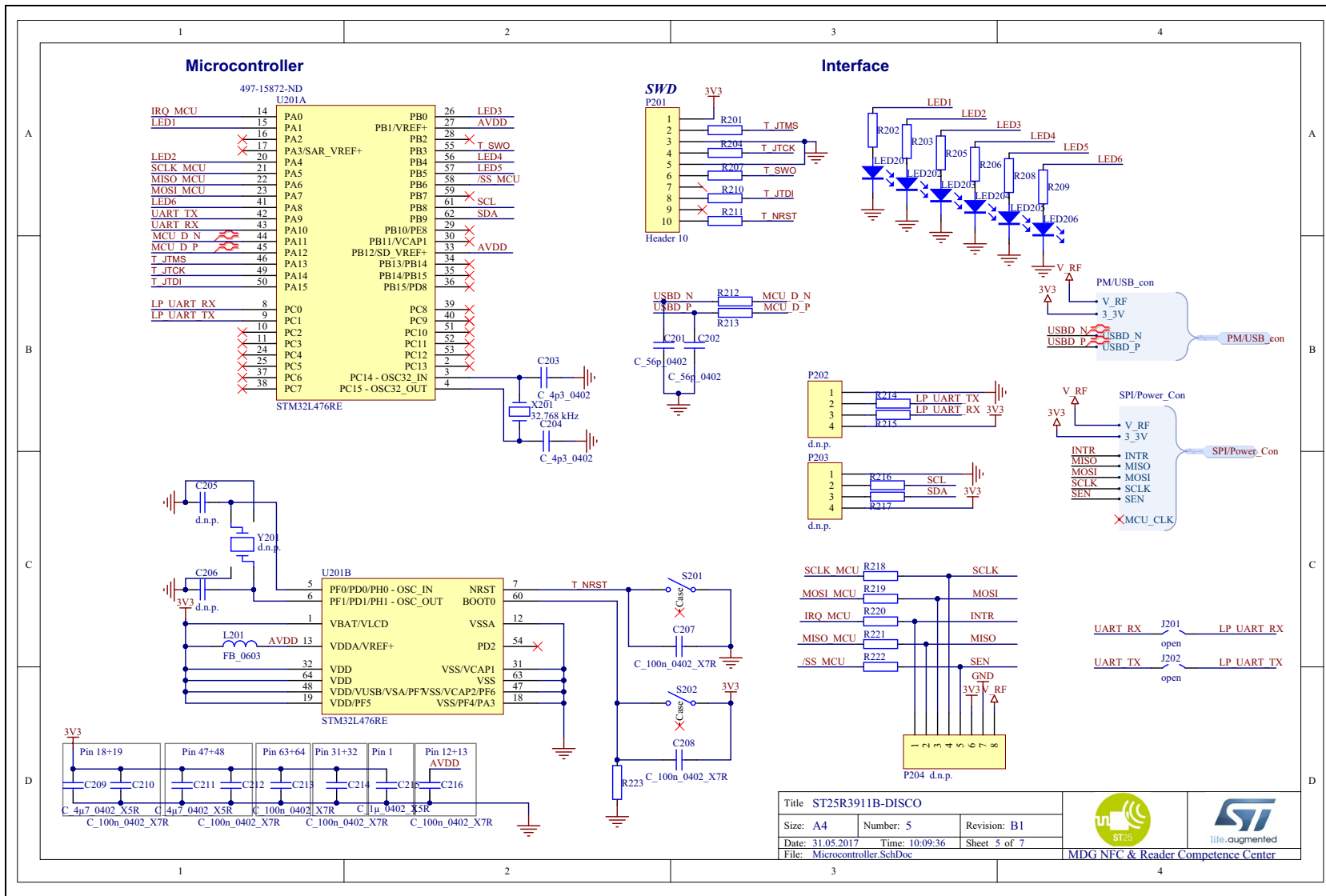
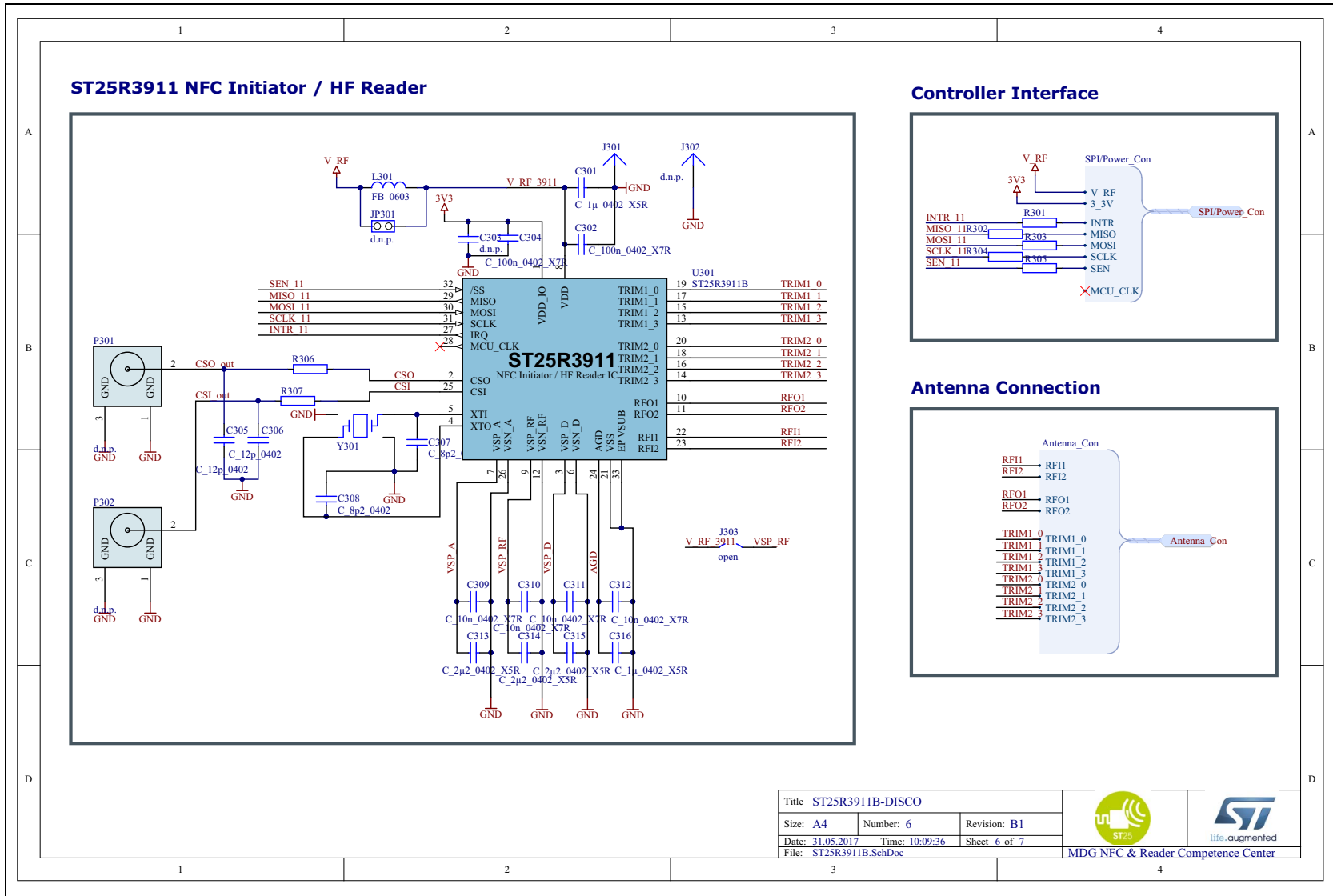




Figure 6. ST25R3911B schematics





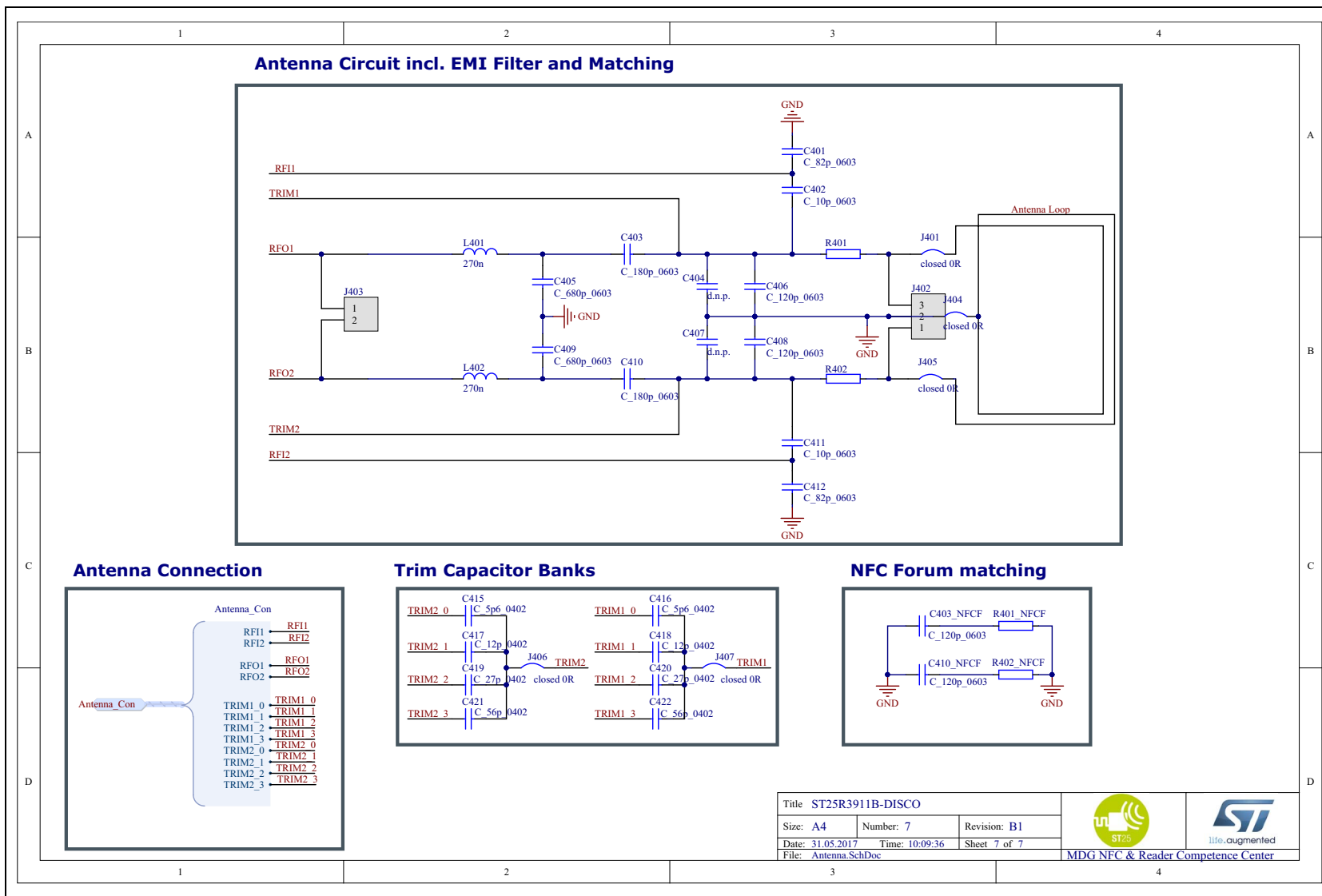
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Date: 31.05.2017	Time: 10:09:36	Sheet 6 of 7			
File: ST25R3911B.SchDoc		MDG NFC & Reader Competence Center			

Figure 7. Antenna and matching network schematics



## 2.3 PCB layout

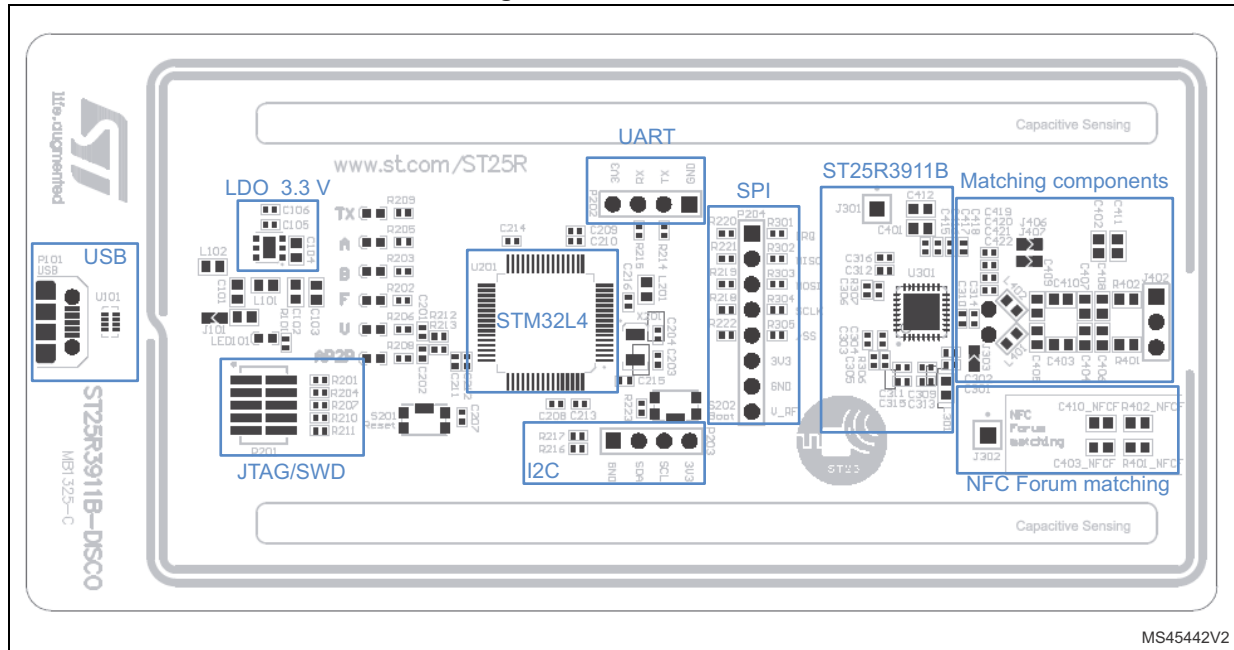
### 2.3.1 PCB overview

The PCB (see [Figure 8](#)) is organized in two halves

- Left side: the SPI header P204 and the digital / MCU sections
- Right side: the analog parts and the ST25R3911B.

The whole PCB is surrounded by a two turns NFC antenna.

**Figure 8. PCB overview**



The boot button can be found right above the I2C header. If this button is pressed during the powering or the resetting of the board, the STM32L4 will enter the boot loader mode. The reset button is positioned between the JTAG/SWD header and the I2C header.

### 2.3.2 PCB layers

The PCB layout is designed considering that the ST25R3911B is a high power RF transmitter, hence the decoupling capacitors are located as close as possible to the positive and negative power supply pins, for example VSP\_RF and VSN\_RF.

Since the chip is using a differential output driver stage, the antenna matching network is treated as a differential network. The space between the components is kept as small as possible and the whole network is routed in a completely symmetrical way.

Via stitching and via shielding is used to maintain a low impedance and prevent short return current loops. The RF traces are protected by via stitching in combination with guard rings to create a via wall. This keeps the PCB electromagnetically “quiet”.

A via shield is used to create a vertical copper barrier through the PCB. This helps to reduce crosstalk and electromagnetic interference in any route carrying an RF signal. The RFI traces and AAT lanes are routed as close as possible to each other.

**Top layer**

The top layer ([Figure 9](#)) contains most of the components and PCB traces. The unused areas around the ICs are filled with GND planes, guarded using via stitching. Furthermore, important analog traces are surrounded by GND vias.

**Mid layer 1**

This layer ([Figure 10](#)) is a pure GND plane, providing a low ohmic DC path for the GND connection.

**Mid layer 2**

Mid layer 2 ([Figure 11](#)) is used for the power distribution. It contains the power planes for the 5 V supply of the ST25R3911B and the 3.3 V supply of the microcontroller.

**Bottom layer**

The bottom layer ([Figure 12](#)) is mainly a GND plane, but some traces are routed through it.

Figure 9. PCB layout, top layer

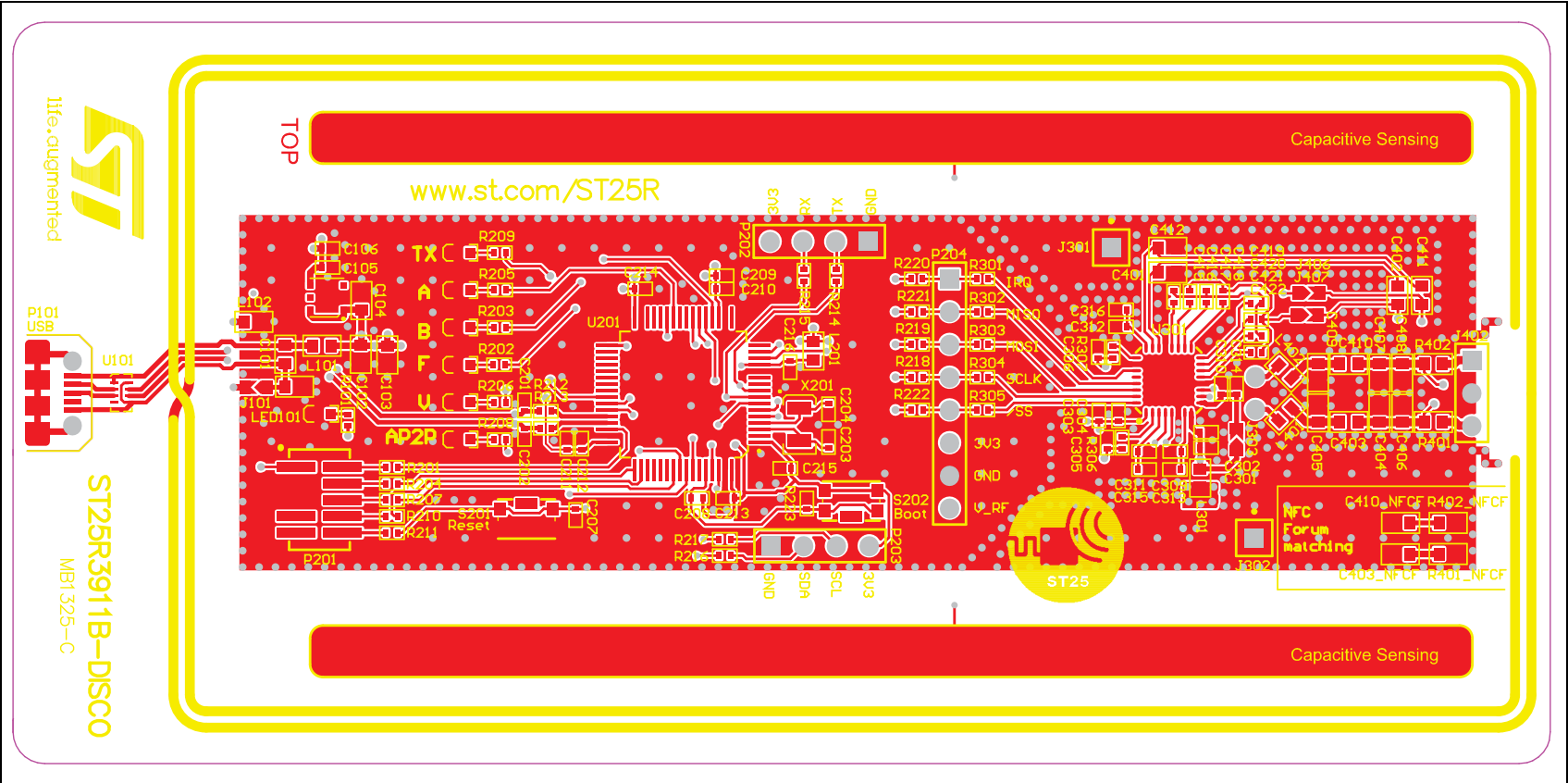




Figure 10. PCB layout, mid layer 1

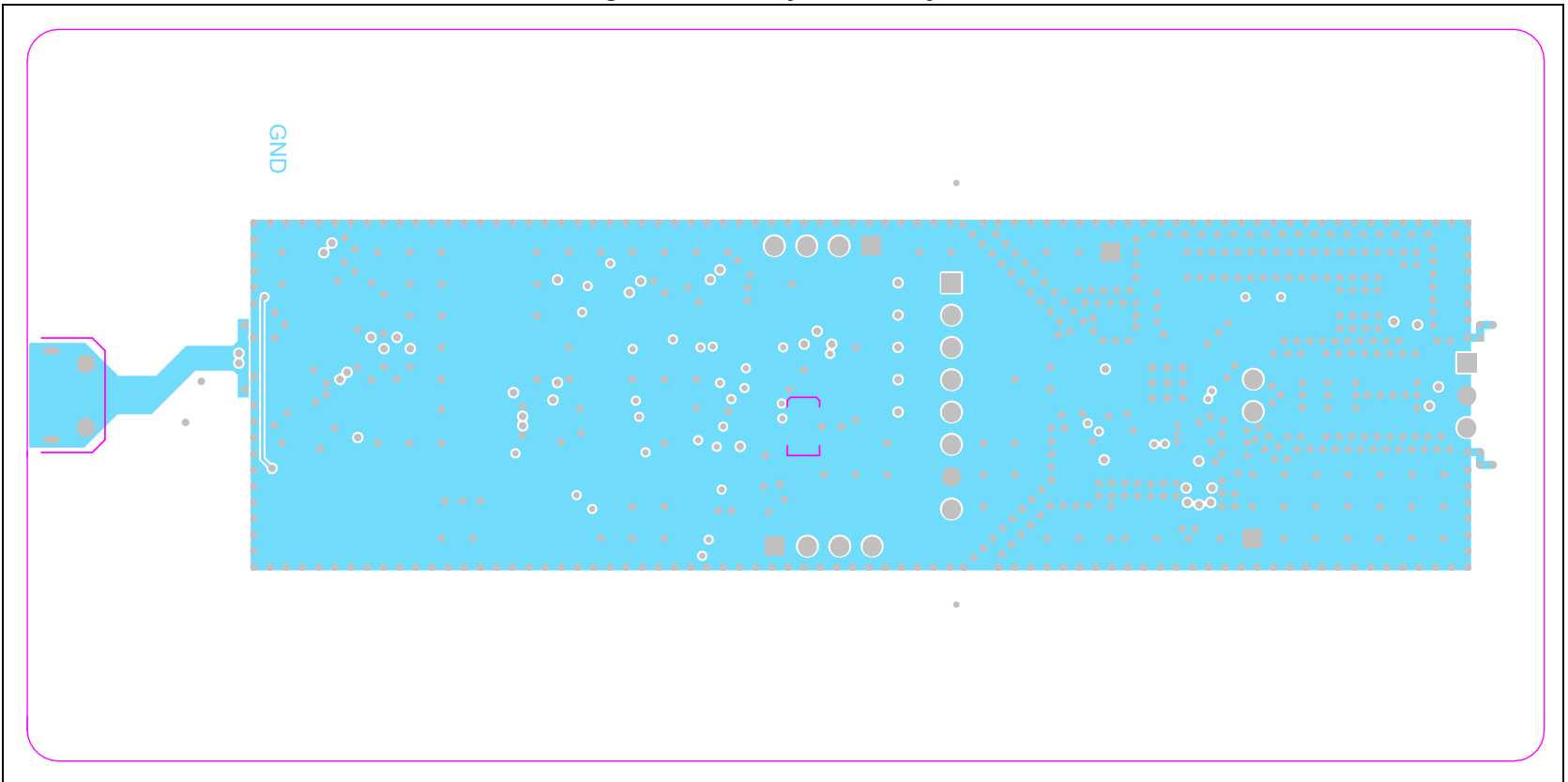


Figure 11. PCB layout, mid layer 2

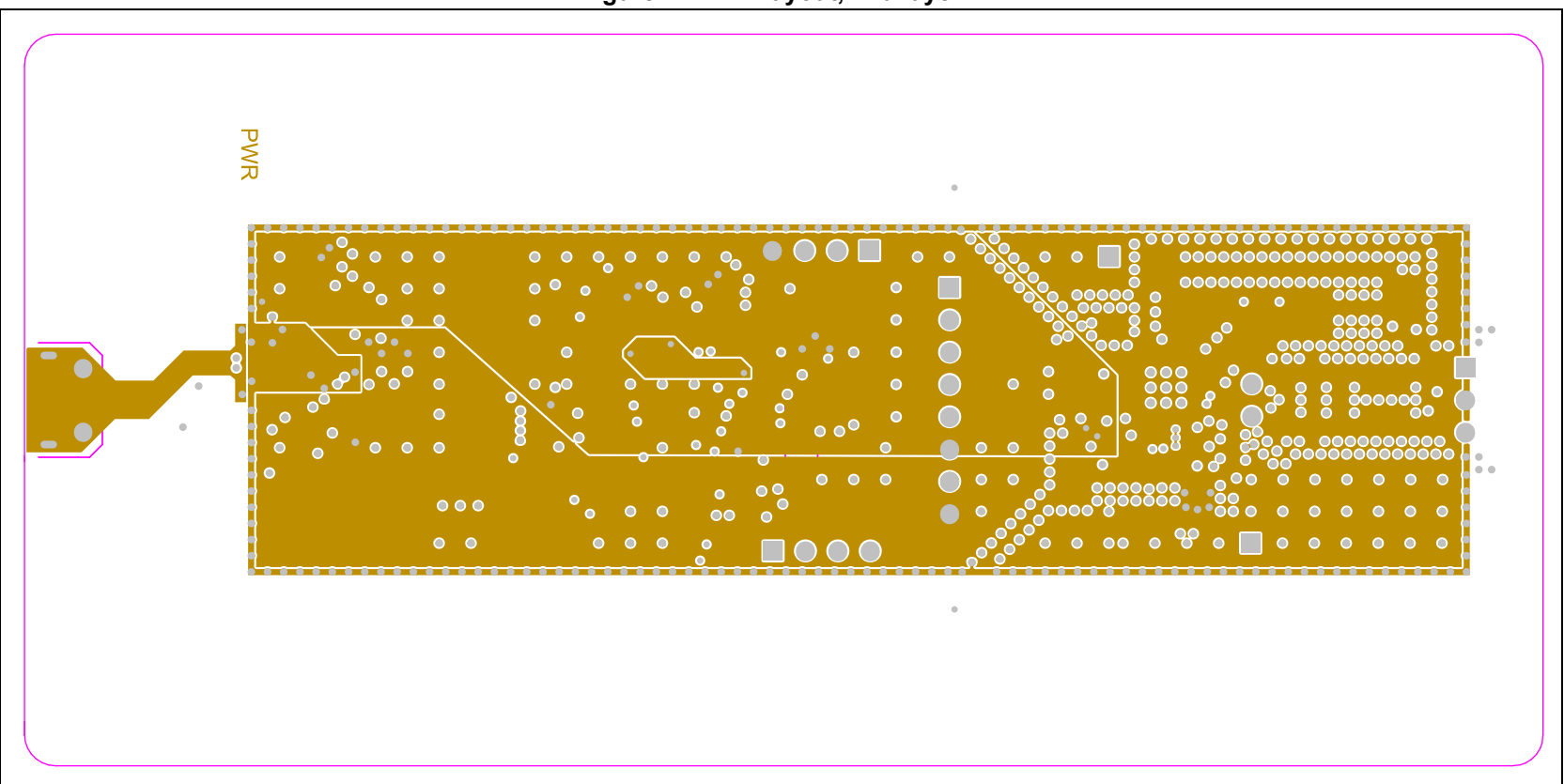
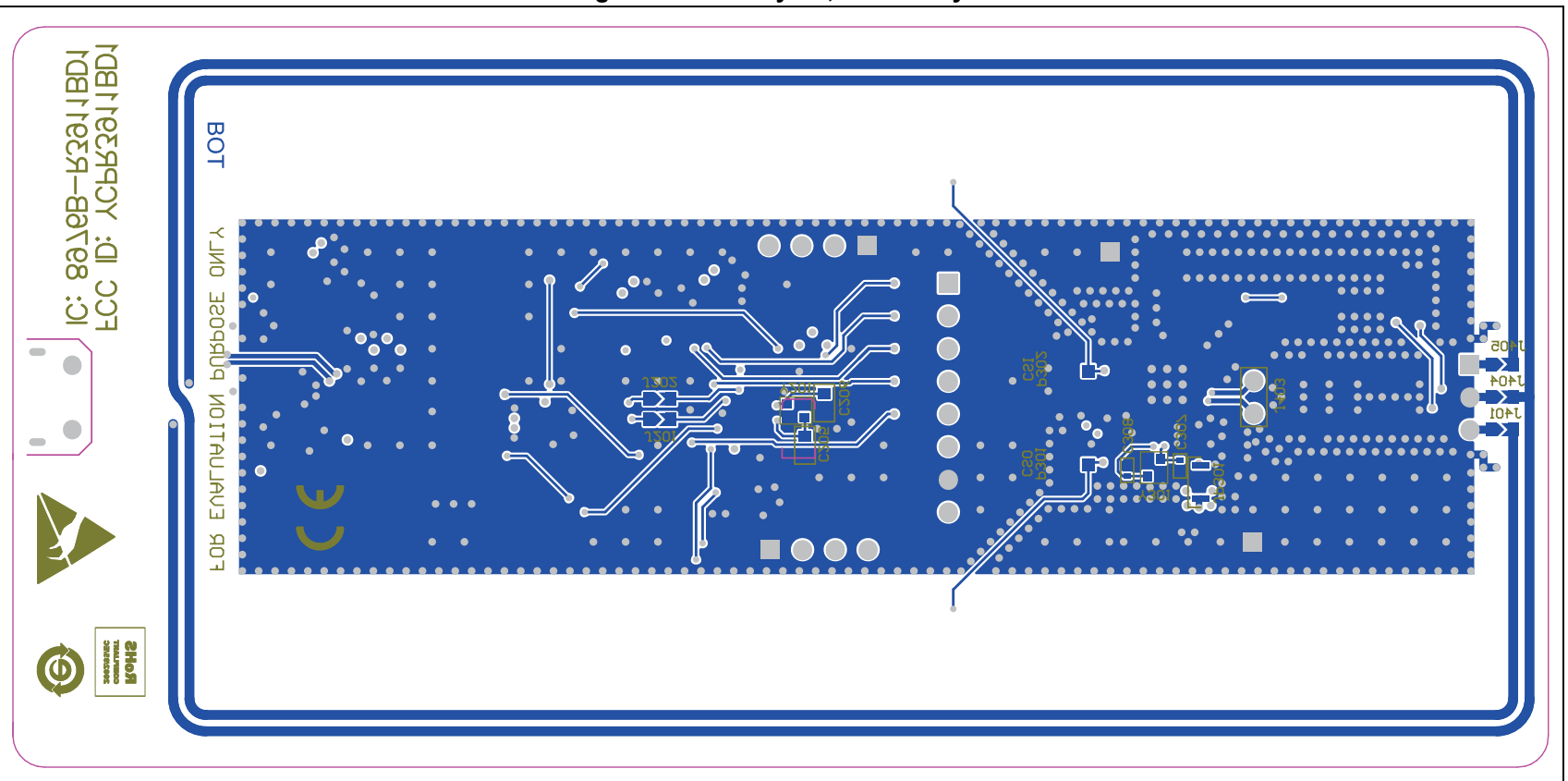


Figure 12. PCB layout, bottom layer



### 3 Antenna matching

The default matching network assembled enables VHBR operation up to 3.4 Mbps.

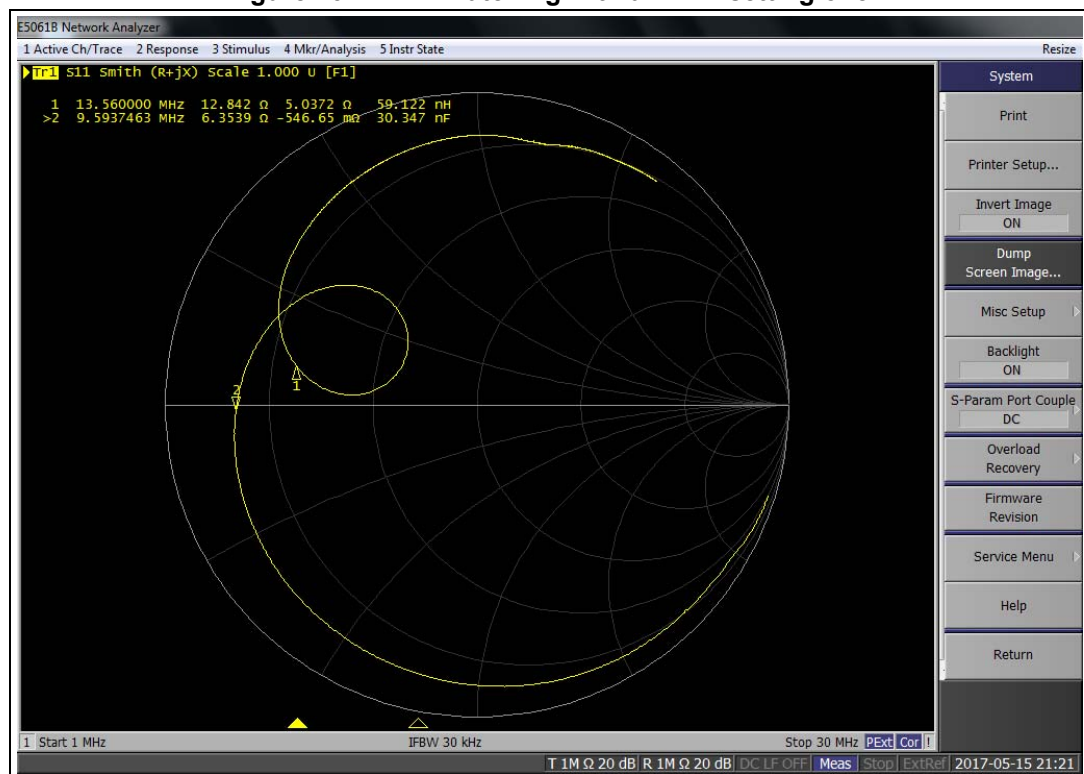
Components for an optional NFC Forum matching are placed on the board. Exchanging the components as indicated in [Table 1](#) will increase the Q factor of the antenna system. VHBR communication at 3.4 Mbps and 1.7 Mbps bit rate will not be supported anymore, but the read range for lower data rate applications will increase, up to 20%.

The matching impedance will remain the same when switching between the two matchings.

#### VHBR matching

The VHBR matching is designed with a target Q-Factor of 8. The matching impedance is around  $12.8 + j5 \Omega$ . The HW based AAT algorithm will typically adjust to an AAT value of 8 (see [Figure 13](#)).

Figure 13. VHBR matching with an AAT setting of 8



#### NFC Forum matching

The NFC Forum matching is designed with a target Q-Factor of 16.

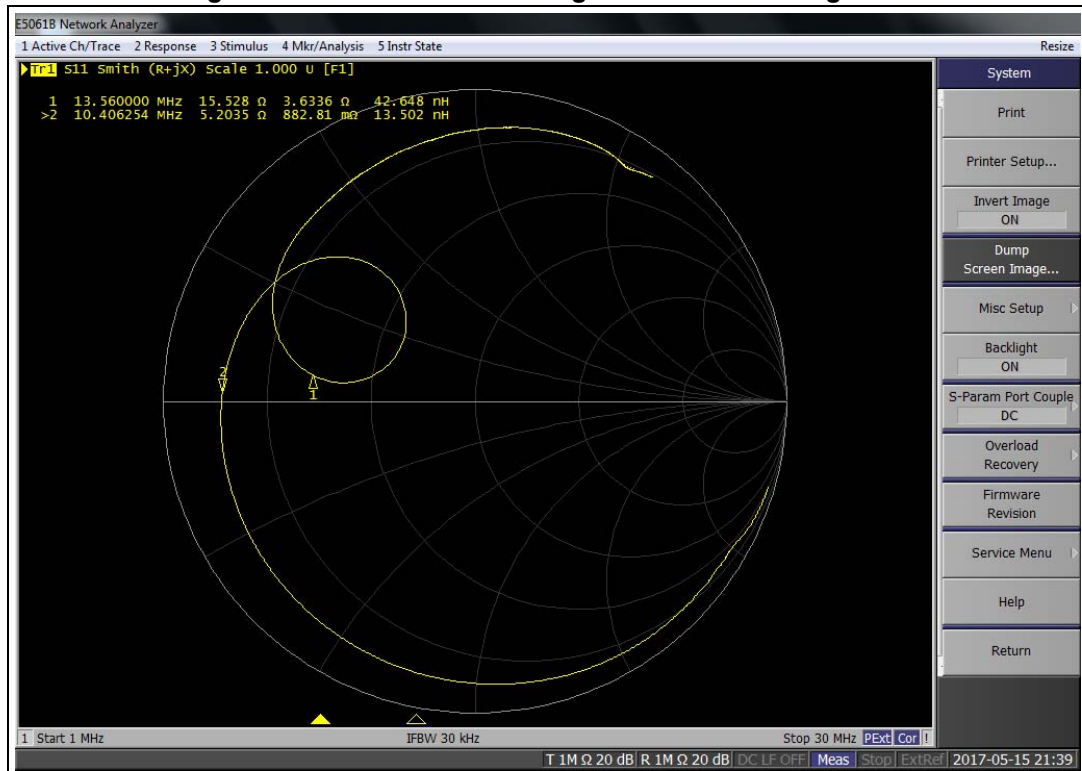
To switch to the NFC Forum matching the user needs to change the components listed in [Table 1](#).

Table 1. NFC Forum matching alternatives

Default assembly	Value	NFC Forum replacement	Value
C403	80 pF	C403_NFCF	120 pF
C410	180 pF	C410_NFCF	120 pF
R401	3R9	R401_NFCF	1R96
R402	3R9	R402_NFCF	1R96

With the new assembled values, the matching impedance looks as in [Figure 14](#), with a value close to  $11 + j6 \Omega$ .

Figure 14. NFC Forum matching with an AAT setting of 11



The HW based AAT algorithm will typically adjust to an AAT value of 11. Due to the higher Q-Factor the voltage on the antenna is also increasing. To put the receiver in an optimum signal level range, the capacitors C401 and C412 can be increased to 100 pF.

## **4 Federal Communications Commission (FCC) and Industry Canada (IC) compliance statements**

### **4.1 FCC Compliance Statement**

#### **4.1.1 Part 15.19**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

#### **4.1.2 Part 15.21**

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

#### **4.1.3 Part 15.105**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/ TV technician for help.

#### **4.1.4 FCC ID**

FCC ID: YCPR3911BD1

### **4.2 Formal notices required by the Industry Canada ("IC")**

#### **4.2.1 Compliance Statement**

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation.

#### **4.2.2 Declaration de Conformité**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **4.2.3 IC ID**

IC ID: 8976B-R3911BD1

## 5 Revision history

**Table 2. Document revision history**

Date	Revision	Changes
23-Jun-2017	1	Initial release.
25-Jul-2017	2	Added <a href="#">Section 4.1.3: Part 15.105</a> . Updated <a href="#">Section 4.1.4: FCC ID</a> and <a href="#">Section 4.2.3: IC ID</a> . Updated <a href="#">Figure 8: PCB overview</a> , <a href="#">Figure 9: PCB layout, top layer</a> and <a href="#">Figure 12: PCB layout, bottom layer</a> .
15-Dec-2017	3	Updated <a href="#">Figure 1: ST25R3911B-DISCO PCB (top view)</a> . Updated <a href="#">Section 2: Hardware</a> .



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