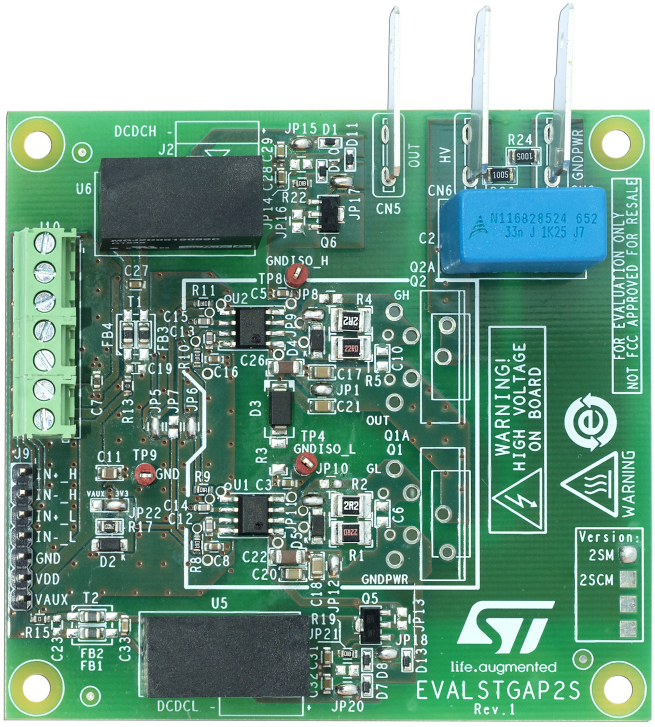
EVALSTGAP2S: isolated 4 A single gate driver demonstration board

Introduction

The EVALSTGAP2S board allows evaluating all the STGAP2S features while driving a half-bridge power stage with voltage rating up to 1700 V in TO-220 or TO-247 package.

The board allows to easily select and modify the values of relevant external components in order to facilitate driver's performance evaluation under different applicative conditions and fine pre-tuning of the final application's components.

Figure 1. EVALSTGAP2S demonstration board



1 Board description and configuration

The board allows tuning several design parameters, giving the possibility to evaluate and optimize the performance and switching characteristics of the power stage.

The user can select and mount the power switch of choice either in TO-220 or TO-247 package; the board also allows installing an optional heatsink.

The demonstration board can be populated with isolated DC-DC converters in the standard SIP7 package to supply the gate driving section, which significantly reduce the effort to supply the system and allow fast and easy evaluation of the gate driving performances.

The board is compatible with the whole STGAP2S family in SO-8 package, so it is possible to evaluate the part number of interest just by replacing the gate driver.

Figure 2 shows the position of the main components and connectors on the board.

Figure 2. Main components and connectors position

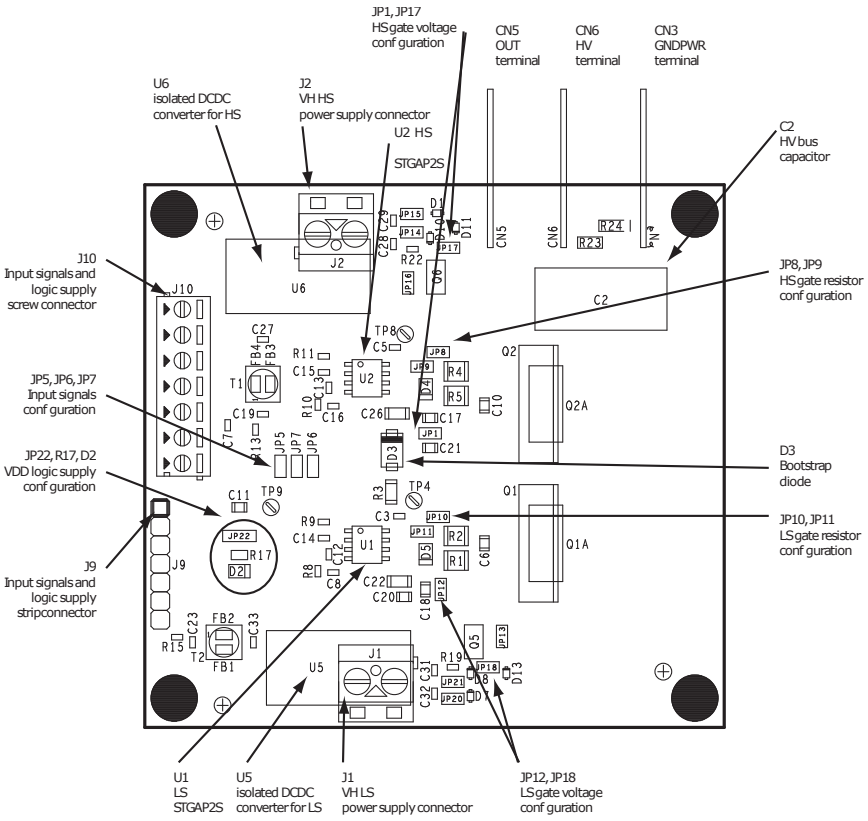


Table 1. Board connectors

Name	Pin	Label	Description
J1	1 - 2	DCDCL	Low-side VH supply voltage
J2	1 - 2	DCDCH	High-side VH supply voltage
J9 J10	1	IN+_H	High-side driver logic input, active high
	2	IN-_H	High-side driver logic input, active low
	3	IN+_L	Low-side driver logic input, active high
	4	IN-_L	Low-side driver logic input, active low
	5	GND	Logic ground
	6	VDD	Logic supply voltage
	7	AUX	Auxiliary power supply
CN3	1	GNDPWR	Power ground
CN5	1	OUT	Power stage output
CN6	1	HV	High voltage power supply

Table 2. Board jumpers setting

Jumper	Permitted configurations	Default condition
JP1	HS gate voltage configuration: selection of negative voltage (refer to Table 5)	Closed
JP5	Input signals configuration: IN-_L connected to IN+_H	Closed
JP6	Input signals configuration: IN+_L connected to IN-_H	Closed
JP7	Input signals configuration: IN-_L connected to IN-_H	Open
JP8	HS gate resistor configuration: connection of CLAMP pin to power gate	Open in EVALSTGAP2SM Closed in EVALSTGAP2SCM
JP9	HS gate resistor configuration: connection of GOFF pin to turn-off gate path	Closed in EVALSTGAP2SM Open in EVALSTGAP2SCM
JP10	LS gate resistor configuration: connection of CLAMP pin to power gate	Open in EVALSTGAP2SM Closed in EVALSTGAP2SCM
JP11	LS gate resistor configuration: connection of GOFF pin to turn-off gate path	Closed in EVALSTGAP2SM Open in EVALSTGAP2SCM
JP12	LS gate voltage configuration: selection of negative voltage (refer to Table 5)	Closed
JP13	LS gate voltage configuration: direct connection of DCDCL+ to VH_L net	Open
JP14	HS gate voltage configuration: connection of DCDCH 0V output reference to OUT net	Open
JP15	HS gate voltage configuration: connection of DCDCH- to GNDISO_H net	Closed
JP16	HS gate voltage configuration: direct connection of DCDCH+ to VH_H net	Open
JP17	HS gate voltage configuration: selection of positive voltage (refer to Table 5)	Closed
JP18	LS gate voltage configuration: selection of positive voltage (refer to Table 5)	Closed
JP20	LS gate voltage configuration: connection of DCDCL- to GNDISO_L net	Closed
JP21	LS gate voltage configuration: connection of DCDCL 0V output reference to GNDPWR net	Open
JP22	VDD logic supply configuration (refer to Table 3)	Closed 2-3

1.1 Logic supply voltage (VDD)

It is possible to provide the gate driver control logic supply VDD in three alternative ways to match driver input threshold with the controlling signals voltage swing:

- Using the onboard 3.3 V Zener D2 regulator to supply VDD. The Zener is supplied from DC-DC input voltage VAUX. So only the 5 V VAUX DC-DC supply input is powered to supply the whole system (default configuration).
- Supplying externally VDD net from J9 or J10 (pin 6) with a voltage between 3 V and 5.5 V.
- Supplying externally VDD and VAUX together (VDD max. 5.5 V).

In case the default option is not used, it is required to modify JP22 according to Table 3 and R17 according to Table 4 also to avoid regulator components damage.

Table 3. Logic supply voltage selection (VDD)

VDD	JP22	Note
3.3 V, onboard (default)	2-3 closed	VDD generated from VAUX with Zener diode D2
3.3 V, external	Open	VDD directly supplied from J9 or J10 (pin 6)
VDD = VAUX, external	1-2 closed	VDD and VAUX (DC-DC supply) tied together by JP22

The R17 resistor value has been selected for using 5 V input DC-DC module. If a different VAUX input voltage is used, follow Table 4 to modify resistor R17 (which biases Zener D2) to avoid resistor overheating.

Table 4. R17 value selection with a 3.3 V Zener diode D2 regulator

DCDC module supply input voltage VAUX	R17	JP22
3.3 V	Do not care	1-2 closed
5 V (default)	240 Ω	2-3 closed or JP22 open
12 V	1200 Ω	2-3 closed or JP22 open
15 V	1500 Ω	2-3 closed or JP22 open
24 V	2700 Ω	2-3 closed or JP22 open

1.2 Gate driver supply voltage (VH)

It is possible to provide the gate driver supply voltage VH in several alternative ways:

- Using isolated DC-DC converters in the standard SIP7 package (U5, U6).
- Using the bootstrap diode D3 by supplying the low-side driver via J1 and mounting the resistor R3 (initial suggested value 10 Ω).
- Supplying directly J1 and J2 connectors (not mounted) with two separated isolated supplies.

The faster, easier and safer way to supply the board is by using isolated DC-DC converters.

The bootstrap diode supplying method is much simpler and less expensive but does not allow evaluating negative gate driving voltage. The bootstrap diode is 1200 V rated; if a higher bus voltage is required the diode must be replaced accordingly.

Supplying externally via J1 and J2 is generally not recommended, unless using supplies specifically designed for this purpose (with high voltage isolation) or batteries.

Supplies provided from the optional DC-DC or from J1 and J2 connectors are post regulated in order to allow an easy modification of the gate driving voltages. Some predefined supply voltages can be selected through solder jumpers; further tuning can be made by changing the value of the relevant Zener diodes.

Table 5. Gate driving voltage configuration (positive/negative)

Gate driving voltage	JP1, JP12	JP17, JP18	Most suited for:
+15 V / 0 V (default)	Closed	Closed	MOSFET/ IGBT
+15 V / -2.7 V	Open	Closed	MOSFET/ IGBT
+19 V / 0 V	Closed	Open	SiC
+19 V / -2.7 V	Open	Open	SiC

The board has been designed for indifferently using 5 V input and 24 V single output or “12 + 12 V” dual output DC-DCs.

Other output voltage DC-DCs can be used by modifying the post regulation network.

Other input voltage DC-DCs can be used by modifying R17 (see Section: Logic supply voltage (VDD)).

DC-DCs input voltage is connected to VAUX signal, available on J9 and J10.

DC-DCs with SIP7 footprint are available mostly with 1 W and 2 W output rated power. For most applications, 1 W power modules are enough.

Especially for high dV/dt applications, low input to output isolation capacitance (referred to as input to output coupling capacitance) regulators are recommended.

During applicative output transients (dV/dt), the possible noise generated by the isolation capacitance could make user measurements difficult and noisy. To simplify user measurements task, DC-DC input supply is filtered with FB1 FB2, FB3 and FB4 ferrite beads. In the final application, beads are usually removed for cost reasons. On the other hand, if the user wants to further improve the filter, we suggest replacing the beads with a common mode filter (T1 and T2), like for instance TDK ACM4520-142.

1.3 Drivers logic input signals

Drivers logic input signals can be applied through the dedicated pins of J9 or J10 connector (refer to Table 1 for details).

It is possible to reduce the required driving signals exploiting the onboard jumpers according to Table 6.

Table 6. Input signals settings

Input configuration	Description	Jumper	Default condition
IN+_H = IN-_L	The same input signal is applied to IN+ of high-side driver U2 and IN- of low-side driver U1	JP5	Closed
IN+_L = IN-_H	The same input signal is applied to IN- of high-side driver U2 and IN+ of low-side driver U1	JP6	Closed
IN-_L = IN-_H	The same input signal is applied to IN- of high-side driver U2 and IN- of low-side driver U1	JP7	Open

1.4 Drivers gate resistors

The gate resistors are selected based on the selected power switch and application topology.

It is possible to evaluate different gate drivers of the STGAP2S family by setting few jumpers according to Table 7.

Table 7. Gate driver resistors and jumper settings

Gate driver	Feature	JP8, JP10	JP9, JP11	Turn-on resistor	Turn-off resistor
STGAP2SM (1)	Separated outputs	Open	Closed	R5, R1	R4, R2
STGAP2SCM (2)	Miller Clamp	Closed	Open	R5, R1	R5 // R4 R1 // R2

1. • *The presence of D4 and D5 does not influence turn-off speed and these diodes are not required in the final application. D4 and D5 are mounted on board to speed-up evaluation of STGAP2SC (Miller Clamp version).*
2. • *R4, D4, R2 and D5 are only required if differentiated turn-on and turn-off speed are required by the user.*

1.5 Power stage decoupling

As for all switching applications, high voltage supply is properly decoupled and appropriate decoupling capacitor is connected to the board to reduce bus ringing and power switch overvoltage spikes during operation.

The board is equipped with a small 1.25 kV DC rated film capacitor (C2) in a convenient position to operate more safely the power switches. Depending on the application, bus decoupling can be modified also by using the provided footprint and holes for the bus capacitors C1, C2, C34, C35, C36.

IMPORTANT NOTE: DANGER OF DEATH!

High voltage present on the board! Before operating on the board, ensure that all capacitors are discharged.

Revision history

Table 8. **Document revision history**

Date	Version	Changes
29-Oct-2020	1	Initial release.

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