Evaluation board with STM32G0C1VE MCU

Introduction

The STM32G0C1E-EV Evaluation board is a high-end development platform for the STM32G0C1VET6 microcontroller operating at up to 64 MHz frequency with internal 512-Kbyte Flash memory, 144-Kbyte RAM, USB 2.0 FS device and host, two CAN FDs, USB Type-C®, and Power Delivery controller interfaces (UCPD) compliant with USB Type-C® r1.2 and USB PD specification r3.0, three I^2Cs, three SPIs, six USARTs, two low-power UARTs, one 12-bit ADC, two 12-bit DACs, three general-purpose comparators, seven general-purpose timers, two low-power timers, HDMI CEC, and SWD debugging support.

The full range of hardware features on the STM32G0C1E-EV Evaluation board includes the mother board, the legacy peripheral daughterboard, and the USB-C® and Power Delivery daughterboard, which help to develop applications, and evaluate all peripherals, such as USB Type-C® connector with USB PD, motor control connector, CAN FD, USB 2.0 FS, RS-232, RS-485, audio DAC, microphone ADC, TFT LCD, IrDA, IR LED, IR receiver, LDR, microSD™ card, CEC on two HDMI connectors, Smartcard slot, RF EEPROM, and temperature sensor.

The board integrates an ST-LINK/V2-1 as an embedded in-circuit debugger and programmer for the STM32 MCU.

The daughterboard and extension connectors provide an easy way to connect a daughterboard or wrapping board for the user's specific application.

The USB-C® and Power Delivery daughterboard features two independent USB-C® ports controlled by STM32G0. USB-C® port 1 is a dual role power (DRP) port and can provide up to 45 W of power. USB-C® port 2 is a sink port only. Both support the USB PD protocol and the alternate mode functionality.

Application firmware examples are provided to evaluate USB-C® technology through various use cases.

Figure 1. STM32G0C1E-EV Evaluation board with legacy peripheral daughterboard

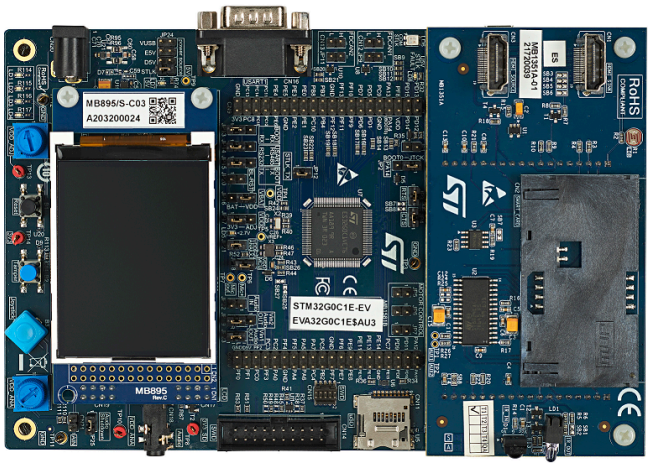
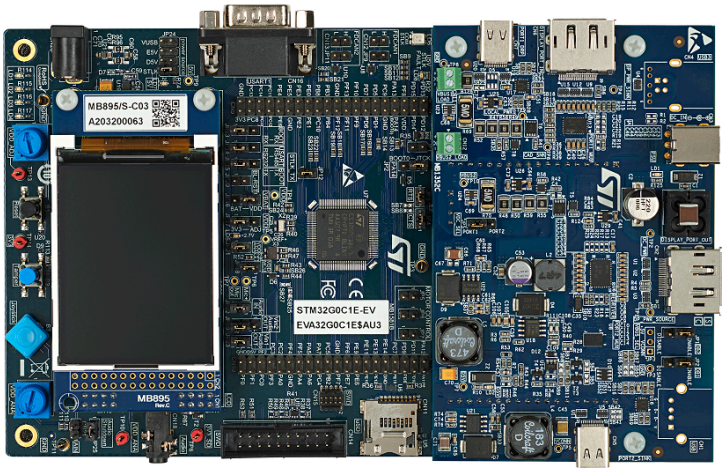


Figure 2. STM32G0C1E-EV Evaluation board with USB-C® daughterboard



Pictures are not contractual.

1 Features

Mother board

- STM32G0C1VET6 Arm® Cortex®-M0+ core-based microcontroller with 512 Kbytes of Flash memory and 144 Kbytes of RAM in LQFP100 package
- MCU voltage choice fixed at 3.3 V or adjustable from 1.65 V to 3.5 V
- I²C compatible serial interface
- RTC with backup battery
- 8-Gbyte or more SPI interface microSD™ card
- Potentiometer
- 4 color user LEDs and one LED as MCU low-power alarm
- Reset, Tamper, and User buttons
- 4-direction joystick with selection button
- Board connectors:
  - 5 V power jack
  - RS-232 and RS485 communications
  - CAN FD
  - Stereo audio jack including analog microphone input
  - microSD™ card
  - Extension I²C connector
  - Motor-control connector
  - Daughterboard connectors for legacy peripheral daughterboard or USB-C® and Power Delivery daughterboard
  - Extension connectors for daughterboard or wire-wrap board
- Flexible power-supply options:
  - 5 V power jack
  - ST-LINK/V2-1 USB connector
  - Daughterboard
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: Virtual COM port and debug port
- Comprehensive free software libraries and examples available with the STM32CubeG0 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

Legacy peripheral daughterboard

- IrDA transceiver
- IR LED and IR receiver
- Light-dependent resistor (LDR)
- Temperature Sensor
- Board connectors:
  - Two HDMI connectors with DDC and CEC
  - Smartcard slot

USB-C® and Power Delivery daughterboard

- Multiplexor for first-generation USB 3.1 Type-B receptacle / DisplayPort™ input and USB Type-C® port 1 output
- Multiplexor for USB Type-C® port 2 input and DisplayPort™ output / USB 2.0 Type-A receptacle
- VCONN on USB Type-C® port 1

- USB PD on USB Type-C® port 1
- Board connectors:
  - USB Type-C® port 1 DRP (dual-role port) and USB 2.0 FS data
  - USB Type-C® port 2 sink
  - DisplayPort™ input
  - DisplayPort™ output
  - First-generation USB 3.1 Type-B receptacle, not installed by default
  - USB 2.0 Type-A receptacle, not installed by default
  - 19 V power jack for USB PD

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the STM32G0C1E-EV Evaluation board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board reference	Target STM32
STM32G0C1E-EV	• MB1581: mother board • MB1351: legacy peripheral daughterboard • MB1352: USB-C® daughterboard • MB895: LCD daughterboard	STM32G0C1VET6U

2.1 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

STM32XXYYT-EV	Description	Example: STM32G0C1E-EV
XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32G0 Series
YY	MCU product line in the series	STM32G0C1
T	STM32 Flash memory size • E for 512 Kbytes	512 Kbytes
EV	Evaluation board	Evaluation board

3 Development environment

3.1 System requirements

- Windows® OS (7, 8, or 10), Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

Note: macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.
All other trademarks are the property of their respective owners.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1) (2)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*
2. *Free MDK-ARM for Arm® Cortex®-M0/M0+ cores.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered

5 Delivery recommendations

Some verifications are needed before using the board for the first time to make sure that nothing was damaged during shipment and that no components are unplugged or lost. When the board is extracted from its plastic bag, check that no component remains in the bag. Before starting the demo, take the microSD™ card from the separated ESD bag and plug it in the CN11 connector, on the right side of the board.

Warning:

There is an explosion risk if the battery is replaced with an incorrect one. Make sure to dispose of used batteries according to the instructions.

6 Hardware layout and configuration

The hardware block diagram (Refer to Figure 3) illustrates the connections between the STM32G0C1VET6 microcontroller and the peripherals on the STM32 G0 Evaluation board (such as motor-control connector, CAN FDs, RS232, RS485, Audio DAC, microphone ADC, TFT LCD, IrDA, IR LED, IR receiver, LDR, microSD™ card, CEC on two HDMI connectors, Smartcard slot, Temperature sensor). Figure 4, Figure 5, and Figure 6 help the user to locate these features on the STM32G0C1E-EV Evaluation board.

Figure 3. Hardware block diagram

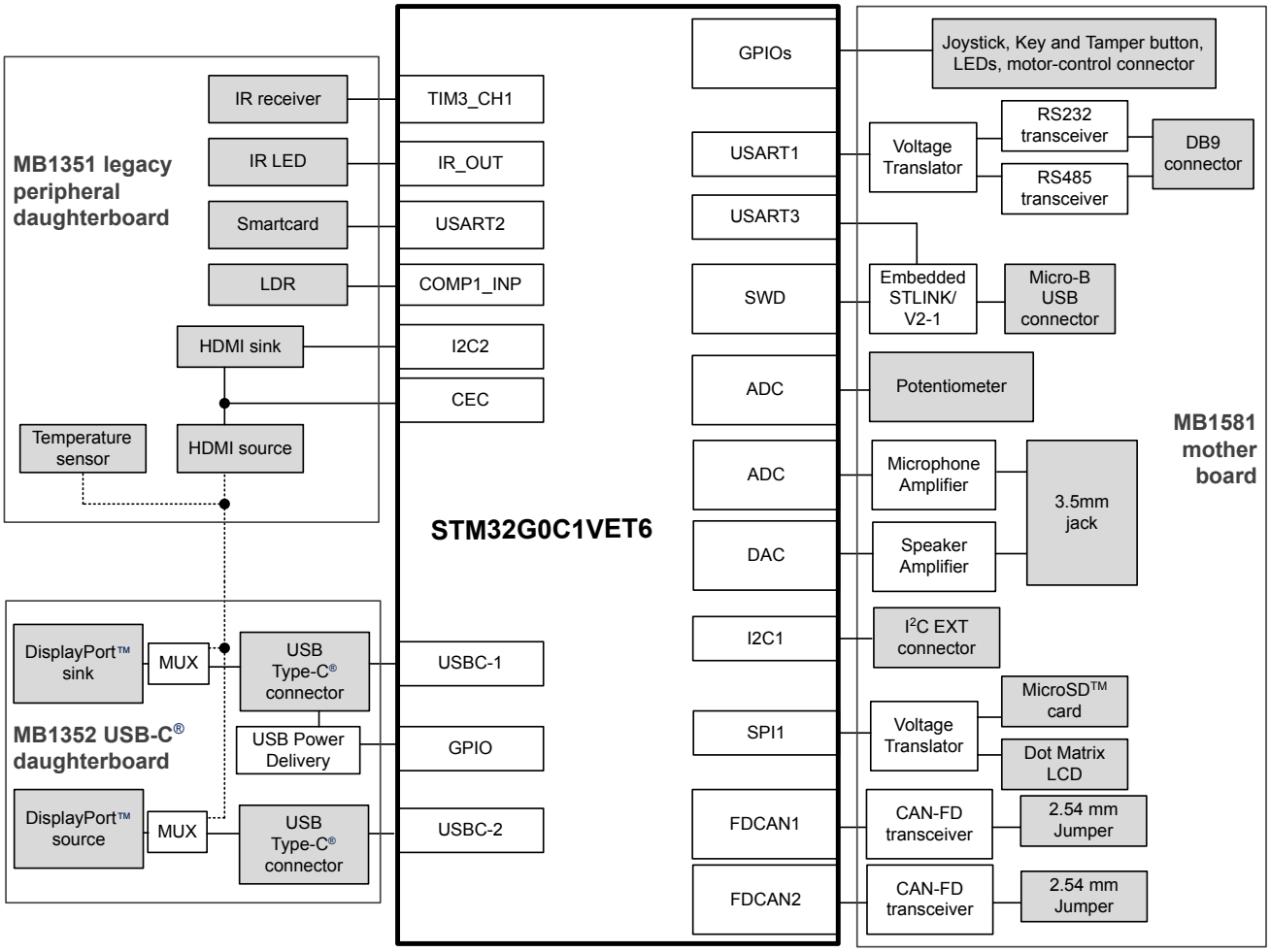


Figure 4. STM32G0C1E-EV Evaluation board layout (MB1581)

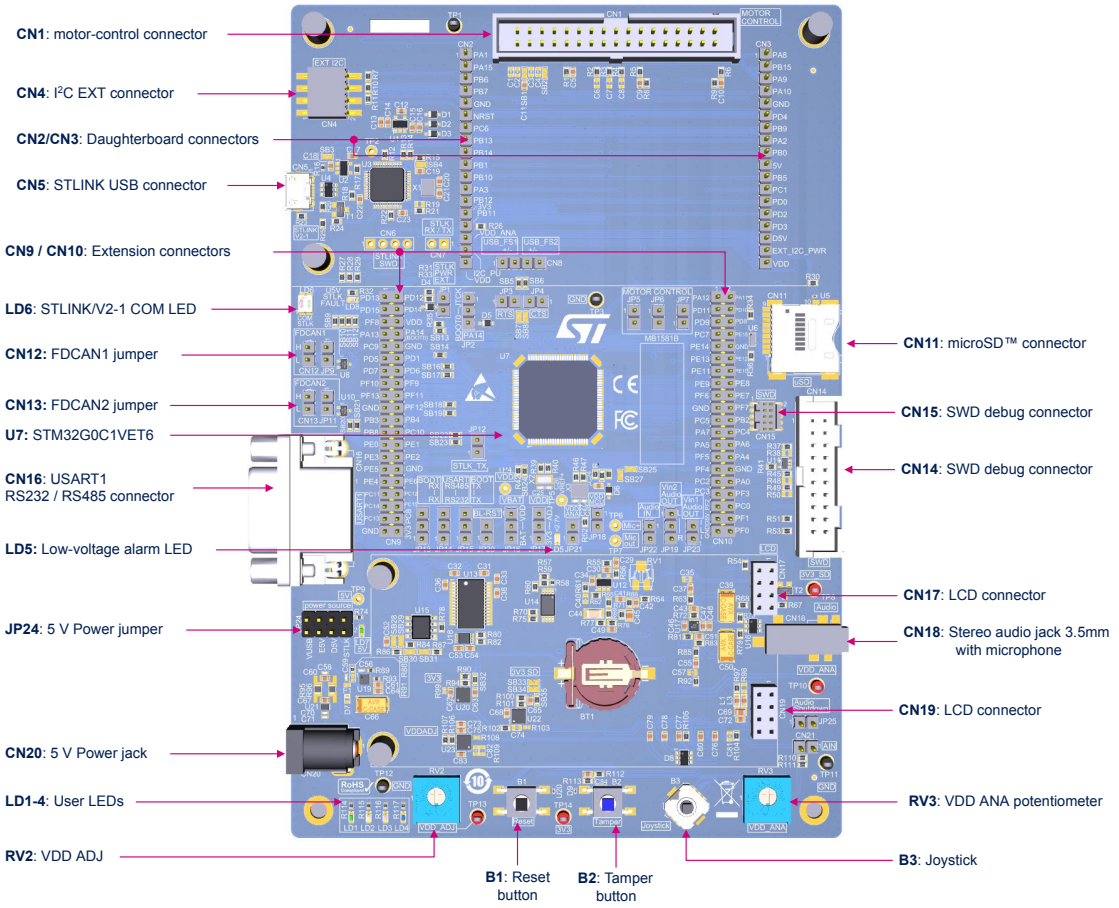


Figure 5. **Legacy peripheral daughterboard (MB1351)**

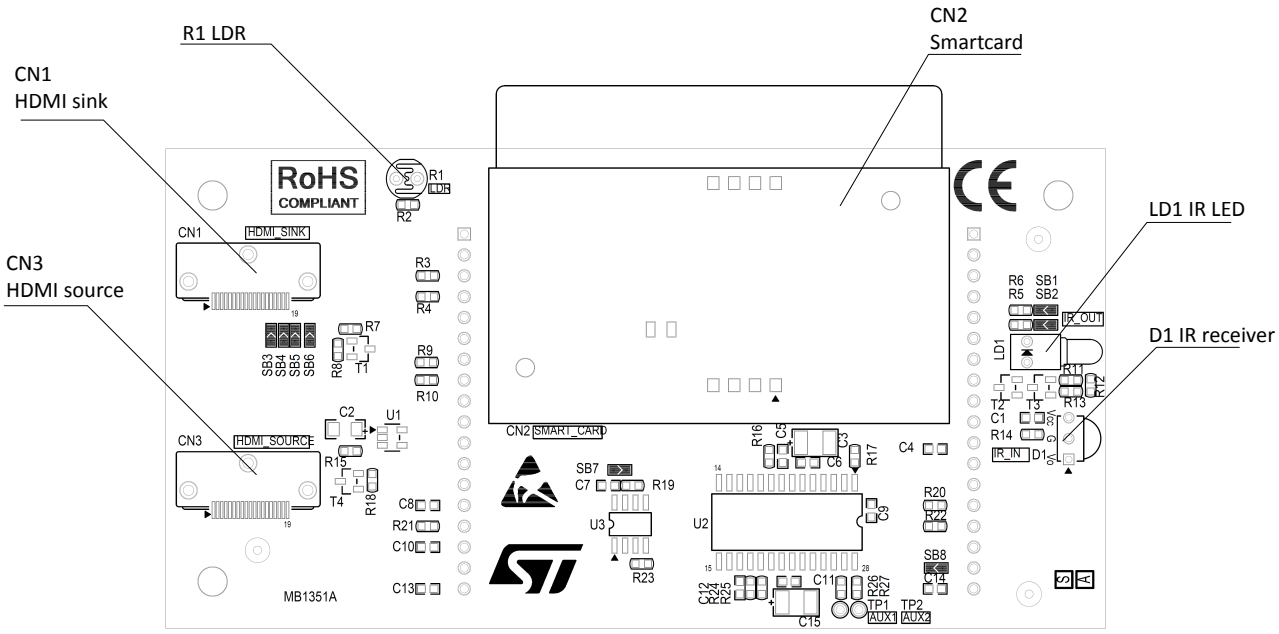
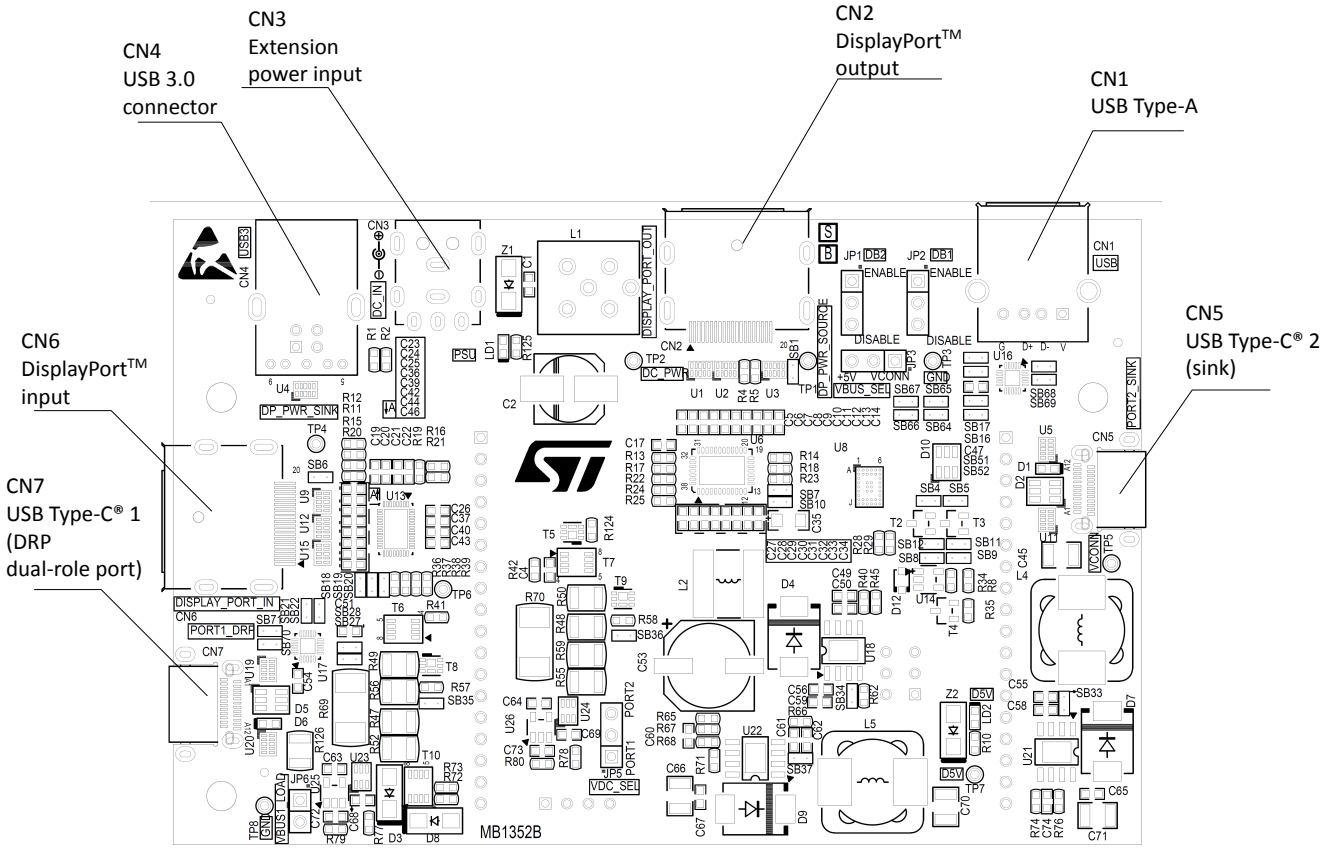


Figure 6. **UCPD daughterboard (MB1352)**



6.1 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 facility for debugging and flashing of STM32G0C1VET6 is integrated on the STM32G0C1E-EV Evaluation board.

Compared to the ST-LINK/V2 stand-alone tool available from STMicroelectronics, ST-LINK/V2-1 offers new features and drops some others.

New features:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB

This feature is no longer supported on ST-LINK/V2-1:

- SWIM interface

For full detail on both versions of the debugging and flashing tool, the stand-alone ST-LINK/V2 and the embedded ST-LINK/V2-1, refer to *ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32* user manual (UM1075).

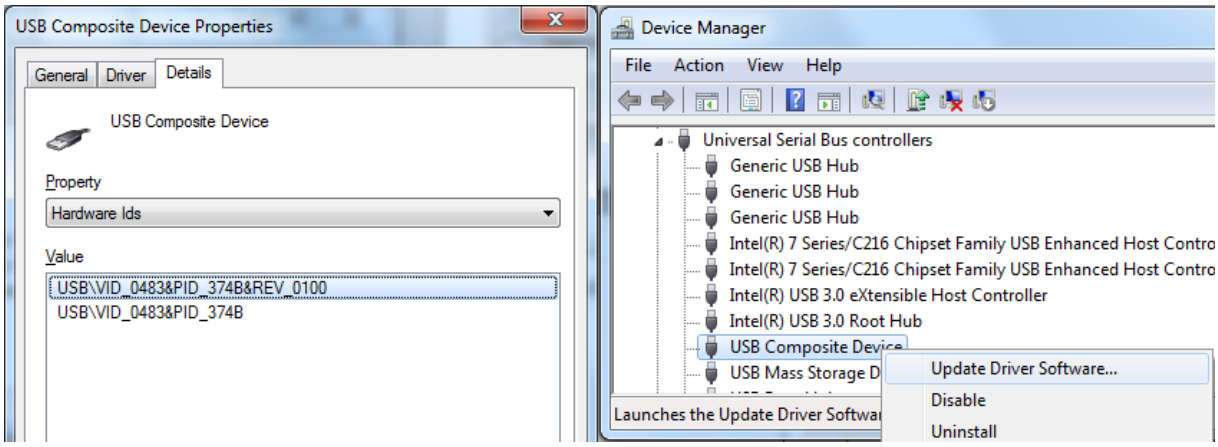
Note: It is possible to power the board via CN5 (Embedded ST-LINK/V2-1 USB connector) even if an external tool is connected to CN14 or CN15 (External SWD connector).

6.1.1 Drivers

Before connecting the STM32G0C1E-EV Evaluation board to a Windows® PC (7, 8, or 10) through a USB, a driver for the ST-LINK/V2-1 must be installed. It is available on the *www.st.com* website.

In case the STM32G0C1E-EV Evaluation board is connected to the PC before the driver is installed, some STM32G0C1E-EV interfaces may be declared as "unknown" in the PC device manager. To recover from this situation, the user must install the driver files, and update the driver of the connected device from the device manager (see).

Figure 7. USB composite device



6.1.2 ST-LINK/V2-1 firmware upgrade

For its operation, ST-LINK/V2-1 employs a dedicated MCU with Flash memory. Its firmware determines ST-LINK/V2-1 functionality and performance. The firmware may evolve during the life span of STM32G0C1E-EV Evaluation board to include new functionality, fix bugs, or support new target microcontroller families. It is therefore recommended to keep ST-LINK/V2-1 firmware up to date. The latest version is available from *www.st.com*.

6.2 Power supply

The STM32G0C1E-EV Evaluation board is designed to be powered by a 5 V DC power supply and is protected from the wrong power plug-in event.

Thanks to the JP24 jumper, it is possible to configure the mother board to use any of the following four sources for the power supply:

JP24 = E5V

5 V DC power adapter connected to CN20, the power jack on the board. The external power supply is provided to the board.

JP24 = STLK (Default configuration)

5 V DC power with 500 mA limitation from CN5, the USB Micro-B connector of ST-LINK/V2-1. If the USB enumeration succeeds, the ST-LINK PWR_EN pin is set to zero, which enables an STMPS2141STR power switch, thus providing 5 V power to the board. This power switch also features a current limitation to protect the PC in case of short-circuit on the board. If an overcurrent (more than 500 mA) happens on the board, the LD8 LED lights up.

JP24 = VUSB

5 V DC power from USB Micro-B connector of ST-LINK/V2-1, CN5 pin 1 (V_{BUS}) directly, without overcurrent protection

JP24 = D5V

5 V DC power from CN3 or CN10 connectors, the extension connectors for a daughterboard power source

The UCPD daughterboard uses its own 19 V power adapter to support USB PD. In this case, the mother board uses D5V from the UCPD daughterboard to supply all circuits on the STM32G0C1E-EV Evaluation board. D5V of the UCPD daughterboard has three sources as below:

- 19 V DC power adapter connected to MB1352_CN3 on the UCPD daughterboard
- Power from USB Type-C® port1 MB1352_CN7 on the UCPD daughterboard
- Power from USB Type-C® port2 MB1352_CN5 on the UCPD daughterboard

19 V DC power adapter and USB Type-C® port1 sources are automatically selected by a circuit (MB1352_D8 and MB1352_T10 on the UCPD daughterboard).

Caution: In case of development based on the boards, note that unexpected high voltage may appear in CN7 when plugging in 19 V power. So when using a 19 V power adaptor, apply default demonstration configuration with the boards, or refer to steps[1] in MB1352 schematic, and install protection on the software side[2].

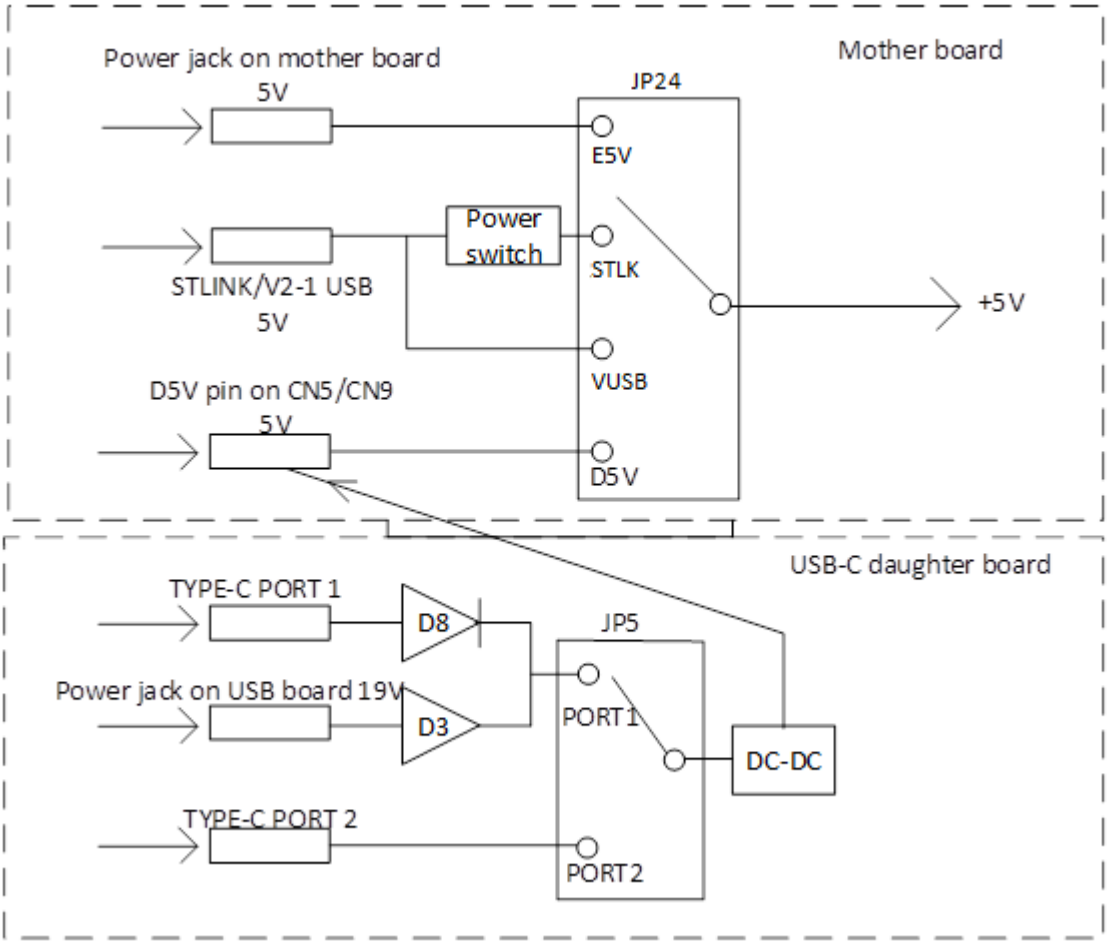
[1] Steps:

1. DCDC_EN detects its voltage to ensure PSU 19V exists.
2. PWM_CTL provides about 0.8 V level before DCDC_EN=1.
3. DCDC_EN=1, then PWM_CTL changes to provide PWM waveform by 0 and open-drain.

[2] Protection on the software side:

- Refer to `/* SAFETY PROTECTION CODE BEGIN */` section in `main.c` of USB_Host applications. This file can be found in STM32Cube_FW_G0_1.4.0 in STM32CubeMX.

Figure 8. **STM32G0C1E-EV 5 V power structure**



The STM32G0C1E-EV Evaluation board can be powered from the mother board's CN5 ST-LINK/V2-1 USB connector with a PC, but only the ST-LINK/V2-1 circuit has the power before USB enumeration because the host PC only provides 100 mA to the boards at that time. During the USB enumeration, the STM32G0C1E-EV Evaluation board requires 300 mA power from the host PC. If the host can provide the required power, the enumeration succeeds, the STMPS2141STR power switch U2 is switched ON, the green LED LD7 is turned ON, and thus the STM32G0C1E-EV Evaluation board is powered and can consume a maximum of 300 mA current. If the host PC is not able to provide the requested current, the enumeration fails. Therefore, the STM32 part including the extension board is not powered. As a consequence, the LD7 green LED remains turned OFF. In this case, it is mandatory to use an external power supply to supply extra power.

E5V (from PSU) or D5V can be used as an external power supply in case the current consumption of the STM32G0C1E-EV Evaluation board exceeds the allowed current on USB. In this condition, it is still possible to use USB for communication, for programming or debugging only, but it is mandatory to power the board first using E5V or D5V JP24 configuration, and then connecting the USB cable to the PC. Proceeding this way ensures that the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

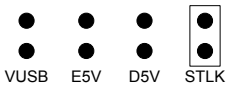
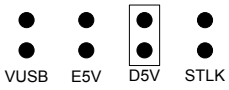
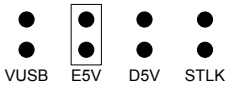
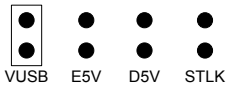
1. Connect the JP24 jumper in E5V or D5V configuration.
2. Check that JP1 is removed.
3. Connect the external power source to PSU or D5V (daughterboard mounted).
4. Check that the LD7 green LED is turned ON.
5. Connect the PC to the CN5 ST-LINK USB connector.

If this order is not respected, the board may be powered by V_{BUS} first then E5V or D5V, and the following risks may be encountered:

1. If more than 300 mA current is needed by the board, the PC may be damaged or the current can be limited by the PC. As a consequence, the board is not powered correctly.
2. 300 mA is requested at enumeration (since JP1 must be OFF), so there is a risk that the request is rejected and enumeration does not succeed if the PC cannot provide such current.
3. Consequently, the board is not powered (LD7 LED remains OFF).

In case the STM32G0C1E-EV Evaluation board is powered by a USB charger through CN5, there is no USB enumeration needed. The user can set JP24 to VUSB to allow the board to be powered anyway from CN5. The power source is selected by setting the JP24, JP16, and JP17 related jumpers as described in Table 4.

Table 4. Power source related jumpers

Jumper	Description[1]
JP24	**For 5 V power supply from USB (CN5) of ST-LINK/V2-1 through STMPS2141STR power switch (with OVC protection) to the STM32G0C1E-EV Evaluation board, JP24 is set as shown:** 
	For 5 V power supply from the daughterboard connectors (CN3 or CN10) to the STM32G0C1E-EV Evaluation board, JP24 is set as shown: 
	For 5 V power supply, from PSU jack (CN20) to the STM32G0C1E-EV Evaluation board, JP24 is set as shown: 
	For 5V power supply directly from CN5 V_{BUS} pin to the STM32G0C1E-EV Evaluation board without OVC protection, JP24 is set as shown: 
JP16	**The V_{BAT} pin of MCU is connected to VDD when JP16 is set as shown:** 
	The V_{BAT} pin of MCU is connected to a 3 V battery when JP16 is set as shown: 
JP17	**VDD is connected to +3.3 V when JP17 is set as shown:** 

Jumper	Description[1]
JP17	VDD is connected to VDD_ADJ when JP17 is set as shown: 

1. *The default setting is in bold.*

Note: The VDD_MCU Idd measurement can be done by the current meter that is mounted on JP18 when it is OFF. But JP18 must not be OFF without a current meter. Otherwise, MCU may be damaged due to the lack of power supply on its power pins.

Note: LD5 is lit when VDD < 2.7 V and in this case IOs and some Analog IPs of MCU work with degraded performances.

Note: The UCPD daughterboard works with VDD = 3.3 V, so it is mandatory to close JP17 pin1 and pin2. The LED LD7 is lit when the STM32G0C1E-EV Evaluation board is powered by the 5 V correctly. Table 5 shows the low-voltage limitations that may apply depending on the characteristics of some peripheral components. Components may work incorrectly when the power level is lower than the limitation.

Table 5. Low voltage limitation

Board	Peripheral	Component	I/O name	Low-voltage limitation
Mother board MB1581	Audio amplifier	U17	Audio output	2.2 V
Mother board MB1581	Microphone amplifier	U12	Audio input	2.7 V
Legacy daughterboardMB1351	Smartcard	MB1351_CN2	USART2	2.7 V

6.3 Clock references

Two clock sources are available on the STM32G0C1E-EV Evaluation board for STM32G0C1VE and its embedded RTC, and other clock sources for their peripherals.

- 32.768 kHz crystal X2 for embedded RTC
- 8 MHz crystal X3 for the STM32G0C1VE microcontroller. It can be disconnected by removing R46 and R47 when the internal RC clock is used.

Table 6. 32 KHz crystal X2 related solder bridges

Solder bridge	Description
SB53	**PC14 is connected to the 32KHz crystal when SB53 is OFF.**
	PC14 is connected to the CN9 extension connector when SB53 is ON. In such a case, R39 must be removed to avoid disturbance due to the 32 Khz quartz.
SB52	**PC15 is connected to the 32KHz crystal when SB52 is OFF.**
	PC15 is connected to the CN9 extension connector when SB52 is ON. In such a case, R40 must be removed to avoid disturbance due to the 32Khz quartz.

1. *The default setting is in bold.*

Table 7. 8 MHz crystal X3 related solder bridges

Solder bridge	Description
SB55	**PF0 is connected to an 8 MHz crystal when SB55 is OFF.**
	PF0 is connected to the CN10 extension connector when SB55 is ON. In such a case, R46 must be removed to avoid disturbance due to the 8 Mhz quartz.
SB54	**PF1 is connected to an 8 MHz crystal when SB54 is OFF.**
	PF1 is connected to the CN10 extension connector when SB54 is ON. In such a case, R47 must be removed to avoid disturbance due to the 8 Mhz quartz.

1. *The default setting is in bold.*

6.4 Reset sources

The general reset of the STM32G0C1E-EV Evaluation board is active LOW. The reset sources include:

- B1 Reset button
- Debugging tools from CN14 and CN15 SWD connectors
- Daughterboard on CN2
- Embedded ST-LINK/V2-1
- CN16 RS-232 connector for ISP

Note: The JP20 jumper must be ON for reset handled by pin8 of CN16 RS-232 connector (CTS signal).

6.5 Boot option

The STM32G0C1E-EV Evaluation board can boot from:

- Embedded user Flash memory
- System memory with boot loader for ISP
- Embedded SRAM for debugging

The boot option is configured by closing JP2 [2-3] and setting one jumper cap on CN9 among pin 6, pin 8, and pin 10 and one option bit. Refer to Table 8 and Table 9.

Table 8. Boot related jumper

Jumper configuration	Bit 25 in user option bytes	Boot from[1]
CN9 pins 8 and 10 closed by jumper	X	**STM32G0C1E-EV Evaluation board boot from user Flash**
CN9 pins 8 and 6 closed by jumper	0	STM32G0C1E-EV Evaluation board boot from embedded SRAM
CN10 pins 8 and 6 closed by jumper	1	STM32G0C1E-EV Evaluation board boot from system memory

1. *The default setting is in bold.*

Table 9. Boot0 related jumper

Solder bridge	Description[1]
JP2	**PA14-BOOT0 is used as SWCLK when JP2 is set as shown here.** 
	The Bootloader_BOOT0 is managed by pin 6 of the CN16 connector (RS-232 DSR signal) and it is connected to PA14-BOOT0 when JP2 is set as shown here. This configuration is used for boot loader application only. 

1. *The default setting is in bold.*

6.6 Peripherals on mother board (MB1581)

6.6.1 Audio

The STM32G0C1E-EV mother board (MB1581) supports stereo audio playback and microphone recording by an external headset connected to the CN18 audio jack. The audio play is connected to the DAC output of the MCU through an audio amplifier, and the microphone on the headset is connected to the ADC input of the MCU through a microphone amplifier. The audio amplifier can be enabled or disabled by the JP25 setting and mono/stereo playback can be chosen by the JP19 setting. Refer to Table 10 for detail.

Table 10. Audio related jumpers

Jumper	Description(1)
JP25	**Speaker amplifier U17 is enabled when JP25 is ON.**
	Speaker amplifier U17 is disabled when JP25 is OFF.
JP23	**PA4 is connected to VIN1 of the audio amplifier when JP23 is ON.**
	PA4 is disconnected to VIN1 of the audio amplifier when JP23 is OFF.
JP19	Mono playback is enabled when JP19 is set as shown here: 
	Stereo playback is enabled when JP19 is set as shown here: 

1. *The default setting is in bold.*

The audio amplifier operates correctly when VDD is superior to 2.2 V and the microphone amplifier operates correctly when VDD is superior to 2.7 V

6.6.2 RS-232 and RS-485

Communication through RS-232 (With Hardware flow control CTS and RTS) and RS-485 are supported by the CN16 D-type 9-pins RS-232/RS-485 connector, which is connected to USART1 of MCU on the STM32G0C1E-EV Evaluation board. The Bootloader_RESET (shared with CTS signal) and Bootloader_BOOT0 (shared with DSR signal) signals are added to the CN16 RS-232 connector for ISP support.

By default, PC4 and PC5 are connected as TX and RX signals. PA9 and PA10 can also be connected as these two signals for bootloader which is NOT supported on PC4 and PC5 by the setting of jumpers in Table 11.

Table 11. **RS-232 and RS-485 related jumpers**

Jumper	Description[1]
JP14	**RS232_RX is connected to the RS232 transceiver and RS232 communication is enabled when JP14 is set as shown here:** 
	RS485_RX is connected to the RS485 transceiver and RS485 communication is enabled when JP14 is set as shown here: 
JP15	**PC4 is connected as a TX signal without bootloader being supported when JP15 is set as shown here:** 
	PA9 is connected as a TX signal with bootloader being supported when JP15 is set as shown here (The CN1 motor-control connector must be OFF in this case): 
JP13	**PC5 is connected as an RX signal without bootloader being supported when JP13 is set as shown here:** 
	PA10 is connected as an RX signal with bootloader being supported when JP13 is set as shown here (CN1 motor-control connector must be OFF in this case): 

1. *The default setting is in bold.*

The RS-485 communication is supported by the ST3485EBDR RS-485 transceiver which is connected to pin 4 and pin 9 of D-type 9-pins CN16 connector and shares the same connector with USART1.

Table 12. **RS-485 related jumpers**

Jumper	Description[1]
SB29, SB31	The external failsafe biasing is enabled when the SB29 and SB31solder bridges are ON.
	OFF
SB30	The bus termination is enabled when the solder bridge SB30 is ON.
	OFF
SB28	The AC termination is disabled when the solder bridge SB28 is ON for high baud-rate communication.
	OFF

1. *The default setting is in bold.*

6.6.3 microSD™ card

The 8-Gbyte (or more) microSD™ card connected to SPI1 port (Shared with color LCD) of MCU is available on the board. The microSD™ card detection is managed by standard I/O port PC9 and it must be set via internal pull-up.

6.6.4 Analog input

The CN21 two-pin header and RV3 10 KΩ potentiometer are connected to PB2 of MCU as analog input. A low-pass filter can be implemented by replacing R104 and C81 with the right value of resistor and capacitor as requested by the end user's application.

6.6.5 External I²C connector

The I2C1 bus of the MCU is connected to CN4 on the STM32G0C1E-EV Evaluation board. The I²C functional daughterboard can be mounted on the CN4 connector and accessed by the microcontroller through the I2C1 bus. It shares the same I2C1 bus with the U3 temperature sensor and DDC on the MB1351_CN3 HDMI_Source connector on the legacy peripheral daughterboard.

The pull-up voltage level of the I2C1 bus is automatically decided by the daughterboard (the legacy peripheral daughterboard or the UCPD daughterboard) on CN2 and CN3. If there is no daughterboard on these connectors, pin 17 and pin 18 must be shortened on CN2 and CN3 by jumpers. Thus I²C and reset pull-up voltages on CN4 are the voltage of VDD.

6.6.6 Motor control

The STM32G0C1E-EV Evaluation board supports both asynchronous and synchronous three-phase brushless motor control via the CN1 34-pins connector, which provides all required control and feedback signals to and from the motor power driving board. Available signals on this connector include emergency stop, motor speed, 3-phase motor current, bus voltage, power heatsink temperature coming from the motor driving board, and six channels of PWM control signal going to the motor driving circuit. The daughterboard on CN2 and CN3 must be removed and some jumpers set for motor-control application:

- JP5, JP6, and JP7 jumpers ON
- JP22 and JP19 jumpers OFF
- JP13[2-3] and JP15[2-3] jumpers OFF.

6.6.7 Display and input devices

The 2.4-inch color TFT LCD connected to the SPI1 port of MCU and four general-purpose color LEDs (LD1, LD2, LD3, and LD4) are available as display devices. The B3 4-direction joystick with selection key is connected to PA0 and supports the wake-up feature. The B2 Tamper button is also available as an input device.

Table 13. CN17/CN19 2.4-inch TFT-LCD connector

Pin	Description	Pin connection	Pin	Description	Pin connection
1	CS	PB8	9	VDD	3.3V
2	SCL	PB3	10	VCI	3.3V
3	SDI	PA7	11	GND	GND
4	RS	-	12	GND	GND
5	WR	-	13	BL_VDD	5V
6	RD	-	14	BL_Control	5V
7	SDO	PB4	15	BL_GND	GND
8	RESET	RESET#	16	BL_GND	GND

Note: The bi-directional voltage translator implemented on the SPI MOSI signal between MCU and LCD to support the 3-wire serial interface of the LCD panel only supports a 3-wire SPI port. The direction of this voltage translator is controlled by I/O PC12 (the IO PA7 is working as MOSI when PC12 is HIGH or as MISO when PC12 is LOW).

6.6.8 CAN FD

U26 and U27 CAN-FD transceivers are connected to STM32G0C1VET6U FDCAN1 and FDCAN2 TX/RX interfaces.

The other sides of the transceivers are connected to the CN12 and CN13 headers for the user to test these interfaces.

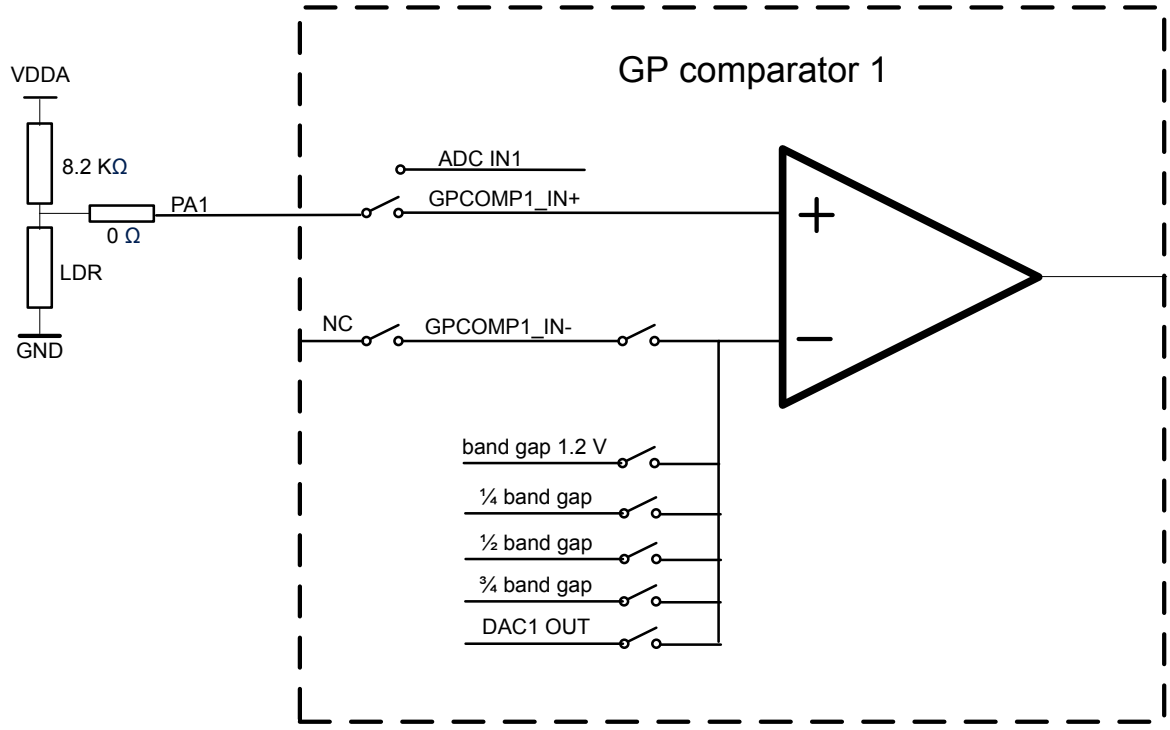
Caution: it is not recommended to use the CAN-FD interface when VDD is 1.8 V, as the VIO pin of both transceivers is connected to 3V3. This limitation is corrected with MB1581C.

6.7 Peripherals on the legacy peripheral daughterboard (MB1351)

6.7.1 LDR - Light-dependent resistor

The VDD is divided by the resistor bridge of LDR VT9ON1 and an 8.2 KΩ resistor and connected to PA1 (COM1_IN+/ADC IN1) as shown in Figure 9 on the STM32G0C1E-EV Evaluation board.

Figure 9. GP comparator 1



It is possible to compare LDR output with 1/4 band gap, 1/2 band gap, 3/4 band gap, band gap, and DAC1 OUT and to connect LDR output to ADC IN1 for AD conversion.

6.7.2 Temperature sensor

An STLM75M2F temperature sensor is connected to the I2C1 bus of MCU and shares the same I2C1 bus with EXT I^2C connector on the mother board and with DDC on the MB1351_CN3 HDMI_Source connector on the legacy daughterboard. I^2C temperature-sensor address is `0b100100(A0)`, `A0` can be 0 or 1, depending on the setting of MB1351_SB7.

Table 14. Temperature-sensor related solder bridge

Solder bridge	Description[1]
MB1351_SB7	**I²C address A0 is 0 when MB1351_SB7 is OFF.**
	I²C address A0 is 1 when MB1351_SB7 is ON.

1. *The default setting is in bold.*

Note: The temperature result measured from STLM75M2F may be a little higher than the ambient temperature due to the power dissipation of components on the board.

6.7.3 Smartcard

STMicroelectronics smartcard interface chip ST8024L is used on the STM32G0C1E-EV Evaluation board for asynchronous 1.8 V, 3 V, and 5 V smartcards. It performs all the supply protection and control functions based on the connections with MCU listed in Table 15.

Table 15. Connection between ST8024L and MCU

ST8024L signal	Description	MCU connection
5V/3V	Smartcard power supply selection pin	PB15
I/OUC	MCU data I/O line	PA2
XTAL1	Crystal or external clock input	PD4
OFF	Card presence detection, MCU interruption	PB12
RSTIN	Card Reset Input from MCU	PA15
CMDVCC	Start activation sequence input (Active LOW)	PB0
1.8V	1.8 V VCC operation selection. Logic high selects 1.8 V operation and overrides any setting on the 5V/3V pin.	PA3

The smartcard operates correctly when VDD is higher than 2.7 V.

6.7.4 HDMI-CEC

MB1351_CN1 and MB1351_CN3 HDMI connectors are available on the STM32G0C1E-EV legacy peripheral daughterboard.

1. The connector MB1351_CN1 is an HDMI sink connector with:
   - DDC connected to I2C2 of MCU
   - HPD controlled by PD2 I/O through MB1351_T1 transistor
   - CEC connected to PB10 through MB1351_T4 transistor
2. The connector MB1351_CN3 is an HDMI source connector with:
   - DDC connected to I2C1 of MCU and shared with the temperature sensor and EXT I²C connector
   - HPD controlled by PD3 I/O
   - CEC connected to PB10 through MB1351_T4 transistor
   - HDMI 5 V powered by the MB1351_U1 power switch

The signals TDMS D+[0..2], TDMS_CLK+, TDMS D-[0..2], and TDMS_CLK- on these two HDMI connectors are connected.

The CEC injector mode can be enabled by some PCB reworks for debugging purpose only:

- Remove MB1351 R3, R4, R7, R9, R10, R15, and R22 MB1351 resistors.
- Close SB3, SB4, SB5, and SB6 MB1351 solder bridges.

Note: The PD2 I/O must be set in open-drain output mode by firmware when working as an HPD signal control on the MB1351_CN1 HDMI sink connector.

6.7.5 IR LED and IR receiver

The TSOP34836 IR receiver is connected to MCU PC6 and current around 100mA on IR LED is driven by PB9 through MB1351_T2 and MB1351_T3 transistors on the board.

Note: The IR LED may be directly driven by PB9 with a 20 mA current when MB1351_SB1 is ON and MB1351_SB2 is OFF.

6.8 USB-C® and Power Delivery daughterboard (MB1352)

The MB1352 UCPD daughterboard is a development platform that can be used together with the MB1581 STM32G0C1E-EV Evaluation board. This daughterboard is used for demonstrating the functionalities of the USB Type-C® and USB Power Delivery (USB PD) technologies, facilitating the users to develop their solutions. Refer to Figure 3 for the daughterboard structure.

Note: The USB PD reference design on the UCPD daughterboard is used to demonstrate the capability of MCU. This USB PD circuit may not pass all USB PD certifications.

Note: UCPD daughterboard works with VDD at 3.3V. So JP17 [1-2] must be ON.

Note: UCPD daughterboard conflicts with the legacy peripheral daughterboard and motor control on the STM32G0C1E-EV Evaluation board

6.8.1 USB Type-C® receptacles

Two MB1352_CN7 and MB1352_CN5 USB Type-C® certified receptacles are present on the UCPD daughterboard, representing respectively port 1 and port 2. Port 1 can be used as DRP (dual-role port), which is eligible to supply another platform plugged by a USB Type-C® cable when they are configured as providers or, otherwise, to be supplied in case of consumer configuration. Port 2 can only be used as a sink.

Video signals on the MB1352_CN6 display port input connector and data signals on the MB1352_CN4 USB3.1 Gen1 Type-B connector are multiplexed on USB Type-C® port 1 thanks to a TUSB546-DCI crosspoint switch IC. These signals on MB1352_CN6 or MB1352_CN4 have to be generated by an external computer or notebook to evaluate the alternate mode (AM) capability of the USB PD technology. The crosspoint switch can be configured through the I^2C bus, and its I^2C address is `0b1000100`. The cable which is plugged into MB1352_CN4 can be detected by PA15.

Same as USB Type-C® port1, video signals on the MB1352_CN2 display port output connector are connected to USB Type-C® port 2 through another CBTL08GP053 crosspoint switch IC and an SN65DP141 DisplayPort™ Linear Redriver IC. The CBTL08GP053 I^2C address is `0b0110000` and the SN65DP141 I^2C default address is `0b0000000`. MB1352_CN1 USB Type-A receptacle D+ and D- signals are also directly connected to USB Type-C® port 2. Its V_{BUS} can be set by MB1352_JP3 as shown in Table 16.

Table 16. V_{BUS} related jumper

Jumper	Description(1)
MB1352_JP3	**V_{BUS} is connected to VCONN when MB1352_JP3 is set as shown here:** 
	V_{BUS} is connected to D5V through the mother board when MB1352_JP3 is set as shown here: 

1. *The default setting is in bold.*

Note: Some weak USB charger cannot provide power to board immediately from port1 USB Type-C® receptacle when the external 19 V power adaptor is plugged off. If the board loses power and resets during such a user case, closing MB1352_JP3 may help to solve this problem. MB1352_JP3 is OFF by default.

6.8.2 Power Delivery and local power management

The UCPD daughterboard has its external power jack (MB1352_CN3, 19 V/4 A input) to support the power delivery function and to provide up to 15 V/3 A on the MB1352_CN7 USB Type-C® port1.

Note: If the extension 19 V power adaptor of the UCPD daughterboard is used, the power supply source of the mother board must be set to D5V on JP24. Refer to Table 17 for the JP24 mother board setting selection.

The STM32G0C1E-EV Evaluation board can be powered by D5V from UCPD daughterboard as shown in Figure 8. D5V on the UCPD daughterboard can be generated by three resources, 19 V from the external power jack, V_{BUS} on port 1, or V_{BUS} on port 2. A circuit is implemented on the UCPD daughterboard to automatically select the external 19 V power supply or V_{BUS} on port1 because external 19 V and V_{BUS} on port 1 are the two power sources for port 1 to D5V. The MB1352_JP5 jumper is used to select D5V resources as shown in Table 17.

Table 17. Local power-related jumper

Jumper	Description(1)
MB1352_JP3	**D5V from UCPD daughterboard is generated from external 19 V or V_{BUS} on port 1 when MB1352_JP5 is set as shown here:** 
	D5V from UCPD daughterboard is generated from V_{BUS} on port 2 when MB1352_JP5 is set as shown here: 

1. *The default setting is in bold.*

6.8.3 V_{BUS} management and discharge mechanism

The MB1352_CN7 USB Type-C® port1 can be used as DRP (dual-role port). Its V_{BUS} can be managed for supplying other platforms as a provider or supplied as a consumer. The MB1352_T6 and MB1352_T7 MOSFETs are set in back-to-back configuration to protect and isolate the V_{BUS} supplying path in both directions.

If the MB1352_CN7 acts as a provider, the V_{BUS} is on the supply path by mean of the discrete load switch (MB1352_T6 and MB1352_T7) driven by the PD3 MCU GPIO. For the consumer case, the same V_{BUS} path is managed by MCU PD3 enabling the discrete load switch. All power profiles are listed in Table 18.

Table 18. V_{BUS} Power Delivery profiles

MB1352_CN7 role	MB1352 solder bridges setting	Power level	Source control signal	Voltage control signal
Provider	MB1352 SB2, SB3, SB23, SB26 ON SB13, SB14, SB15 OFF	PWM mode: PWM voltage-3A	PD3 High	PC1-PWM signal PA1-DCDC enable
	MB1352 SB13, SB14, SB15 ON SB2, SB3, SB23, SB26 OFF	GPIO mode: 5 V / 9 V / 15 V- 3 A	PD3 High	5 V: PC1 (VSOURCE - 9 V) and PA1 (VSOURCE - 15 V) tristate
				9 V: PC1 (VSOURCE - 9 V) low
				15V: PA1 (VSOURCE - 15 V) low
Consumer	-	Decided by the provider which is connected through USB Type-C® cable	PD3 low	-

Moreover, the V_{BUS} path on port 1 presents a discharge mechanism implemented by the T8 MOSFET and an RC filter controlled by PB13 and the V_{BUS} path on port 2 presents a discharge mechanism implemented by the T9 MOSFET and an RC filter controlled by PB14.

6.8.4 V_{BUS} voltage-sensing and current-sensing stages

Each USB Type-C® port is equipped with a voltage-sensing and current-sensing stages which are matched with the voltage sensing carried by the MCU ADC peripherals. Refer to Table 19 for details. They can monitor the right power level applied to the V_{BUS} port.

Table 19. Voltage-sensing and current-sensing ADCs

Port	Vsense ADC		Isense ADC	
Port 1	PB1	ADC_IN9	PB10	ADC_IN11
Port 2	PA3	ADC_IN3	PB12	ADC_IN16

6.8.5 CC management

Dead battery, VCONN output, and fast role swap functions are supported on the CC signal of USB Type-C® port 1.

1. Dead battery enable

The dead battery function is supported by MB1352_U17 and MB1352_U16 OVP chips. This function is also embedded in MCU. When the U17 OVP part is bypassed, the dead battery function in MCU can be enabled or disabled through enabling signals by setting MB1352_JP2 (CC1) or MB1352_JP1 (CC2). Refer to Table 20 for detail.

Table 20. Dead battery-related jumpers

Jumper	Description(1)
MB1352_JP1	**Embedded dead battery function is enabled when MB1352_JP1 is set as shown here:** 
	Embedded dead battery function is disabled when MB1352_JP1 is set as shown here: 
MB1352_JP2	**Embedded dead battery function is enabled when MB1352_JP2 is set as shown here:** 
	Embedded dead battery function is disabled when MB1352_JP2 is set as shown here: 

1. *The default setting is in bold.*

2. VCONN output control

When the full-featured cable is connected to port 1, the VCONN is directly managed by the MCU by mean of the PD4 or PB9, and the STMPS2161 MB1352_U10 and MB1352_U14 load switches.

3. Fast role swap

The USB Type-C® port 1 can be configured to action fast role swap managed by MCU through PA2 (CC1) and PB0 (CC2).

6.8.6 USB 2.0 FS host and device

Both USB Type-C® connectors are connected through MB1352_CN10 and MB1581_CN8 to MCU USB 2.0 FS interface through PA11 (DM) and PA12 (DP).

7 Connectors

7.1 Connectors on mother board (MB1581)

7.1.1 CN1 motor-control connector

Figure 10. **CN1 motor-control connector**

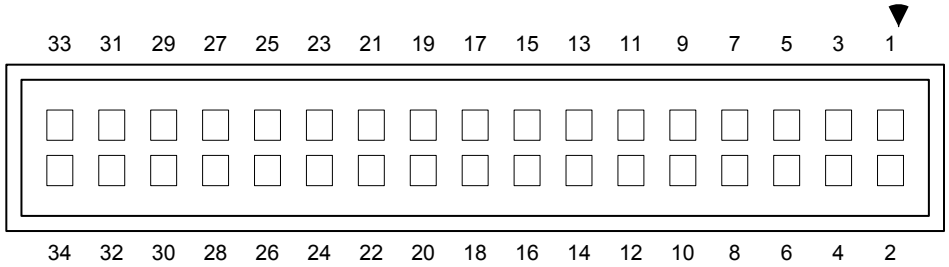


Table 21. **Voltage-sensing and current-sensing ADCs**

Description	MCU pin	CN1 pin number	CN1 pin number	MCU pin	Description
Emergency STOP	PB12	1	2	-	GND
PWM-UH	PA8	3	4	-	GND
PWM-UL	PD2	5	6	-	GND
PWM-VH	PA9	7	8	-	GND
PWM-VL	PD3	9	10	-	GND
PWM-WH	PA10	11	12	-	GND
PWM-WL	PD4	13	14	PA1	BUS VOLTAGE
PHASE A CURRENT	PA2	15	16	-	GND
PHASE B CURRENT	PA6	17	18	-	GND
PHASE C CURRENT	PB10	19	20	-	GND
NTC BYPASS RELAY	PB9	21	22	-	GND
DISSIPATIVE BRAKE PWM	PB15	23	24	-	GND
+5V power	-	25	26	PA3	Heatsink temperature
PFC SYNC2	PD0	27	28	-	3.3V power
PFC SYNC1	PC1				
PFC PWM	PB1	29	30	-	GND
Encoder A	PC6	31	32	-	GND
Encoder B	PB5	33	34	PB0	Encoder Index

7.1.2 CN4 external I²C connector

Figure 11. **CN4 external I²C connector**

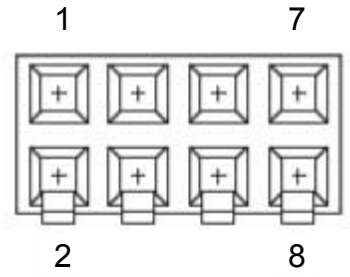


Table 22. **CN4 external I²C connector**

Pin number	Description	Pin number	Description
1	I2C1_SDA (PB7)	5	PWR (Defined by daughterboard on CN3, or VDD when short CN3 pin17 and pin18)
2	NC	6	NC
3	I2C1_SCL (PB6)	7	GND
4	EX_RESET(PC0)	8	NC

7.1.3 CN2 and CN3 daughterboard connectors

The two CN2 and CN3 18-pin male headers are designed to connect with the legacy peripheral daughterboard or the UCPD daughterboard to the STM32 G0 Evaluation mother board (MB1581). All GPIOs are available on CN2/CN3 connectors, and on CN9/C10 extension connectors.

Each pin on CN2 and CN3 can be used by a daughterboard after disconnecting it from the corresponding function block on the STM32G0C1E-EV Evaluation board. Refer to Table 23 and Table 24 for details.

Table 23. **CN2 daughterboard connector**

Pin	Signal	Mother board function	Legacy daughterboard function (MB1351_CN5)	UCPD daughterboard function (MB1352_CN9)	How to disconnect with function block on mother board
1	PA1	MC_BusVoltage	LDR_OUT	DCDC_EN	Keep JP6 OFF
2	PA15	-	SmartCard RST	USB3_DET	-
3	PB6	I2C1_SCL	I2C1_SCL	I2C1_SCL	-
4	PB7	I2C1_SDA	I2C1_SDA	I2C1_SDA	-
5	GND	-	-	-	-
6	RESET#	-	-	-	-
7	PC6	MC_ENA	IR_IN	Display port HPD_SOURCE	-
8	PB13	-	I2C2_SCL	DISCHARGE 1	-
9	PB14	-	I2C2_SDA	DISCHARGE 2	-
10	PB1	MC_PFCpwm	-	VSENSE 1	-

Pin	Signal	Mother board function	Legacy daughterboard function (MB1351_CN5)	UCPD daughterboard function (MB1352_CN9)	How to disconnect with function block on mother board
11	PB10	MC_CurrentC	HDMI_CEC	ISENSE 1	-
12	PA3	MC_heatsinkTemp	SmartCard 1V8	VSENSE 2	Keep JP5 OFF
13	PB12	MC_EmergencySTOP	SmartCard OFF	ISENSE 2	Keep JP7 OFF
14	+3V3	-	-	-	-
15	PB11	Daughterboard detection	Daughterboard detection	Daughterboard detection	-
16	VDD_ANA	-	-	-	-
17	I2C_PU	I^2C pull-up power of CN4	-	-	-
18	VDD	-	-	-	-

Table 24. CN3 daughterboard connector

Pin	Signal	Mother board function	Legacy daughterboard function (MB1351_CN4)	UCPD daughterboard function (MB1352_CN8)	How to disconnect with function block on mother board
1	PA8	MC_UH	-	PORT1_CC1	-
2	PB15	MC_Dissipativebrake	SmartCard 3 V/5 V	PORT1_CC2	-
3	PA9	MC_VH/ USART1_TX_BOOT	-	PORT1_DB1	Keep JP15 pin2-3 OFF
4	PA10	MC_WH/ USART1_RX_BOOT	-	PORT1_DB2	Keep JP13 pin2-3 OFF
5	GND	-	-	-	-
6	PD4	MC_WL	SmartCard CK	VCONN_EN1	-
7	PB9	MC_NTC	IR_OUT	VCONN_EN2	-
8	PA2	MC_Current A	SmartCard TX	FRS_TX1	-
9	PB0	MC_ENINDEX	SmartCard CMDVCC	FRS_TX2	-
10	+5V	-	-	-	-
11	PB5	MC_ENB	Temp Sensor INT	DisplayPort™ HPD_IN	-
12	PC1	MC_PFCsync1	-	PWM_CTL	-
13	PD0	MC_PFCsync2	-	PORT2_CC1	-
14	PD2	MC_UL	HDMI_ HPD_SINK	PORT2_CC2	-
15	PD3	MC_VL	HDMI_ HPD_SOURCE	SOURCE_EN	-
16	D5V	-	-	-	-
17	EXT I2C PWR	Power of CN4	5 V	VDD	-
18	VDD	-	-	-	-

7.1.4 CN8 USB 2.0 FS board to board connector

The CN8 male connector is used to connect the mother board USB 2.0 FS data interface (DP/DM) to the USB Type-C® daughterboard connectors.

- If the user wants to connect MCU USB D+/D- to MB1352_CN7 connector (USB Type-C® port 1), then he must fit SB5 and SB6, and remove SB39 and SB38 on MB1581 (default configuration).
- If the user wants to connect MCU USB D+/D- to MB1352_CN5 connector (USB Type-C® sink port 2), then he must fit SB39 and SB38, and remove SB5 and SB6 on MB1581.

Table 25. CN8 USB 2.0 FS board to board connector

Pin	Signal	Mother board function	UCPD daughterboard function (MB1352_CN10)	How to disconnect with function block on mother board
1	PA12	USART1_RTS	C1_D+	Keep JP3 OFF
2	PA11	USART1_CTS_3V3	C1_D-	Keep JP4 OFF
3	PA12	USART1_RTS	C2_D+	Keep JP3 OFF
4	PA11	USART1_CTS_3V3	C2_D-	Keep JP4 OFF

7.1.5 CN5 ST-LINK/V2-1 USB Micro-B connector

The CN5 USB Micro-B connector is used to connect embedded ST-LINK/V2-1 to the PC for debugging of the board.

Figure 12. CN5 USB Micro-B connector (Front view)

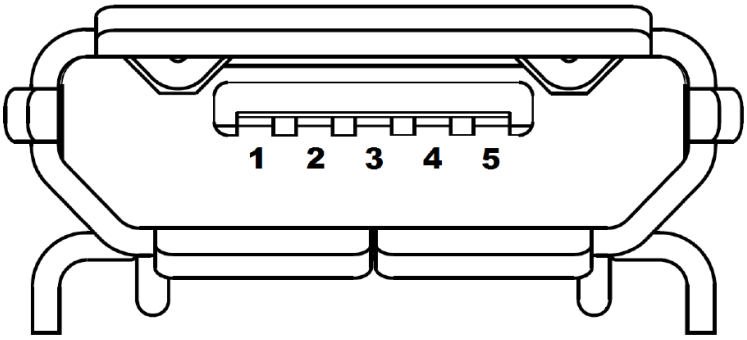


Table 26. CN5 USB Micro-B connector pinout

Pin number	Description	Pin number	Description
1	V_{BUS} (power)	4	ID
2	DM	5	GND
3	DP	-	-

7.1.6 CN6 ST-LINK/V2-1 programming connector

The CN6 connector is only used for embedded ST-LINK/V2-1 programming during board manufacturing. It is not populated by default and not for the end-user.

7.1.7 CN11 microSD™ connector

Figure 13. **CN11 microSD™ connector (front view)**

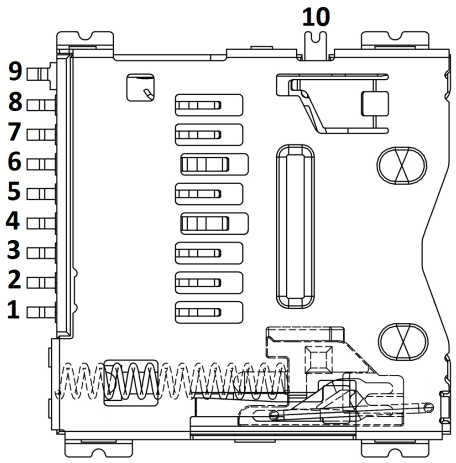


Table 27. **CN11 microSD™ connector**

Pin number	Description	Pin number	Description
1	NC	5	MicroSDcard_CLK (PB3)
2	MicroSDcard_CS (PD1)	6	Vss/GND
3	MicroSDcard_DIN(PA7)	7	MicroSDcard_DOUT(PB4)
4	+3V3	8	NC
-	-	10	MicroSDcard_detect (PC9)

7.1.8 CN9 and CN10 extension connectors

The two CN9 and CN10 22-pin male headers are designed to connect with daughterboard or standard wrapping board to STM32G0C1E-EV Evaluation board. The standard width between CN9 pin1 and CN10 pin1 is 2700 mils (68.58 mm). The standard is implemented on the majority of evaluation boards. Each pin on CN9 and CN10 can be used by a daughterboard after disconnecting it from the corresponding function block on STM32G0C1E-EV Evaluation board. Refer to Table 28 and Table 29 for details.

Table 28. **CN9 extension connector**

Pin	Description	Alternative function	How to disconnect with function block on STM32G0C1E-EV Evaluation board
1	PD13	FDCAN1_TX	Remove SB9
3	PD15	FDCAN2_TX	Remove SB11
5	PF8	-	-
7	PA13	T_JTMS / SWDIO / SWDAT	Remove SB13
9	PC9	SDCARD_DETECT	Remove SB42
11	PD5	LED1	Remove SB16
13	PD7	-	-
15	PF10	-	-
17	PF13	-	-
19	GND	-	-

Pin	Description	Alternative function	How to disconnect with function block on STM32G0C1E-EV Evaluation board
21	PB3	SPI1_SCK	Remove SB18
23	PB8	LCD_CS_OD	Remove SB51
25	PE0	FDCAN1_STBY	Remove SB20
27	PE3	-	-
29	PE5	-	-
31	PE4	-	-
33	PC11	VCP_RX (STLINK TX)	Open JP12
35	PC14	OSC32_IN	Fit SB53, Remove R39
37	PC13	TAMPER_KEY	Remove SB24
39	GND	-	-
2	PD12	FDCAN1_RX	Remove SB10
4	PD14	FDCAN2_RX	Remove SB12
6	VDD	-	-
8	PA14	T_JTCK / TCK/SWCLK, BOOT0	Open JP2
10	GND	-	-
12	PD1	MicroSD_CS_OD	Remove SB14
14	PD6	LED2	Remove SB17
16	PF9	-	-
18	PF11	-	-
20	PF12	-	-
22	PB4	SPI1_MISO	Remove SB19
24	PC10	VCP_TX (STLINK RX)	Remove SB37
26	PE1	FDCAN2_STBY	Remove SB21
28	PE2	-	-
30	GND	-	-
32	PE6	-	-
34	PC12	SPI1_MOSI_DIR	Remove SB23
36	PC15	OSC32_OUT	Fit SB52, Remove R40
38	PC8	JOY_LEFT	Remove SB59
40	3V3	-	-

Table 29. CN10 extension connector

Pin	Description	Alternative function	How to disconnect with function block on STM32G0C1E-EV Evaluation board
1	PA12	USB_FS_P	Fit SB7, Remove SB5, Open JP3
3	PD11	-	-
5	PD9	LED4	Remove SB40
7	PC7	JOY_RIGHT	Remove SB41
9	PE14	-	-
11	PE13	-	-

Pin	Description	Alternative function	How to disconnect with function block on STM32G0C1E-EV Evaluation board
13	PE11	-	-
15	PE9	-	-
17	PF6	-	-
19	GND	-	-
21	PC5	USART1_RX	Open JP13
23	PA7	SPI1_MOSI	Remove SB22
25	PA5	Audio_OUT_R	Open JP19
27	PF5	-	-
29	PF4	-	Fit SB25
31	PC2	JOY_UP	Remove SB58
33	PC3	JOY_DOWN	Remove SB57
35	PF2	T_NRST	Remove SB26
37	D5V	-	-
39	GND	-	-
2	PA11	USB_FS_N	Fit SB8, Remove SB6, Open JP4
4	PD10	-	-
6	PD8	LED3	Remove SB44
8	PE15	-	-
10	GND	-	-
12	PE12	-	-
14	PE10	-	-
16	PE8	-	-
18	PE7	-	-
20	PF7	-	-
22	PB2	Potentiometer / VREF+	Remove SB45
24	PC4	USART1_TX	Open JP15
26	PA6	Audio_IN	Open JP22, Do not connect anything to CN1
28	PA4	Audio_OUT_L	Open JP23 & JP19
30	GND	-	-
32	PA0	JOY_SEL	Remove SB56
34	PF3	-	Fit SB27
36	PC0	GPIO_EXT_RST	Remove R11, Do not connect anything to CN4
38	PF1	OSC_OUT	Fit SB54, Remove R47
40	PF0	OSC_IN	Fit SB55, Remove R46

7.1.9 CN16 RS-232 and RS-485 connector

Figure 14. **CN16 RS-232 and RS-485 connector (front view)**

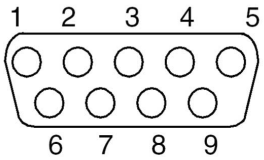


Table 30. **CN16 RS-232 and RS-485 connector**

Pin number	Description	Pin number	Description
1	NC	6	Bootloader_BOOT0
2	RS232_RX (PC5 or PA10)	7	RS232_RTS(PA12)
3	RS232_TX (PC4 or PA9)	8	RS232_CTS(PA11) / bootloader_RESET
4	RS485_A	9	RS485_B

7.1.10 CN14 SWD standard connector

Figure 15. **CN14 SWD standard connector (top view)**

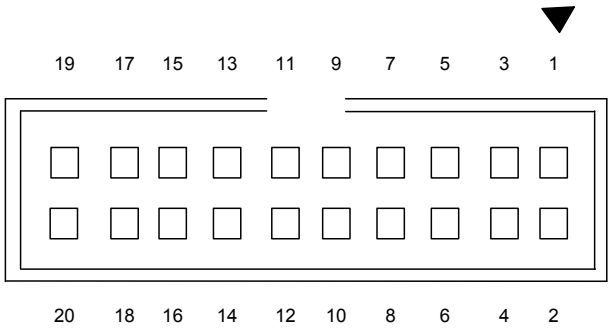


Table 31. **CN14 SWD debugging connector**

Pin number	Description	Pin number	Description
1	VDD	2	VDD
3	NC	4	GND
5	NC	6	GND
7	SWDAT(PA13)	8	GND
9	SWCLK(PA14)	10	GND

Pin number	Description	Pin number	Description
11	10K pull-down	12	GND
13	NC	14	GND
15	RESET#	16	GND
17	10K pull-down	18	GND
19	10K pull-down	20	GND

7.1.11 CN15 high-density SWD debugging connector

Figure 16. CN15 high-density SWD debugging connector (top view)

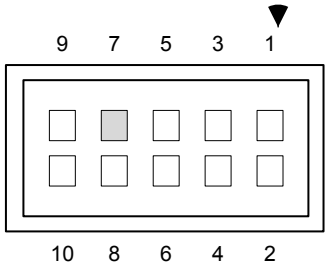


Table 32. CN15 high-density SWD debugging connector

Pin number	Description	Pin number	Description
1	VDD	2	SWDAT(PA13)
3	GND	4	SWCLK(PA14)
5	GND	6	NC
7	KEY	8	NC
9	GND	10	RESET#

7.1.12 CN17/CN19 TFT-LCD connector

A TFT colored-LCD board is mounted on CN17/CN19. Refer to Section 6.6.7 for detail.

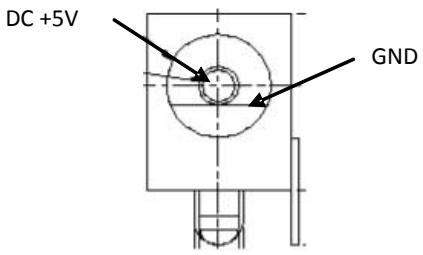
7.1.13 CN18 audio jack

A CN18 3.5 mm stereo audio jack connected to audio DAC and ADC is available on the STM32G0C1E-EV Evaluation board.

7.1.14 CN20 5 V power connector

The STM32G0C1E-EV Evaluation board (MB1581) can be powered from a DC 5 V power supply via the CN20 external power supply jack as shown in Figure 17. The central pin of CN20 must be positive.

Figure 17. CN20 power supply connector (front view)



7.1.15 CN21 analog input connector

Figure 18. CN21 analog I/O connector (top view)

Table 33. CN21 analog I/O connector

Pin number	Description	Pin number	Description
1	Analog I/O PB2	2	GND

7.1.16 CN12 and CN13 CAN-FD connectors

Figure 19. CN12 and CN13 CAN-FD connectors (top view)

Table 34. CN12 FDCAN1 connector

Pin number	Description
1	CAN1H
2	CAN1L

Table 35. CN13 FDCAN2 connector

Pin number	Description
1	CAN2H

Pin number	Description
2	CAN2L

7.2 Connectors on the legacy peripheral daughterboard (MB1351)

7.2.1 MB1351_CN1 HDMI sink connector

Figure 20. **MB1351_CN1 HDMI sink connector (front view)**

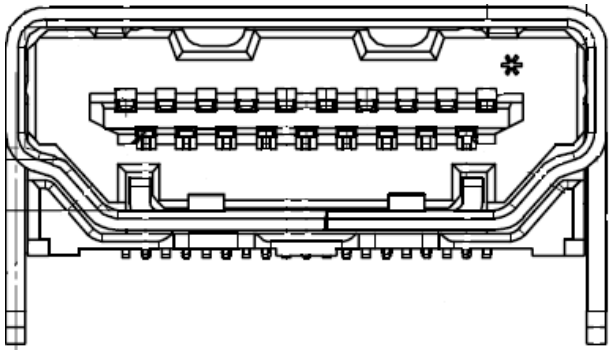


Table 36. **MB1351_CN1 HDMI sink connector**

Pin number	Description	Pin number	Description
1,3,4,6,7,9,10,12	TMDS differential signal pair connected to MB1351_CN3	16	I2C2_SDA (PB14)
13	CEC (PB10)	2,5,8,11,17	GND
14	NC	18	HDMI_5V_Sink
15	I2C2_SCL (PB13)	19	HPD (PD2 through transistor)

7.2.2 MB1351_CN2 smartcard connector

Figure 21. **MB1351_CN2 smartcard connector (top view)**

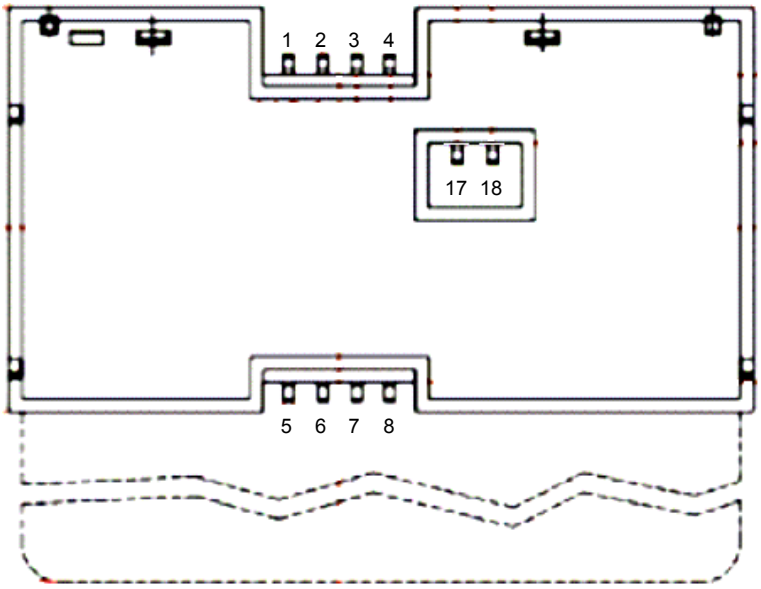


Table 37. **MB1351_CN2 smartcard connector**

Pin number	Description	Pin number	Description
1	VCC	5	GND
2	RST	6	NC
3	CLK	7	I/O
4	NC	8	NC
17	Card presence detection pin	18	Card presence detection pin

7.2.3 MB1351_CN3 HDMI source connector

Figure 22. **MB1351_CN3 HDMI source connector (front view)**

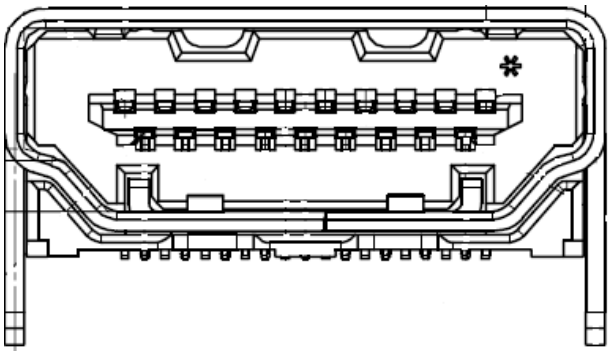


Table 38. **MB1351_CN3 HDMI source connector**

Pin number	Description	Pin number	Description
1,3,4,6,7,9,10,12	TMDS differential signal pair connected to MB1351_CN1	16	I2C1_SDA (PB7)
13	CEC (PB10)	2,5,8,11,17	GND
14	NC	18	HDMI_5V_Source from the U1 power switch
15	I2C1_SCL (PB6)	19	HPD (PD3)

7.2.4 CN4 and CN5 daughterboard female connectors

CN4 and CN5 female connectors are used to implement the legacy peripheral daughterboard on the mother board. CN4 on the legacy daughterboard is connected to CN3 on the mother board, and CN5 on the legacy daughterboard is connected to CN2 on the mother board. Refer to Section 7.1.3 for a detailed signal definition of these connectors.

7.3 Connectors on UCPD daughterboard (MB1352)

7.3.1 MB1352_CN1 USB Type-A connector

Figure 23. **MB1352_CN1 USB Type-A connector (front view)**

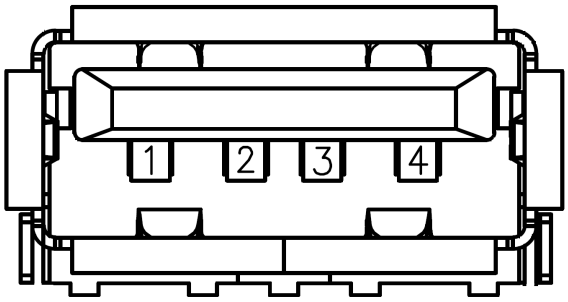


Table 39. **MB1352_CN1 USB Type-A connector**

Pin number	Description	Pin number	Description
1	V_{BUS} (power)	3	D+
2	D-	4	GND

7.3.2 MB1352_CN2 DisplayPort™ source connector

Figure 24. **MB1352_CN2 DisplayPort™ source connector (front view)**

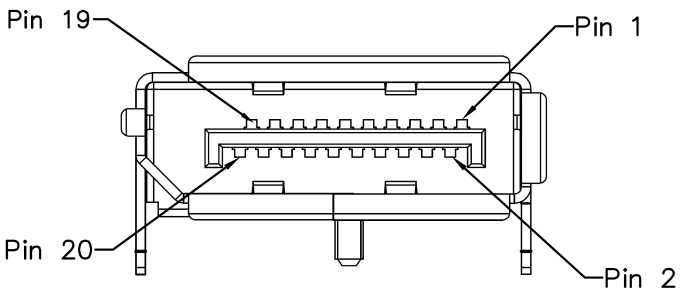


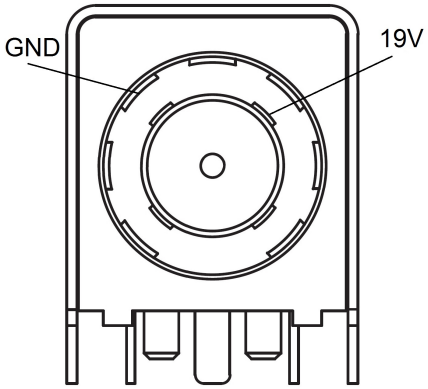
Table 40. **MB1352_CN2 DisplayPort™ source connector**

Pin number	Description	Pin number	Description
1	LANE0_P	13	CONFIG1
3	LANE0_N	14	CONFIG2
4	LANE1_P	15	AUX_CH_P
6	LANE1_N	17	AUX_CH_N
7	LANE2_P	18	HPD (PC6)
9	LANE2_N	19	RETURN
10	LANE3_P	20	DP_PWR
12	LANE3_N	2,5,8,11,16	GND

7.3.3 MB1352_CN3 19 V Power connector

The UCPD daughterboard can be powered from a DC 19 V power supply via the MB1352_CN3 external power supply jack as shown in Figure 25. And it is used for USB Power Delivery.

Figure 25. **MB1352_CN3 Power connector (front view)**



7.3.4 MB1352_CN4 USB3.1 Gen1 Type-B connector

Figure 26. **MB1352_CN4 USB3.1 Gen1 Type-B connector (front view)**

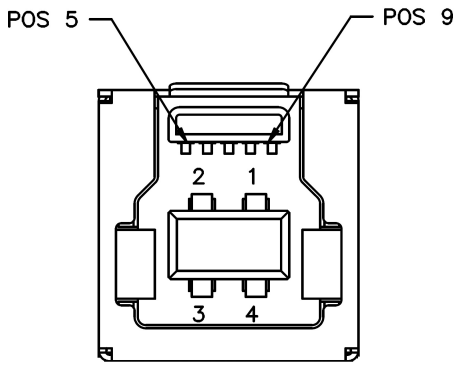


Table 41. **MB1352_CN4 USB3.1 Gen1 Type-B connector**

Pin number	Description	Pin number	Description
1	V_{BUS} (power)	5	SSTX-
2	D-	6	SSTX+
3	D+	7	GND_DRAIN
4	GND	8	SSRX-
-	-	9	SSRX+

7.3.5 PORT2 MB1352_CN5 USB Type-C® connector

Figure 27. **PORT2 MB1352_CN5 USB Type-C® connector (front view)**

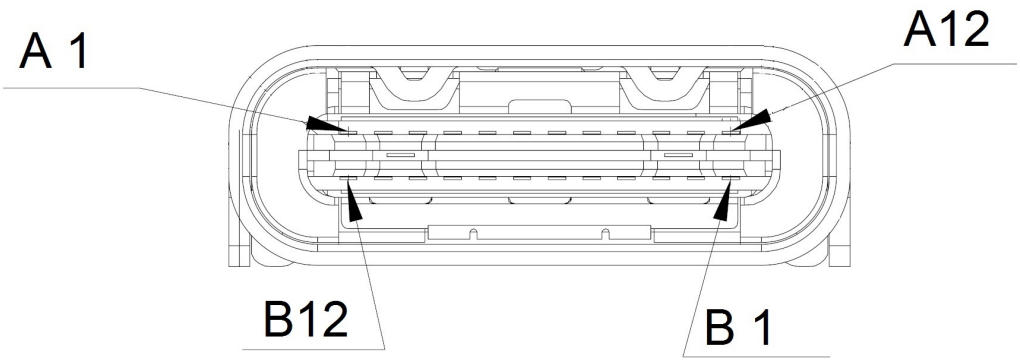


Table 42. **PORT2 MB1352_CN5 USB Type-C® connector**

Pin number	Description	Pin number	Description
A1	GND	B1	GND
A2	TX1+	B2	TX2+
A3	TX1-	B3	TX2-
A4	V_{BUS}	B4	V_{BUS}
A5	CC1 (PD0)	B5	CC2 (PD2)
A6	D+	B6	D+
A7	D-	B7	D-
A8	SBU1	B8	SBU2
A9	V_{BUS}	B9	V_{BUS}
A10	RX2-	B10	RX1-
A11	RX2+	B11	RX1+
A12	GND	B12	GND

7.3.6 MB1352_CN6 DisplayPort™ sink connector

Figure 28. MB1352_CN6 DisplayPort™ sink connector (front view)

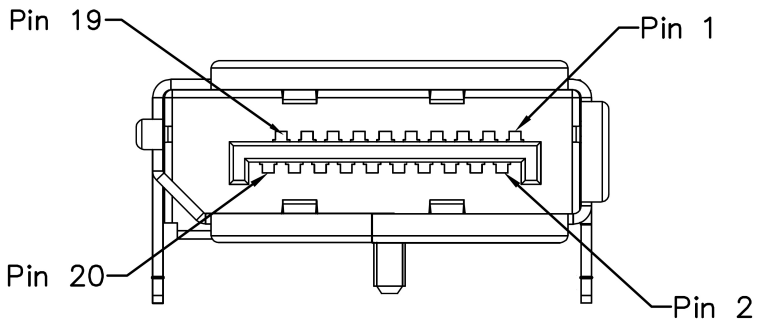


Table 43. MB1352_CN6 DisplayPort™ sink connector

Pin number	Description	Pin number	Description
1	LANE3_N	13	CONFIG1
3	LANE3_P	14	CONFIG2
4	LANE2_N	15	AUX_CH_P
6	LANE2_P	17	AUX_CH_N
7	LANE1_N	18	HPD (PB5)
9	LANE1_P	19	RETURN
10	LANE0_N	20	DP_PWR
12	LANE0_P	2,5,8,11,16	GND

7.3.7 PORT1 MB1352_CN7 USB Type-C®connector

Figure 29. PORT1 MB1352_CN7 USB Type-C®connector (front view)

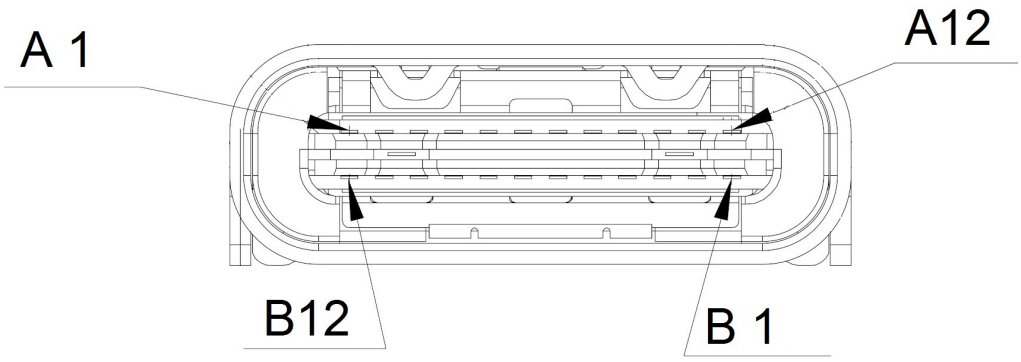


Table 44. PORT1 MB1352_CN7 USB Type-C®connector

Pin number	Description	Pin number	Description
A1	GND	B1	GND
A2	TX1+	B2	TX2+

Pin number	Description	Pin number	Description
A3	TX1-	B3	TX2-
A4	V_{BUS}	B4	V_{BUS}
A5	CC1 (PA8)	B5	CC2 (PB15)
A6	D+	B6	D+
A7	D-	B7	D-
A8	SBU1	B8	SBU2
A9	V_{BUS}	B9	V_{BUS}
A10	RX2-	B10	RX1-
A11	RX2+	B11	RX1+
A12	GND	B12	GND

7.3.8 MB1352_CN8 and MB1352_CN9 daughterboard female connectors

MB1352_CN8 and MB1352_CN9 female connectors are used to implement the USB-C® daughterboard on the mother board. MB1352_CN8 on the USB-C® daughterboard is connected to CN3 on the mother board, and MB1352_CN9 on the USB-C® daughterboard is connected to CN2 on the mother board. Refer to Section 7.1.3 for a detailed signal definition of these connectors.

7.3.9 MB1352_CN10 USB 2.0 FS board to board connector

One female connector MB1352_CN10 is used to connect the mother board USB 2.0 FS data interface (DP/DM) to USB Type-C® daughterboard connectors.

Table 45. MB1352_CN10 USB 2.0 FS board to board connector

Pin	Signal
1	PA12
2	PA11
3	PA12
4	PA11

8 STM32G0C1E-EV Evaluation board information

8.1 Product marking

The sticker located on the top or bottom side of the PCB shows the information about product identification such as board reference, revision, and serial number.

The first identification line has the following format: “MBxxxx-Variant-yzz”, where “MBxxxx” is the board reference, “Variant” (optional) identifies the mounting variant when several exist, "y" is the PCB revision and "zz" is the assembly revision, for example B01.

The second identification line is the board serial number used for traceability.

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

In order to use the same commercial stack in his application, a developer may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

8.2 Board revision history

8.2.1 MB1581 mother board

Revision B02

The revision B02 of the MB1581 is the initially released version.

8.2.2 MB895 LCD daughterboard

Revision C03

The revision C03 of the MB895 is the initially released version.

8.2.3 MB1351 legacy peripheral daughterboard

Revision A01

The revision A01 of the MB1351 is the initially released version.

8.2.4 MB1352 USB-C® daughterboard

Revision C03

The revision C03 of the MB1352 is the initially released version.

8.3 Known limitations

8.3.1 MB1581 mother board

Revision B02

Table 46. **STM32G0C1E-EV I/O assignment**

ID	Description	Workaround
91631	CAN-FD transceivers VIO rail 3V3 only	Use CAN with VDD = 3.3 V
84750	Wrong silkscreen information: • U20 instead of U24 • RV3: VDD_ANA instead of ADC ref • CN21: AIN instead of Analog I/O • CN20: PSU 5 V (E5V)	No workaround
92534	ST-Link I/O level shifter must be connected to 3V3_STLK instead of 3V3	No workaround

8.3.2 MB895 LCD daughterboard

Revision C03

No known limitations

8.3.3 MB1351 legacy peripheral daughterboard

Revision A01

No known limitations

8.3.4 MB1352 USB-C® daughterboard

Revision C03

No known limitations

Appendix A STM32G0C1E-EV I/O Assignment

Table 47. **STM32G0C1E-EV I/O assignment**

Pin number	Pin name	I/O assignment on mother board	I/O assignment on legacy daughterboard	I/O assignment on UCPD daughterboard
1	PB9	MC_IO_(NTC_bypass)	IR_OUT	GPIO_VCONN_EN_1_2
2	PC10	VCP_USART_3_TX	-	-
3	PC11	VCP_USART_3_RX	-	-
4	PE4	FREE	-	-
5	PE5	FREE	-	-
6	PE6	FREE	-	-
7	PC12	GPIO_LCD / SD_MOSI_DIR	-	-
8	PC13	KEY_TAMP_IN1, RTC_TS, RTC_OUT1, WKUP2	-	-
9	PC14-OSC32_IN	OSC32_IN	-	-
10	PC15-OSC32_OUT	OSC32_OUT	-	-
11	VBAT	VBAT	-	-
12	VREFP	VREFP	-	-
13	VDD_1	VDD	-	-
14	VSS_1	GND	-	-
15	PF0-OSC_IN	OSC_IN	-	-
16	PF1-OSC_OUT	OSC_OUT	-	-
17	PF2-NRST	NRST, (WKUP8)	-	-
18	PF3	FREE	-	-
19	PF4	FREE	-	-
20	PF5	FREE	-	-
21	PC0	GPIO_EXT_RST	-	-
22	PC1	MC_IO_(PFC_sync1)	-	GPIO_9V_EN_LPTIM1_OUT
23	PC2	GPIO_JOY_UP	-	-
24	PC3	GPIO_JOY_DOWN	-	-
25	PA0	JOY_SEL_TAMP_IN2, WKUP1	-	-
26	PA1	MC_AIN1_COMP_1_INP(Bus voltage)	LDR_OUT_COMP_1_INP_ADC_IN1	GPIO_15V_EN_DCDC_EN
27	PA2	MC_ADC_IN2(CurrentA)	SMART_2_TX	TYPE-C_1_FRSTX
28	PA3	MC_ADC_IN3(Heatsink temp)	GPIO_SMART_1V8	TYPE-C_2_V_ADC_IN3
29	PA4	AUDIO_OUT_DAC1_OUT1	-	-
30	PA5	AUDIO_OUT_DAC1_OUT2	-	-
31	PA6	AUDIO_IN_ADC_IN6 / MC_ADC_IN6(CurrentB)	-	-
32	PA7	LCD/SD1_MOSI	-	-
33	PC4	USART_1_TX	-	-

Pin number	Pin name	I/O assignment on mother board	I/O assignment on legacy daughterboard	I/O assignment on UCPD daughterboard
34	PC5	USART_1_RX	-	-
35	PB0	MC_TIM_3_CH3(Encoder index)	GPIO_SMART_CMDVCC	TYPE-C_1_FRSTX
36	PB1	MC_TIM_3_CH4(PFC_PWM)	-	TYPE-C_1_V_ADC_IN9
37	PB2	POT_ADC_IN10	-	-
38	PF6	FREE	-	-
39	PF7	FREE	-	-
40	PE7	FREE	-	-
41	PE8	FREE	-	-
42	PE9	FREE	-	-
43	PE10	FREE	-	-
44	PE11	FREE	-	-
45	PE12	FREE	-	-
46	PE13	FREE	-	-
47	PE14	FREE	-	-
48	PE15	FREE	-	-
49	PB10	MC_ADC_IN11 (CurrentC)	HDMI_CEC	TYPE-C_1_I_ADC_IN11
50	PB11	BOARD_DET_ADC_IN15	BOARD_DET_ADC_IN15	BOARD_DET_ADC_IN15
51	PB12	MC_TIM_1_BK (Emergency STOP)	GPIO_SMART_OFF	TYPE-C_2_I_ADC_IN16
52	PB13	-	I2C2_SCL (HDMI_SINK)	GPIO_DISCHARGE_1
53	PB14	-	I2C2_SDA (HDMI_SINK)	GPIO_DISCHARGE_2
54	PB15	MC_IO_(Dissipative brake)	GPIO_SMART_3V or GPIO_SMART_5V	TYPE-C_1_CC2
55	PA8	MC_TIM_1_CH1(UH)	-	TYPE-C_1_CC1
56	PA9	USART_BOOT_1_TX / MC_TIM_1_CH2(VH)	-	TYPE-C_1_DBCC1
57	PC6	MC_TIM_3_CH1 (EncoderA)	IR_IN_TIM3_CH1	GPIO_DP2_HPD
58	PC7	GPIO_JOY_RIGHT	-	-
59	PD8	LED3	-	-
60	PD9	LED4	-	-
61	PD10	FREE	-	-
62	PD11	FREE	-	-
63	VSS_3	GND	-	-
64	VDDIO2	VDD	-	-
65	PD12	FDCAN1_RX	-	-
66	PD13	FDCAN1_TX	-	-
67	PD14	FDCAN2_RX	-	-
68	PD15	FDCAN2_TX	-	-
69	PA10	USART_BOOT_1_RX / MC_TIM_1_CH3(WH)	-	TYPE-C_1_DBCC2
70	PA11 [PA9]	USART_1_CTS	-	USB_FS_N

Pin number	Pin name	I/O assignment on mother board	I/O assignment on legacy daughterboard	I/O assignment on UCPD daughterboard
71	PA12 [PA10]	USART_1_RTS_DE_CK	-	USB_FS_P
72	PF8	FREE	-	-
73	PA13	SWDIO	-	-
74	PA14-BOOT0	SWCLK / BOOT0	-	-
75	PA15	-	GPIO_SMART_RST	GPIO_USB3_DET
76	PC8	GPIO_JOY_LEFT	-	-
77	PC9	GPIO_SD_DETECT	-	-
78	PD0	MC_TIM_16_CH1(PFC_sync 2)	-	TYPE-C_2_CC1
79	PD1	GPIO_SD_CS	-	-
80	PD2	MC_TIM_1_CH1N(UL)	GPIO_HDMI_HPD_SINK	TYPE-C_2_CC2
81	PD3	MC_TIM_1_CH2N(VL)	GPIO_HDMI_HPD_SOURCE	GPIO_SOURCE_EN
82	PD4	MC_TIM_1_CH3N(WL)	SMART_2_RTS_DE_CK	GPIO_VCONN_EN_1_1
83	PD5	LED1	-	-
84	PD6	LED2	-	-
85	PD7	FREE	-	-
86	PF9	FREE	-	-
87	PF10	FREE	-	-
88	PF11	FREE	-	-
89	PF12	FREE	-	-
90	PF13	FREE	-	-
91	PB3	LCD/SD1_SCK	-	-
92	PB4	LCD/SD1_MISO	-	-
93	PB5	MC_TIM_3_CH2(EncoderB)	TEMP_SENSOR_INT_WKUP 6	GPIO_DP1_DET
94	PE0	FDCAN1_STBY	-	-
95	PE1	FDCAN2_STBY	-	-
96	PE2	FREE	-	-
97	PE3	FREE	-	-
98	PB6	I2C1_SCL	HDMI_SOURCE_I2C1_SCL	MUX_I2C1_SCL
99	PB7	I2C1_SDA	HDMI_SOURCE_I2C1_SDA	MUX_I2C1_SDA
100	PB8	GPIO_LCD_CS	-	-

Appendix B STM32G0C1E-EV mechanical dimensions

Figure 30. **STM32G0C1E-EV mechanical dimensions**

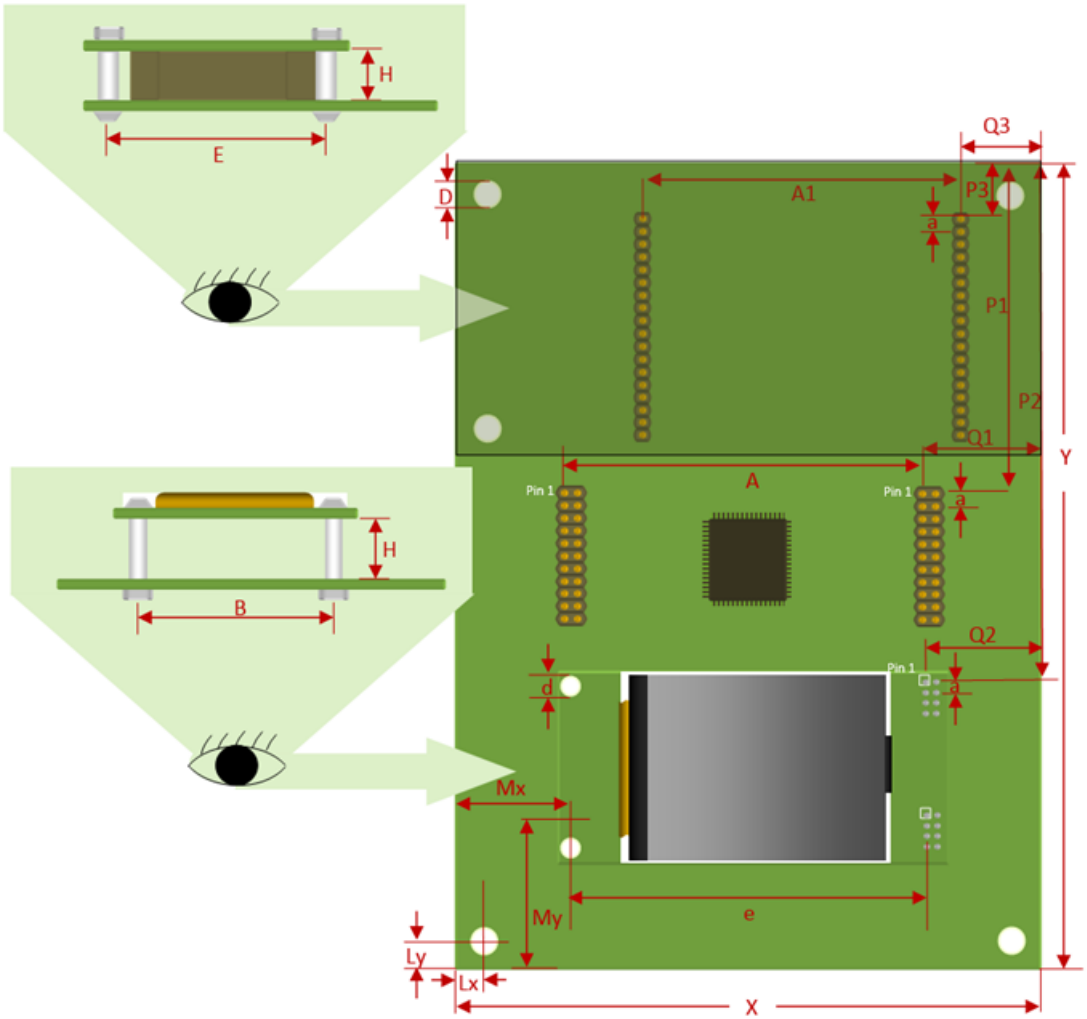


Table 48. **STM32G0C1E-EV mechanical dimensions**

Symbol	Size in millimeters	Symbol	Size in millimeters	Symbol	Size in millimeters
A	68.58	e	77.44	P2	111.76
A1	61.97	H	11	P3	10.41
a	2.54	Lx	5.715	Q1	24.12
B	36	Ly	5.715	Q2	17.70
D	3.5	Mx	19.08	Q3	16
d	3.2	My	18.73	X	114.3
E	47	P1	60.71	Y	172.72

Appendix C Federal Communications Commission (FCC) and Innovation, Science and Economic Development Canada (ISED) Compliance Statements

C.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Responsible party (in the USA)

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Telephone: +1 972-466-7845

C.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada: CAN ICES-3 (A) / NMB-3 (A).

Appendix D CE conformity

D.1 Warning

EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

D.2 Simplified declaration of conformity

Hereby, STMicroelectronics declares that the STM32G0C1E-EV Evaluation board with STM32G0C1VE MCU comply with the applicable CE requirements stated below:

- EN 55032 (2012/2015) / EN 55035 (2017)
- EN 60950-1 (2006 + A11/2009 + A1/2010 + A12/2011 + A2/2013) / EN 62368-1 (2014 +A1/2017)
- CFR 47, FCC Part 15 B / ICES-003: Issue 6/2016

The complete declaration of conformity is available upon request from STMicroelectronics.

Revision history

Table 49. **Document revision history**

Date	Revision	Changes
1-Dec-2020	1	Initial release.

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