UM2792

User manual

Getting started with the STEVAL-DPSTPFC1 3.6 kW PFC totem pole with inrush current limiter reference design

Introduction

The STEVAL-DPSTPFC1 3.6 kW bridgeless totem pole boost circuit achieves a digital power factor correction (PFC) with inrush current limiter (ICL). It helps you to design an innovative topology with the latest ST power kit devices: silicon carbide MOSFETs (SCTW35N65G2V), thyristor SCRs (TN3050H-12WY), isolated FET drivers (STGAP2S) and a 32-bit MCU (STM32F334).

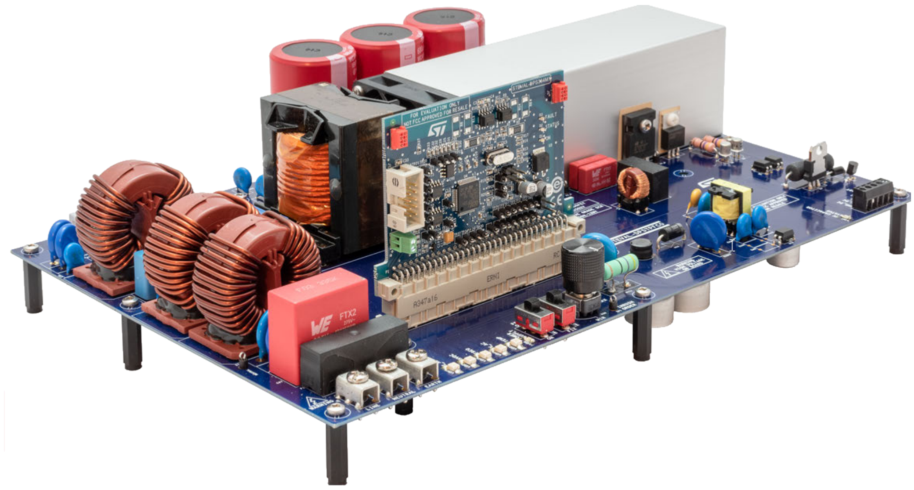
This reference design also opens the path to a compact converter running at 72 kHz offering a high peak efficiency, low THD distortion (97.65 % with 3.6 % THD) and reduced bill of materials.

It achieves a robust circuit that meets EMC standards up to 4 kV delivering high switching lifetime with reduced EMI emissions.

Thyristor SCRs used as AC line polarity switches allow achieving an active current limitation at power up or line drop recovery: the PFC efficiency is optimal and no EMI bouncing effect occurs.

The reference design includes a power board with a bridgeless totem pole boost (with an inrush limiter circuit, switch drivers and an auxiliary power supply), a control board with its MCU, a PFC/ICL control firmware and an adapter board for software debug.

Figure 1. **STEVAL-DPSTPFC1 totem pole**



1 Getting started

1.1 Safety instructions

Attention: *The STEVAL-DPSTPFC1 evaluation board is designed for demonstration purposes only and is not intended for domestic or industrial installations.*

Danger: *The high voltage levels used to operate the STEVAL-DPSTPFC1 evaluation board could provoke a serious electrical shock. This evaluation board has to be used in a suitable laboratory by qualified personnel only, familiar with the installation, use, and maintenance of power electrical systems.*

The STEVAL-DPSTPFC1 radiated field levels could exceed the general public exposure limit if positioned at less than 60 cm.

During operation, do not touch the board as some of its components could reach a very high temperature.

1.2 Overview

The STEVAL-DPSTPFC1 is a 3.6 kW PFC totem pole controlled by an STM32 MCU. It has been designed to offer high performances in terms of efficiency, THD, power factor and reliability by controlling the inrush current at board startup.

The totem pole board is composed of three different boards:

- an AC-DC power board
- a digital control board based on the STM32F334 microcontroller used to control the PFC stage
- an adapter board to debug the MCU firmware

Figure 2. STEVAL-DPSTPFC1 AC-DC power board and PFC control board (highlighted in yellow)

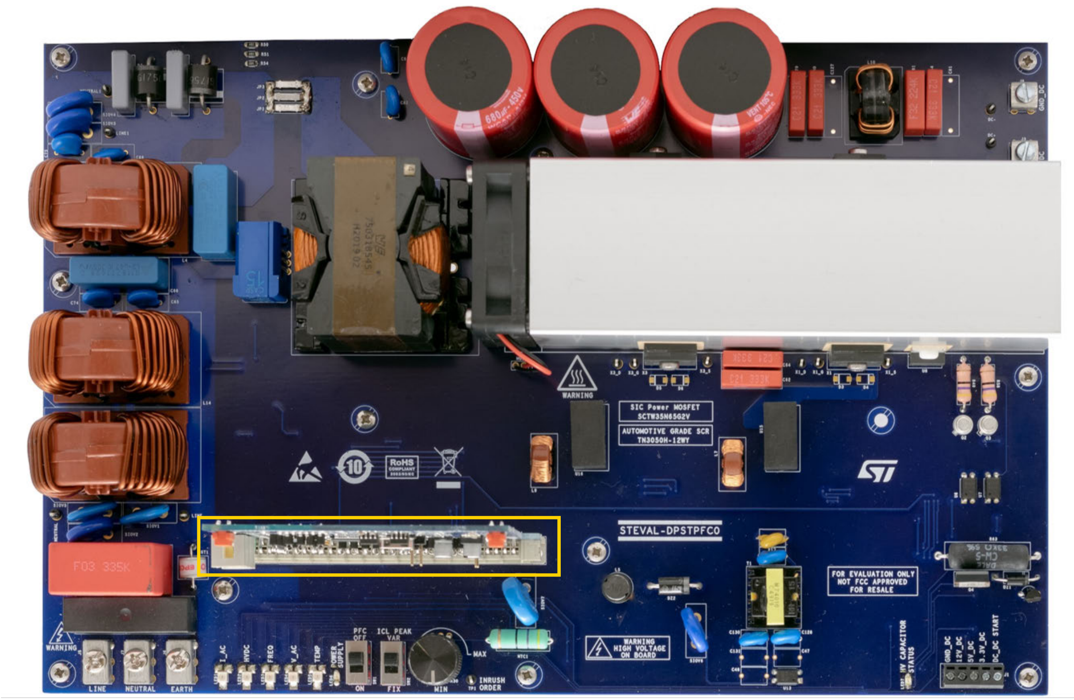
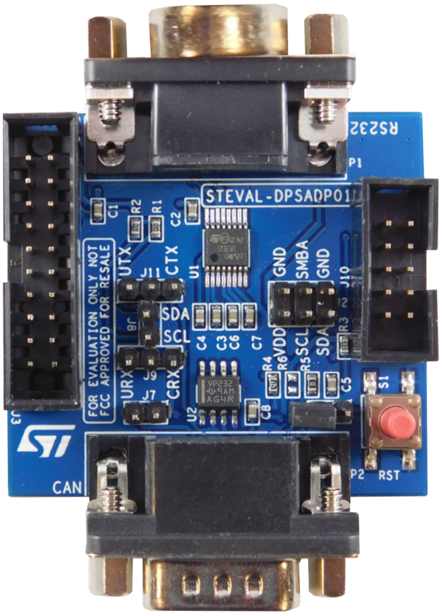


Figure 3. STEVAL-DPSTPFC1 adapter board



The STEVAL-DPSTPFC1 offers:

- inrush current limitation without inrush current resistor or NTC and relay
- very high efficiency AC-DC conversion
- DC power stage disconnection from the AC line grid thanks to SCRs

1.3 Main components

The STEVAL-DPSTPFC1 main components are:

- TN3050H-12WY inrush current limiter SCRs
- SCTW35N65G2V SiC MOSFETs
- STM32F334 MCU
- VIPER26LD flyback IC

Figure 4. STEVAL-DPSTPFC1 main component diagram

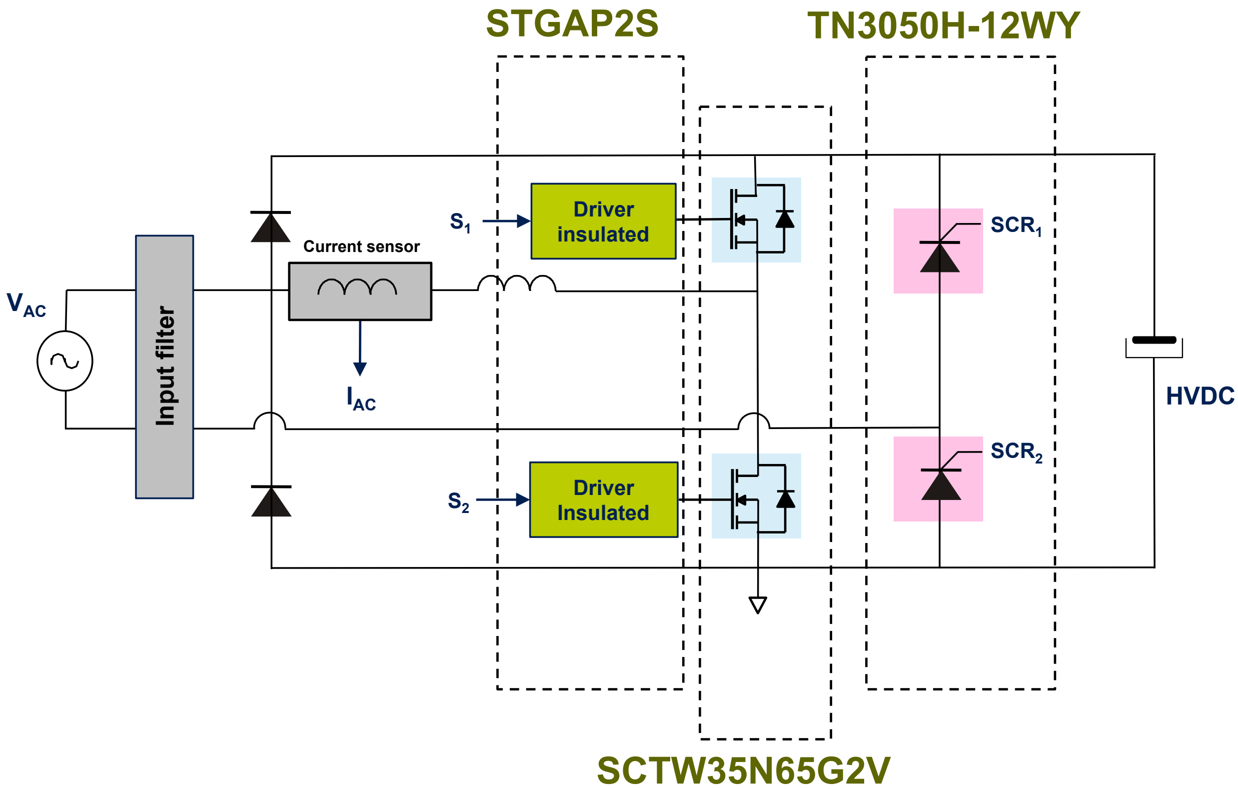
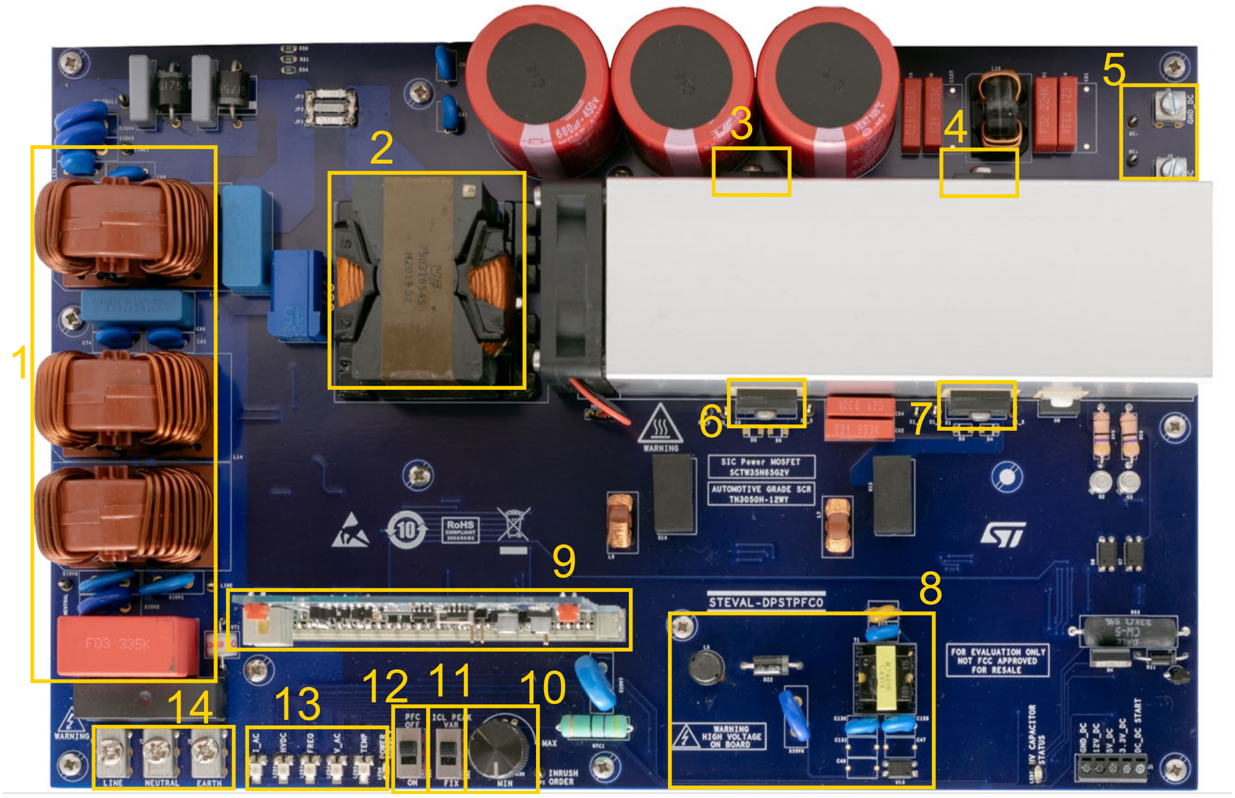


Figure 5. **STEVAL-DPSTPFC1 components - overview**

1. Common mode filter + MOV
2. Boost inductor
3. SCR
4. SCR
5. DC load connectors
6. SiC MOSFET
7. SiC MOSFET
8. DC power supply
9. MCU daughter board
10. Potentiometer to control peak inrush current
11. ICL strategy control switch
12. ICL startup switch
13. PFC LEDs status
14. AC line connectors



1.4 Totem pole PFC specifications

Table 1. PFC electrical specifications

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Input						
AC line voltage	V_{AC}	85		264	V_{RMS}	
AC line frequency	HZ	45		65		
AC line current	I_{AC} MAX			16	A_{RMS}	
Maximum input power	PIN MAX			3.6	kW	V_{AC} = 230 V_{RMS} I_{AC} MAX = 16 A_{RMS}
				1.8	kW	V_{AC} = 115 V_{RMS} I_{AC} MAX = 16 A_{RMS}
Output						
Output voltage regulated	HVDC		400	420	V_{DC}	
HVDC ripple	Vripple (PK-PK)		15		V	P_{OUT} = 3.6 kW V_{AC} = 230 V_{RMS} I_{AC} MAX = 16 A_{RMS}
Maximum output DC current	I_{DC} Max			9	A	P_{OUT} = 3.6 kW V_{AC} = 230 V_{RMS} I_{AC} MAX = 16 A_{RMS}
				4	A	P_{OUT} = 1.7 kW V_{AC} = 115 V_{RMS} I_{AC} = 16 A_{RMS}
Control						
Switching frequency	Fs		72		kHz	
Operating temperature						
Maximum ambient temperature	T_{AMB} MAX			45	°C	

Table 2. PFC temperature specifications

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Thermal components						
Inductor	T_Choke		120		°C	T_{AMB} = 30°C FAN ON P_{OUT} = 3.6 kW V_{AC} = 230 V_{RMS} I_{AC} MAX = 16 A_{RMS}
Sic MOSFETs	TC_MOS		80		°C	
SCRs	TC_SCR		65		°C	

Table 3. PFC protection specifications

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
HVDC overvoltage protection				450	VDC	
I_{AC} peak overcurrent protection				24	A	

Table 4. **Passive component specifications**

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Primary EMI filter inductor	L_FILT L3 / L4 / L14		3 x 1.6		mH	
Output capacitor	C_HVDC C76/C77/C78		3 x 680		μF	

Table 5. **PFC efficiency specifications**

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
Power factor						
	PF		0.9903		N.A.	230 V_{RMS}/50 Hz I_{AC} = 4.5 A $_{RMS}$
	PF		0.9956		N.A.	230 V_{RMS}/50 Hz I_{AC} = 8.8 A_{RMS}
	PF		0.9965		N.A.	230 V_{RMS}/50 Hz I_{AC} = 15.5 A_{RMS}
	PF		0.9932		N.A.	115 V_{RMS}/60 Hz I_{AC} = 3.8 A_{RMS}
	PF		0.9982		N.A.	115 V_{RMS}/50 Hz I_{AC} = 9.5 A_{RMS}
	PF		0.9981		N.A.	115 V_{RMS}/60 Hz I_{AC} = 15.5 A_{RMS}
Distortion						
	THD		9.1		%	230 V_{RMS}/50 Hz I_{AC} = 4.5 A_{RMS}
	THD		4.6		%	230 V_{RMS}/50 Hz I_{AC} = 8.8 A_{RMS}
	THD		3.7		%	230 V_{RMS}/50 Hz I_{AC} = 15.5 A_{RMS}
	THD		9		%	115 V_{RMS}/60 Hz I_{AC} = 3.8 A_{RMS}
	THD		4.5		%	115 V_{RMS}/50 Hz I_{AC} = 9.5 A $_{RMS}$
	THD		4.1		%	115 V_{RMS}/60 Hz I_{AC} = 15.5 A_{RMS}
Efficiency						
	η		97.2		%	230 V_{RMS}/50 Hz I_{AC} = 4.5 A_{RMS}
	η		97.6		%	230 V_{RMS}/50 Hz I_{AC} = 8.8 A_{RMS}
	η		97		%	230 V_{RMS}/50 Hz

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
						I_{AC} = 15.5 A_{RMS}
	η		94		%	115 V_{RMS}/60 Hz I_{AC} = 3.8 A_{RMS}
	η		95.1		%	115 V_{RMS}/50 Hz I_{AC} = 9.5 A $_{RMS}$
	η		94.3		%	115 V_{RMS}/60 Hz I_{AC} = 15.5 A_{RMS}

1.5 Status LEDs

The following board LEDs define the PFC status:

- HV CAPACITOR DISCHARGE - LED7: lights up in red when the HVDC output voltage is higher than 30 V_{DC} (voltage between HVDC and GND_DC terminals)

Danger: *While LED7 is red, the DC output capacitor is not discharged and could provoke a serious electrical shock*

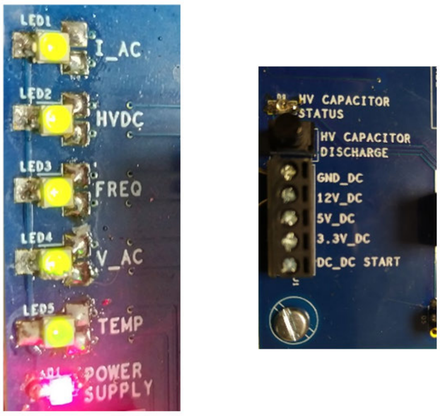
- POWER_SUPPLY - LED6: lights up in red when the PFC totem pole board is powered
- PFC STATUS LEDs (LED 1/2/3/4/5): at board startup, all these LEDs are alternatively lit in red, then orange, green and then OFF. This indicates the microcontroller has finalized the initialization procedure (right mains connection, line frequency measurement, power supply available, etc.) and the board is ready to be used. From this moment, the DC output capacitor can be charged when the HVDC switch (SW1) is in the ON position.

Table 6. Status LEDs

LEDs definition	LEDs state	Comments
IAC (LED1)	OFF	PFC board not supplied
	GREEN	IAC < 16 A_{RMS}
	RED	IAC_Peak > 25 A
HVDC (LED2)	OFF	PFC board not supplied
	GREEN	HVDC = 400 V_{DC}
	GREEN FLASHING	DC output capacitor in charge
	ORANGE	HVDC < 380 V_{DC}
	RED	HVDC > 450 V_{DC}
FREQ (LED3)	OFF	PFC board not supplied
	GREEN	45 Hz < AC Line frequency < 65 Hz
	ORANGE	AC Line frequency < 45 Hz
	RED	AC Line frequency > 65 Hz
VAC (LED4)	OFF	PFC board not supplied
	GREEN	85 V_{RMS} < V_{AC} < 264 V_{RMS}
	ORANGE	V_{AC} < 85 V_{RMS}
	RED	V_{AC} > 264 V_{RMS}
TEMP (LED5)	OFF	PFC board not supplied
	GREEN	Heat sink temperature < 120 °C
	ORANGE	N.A.

LEDs definition	LEDs state	Comments
TEMP (LED5)	RED	Heat sink temperature > 120°C

Figure 6. **PFC status LEDs overview**



2 Board connection and startup

2.1 Mechanical switches and potentiometer configuration

Step 1. Push the FC switch (SW1) on OFF position

Step 2. To control the inrush current by SCRs with a constant progressive phase control, push the ICL_PEAK switch (SW2) on VAR position. The constant progressive phase control value is defined by the max. inrush current potentiometer (R30)

Step 3. To control the inrush current by SCRs with a variable progressive phase control, push the ICL_PEAK switch on FIX position.

Step 4. The max. inrush current potentiometer (R30) value is read only by the MCU if the ICL_PEAK switch is set to VAR position. Max. inrush current potentiometer is used to define the constant progressive phase control value. The DC capacitor charge speed can be increased if the allowed peak current is increased. For this purpose, the max. inrush current potentiometer has to be turned clockwise.

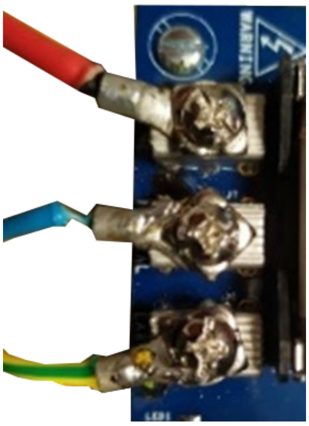
Figure 7. STEVAL-DPSTPFC1 switches and potentiometer

1. PFC switch (SW1)
2. ICL_PEAK switch (SW2)
3. Max. inrush current potentiometer (R30)

2.2 AC line wires connection

Step 1. Connect the line (L), neutral (N) and earth (PE) wires with J3, J6 and J7 headers, respectively, to an unpowered mains plug.

Figure 8. **AC line wire connection overview**



2.3 Output DC load connection

Step 1. Connect the DC load between the HVDC and GND_DC connectors.

Figure 9. **STEVAL-DPSTPFC1 output HVDC connection**

If an electronic DC load is used:

– connect the positive input of the electronic DC load to HVDC connector
– connect the negative input of the electronic DC load to GND_DC connector

2.4 PFC board power on

Step 1. Put the AC line voltage ON.

Danger: *Do not touch components under the AC line voltage.*

The power supply LED6 lights up in red to signal the PFC totem pole board is powered. The PFC status LEDs (LED1/2/3/4/5) blinking sequence is red, orange, green. At board startup, parameters like VAC, IAC, temperature and current sensor are checked. After board initialization, the PFC status LEDs light up as per the table and figure below.

Table 7. STEVAL-DPSTPFC1 LEDs

Definition	State
I_AC - LED1	OFF
HVDAC - LED2	OFF
FREQ - LED3	Green light
V_AC - LED4	Green light
TEMP - LED5	Green light
POWER SUPPLY - LED6	Red light

Figure 10. LED status overview

1. PFC status LEDs (LED1/2/3/4/5)
2. Power supply (LED6)

2.5 PFC startup

Step 1. Slide the PFC switch (SW1) to ON to start up the PFC totem pole board (see Figure 7)
The PFC status LEDs must light up as per the following table and Figure 6.

Table 8. PFC LED status

Definition	Status
I_AC - LED1	Green light
HVDAC - LED2	Green light
FREQ - LED3	Green light
V_AC - LED4	Green light
TEMP - LED5	Green light
POWER SUPPLY - LED6	Red light
HV_CAPACITOR STATUS	Red light

2.6 PFC board turn off

Step 1. Slide the PFC switch (SW1) to OFF position to start up the PFC totem pole board (see Figure 7)
The PFC status LEDs must light up as per the following table and Figure 6. PFC status LEDs overview.

Table 9. PFC LED status

Definition	Status
I_AC - LED1	OFF
HVDAC - LED2	OFF
FREQ - LED3	Green light
V_AC - LED4	Green light
TEMP - LED5	Green light
POWER SUPPLY - LED6	Red light
HV_CAPACITOR STATUS - LED7	OFF

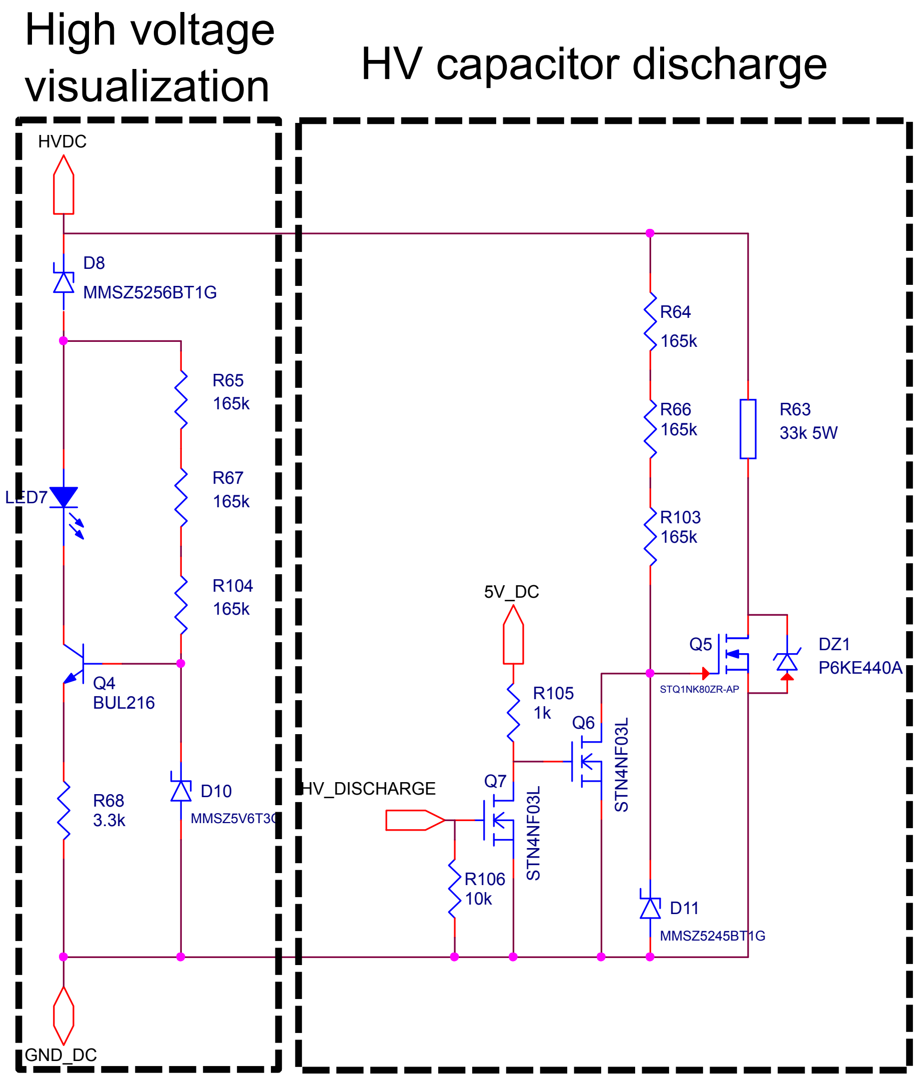
Note: HV_CAPACITOR STATUS (LED7) switches off after an interval of time that depends on the DC load impedance (around 3 minutes if no DC load is connected to the HVDC output).

Danger: *When HV_CAPACITOR STATUS (LED7) lights up in red, the DC output capacitor is not discharged and could provoke a serious electrical shock. This LED remains switched on as long as the HVDC voltage remains above 30 V.*

3 DC bus capacitor discharge

A circuit has been implemented to accelerate the output DC capacitors (C76, C77 and C78) discharge through R63 resistor. This circuit is turned on every time the PFC board is in OFF state. The full discharge time takes around 3 minutes when no DC load is connected. LED7 (HV CAPACITOR DISCHARGE) is lit up as long as the HVDC voltage remains above 30 V.

Figure 11. DC bus capacitor discharge circuit



4 Additional external components

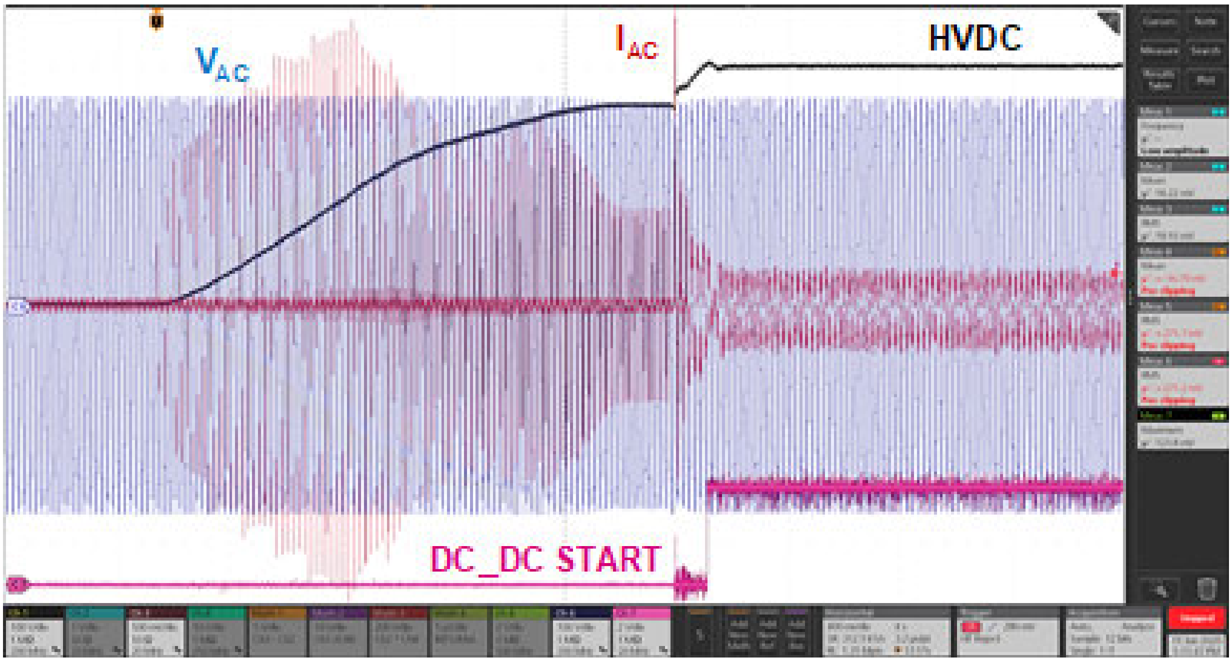
The STEVAL-DPSTPFC1 board allows adding some external components to the front-end circuit.

4.1 DC-DC circuit connection

A DC-DC converter can be connected to the HVDC bus via HVDC (J3) and GND_DC (J8) connectors. To allow the correct operation of the STEVAL-DPSTPFC1 front-end circuit, the DC-DC converter has to be activated after the PFC_START signal has been set to high level state. The PFC_START signal indicates the PFC is operational and the HVDC output voltage is 400 V_{DC}. This signal refers to GND_DC terminal and is available from the J1 header.

Figure 12. **DC-DC converter activation (DC_DC_Start signal) when PFC totem pole is operational**

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



4.2 Motor inverter connection

An inverter can be added behind the HVDC bus output. A 12 V positive output, referred to the DC Bus Ground (GND_DC), is available on header J1 to supply an IPM module, if needed.

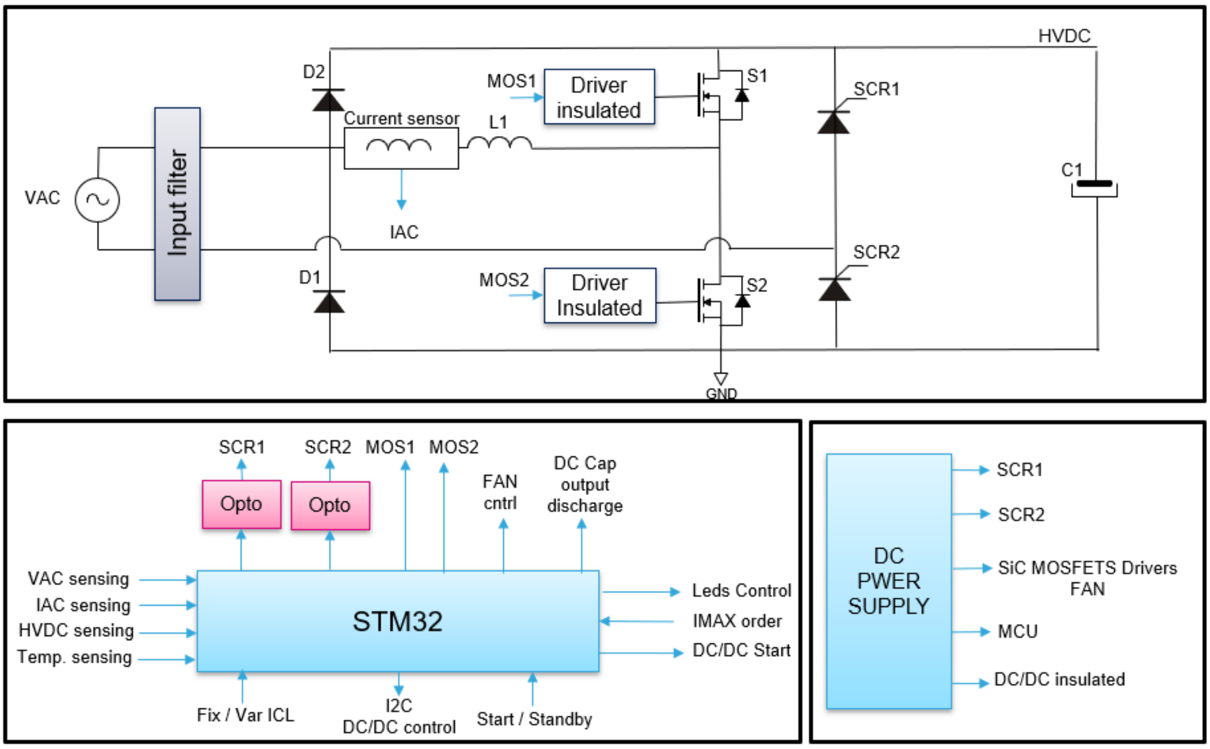
4.3 Control through an external microcontroller

Instead of using the embedded MCU daughter board, the STEVAL-DPSTPFC1 can be controlled through an external MCU daughter board to directly check the compliance of its firmware with this board circuit. For pin numbers and names of the daughter board connectors, refer to the external connectors section shown in Figure 87. STEVAL-DPSTPFC0 circuit schematic (1 of 4).

5 Totem pole PFC control

5.1 Bridgeless PFC totem pole overview

Figure 13. **Bridgeless PFC totem pole synoptic**



The figure above highlights the main components:

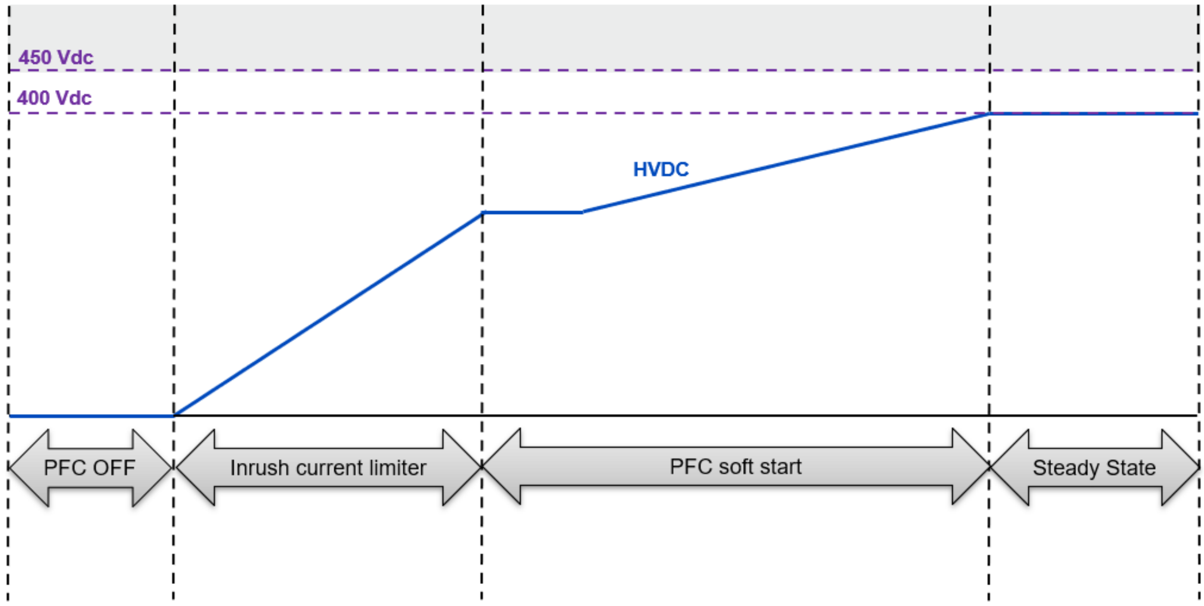
- SCRs (SCR1 and SCR2) in the bridgeless PFC totem pole to:
  - control inrush current at board startup
  - disconnect the DC link bus (HVDC) from the AC line voltage
- SiC MOSFETs (S1 and S2) to shape the input AC line current
- STGAP2S drivers to control SiC MOSFETs
- an STM32 MCU which mainly drives SCRs and SiC MOSFETs
- a flyback power converter providing:
  - 5V_SCR1: 5 V_{DC} insulated output. This supply is used to control SCR1
  - 5V_SCR2: 5 V_{DC} insulated output. This supply is used to control SCR2
  - 12V_DC: 12 V_{DC} insulated regulated output referenced to the DC bus ground (GND_DC). This supply is used to supply the insulated DC-DC converter (needed by SiC MOSFETs) and the fan. From this 12 V_{DC}:
    - a 5V_DC is created to supply current sensor
    - a 3V3_DC is created to supply the PFC board control and all the control circuits

5.2 Soft start

To ensure a smooth PFC startup, a soft start procedure has been implemented in the STM32 MCU:

- to reduce the inrush current at board startup, SCRs are controlled by a progressive phase control and the output DC capacitor can smoothly increase up to the AC line peak voltage
- to reduce the inrush current when the PFC output voltage (HVDC) switches from the peak AC line voltage to regulated 400 V_{DC}
- once the PFC output voltage reference is reached, the PFC output DC voltage (HVDC) is regulated according to output and input conditions

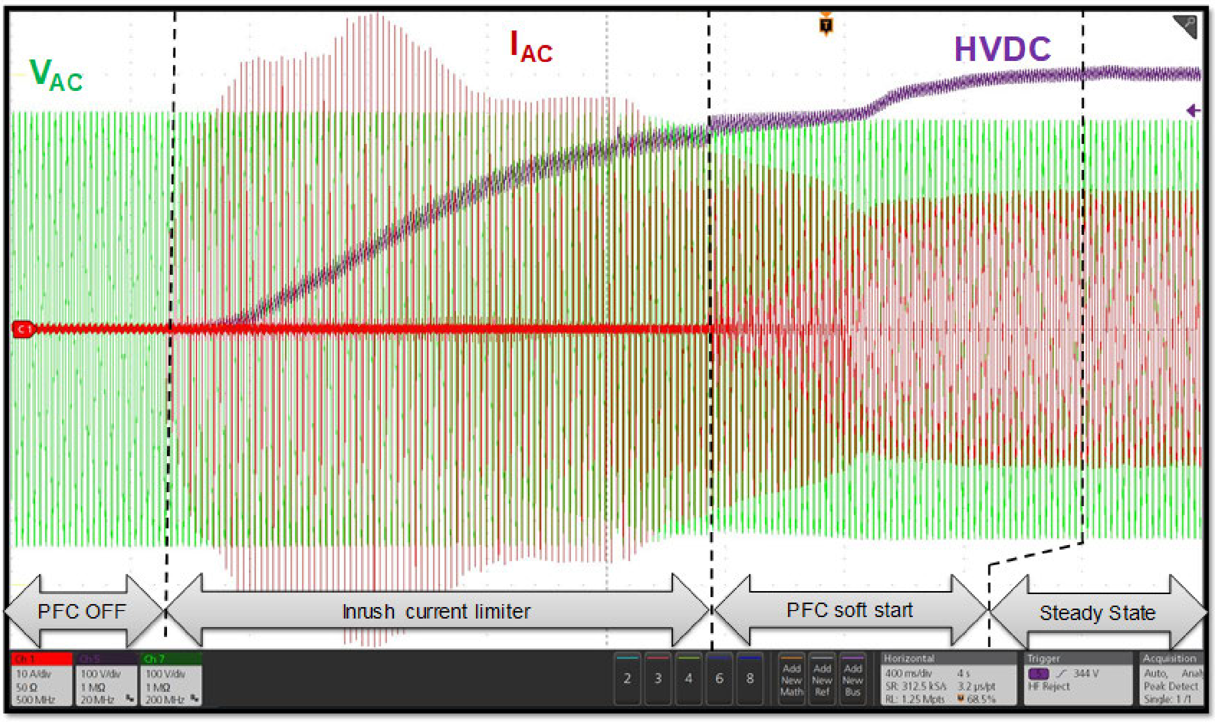
Figure 14. **PFC soft start principle**



The following figure shows an example of the described progressive PFC soft start. Tests have been performed at board startup with the board connected to a 230 V 50 Hz grid (V_{AC}) with a 3.3 kW DC load.

Figure 15. **PFC soft start procedure**

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



5.3 Inrush current control

5.3.1 IEC 61000-3-3 standard

The IEC 61000-3-3 standard gives the limitation of voltage changes and fluctuations for equipment with rated RMS current lower than 16 A when connected to a public low voltage grid.

If a too high current is sunk from the grid, the equipment causes these voltage fluctuations and voltage drop occurs due to the line impedance.

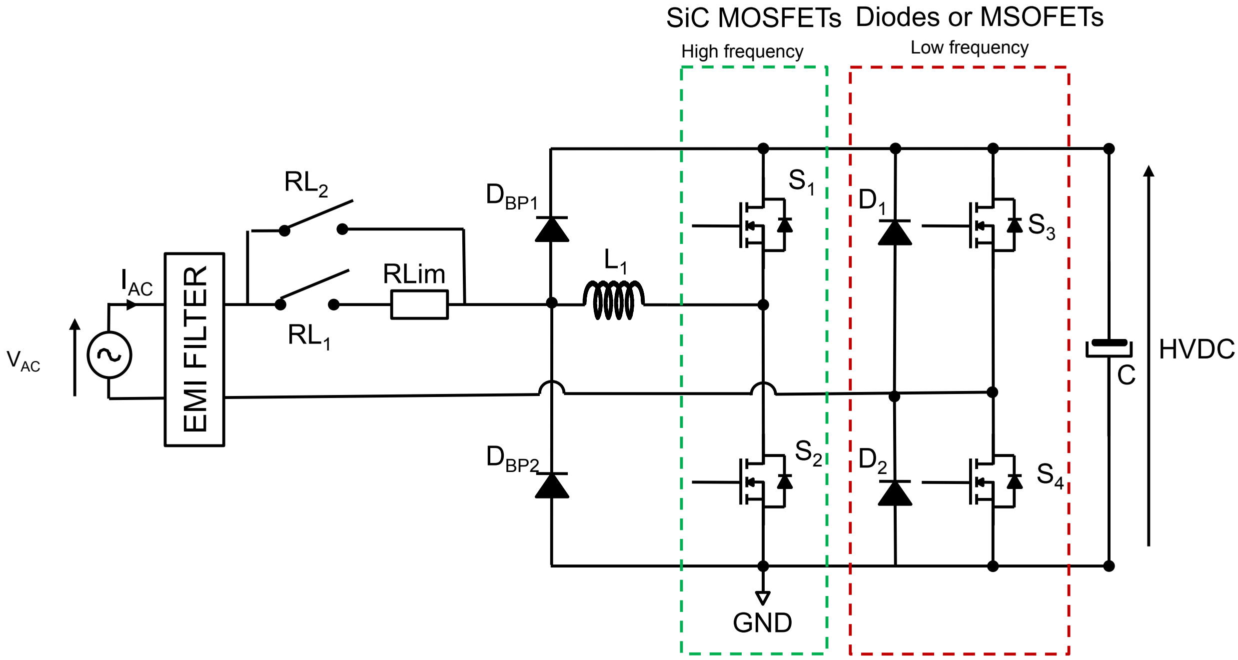
The mains voltage fluctuation causes undesired brightness variation of lamps and displays (flicker phenomenon). For this reason, you should keep the inrush current sunk by your equipment lower than the specified limits.

5.3.2 Inrush current controlled by NTC resistor

Usually, the PFC totem pole uses diodes (D1/D2) or a standard MOSFET (S3/S4) operating at low frequency. However, MOSFETs or diodes need a resistor or an NTC (RLim) to control the inrush current at board startup. The resistor has then to be bypassed by a relay (RL2) to limit the power losses during steady state operation. To disconnect the DC bus in standby mode, a second relay (RL1) is required. In steady state operation, this solution increases global power losses due to the relay contact resistor as well as the PFC converter cost.

Note: The contact resistor value increases according to the number of operating cycles and, therefore, decreases PFC efficiency.

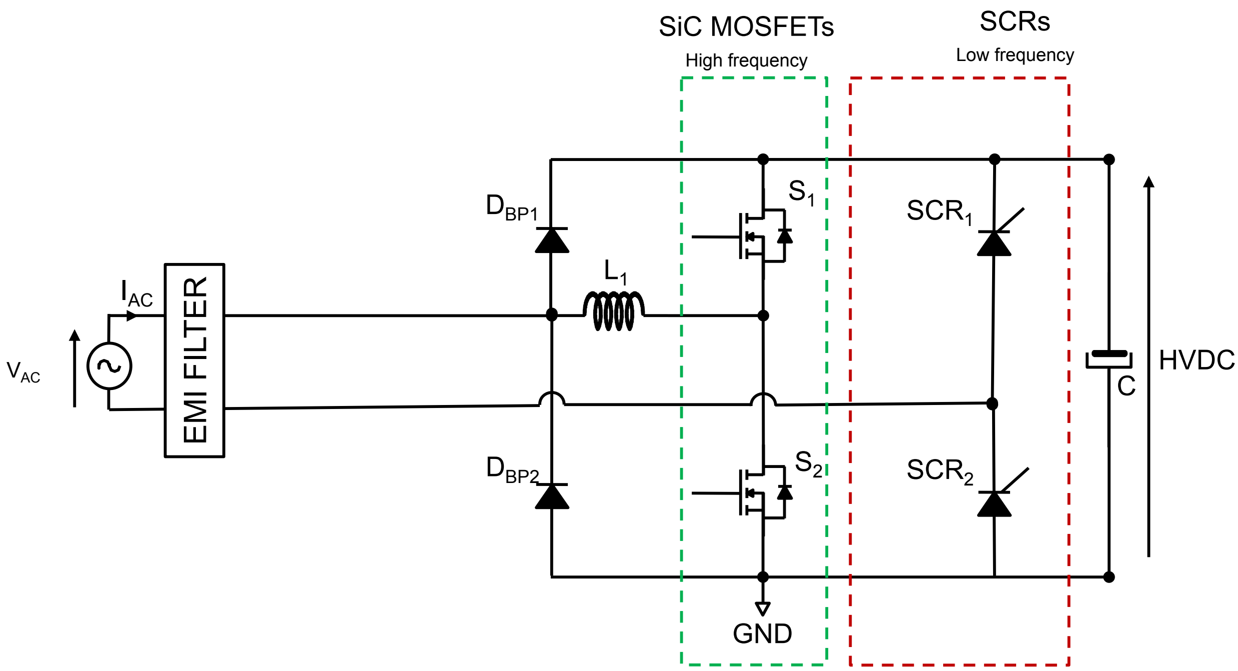
Figure 16. **PFC totem pole topology with NTC resistor**



5.3.3 Inrush current controlled by SCRs

With the totem pole PFC the capacitor can be smoothly charged with a progressive phase control and avoid the use of an NTC or a resistor thanks to SCRs.

Figure 17. **PFC totem pole topology with SCRs**



As long as SCRs are not triggered, the bridge does not conduct current and the DC bus capacitor is not charged. To start charging the DC capacitor, SCR1 and SCR2 have to be turned on according to the AC line voltage polarity (SCR1 is turned on when the AC line polarity is negative and SCR2 is turned on when the AC line polarity is positive). To reduce the inrush current, SCRs are alternatively triggered at the end of the half line voltage cycle, just few hundreds of microseconds before the line zero voltage. This allows the output capacitor to be charged to a low level (around 10 to 30 V) and not directly to the peak line voltage. The current driven from the line is then much lower than in case of a direct full charge of the DC capacitor.

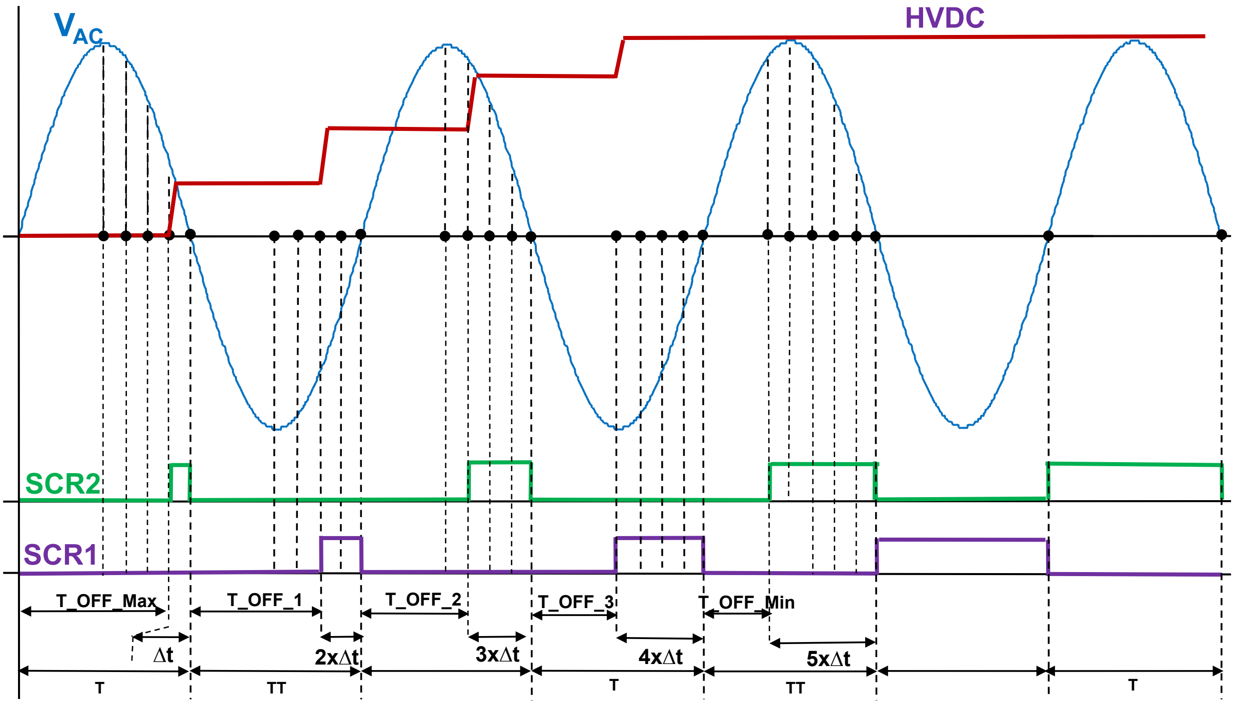
This soft start solution can work only when an inductor is present on the line side as the rate of current increase has also to be limited to prevent SCRs damage. The inductor is already present for most applications where the EMI filter usually embeds a common mode choke which has a differential mode parasitic inductor due to the copper turns of the windings.

To control the inrush current at PFC board startup with SCRs, two solutions have been implemented in the MCU firmware: fixed SCRs on delay and variable SCRs on delay

Fixed SCRs on delay

To allow a complete charge of this capacitor to the peak line voltage, SCRs have to be triggered on the subsequent half cycle with a shorter turn on delay than the one used to start charging. With V_{AC}, the AC line voltage and HVDC represent the PFC output voltage.

Figure 18. HV capacitor charges controlled by SCRs



By reducing SCRs turn-on delay by few tens or hundreds of microseconds from half-cycle to half-cycle, the output capacitor is progressively charged while the line current is kept low. The step of SCRs turn-on delay reduction is constant from one half-cycle to the following one.

The step of SCRs turn-on delay is defined by reading the `MAX_INRUSH CURRENT` potentiometer value on the PFC totem pole board (see Eq. (1)). In the firmware, the step of SCRs turn-on delay is called `Delta_Phase_Angle_µs`. `Step_Phase_Control_Min_µs` is the allowed minimum step of SCRs turn-on delay (30 µs) and the `Delta_Phase_Control_Max_µs` parameter is the allowed maximum step of SCRs turn-on delay (200 µs).

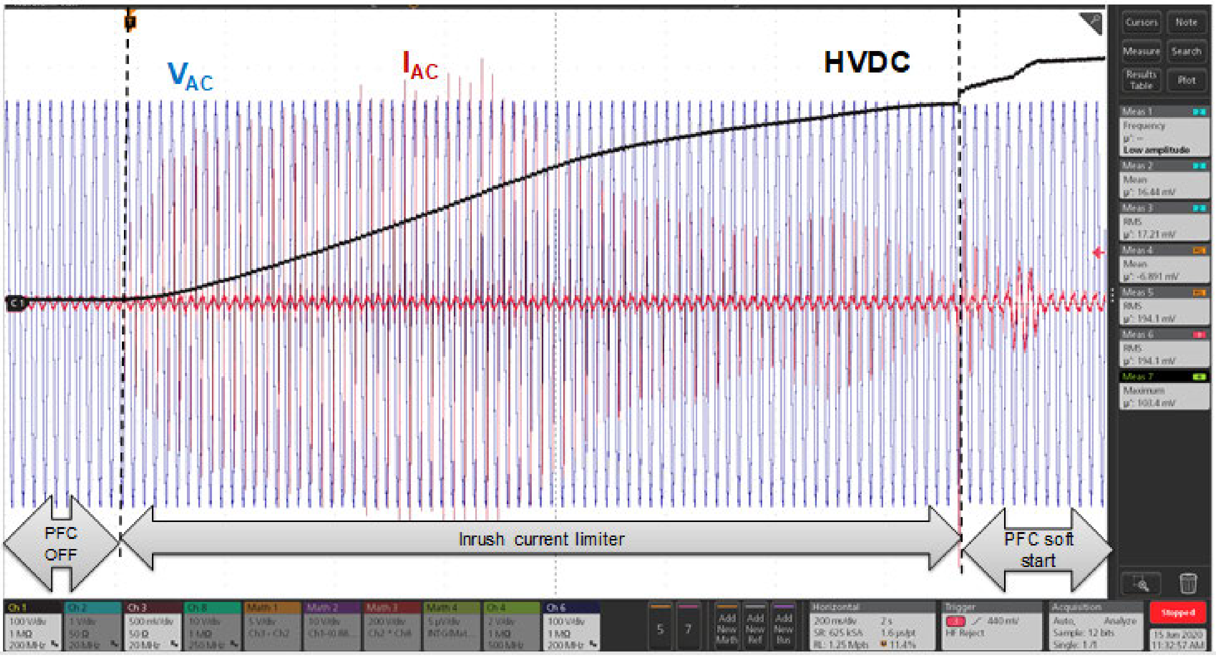
$$Delta\_Phase\_Angle\_\mu s = \frac{Delta\_Control\_Max\_\mu s \times ADC\_Value}{2^{12}} + Step\_Phase\_Control\_Min\_\mu s \quad (1)$$

When the SCRs turn-on delay is lower than 3 ms, the SCRs gate pulse is directly set to a continuous DC pulse according to the AC line polarity (SCR1 is set to continuous DC pulse when the AC line polarity is negative and SCR2 is set to continuous DC pulse when the AC line polarity is positive). Below approximately a 5 ms or 4.2 ms delay (respectively for 50 and 60 Hz line frequency), the output DC capacitor is fully charged. So it is not necessary to ensure a soft start for turn-on delays much lower than a fourth cycle. In the firmware, the SCRs turn-on delay to switch SCRs to a continuous DC pulse is called `Phase_Control_ON_Max_µs`.

The following figure shows an example of progressive DC capacitor charge. The test has been performed at startup when the STEVAL-DPSTPFC1 board is connected to a 230 V 50 Hz grid without an output DC load, while the output DC capacitor is fully uncharged (i.e., its initial voltage is null). In these conditions, the maximum inrush peak current is around 30 A and the output capacitor is charged in 1.5 s.

Figure 19. Inrush current control at board startup (with fixed SCRs on delay)

HVDC=PFC output voltage
I_{AC} = AC line current
V_{AC} = AC line voltage



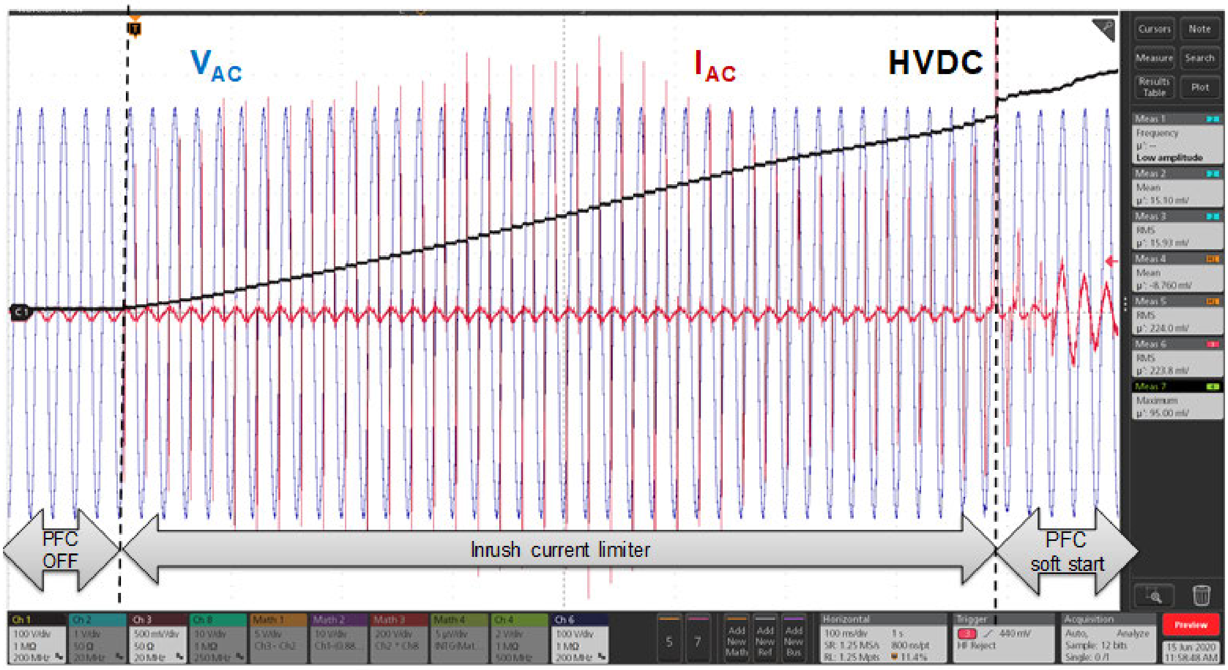
Variable SCRs on delay

The peak current during the output capacitor charge is not constant. Only the reduction step of the SCRs turn-on delay is constant. According to the time of the SCR turn-on, peak current can slightly vary from one period of the AC line voltage to another. In this case, a second solution has been implemented in the firmware: by reducing the SCRs turn-on delay defined in a look-up table, half-cycle to half-cycle, the output capacitor is progressively charged while the line current is kept low with a constant value.

The look up table is defined according to the AC line voltage model (equivalent inductance and resistance), the input common filter, the output DC bulk capacitor and the dynamic resistance of the SCRs and MOSFETs.

Figure 20. **Inrush current control at board startup (with variable SCRs on delay)**

HVDC=PFC output voltage
I_{AC} = AC line current
V_{AC} = AC line voltage



The look-up table listing the steps of SCRs turn-on delay reduction is defined by the `TAB_SCRs_Delay_us` table in the ICL_Current_Constant.h file.

Note: The look-up table has been defined without DC load connected at the output PFC.

5.3.4 Inrush current control flowchart

SCRs are controlled to limit the inrush current at board startup (refer to Figure 21).

At each AC line voltage zero cross (see Figure 22. ICL flowchart (1 of 2) and Figure 23. ICL flowchart (2 of 2)):

- SCRs are switched to OFF state
- a timer is initialized to reduce SCR control turn-on delay from half-cycle to half-cycle
- test end of ICL procedure is performed:
  - to check if the SCR turn-on delay is lower than 3 ms, the SCR gate pulse is directly set to a continuous DC pulse according to the AC line polarity (SCR1 is set to continuous DC pulse when the AC line polarity is negative and SCR2 is set to continuous DC pulse when the AC line polarity is positive). In the firmware, the SCR turn-on delay is called `Phase_Control_ON_Max_us`.
  - to check if the HVDC output DC voltage are charged at least 70% of the peak AC line voltage. In the firmware, this value is called `VAC_Rate_ICL_Min`.

At each timer interrupt:

- SCRs are controlled according to the AC line voltage polarity
- the SCR control turn-on delay decreases

Figure 21. SCR control management

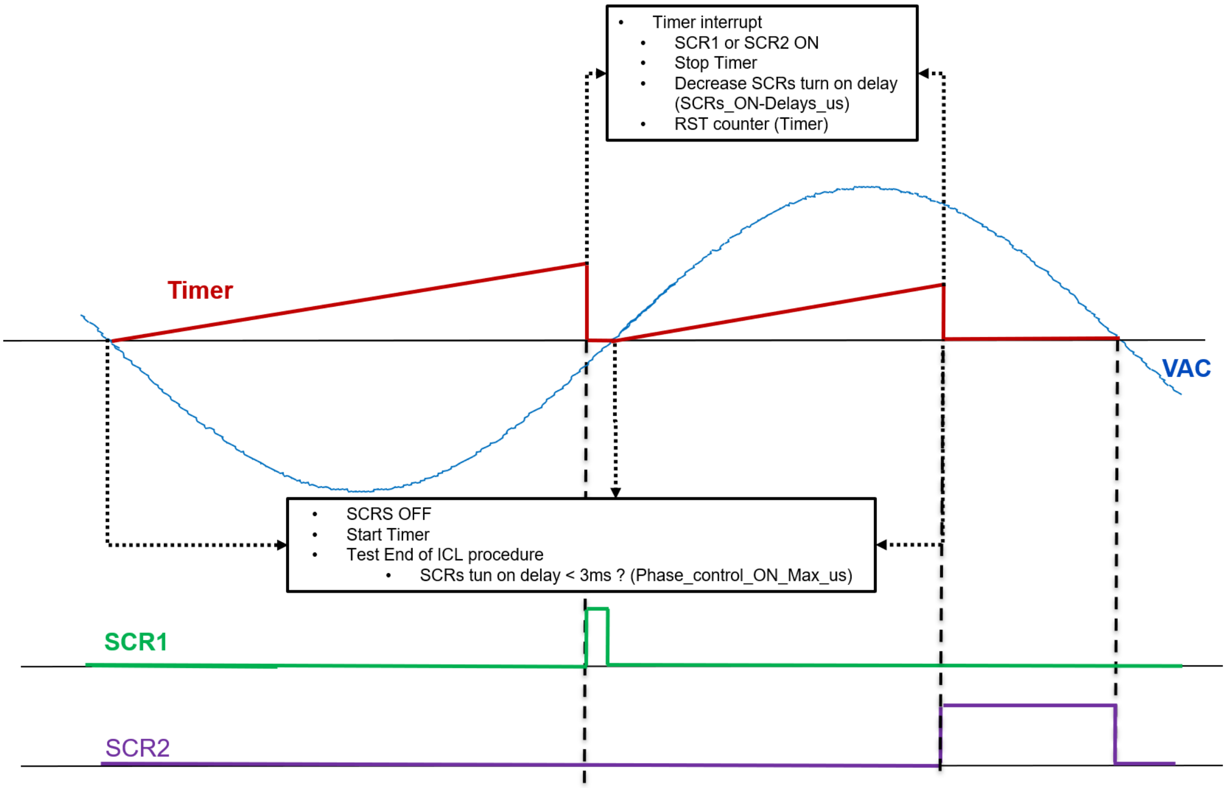


Figure 22. ICL flowchart (1 of 2)

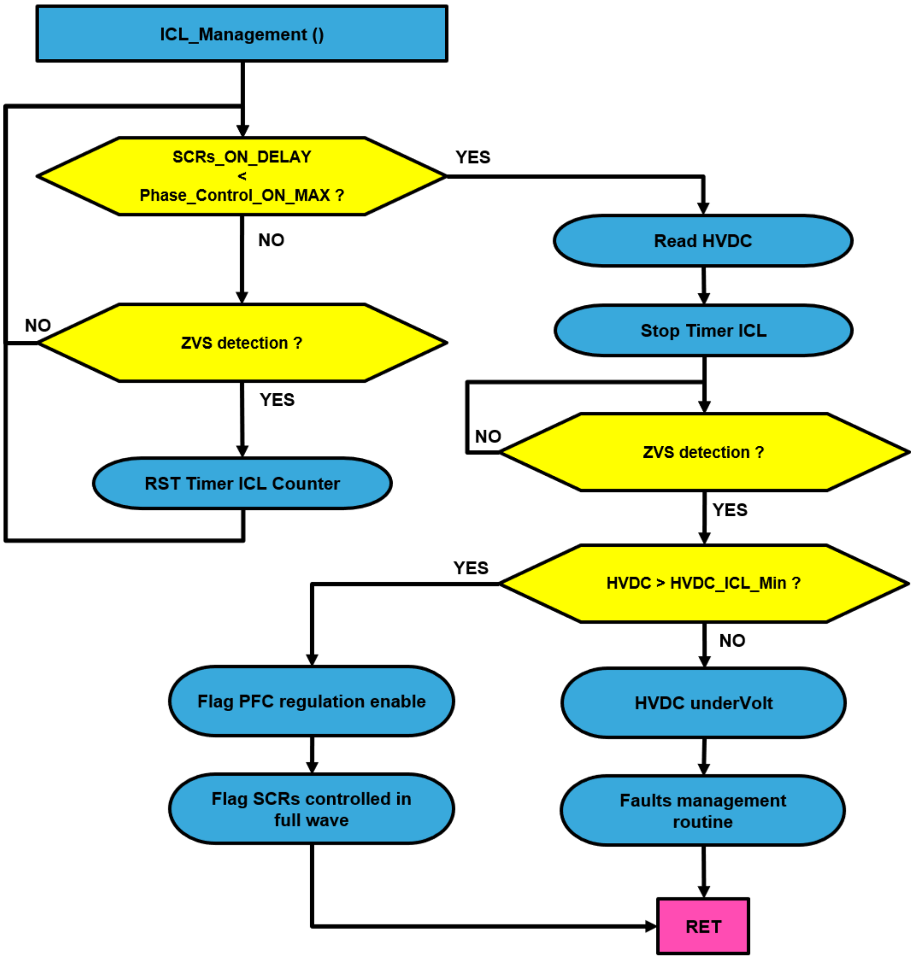
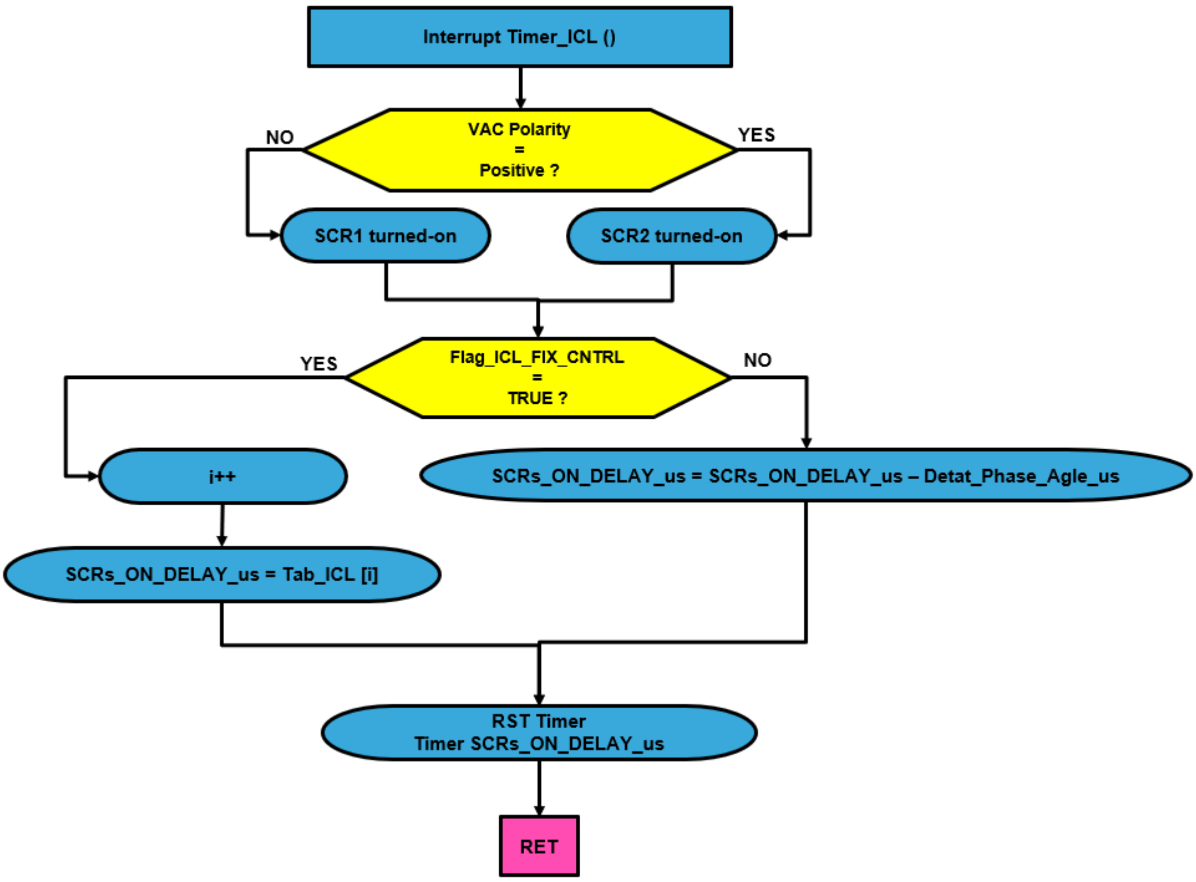


Figure 23. **ICL flowchart (2 of 2)**



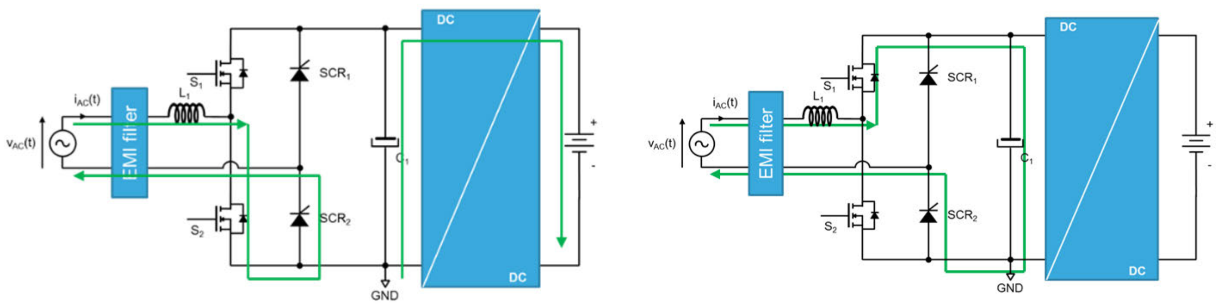
5.4 Steady state operation

The bridgeless PFC totem pole increases its efficiency by eliminating the diode bridge in the conventional PFC. It uses two SiC MOSFETs (S1 and S2) that operate at fixed PWM frequency and two SCRs (SCR1 and SCR2) which operate at AC line frequency.

During the positive AC line cycle, SCR2 is always ON and SCR1 is always OFF. S1 and S2 are controlled in synchronous mode. S1 and S2, together with the input inductor L1 and the output capacitor C1, form a boost converter topology. S2 switch increases the boost inductor current and S1 acts as freewheeling boost diode.

Figure 24. **Positive AC line cycle operation**

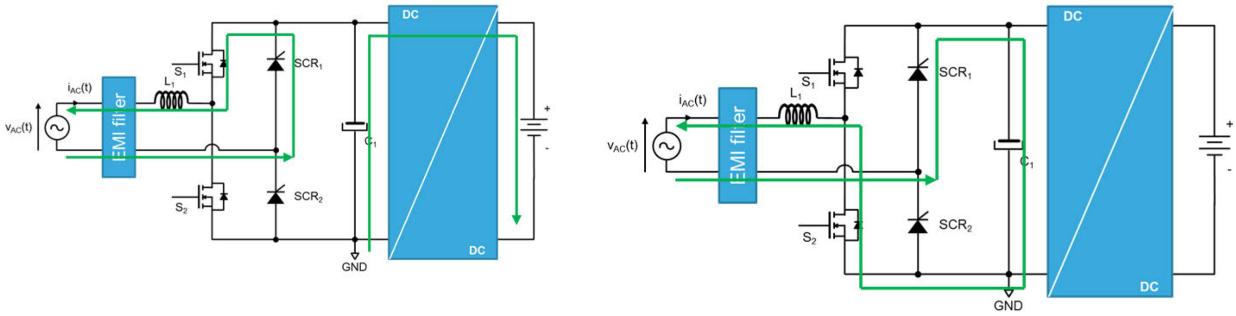
[0 ; d.TS] on the left
[d.Ts ; TS] on the right



During the negative AC line cycle, SCR1 is always ON and SCR2 is always OFF. S1 and S2 are controlled in synchronous mode. S1 and S2, together with the input inductor L1 and the output capacitor C1, form a boost converter topology. S2 switch increases the boost inductor current and S1 acts as a freewheeling boost diode.

Figure 25. Negative AC line cycle operation

[0 ; d.TS] on the left
[d.Ts ; TS] on the right

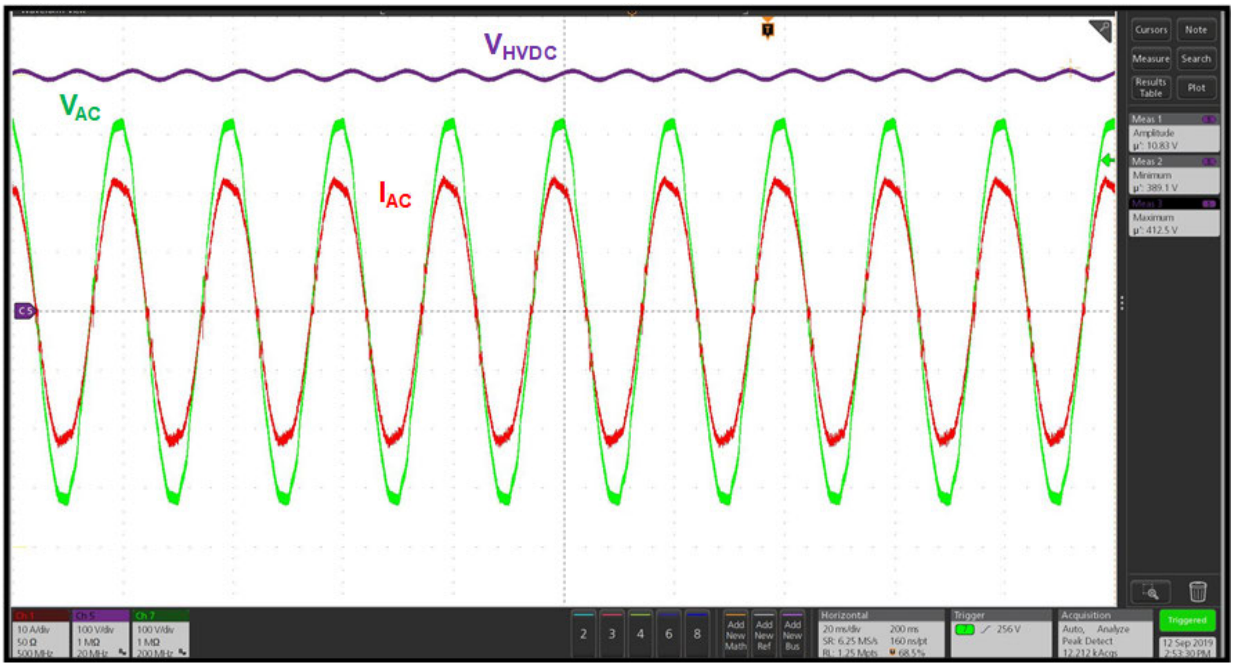


The following figure shows an example of the PFC totem pole behaviour in steady state operation with a 3.6 kW DC load and V_{AC} = 230 V_{RMS}.

Note: Under the previous conditions, the HVDC peak to peak ripple is around 15 V.

Figure 26. Steady state operation

HVDC = PFC output voltage
I_{AC} = AC line current
V_{AC} = AC line voltage



5.5 PFC soft start

After the inrush current control procedure, the internal voltage loop output increases from initial voltage under the soft start control to reduce the current stress due to all power switches. Once HVDC has reached 400 V_{DC}, the soft start control is released to achieve the desired regulation.

Figure 27. **PFC soft start**

HVDC = PFC output voltage
I_{AC} = AC line current
V_{AC} = AC line voltage

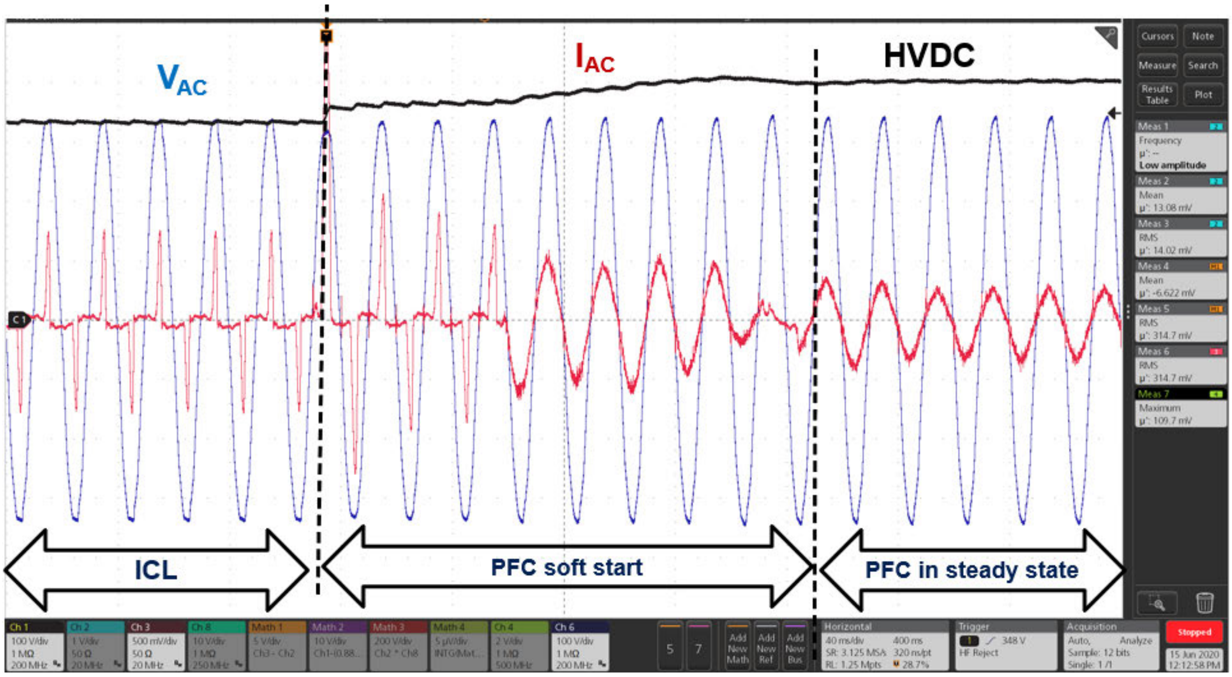


Figure 28 shows how the PFC soft start is managed after the inrush current control procedure. The soft start PFC management routine is called at each zero cross of the AC line voltage (see Figure 29). This routine increases the HVDC output voltage target up to 400 V_{DC}.

Figure 28. **PFC startup soft start management after inrush control procedure**

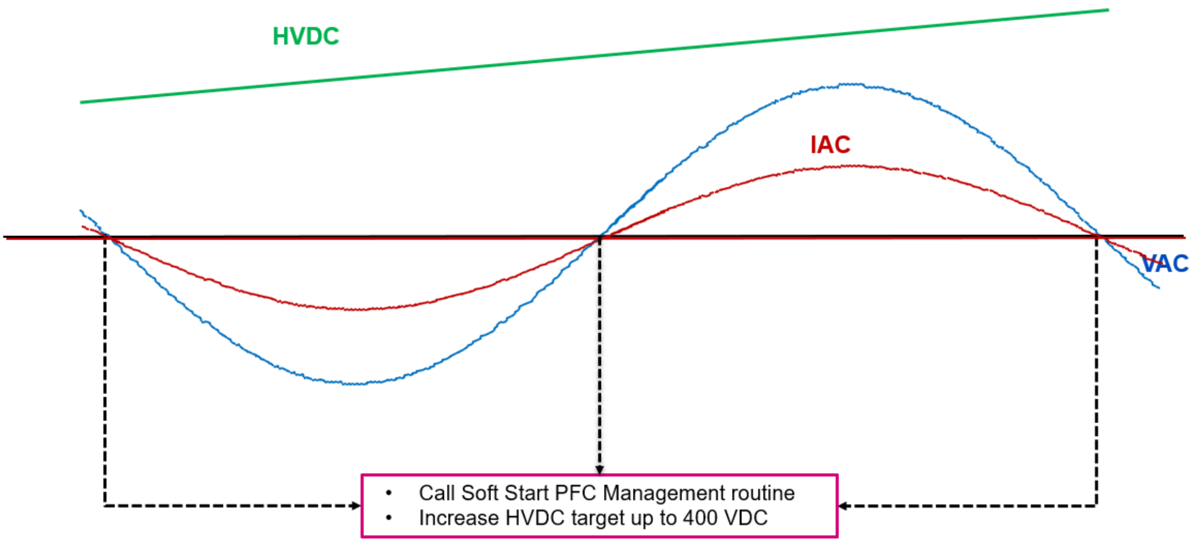
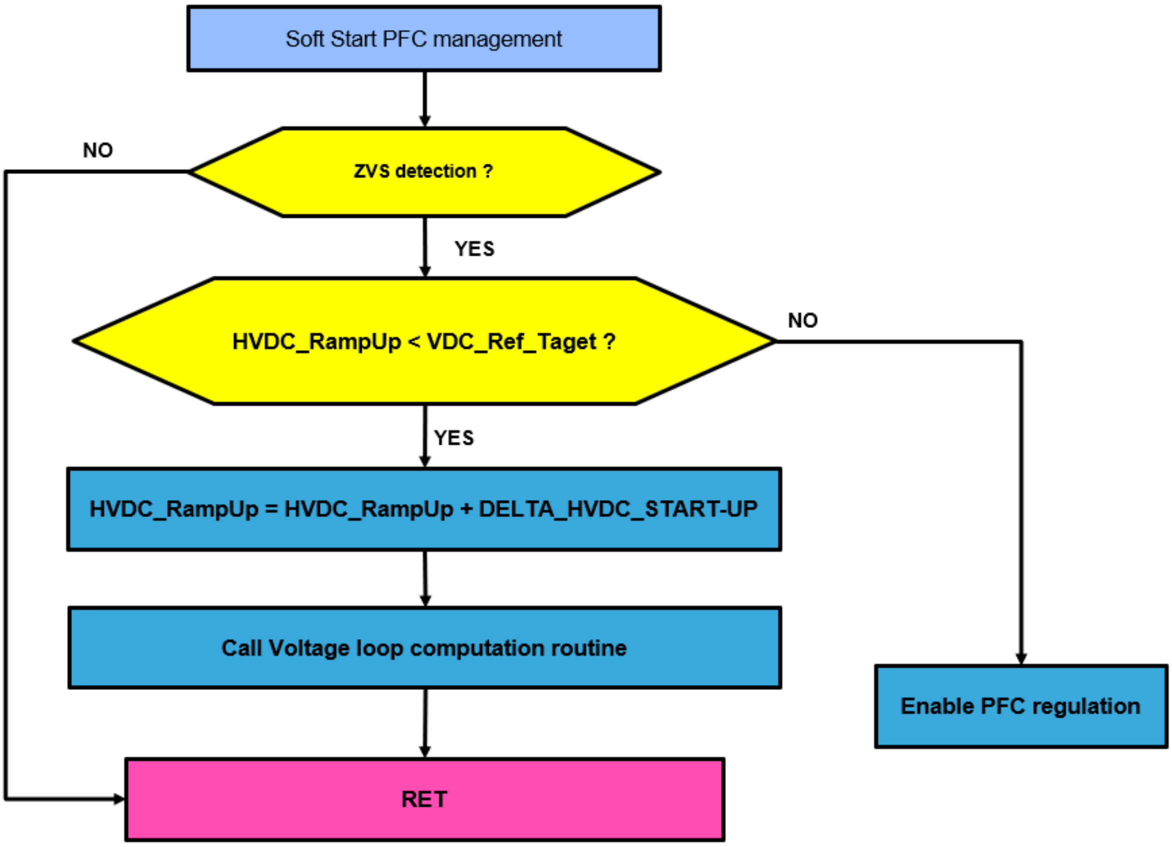


Figure 29. PFC startup soft start flowchart



6 Switch control

6.1 SiC MOSFET control

A digital PWM signal is used to control SiC MOSFETs though STM32 timer (TIM1). Digital TIM1 counter period is defined by Equation 2 where F_s is the PWM frequency fixed at 72 kHz and F_{CPU} is the STM32 oscillator frequency fixed at 72 MHz.

Note: The duty cycle of the PWM control is defined by the STM32 TIM1 CCR2 register.

$$TIM1_{Counter\_Period} = \frac{F_{CPU}}{F_s} = \frac{72 \times 10^6}{72 \times 10^3} = 1000 \quad (2)$$

The Duty cycle is clamped at the minimum (100 pulses) and the maximum (970 periods) of the digital TIM1 timer counter.

To improve the PFC totem pole bridgeless efficiency, S1 and S2 SiC MOSFETS are operating in synchronous conduction mode. Two complementary PWM signals (CH2 and CH2N) are used to control SiC MOSFETs. To avoid the short circuits due to a slight turns ON and OFF of SiC MOSFETs, a dead time (DT) has been added (see the following figure) with IL as the inductor current.

Figure 30. Synchronous SiC MOSFET control

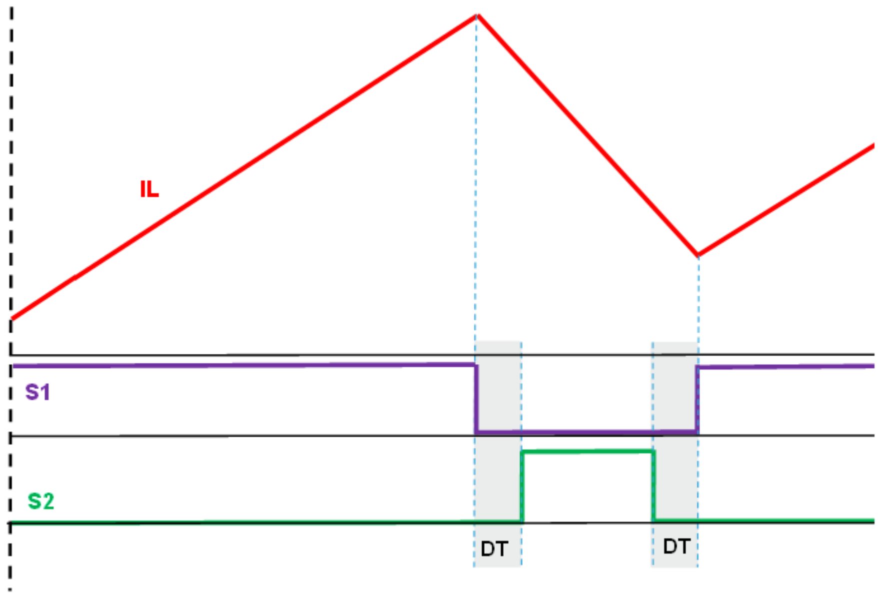
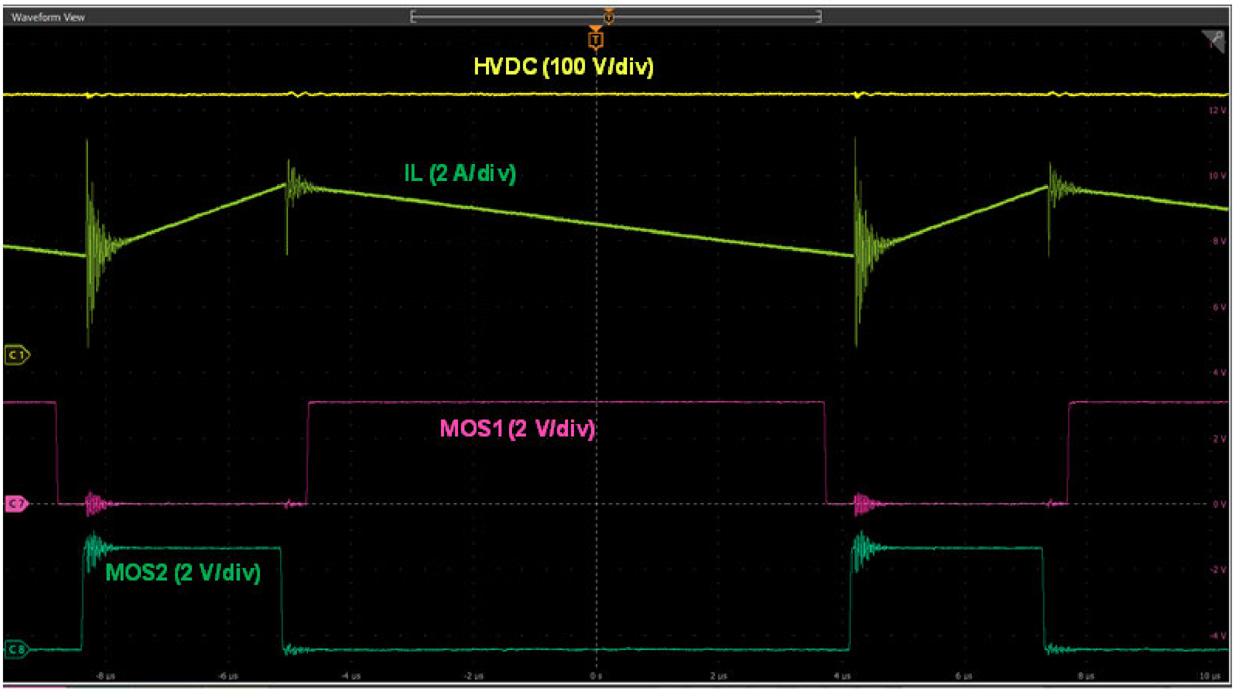


Figure 31. **Synchronous SiC MOSFET control waveform**



The digital dead time is called “DeadTime_MOSFET” in the firmware and this parameter is fixed at 20 periods of the TIM1 Timer.

$$DT = \frac{DeadTime_{MOSFET}}{F_S \cdot TIM1_{Counter\_Period}} = \frac{20}{72000 \cdot 1000} = 278\ ns \quad (3)$$

6.2 Zero cross current spike control

An input current (I_{AC}) spike is generated at each AC line zero cross (V_{AC}). This issue is related to the PFC totem pole. For example, during the negative AC line cycle, SCR1 is always on and SCR2 is always off and the PFC output voltage (400 V_{DC}) is applied across SCR2. S1 SiC MOSFET switch increases the boost inductor current and S2 SiC MOSFET acts as a freewheeling boost diode. When the AC line voltage polarity is changing from negative to positive AC line cycle, the duty cycle of the S1 SiC MOSFET changes from 100% to zero and the active S2 SiC MOSFET change from zero to 100%. The SCR1 voltage is then applied across the boost inductor and current spike is generated (see Figure 32 and Figure 33). The same phenomenon occurs with diodes or MOSFETs.

Figure 32. PFC totem pole topology

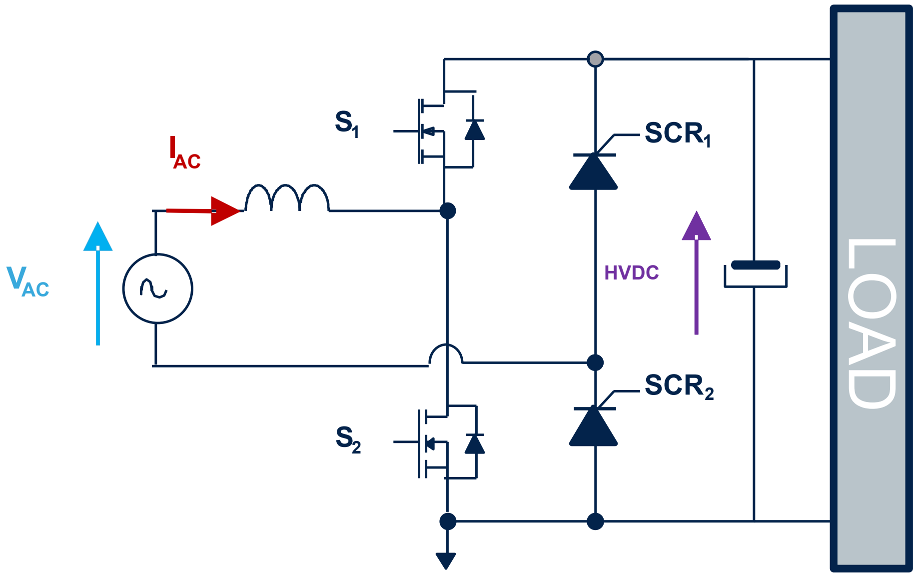
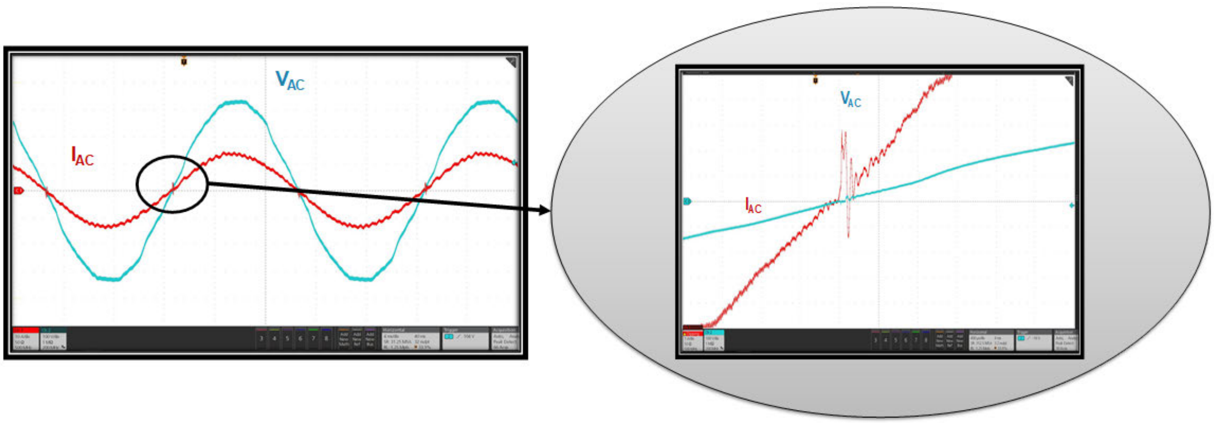


Figure 33. I_{AC} current spike at each AC line voltage zero crossing



To reduce this current spike at each zero cross of the AC line voltage, S1 or S2 active switches (according to the AC line polarity) are controlled by a small pulse width. This pulse is then gradually increased up to normal duty cycle.

Figure 34. Smart duty cycle control flowchart

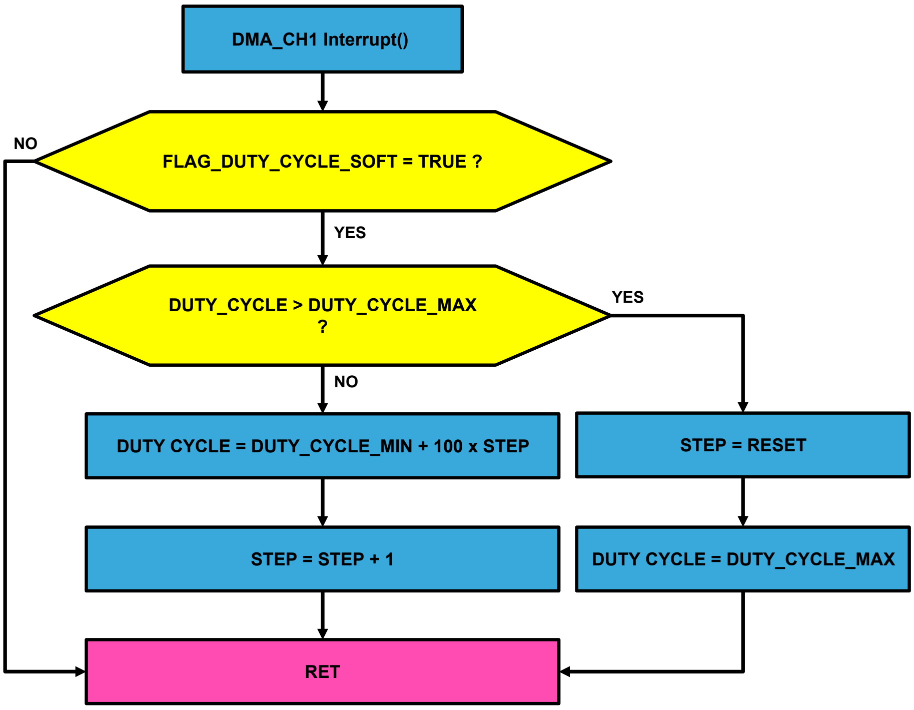
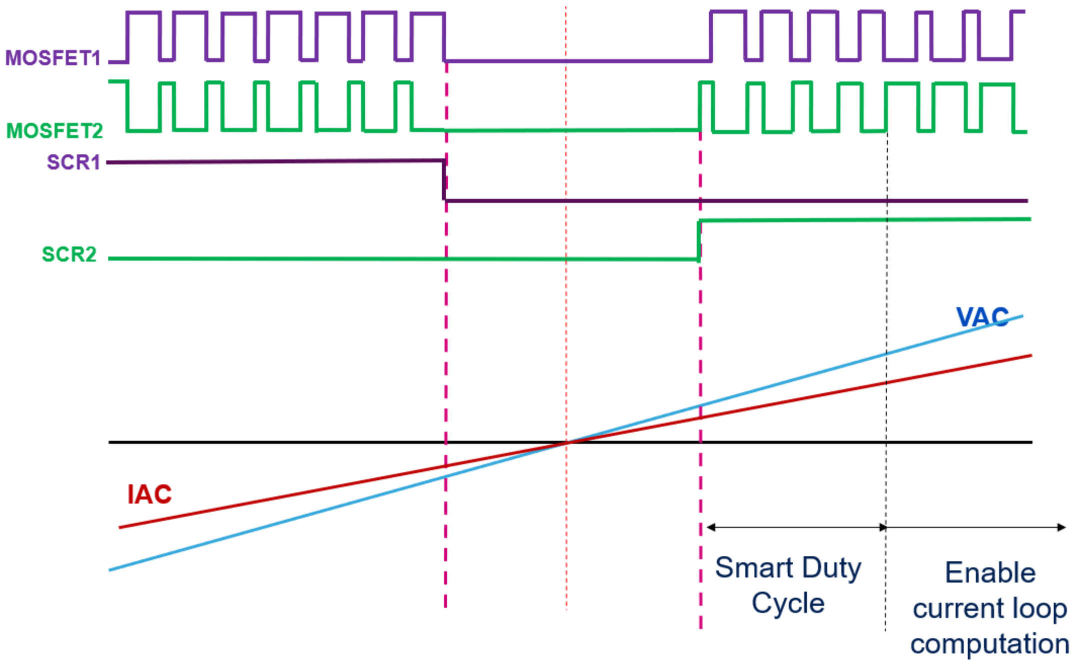


Figure 35. Soft duty cycle control principle



The following figures show how the AC line current spike peak is reduced thanks to this solution. During the smart duty cycle control, the control loop is frozen.

Note: At each zero cross of the AC line voltage, SCRs and SiC MOSFETs are turned off to ensure a safe permutation of the power switches control and to avoid short-circuiting the output DC capacitor.

Figure 36. Smart duty control principle

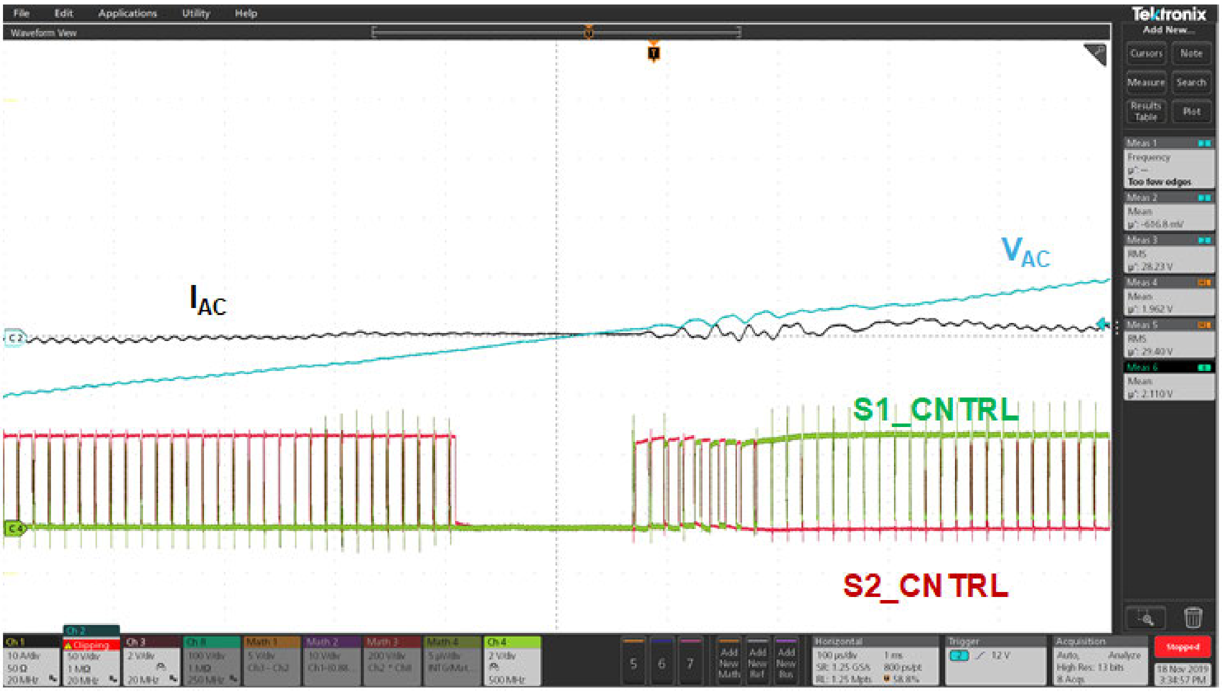


Figure 37. I_{AC} current spike at each AC line voltage zero crossing

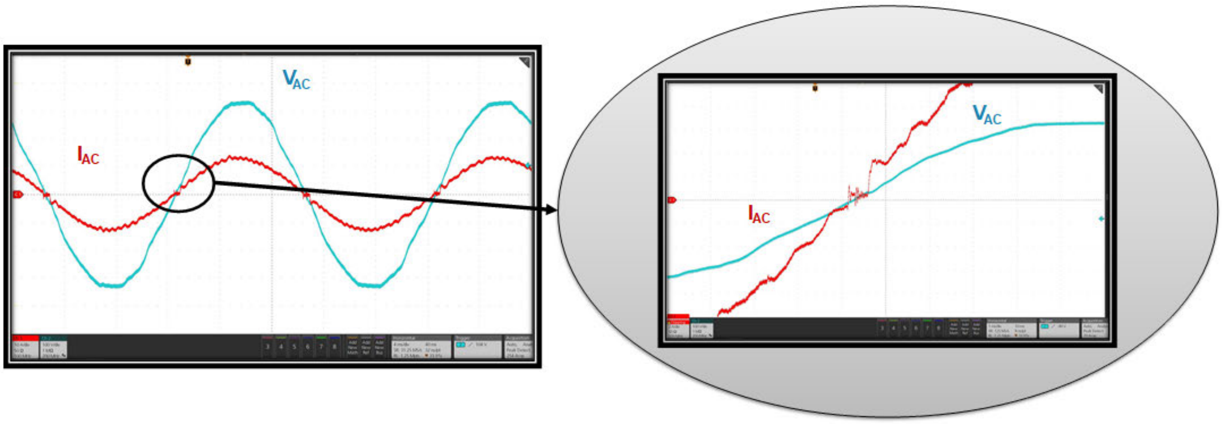


Figure 38 defines the common mode noise without smart duty cycle control and Figure 39 defines the common mode noise with smart duty cycle control with P_{OUT} = 800 W and V_{AC} = 240 V_{RMS}/50 Hz. Thanks to a smart duty cycle SiC MOSFET control, the common mode is widely reduced at each zero cross of the AC line voltage.

Note: For these two common mode noise measurements a snap ferrite has been connected to the AC line wires (Ref: 742 758 15 from Wurth).

Figure 38. Common mode without smart SiC MOSFET control

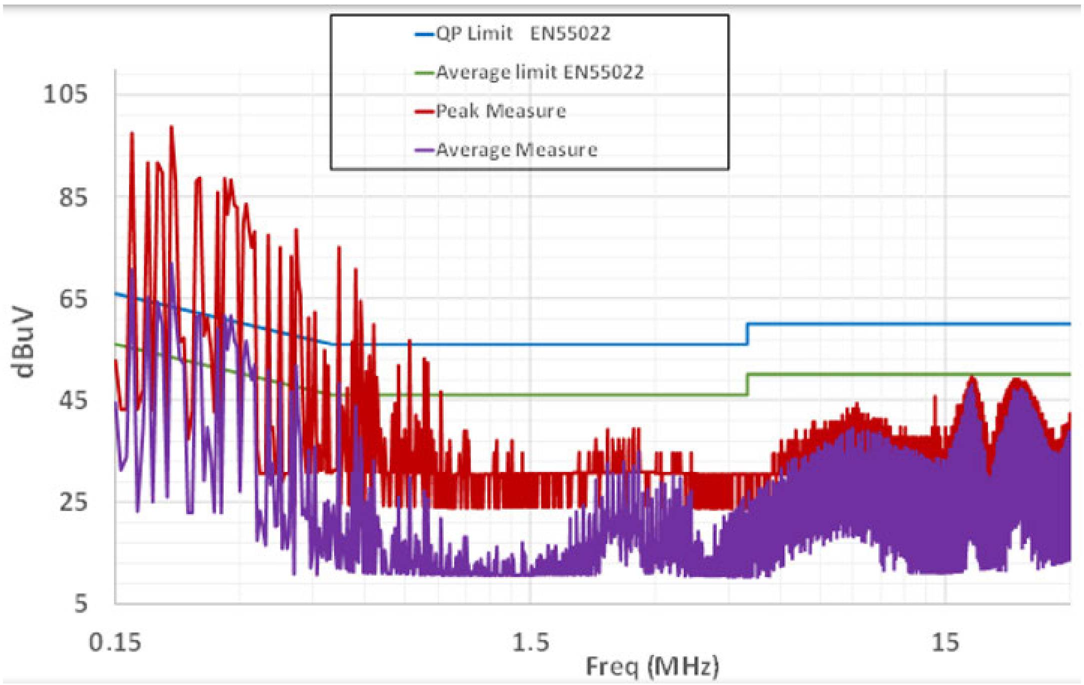
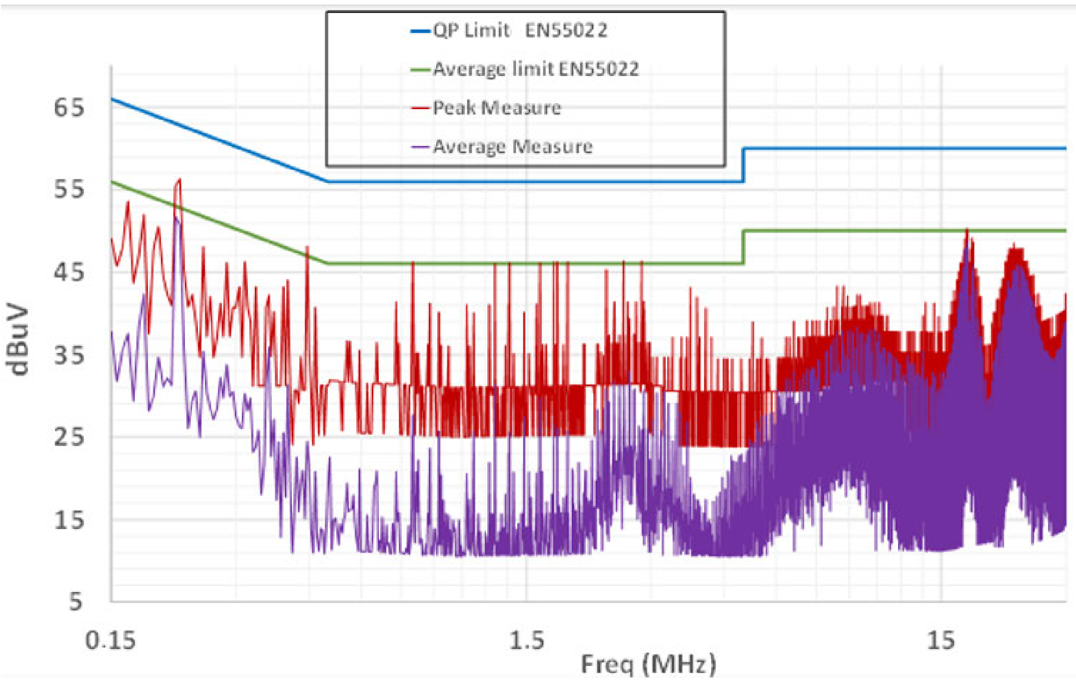


Figure 39. Common mode with smart SiC MOSFET control



7 PFC totem pole design

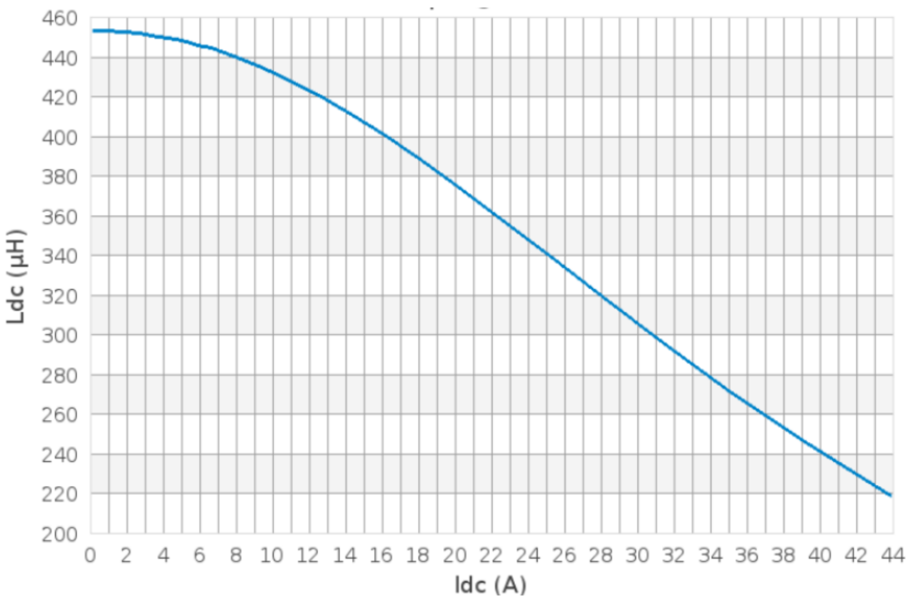
7.1 Input inductor design

The PFC choke is designed to keep the inductor current ripple under 20% of the maximum peak input current in CCM (16 A_{RMS}). Equation 4 defines the minimum inductance to operate in CCM at full load (3.6 kW). D is the duty cycle of S1 and S2 SiC MOSFETs. The minimum inductor value is defined when D = 0.5 (see Eq. (3)). HVDC is 400 V_{DC} output voltage and F_s is the 72 kHz frequency switching of S1 and S2 Sic MOSFETs.

$$L \geq \frac{D \times (1 - D) \times HVDC}{I_{L\_Ripple\_\%} \times F_s} = \frac{0.5 \times (1 - 0.5) \times 400}{0.2 \times 16 \times \sqrt{2} \times 72 \times 10^3} = 307\mu H \tag{4}$$

To meet the previous criterion with 10% of inductance tolerance, a 337 µH inductor has been selected for this PFC totem pole at the maximum peak input current in CCM (16 A_{RMS}).

Figure 40. **PFC estimated nominal inductance vs. current**



7.2 Output DC capacitor

The output DC capacitor is defined by the equations below according to the hold time and output voltage ripple regulation. In this evaluation board, the hold time is set to 1 half AC line cycle (45 Hz in the worst case). HVDC is 400 V_{DC} output voltage, the minimum normal operation output voltage is 290 V, the maximum input power is 3.6 kW and the output voltage ripple is set to 5%.

$$C_{OUT} \geq \frac{P_{OUT}}{2 \times \pi \times f \times HVDC \times HVDC_{Ripple}} = \frac{3600}{2 \times \pi \times 45 \times 400 \times 20} = 1.59mF \tag{5}$$

$$C_{OUT} \geq \frac{2 \times P_{OUT} \times t_{hold}}{HVDC^2 - HVDC_{\min}^2} = \frac{2 \times 3600 \times \frac{1}{2 \times 45}}{400^2 - 290^2} = 1.05mF \tag{6}$$

To meet the previous criteria with 20% of capacitor tolerance, 3 x 680 µF/450 V_{DC} electrolytic capacitors are connected in parallel.

7.3 Analog signal sensing

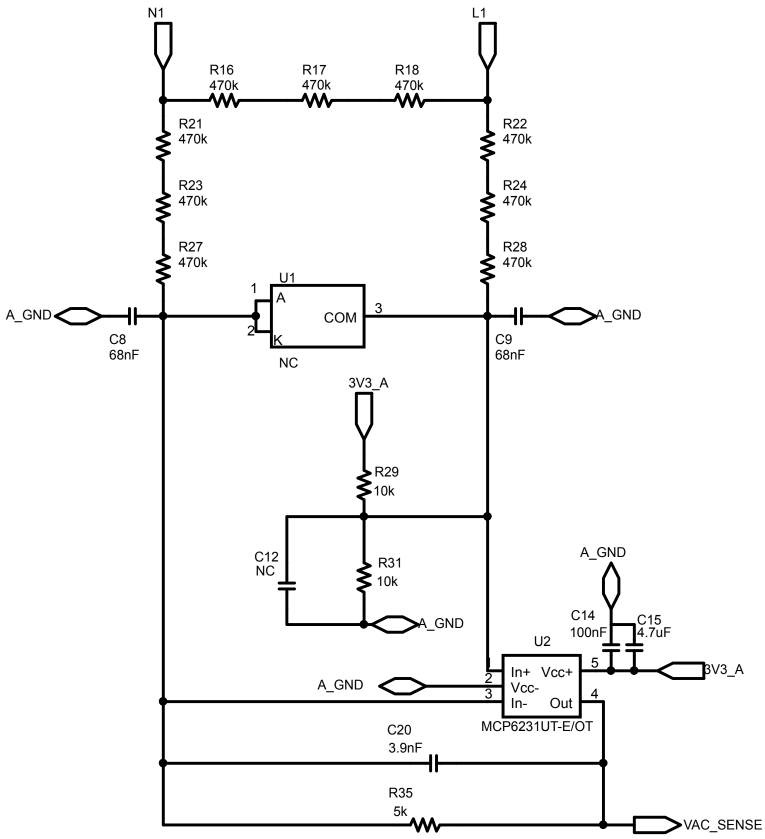
7.3.1 AC line voltage (V_{AC}) measurement

The AC line voltage (V_{AC}) measurement is mainly used to:

- control the inrush current at board startup
- shape the I_{AC} line current to the AC line voltage in PFC steady state operation
- detect the zero cross of the AC line voltage
- manage the AC line dips

A differential measurement is performed to measure V_{AC} based on the line voltage (V_L) and the neutral voltage (V_N) measurements ($V_{AC} = V_L - V_N$). To sense V_L and V_N, a resistor divider bridge is used. The typical voltage sensor is 3.545 mV/V_{AC}.

Figure 41. AC line voltage measurement

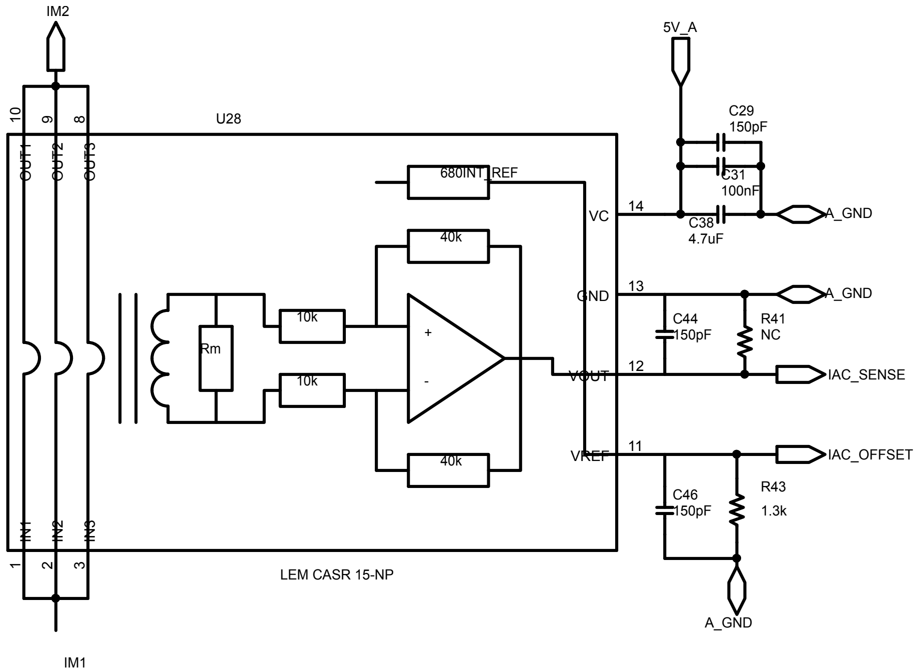


7.3.2 AC line current (I_{AC}) measurement

The PFC choke inductor current is measured to shape the AC line current to the AC line voltage. A CASR 15-NP current transducer is used in series with the PFC choke as shown in the figure below. The typical current transducer is 41.6 mV/I_{AC}.

As the AC line current is an alternative signal, an offset is needed to be read by the MCU. The current transducer sensor is supplied with 5 V_{DC}. R3 resistor (1.3 kOhms) is connected to the VREF pin of the current transducer sensor to set the offset to 1.64 V_{DC}.

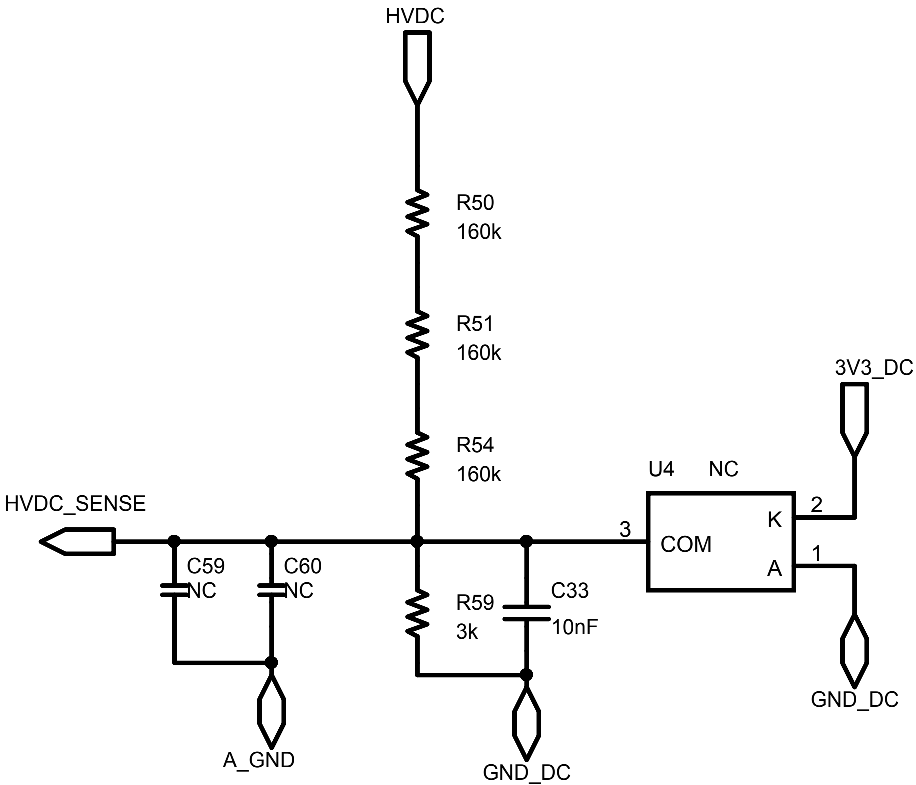
Figure 42. PFC choke inductor current sensor



7.3.3 Output PFC HVDC measurement

A resistor divider circuit is used to measure the output PFC voltage (HVDC). As the MCU ADC input port is a high resistance, an amplifier is not needed. The typical voltage sensor is 6.2 mV/HVDC.

Figure 43. HVDC output measurement



7.3.4 Signal sense filter

An RC filter is used to filter all analog signals (V_{AC}, I_{AC}, HVDC, TEMP).

7.4 Power circuit driver

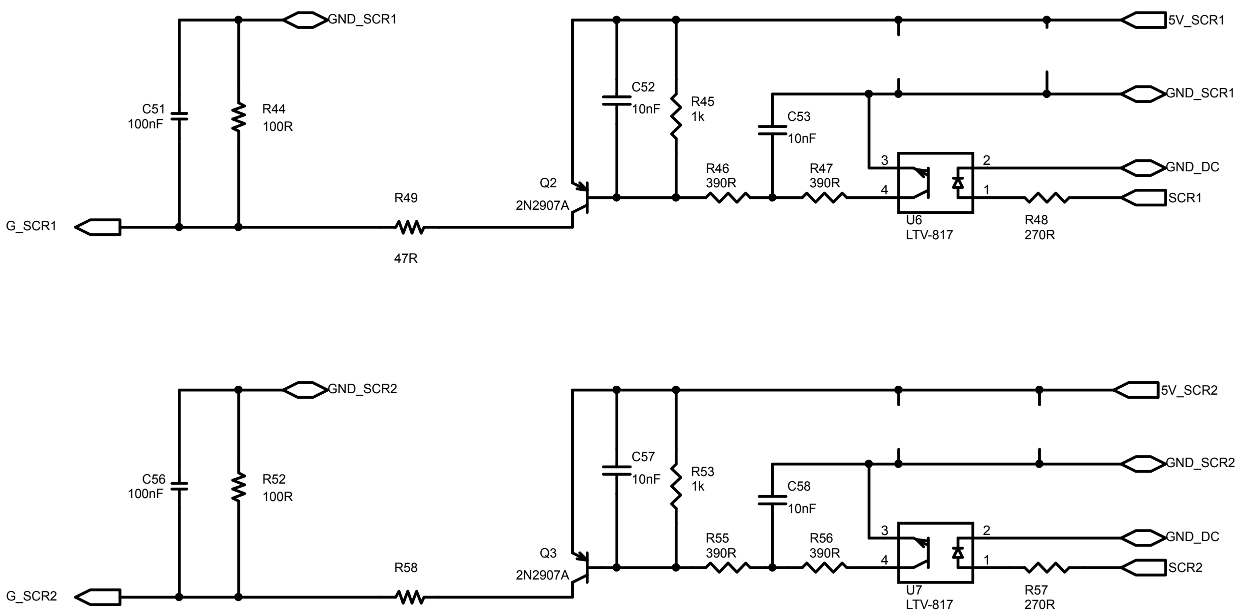
7.4.1 SCR control circuit

The VIPER26LD flyback provides two insulated DC output voltage to control SCR1 and SCR2. Insulated positive power supplies are required to supply current to SCR gates. As the MCU is not at the same ground reference as SCRs, optocouplers are needed as shown in the figure below.

To improve the circuit control immunity filters have been added:

- an RC filter connected between the base and the emitter of the PNP transistors (Q2 and Q3)
- R45/R53 = 1 kΩ
- C52/C57 = 10 nF
- capacitors (C53 and C58) associated with R46/R47 and R55/R56 resistors improve the immunity of the optocouplers (U6 and U7)

Figure 44. SCR insulated control



To define the resistor value of the SCR control circuit, the block of equations below define the new resistor definition according to the previous figure.

$$R_{GK} = R_{44} = R_{52} \tag{7}$$

$$R_g = R_{49} = R_{58} \tag{8}$$

$$R_{F1} = R_{45} = R_{53} \tag{9}$$

$$R_{F2} = R_{47} = R_{56} \tag{10}$$

$$R_{F3} = R_{46} = R_{55} \tag{11}$$

$$R_L = R_{48} = R_{57} \tag{12}$$

$$C_{F1} = C_{52} = C_{57} \tag{13}$$

$$C_{F2} = C_{53} = C_{58} \tag{14}$$

Knowing the SCR gate current (IGT), the gate resistor R_{GK} to limit the SCR gate current can be defined according to the equation below, where 5VSCR is the power supply to provide the gate current to the SCRs, VCE_SAT_{PNP} is the transistor collector/emitter of the PNP transistors (Q2 and Q3), V_{GT} is the SCR gate triggering voltage and R_{GK} is the gate cathode resistor used to increase the SCR immunity.

$$R_g < \frac{5V_{SCR} - VCE_{SAT\_PNP} - VGT_{SCR}}{IGT_{SCR} + \frac{VGT_{SCR}}{R_{GK}}} \quad (15)$$

The collector resistors (RF2 and RF3) of the optocoupler are defined by the equation below, where RF1 is the PNP transistor resistor filter, VCC_AC is the power supply to provide the gate current to the AC switch, VCE_SAT_{Opto} is the transistor collector/emitter of the optocoupler, β is the PNP transistor gain and VBE_SAT_{PNP} is the PNP transistor base/emitter.

$$R_{F2} + R_{F3} = \frac{5V_{SCR} - VCE_{SAT\_OPTO} - VBE_{SAT\_PNP}}{\frac{5V_{SCR} - VCE_{SAT\_NPN} - VGT\_SCR}{\beta \cdot R_G} + \frac{VBE_{SAT\_PNP}}{R_{F1}}} \quad (16)$$

Knowing the optocoupler CTR, RF2 and RF3 resistors value, the LED resistor R_L of the optocoupler is defined by the equation below, where 5VSCR is the power supply to provide the gate current to the AC switch, VCE_SAT_{Opto} is the transistor collector/emitter of the optocoupler, VBE_SAT_{PNP} is the PNP transistor base/emitter and VOH_Min_MCU is the output MCU voltage to drive the optocoupler.

$$R_L = \frac{VOH\_Min\_MCU - VF_{Opto}}{\frac{1}{CTR} \times \frac{VCC\_AC - VCE\_SAT_{Opto} - VBE\_SAT_{PNP}}{R_{F2} + R_{F3}}} \quad (17)$$

With LTV-817 optocoupler and 2N2907 PNP transistor, you have to choose the following resistor values.

$$R_{GK} = R_{44} = R_{52} = 1k\Omega \quad (18)$$

$$R_g = R_{49} = R_{58} = 47k\Omega \quad (19)$$

$$R_{F1} = R_{45} = R_{53} = 1k\Omega \quad (20)$$

$$R_{F2} = R_{47} = R_{56} = 390k\Omega \quad (21)$$

$$R_{F3} = R_{46} = R_{55} = 390k\Omega \quad (22)$$

$$R_L = R_{48} = R_{57} = 1k\Omega \quad (23)$$

$$C_{F1} = C_{52} = C_{57} = 10nF \quad (24)$$

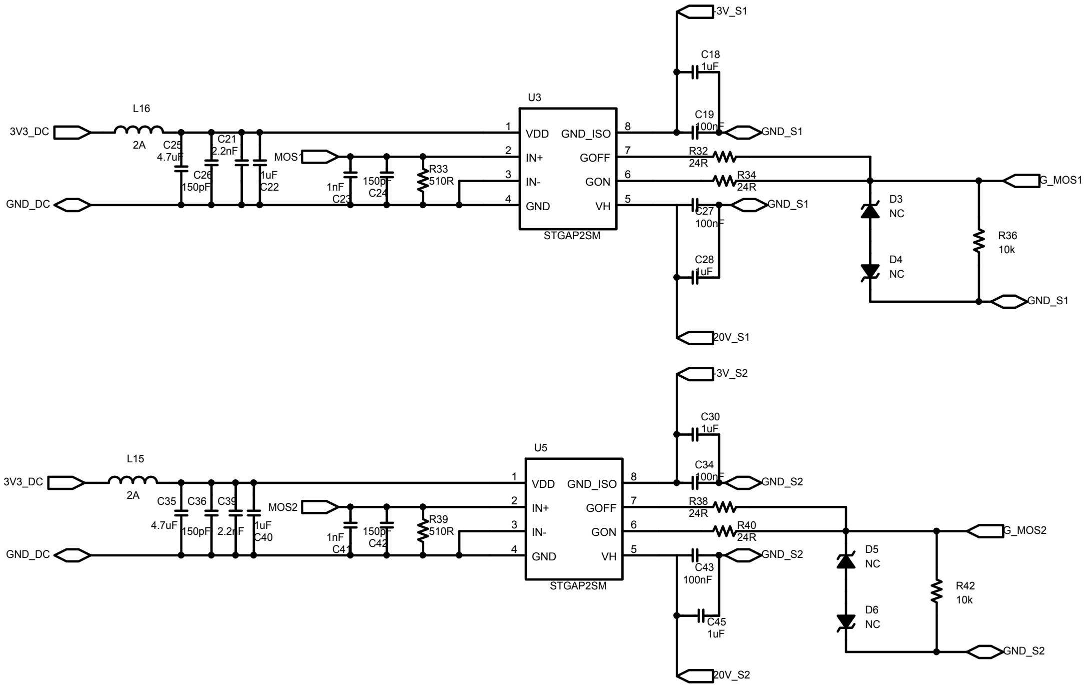
$$C_{F2} = C_{53} = C_{58} = 10nF \quad (25)$$

7.4.2 SiC MOSFET control circuit

The STGAP2S driver is designed to drive ST SiC MOSFET providing high peak current during turn-on and turn-off and to minimize the switching losses for better system efficiency and EMI.

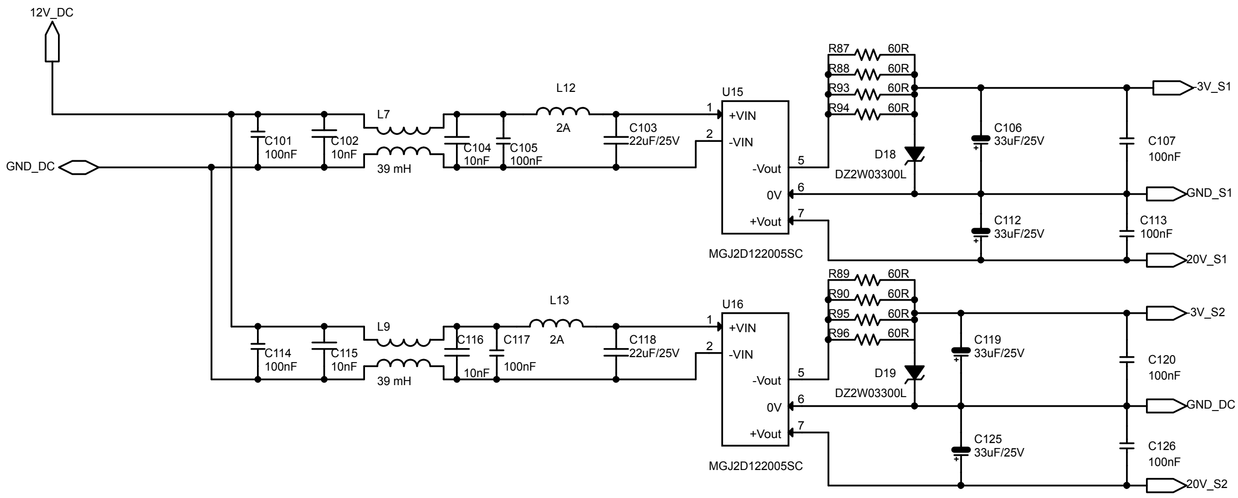
SiC MOSFET switches have different requirements for gate turn-on and turn-off voltage levels. The turn-on voltage level is performed with +20 V_{DC} and the turn-off is operated with -3.3 V_{DC} to ensure the gate source safe operating area.

Figure 45. **STGAP2S driver**



The asymmetric SiC MOSFET gate voltages (+20 V_{DC}/-3.3 V_{DC}) are achieved thanks to a high insulated DC-DC converter (MGJ2 series from MURATA) to power the high side and the low side gate drive circuits for SiC MOSFETs.

Figure 46. **STGAP2S driver - DC-DC converter**



8 PFC protections

8.1 Analogue overcurrent protection

Two comparators are used to detect the positive and negative PFC choke inductor overcurrent. This I_{AC} overcurrent detection is achieved thanks to STM32 comparators (COMP2 and COMP4) and STM32 digital analog converters (DAC CH1 and DAC CH2).

Figure 47. **STM32 comparator configuration**

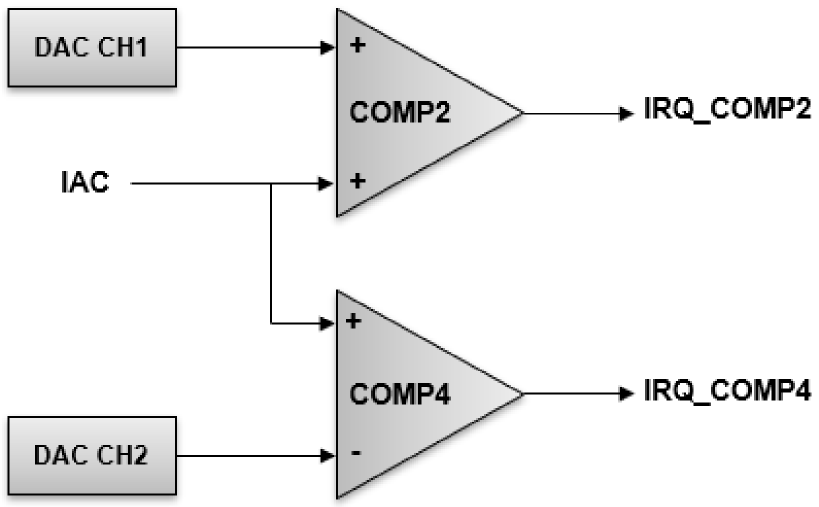
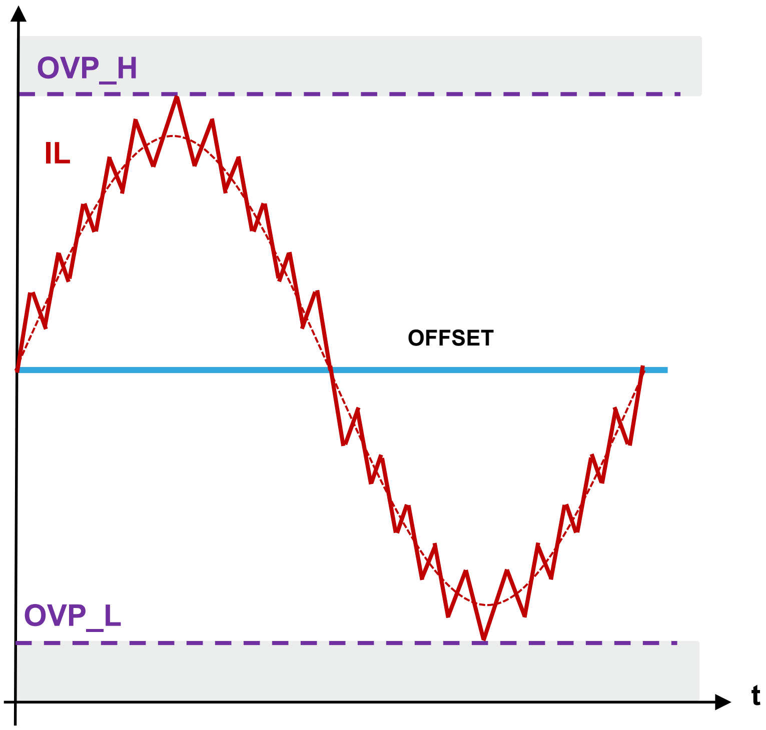


Figure 48. **Positive and negative overcurrent detection**



An interrupt is generated by COMP2 or COMP4 peripherals if the PFC inductor current image is higher than OVP_H limit or lower than lower OVP_L limit, respectively. Upper limit (OVP_H) and lower limit (OVP_L) are defined by the STM32 digital analog converter peripherals (DAC CH1 and DAC CH2). The equations below define the digital upper and lower limit with IAC_OFFSET the digital value (2070) of the IAC current sensor offset value. The PFC totem pole turns off if the maximum PFC choke inductor current is higher than 25 A peak.

$$DAC_{CH1} = \frac{2^n}{V_{ref}} \times \left(I_{L\_MAX} + \frac{\Delta I_L}{2}\right) \times K_{i\_sense} + I_{AC\_OFFSET} \quad (26)$$

$$DAC_{CH2} = \frac{2^n}{V_{ref}} \times \left(I_{L\_MAX} + \frac{\Delta I_L}{2}\right) \times K_{i\_sense} - I_{AC\_OFFSET} \quad (27)$$

8.2 Digital PFC choke inductor current clamping

The PFC totem pole has been designed to limit the AC line current at 16 A_{RMS} (I_{AC}). In this case, as the input current is clamped to 16 A_{RMS}, if the output DC current (I_{DC}) increases, the HVDC voltage decreases. This is performed by clamping the peak current reference in the firmware. The PFC totem pole board switches off if the HVDC voltage is lower than the peak AC line voltage measured at board startup.

Figure 49. Over input current protection

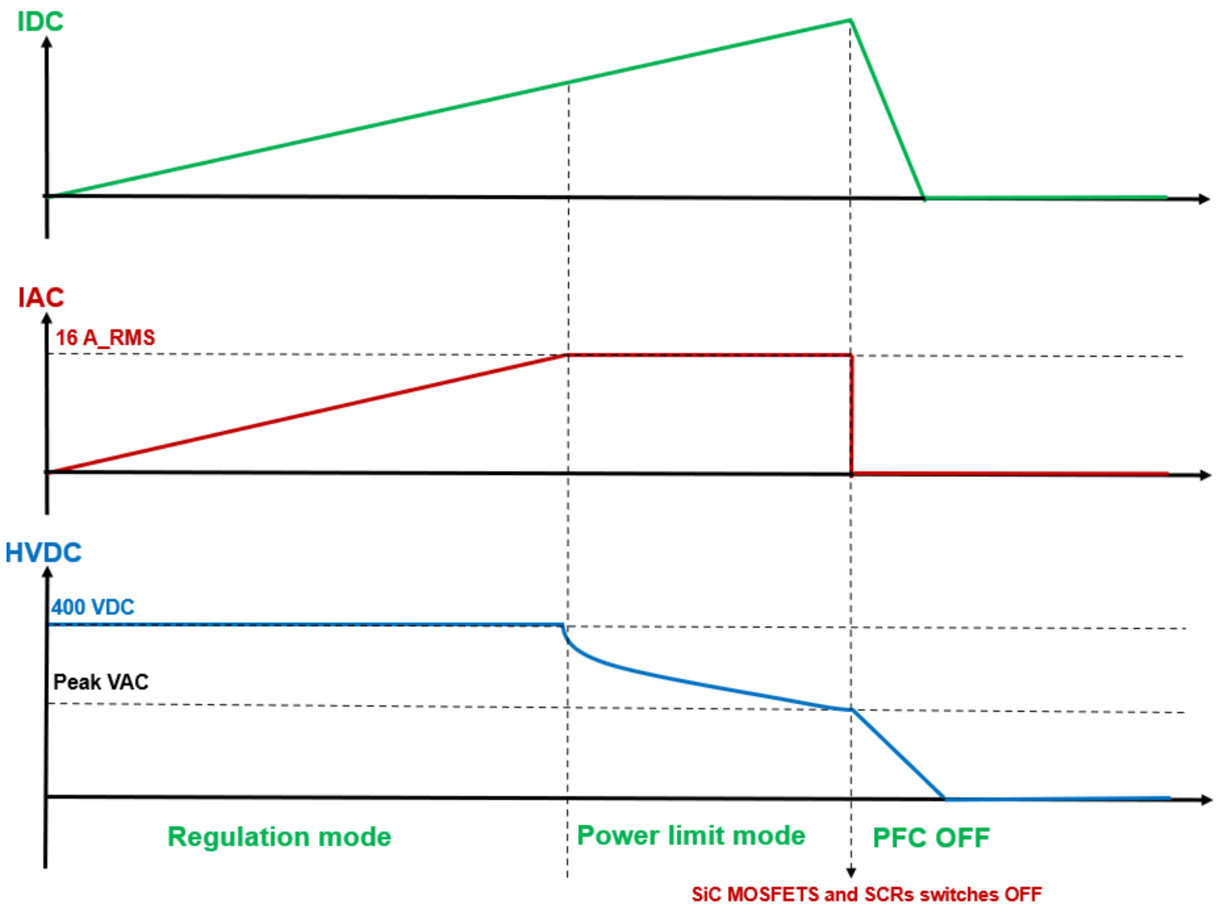
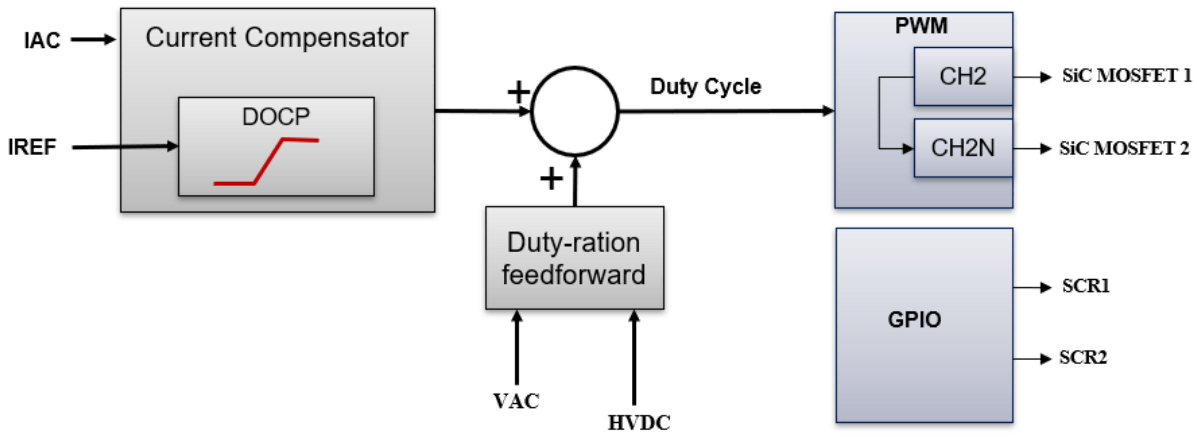


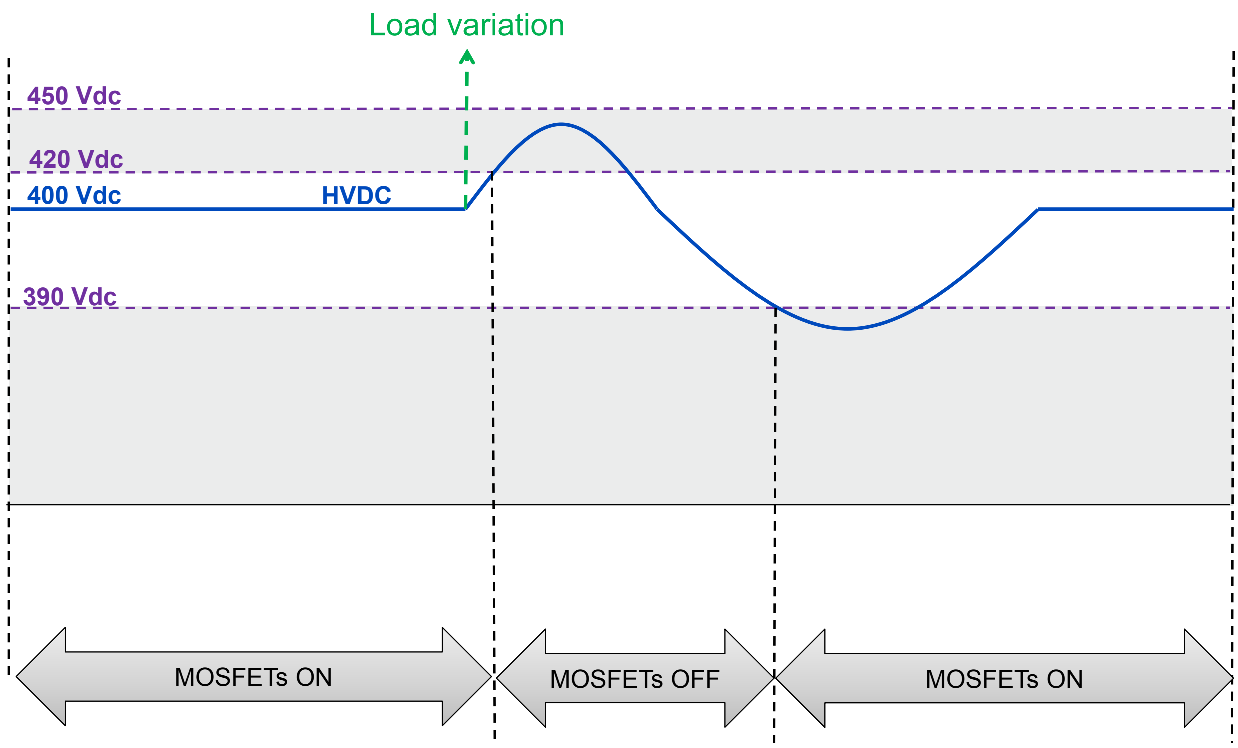
Figure 50. I_{AC} inductor current clamp



8.3 HVDC overvoltage protection

HVDC output overvoltage might occur with a DC load variation from high to light load. SiC MOSFETs are switched off if the HVDC output voltage is higher than 420 V_{DC} and switched on again if the HVDC output voltage is lower than 390 V_{DC} at the zero cross of the AC line voltage.

Figure 51. Overvoltage protection



8.4 Overtemperature protection

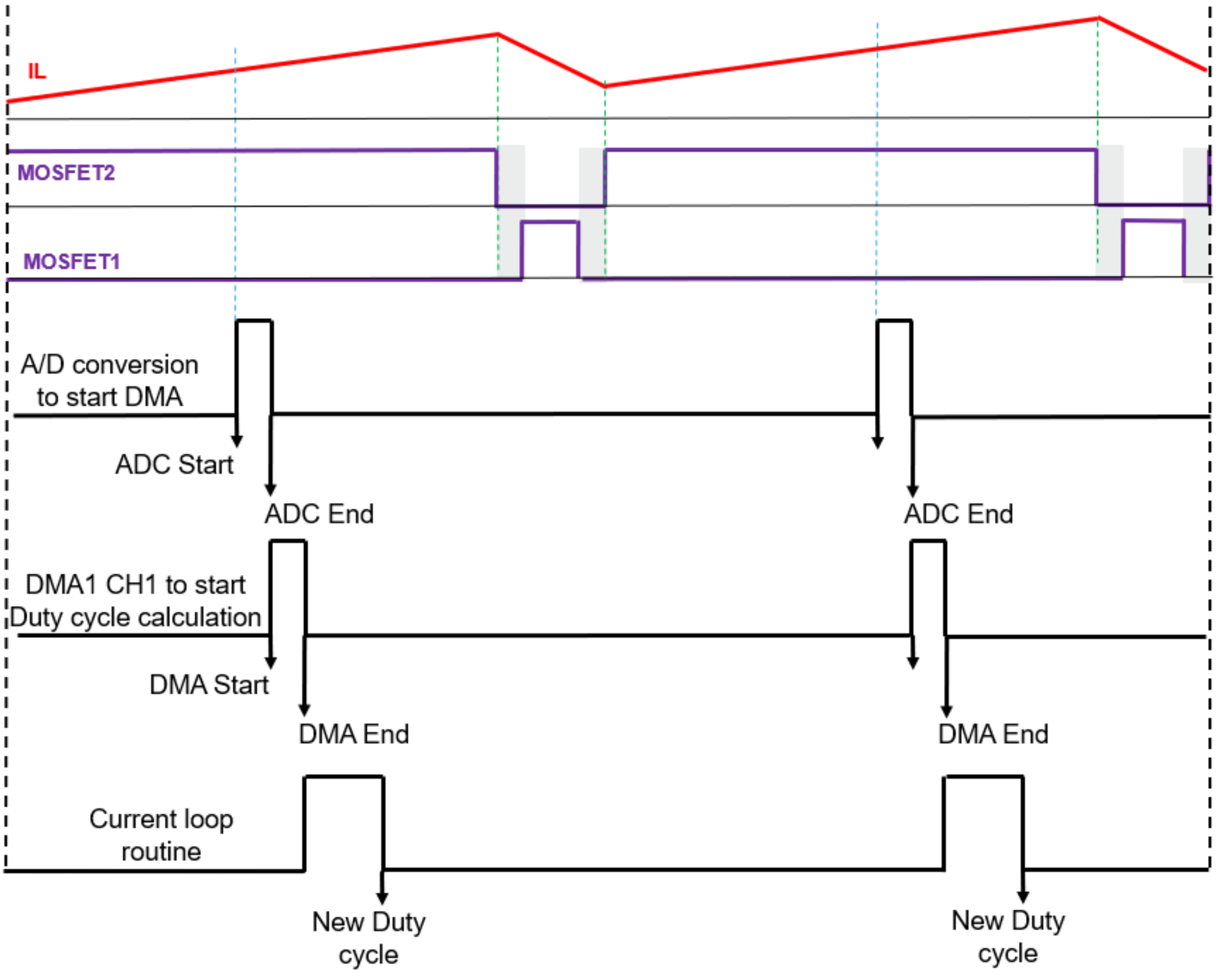
The PFC totem pole temperature protection is made with a TO-220 temperature sensor mounted on the heatsink and connected to an MCU GPIO. If overtemperature is detected by the MCU, the PFC totem pole turns off.

9 Control loop design

9.1 Timing diagram

The AC line voltage (V_{AC}), the PFC chock current (I_L) and HVDC output voltage are sampled at the center of the PWM signal used to control SiC MOSFET switches. The inner current loop computation is executed at 72 kHz to get the desired switching signal and configured accordingly. The outer voltage loop computation is executed at each AC line zero crossing.

Figure 52. **Timing diagram**

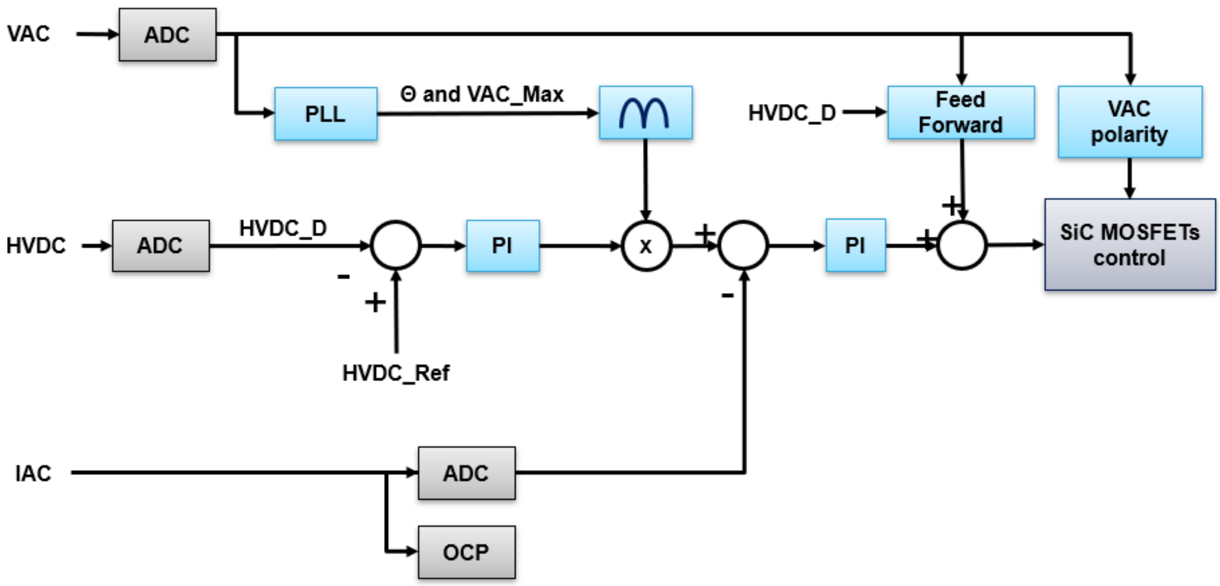


9.2 Digital power factor correction (DPFC)

The figure below shows the PFC totem pole regulation principle using a digital control implemented in the STM32 microcontroller:

- the outer voltage loop regulates the totem pole HVDC output voltage
- the current loop is the faster loop and is used to shape the current inductor to the sinusoidal reference (I_{L_REF})
- PLL is used to synchronize the PFC to the AC line cycle

Figure 53. **Digital PFC control diagram**



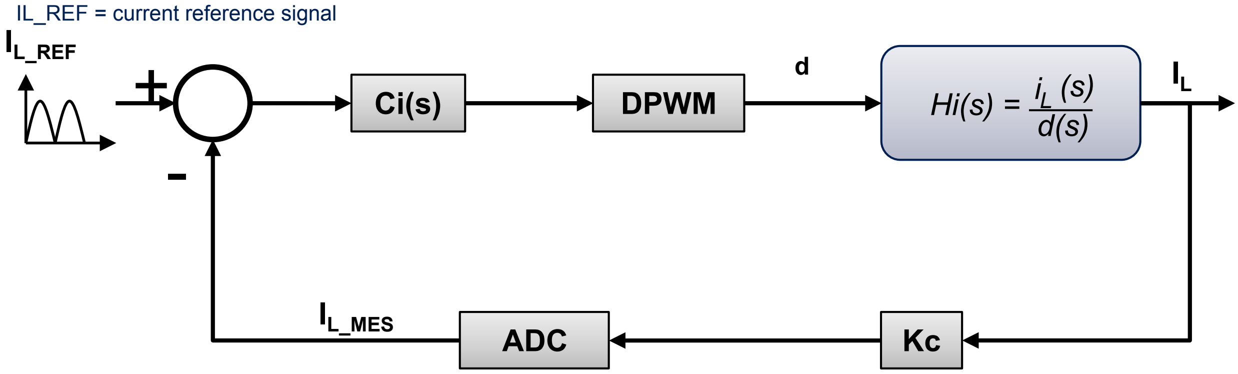
9.3 Current loop control design

9.3.1 Current loop model

The figure below shows the current loop small signal model block diagram. The current loop controller keeps the error between the reference and the current inductor at zero.

Figure 54. **Current loop diagram**

Ci(s) = current loop controller
Hi(s) = current transfer function duty cycle
DPWM = digital PWM gain
ADC = ADC transfer function
kc = current sensor transfer function to measure PFC choke inductor current
IL_REF = current reference signal



The controller output is fed by the DPWM block to control SiC MOSFET. The duty cycle adapts the inductor current to be in phase with the reference signal (I_{L_REF}).

The full transfer function of open current loop is defined by the following equation

$$T_i(s) = C_i(s) \times H_i(s) \times ADC \times DPWM \times K_c \quad (28)$$

The PFC duty cycle of current transfer function is defined by

$$H_i(s) = \frac{I_L(s)}{d(s)} = \frac{2 \cdot HVDC}{R \cdot (1 - d_E)^2} \cdot \left(\frac{1 + \frac{R \cdot C}{2} \cdot s}{1 + \frac{L}{R \cdot (1 - d_E)^2} \cdot s + \frac{L \cdot C}{(1 - d_E)^2} \cdot s^2} \right) \tag{29}$$

In high frequency:

$$H_i(s) = \frac{I_L(s)}{d(s)} = \frac{HVDC}{L \cdot s} \tag{30}$$

with

$$R = \frac{HVDC^2}{POUT} \tag{31}$$

and duty cycle equilibrium point:

$$d_E = 1 - \frac{VAC}{HVDC} \tag{32}$$

where:

- POUT: PFC output power
- L: PFC boost inductance
- C : DC output capacitor
- VAC: Input AC line voltage
- HVDC : DC output voltage

The current loop controller Ci(s) is defined by the following equation with Kp_i and Ki_i PI controller analog coefficients

$$C_i(s) = K_{p\_i} + \frac{K_{i\_i}}{s} = K_{p\_i} \times \left(\frac{1 + \tau_i \times s}{\tau_i \times s} \right) \tag{33}$$

with

$$\tau_i = \frac{K_{p\_i}}{K_{i\_i}} \tag{34}$$

The current sensor sensitive coefficient is defined by

$$K_c = 0.0416 \tag{35}$$

The ADC STM32 transfer function is defined by

$$ADC = \frac{2^n}{V_{ref}} = \frac{2^{12}}{3.3} = 1241 \tag{36}$$

The Digital PWM gain based on 72 MHz timer resolution and a 72 kHz switching frequency (Fs_i) is defined by

$$DPWM = \frac{F_{s\_i}}{F_{CLK\_MCU}} = \frac{72 \times 10^3}{72 \times 10^6} = 1 \times 10^{-3} \tag{37}$$

9.3.2 Controller design

A good current loop performance needs the crossover frequency F_{C_i} to be around 15 time lower than the switching frequency. To ensure the stability of the loop, two criteria must be verified with PM_i as phase margin.

$$20 \times \log(|T_i(s)|) = 1 \tag{38}$$

$$\arg(T_i(s)) = +180 + PM_i \tag{39}$$

According to the previous equations, τi, Kp_i and Ki_i analog coefficients are defined by

$$\tau_i = \frac{\tan(PM_i)}{2 \times \pi \times F_{c\_i}} \tag{40}$$

$$K_{p\_i} = \frac{L \times (\tau_i \times 2 \times \pi \times F_{c\_i})^2}{HVDC \times ADC \times DPWM \times K_c \times \sqrt{1 + (\tau_i \times 2 \times \pi \times F_{c\_i})^2}} \tag{41}$$

$$K_{i\_i} = \frac{K_{p\_i}}{\tau_i} \tag{42}$$

In bilinear transformation, the formula below is used

$$s = \frac{2}{T_s} \times \frac{z-1}{z+1} \tag{43}$$

The current loop controller Ci(z) is defined by

$$C_i(z) = \frac{\left(\frac{K_{p\_i} \cdot T_{s\_i}}{2 \cdot \tau_i} - K_{p\_i}\right) + \left(\frac{K_{p\_i} \cdot T_{s\_i}}{2 \times \tau_i}\right) \cdot z}{-1+z} \tag{44}$$

where

$$\tau_i = \frac{K_{p\_i}}{K_{i\_i}} \tag{45}$$

According to the previous equations Kpz_i and Kiz_i are defined by

$$K_{pz\_i} = \left(K_{p\_i} - \frac{K_{p\_i}}{2 \times \tau_i \times F_{s\_i}}\right) \tag{46}$$

$$K_{iz\_i} = \frac{K_{p\_i}}{2 \times \tau_i \times F_{s\_i}} \tag{47}$$

Note: The current loop is executed at the MOSFETs switching frequency and fixed at 72 kHz. Ts_i and Fs_i are repectively the MOSFETs switching period and the MOSFETs switching frequency.

To thoroughly use MCU resources, the PI corrector coefficients are normalized to fixed-point decimal format (Q15 data format). The relation between the actual and normalized values is defined by

$$K_{pz\_i\_Q15} = K_{pz\_i} \times 8192 \tag{48}$$

$$K_{iz\_i\_Q15} = K_{iz\_i} \times 8192 \tag{49}$$

To optimize the HVDC regulation, the PI current loop coefficient has been defined according to the AC line voltage.

The table below defines the controller coefficient to be set in the MCU. In the firmware:

- the integral gain is defined by “PI_IAC_KI_230” and “PI_IAC_KI_110” according to the AC line voltage range
- the proportional gain is defined by “PI_IAC_KP_230” and “PI_IAC_KP_110” according to the AC line voltage range

Table 10. Integral and proportional gains of the current loop PI controller

Parameter	V_{AC} = 110 V_{RMS} P_{OUT_MAX} = 1.8 kW	V_{AC} = 230 V_{RMS} P_{OUT_MAX} = 3.6 kW
Kpz_i_Q15	3400	3400
Kiz_i_Q15	40	260

9.4 Feedforward design

When the main voltage or load current changes suddenly, the low bandwidth of the voltage loop may cause output voltage fluctuations. To alleviate the feedback controller, a digital feedforward control (DFF) has been included in the current loop to pre-calculate a duty ratio as defined by the equation below where HVDC is the PFC output voltage and V_{AC} the AC is the line voltage.

$$d_{FF} = \frac{HVDC - VAC}{HVDC} \tag{50}$$

The feedforward duty ratio is added to the average current mode control output to generate the final duty ratio. The regular current loop compensator changes the duty ratio around this calculated duty ratio pattern.

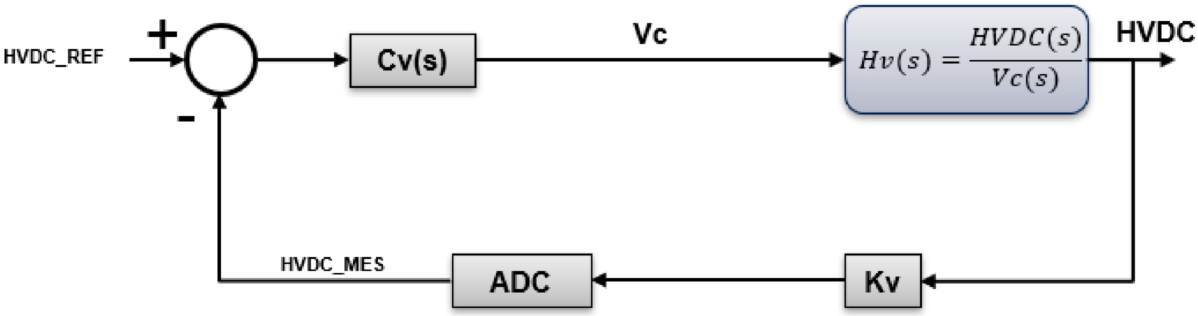
10 Voltage loop control design

10.1 Voltage loop model

The figure below shows the small signal model block diagram.

Figure 55. Voltage loop diagram

Cv(s) = voltage loop controller
Hv(s) = inductor current to output voltage transfer function
ADC = ADC transfer function
kv= inductor current transfer function



The full transfer function of open voltage loop is defined by

$$T_v(s) = H_v(s) \times C_v(s) \times ADC \times K_v \tag{51}$$

The output voltage transfer function is defined by

$$H_v(s) = \frac{V_{AC} \cdot R}{2 \cdot HVDC \cdot K_c \cdot ADC} \times \frac{1}{1 + \frac{R \cdot C}{2} \cdot s} \tag{52}$$

with

$$R = \frac{HVDC^2}{POUT} \tag{53}$$

where:
- POUT: PFC output power
- C : The DC output capacitor
- VAC: Input AC line voltage
- HVDC : DC output voltage
- Kc = 0.0416 (current sensor sensitive coefficient)

The voltage loop controller Cv(s) is defined by with Kp_v and Ki_v PI controller analog coefficients

$$C_v(s) = K_{p\_v} + \frac{K_{i\_v}}{s} = K_{p\_v} \times \left(\frac{1 + \tau_v \times s}{\tau_v \times s}\right) \tag{54}$$

with

$$\tau_i = \frac{K_{p\_v}}{K_{i\_v}} \tag{55}$$

The output voltage sense gain is defined by

$$K_v = \frac{R_2}{R_1 + R_2} = 0.0062 \tag{56}$$

The ADC STM32 transfer function is defined by

$$ADC = \frac{2^n}{V_{ref}} = \frac{2^{12}}{3.3} = 1241 \tag{57}$$

The equivalent resistor on the PFC output with HVDC, the PFC output voltage and P_{out}, and the PFC output power are defined by

$$R = \frac{HVDC^2}{P_{OUT}} \tag{58}$$

10.2 Controller design

A good current loop performance needs the crossover frequency F_{C_v} to be around 15 time lower than the switching frequency. To ensure the stability of the loop, two criteria must be verified with PM_i as phase margin.

$$20 \times \log(|T_v(s)|) = 1 \tag{59}$$

$$\arg(T_v(s)) = +180 + PM_i \tag{60}$$

According to the previous equations, τv, Kp_v and Ki_v are defined by

$$\tau_v = \frac{R \times C \times F_{c\_v} - \tan(PM_i + 90)}{\tan(PM_i + 90) \times 2 \times R \times C \times \pi^2 \times F_{c\_v}^2 + 2 \times \pi \times F_{c\_v}} \tag{61}$$

$$K_{p\_v} = \frac{4 \times HVDC \times K_v \times \pi \times F_{c\_v} \times \tau_v \times \sqrt{1 + (R \times C \times \pi \times F_{c\_v})^2}}{V_{AC} \times V_R \times R \times K_v \times \sqrt{1 + (\tau_i \times 2 \times \pi \times F_{c\_v})^2}} \tag{62}$$

$$K_{i\_v} = \frac{K_{p\_v}}{\tau_v} \tag{63}$$

In bilinear transformation, the formula below is used

$$s = \frac{2}{T_s} \times \frac{z-1}{z+1} \tag{64}$$

The voltage loop controller Cv(z) is defined by

$$C_v(z) = \frac{\left(\frac{K_{p\_v} \cdot T_{s\_v}}{2 \cdot \tau_v} - K_{p\_v}\right) + \left(\frac{K_{p\_v} \cdot T_{s\_v}}{2 \times \tau_v} + K_{p\_v}\right) \cdot z}{-1 + z} \tag{65}$$

where

$$\tau_v = \frac{K_{p\_v}}{K_{i\_v}} \tag{66}$$

According to the previous equations Kpz_i and Kiz_i are defined by

$$K_{pz\_v} = \left(K_{p\_v} - \frac{K_{p\_v}}{2 \times \tau_v \times F_{s\_v}}\right) \tag{67}$$

$$K_{iz\_v} = \frac{K_{p\_v}}{2 \times \tau_v \times F_{s\_v}} \tag{68}$$

Note: The voltage loop is executed at each zero cross of the AC line voltage. Fs_v is fixed at twice the AC line frequency.

To thoroughly use MCU resources, the PI corrector coefficients are normalized to fixed-point decimal format (Q15 data format). The relation between the actual and normalized values is defined by

$$K_{pz\_v\_Q15} = K_{pz\_v} \times 2048 \tag{69}$$

$$K_{iz\_v\_Q15} = K_{iz\_v} \times 2048 \tag{70}$$

To optimize the HVDC regulation, the PI voltage loop coefficient has been defined according to the AC line voltage.

The table below defines the controller coefficient to be set in the MCU. In the firmware:

- the integral gain is defined by “PI_VBUS_KI_230” and “PI_VBUS_KI_110” according to the AC line voltage range
- the proportional gain is defined by “PI_VBUS_KP_230” and “PI_VBUS_KP_110” according to the AC line voltage range

Table 11. Integral and proportional gains of the current loop PI controller

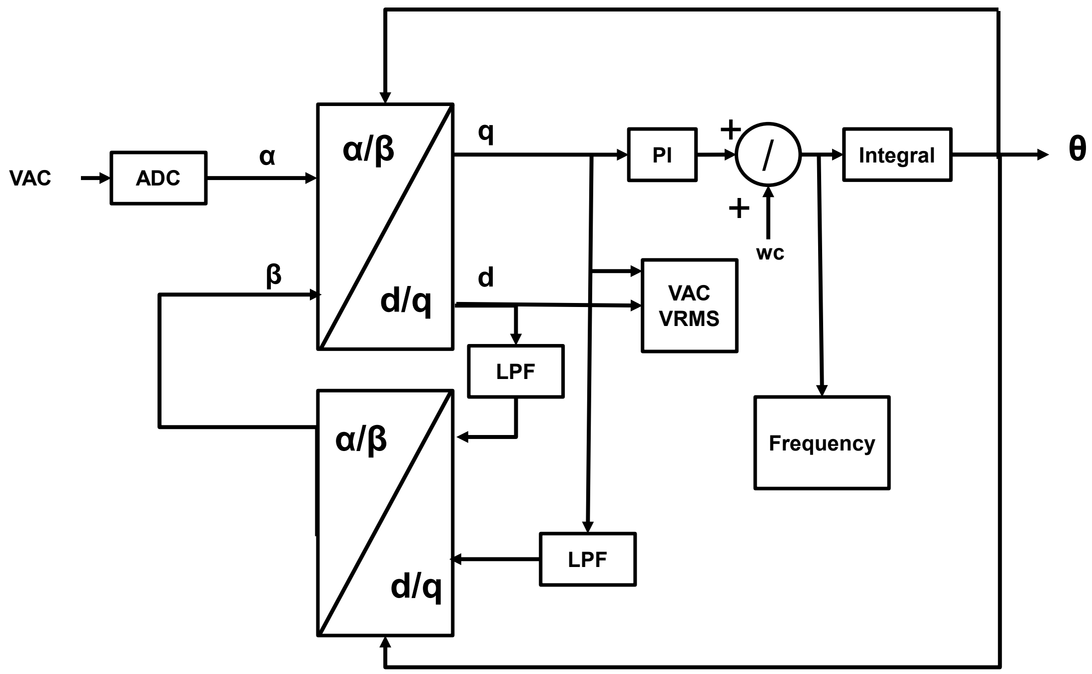
Parameter	V_{AC} = 110 V_{RMS} P_{OUT_MAX} = 1.8 kW	V_{AC} = 230 V_{RMS} P_{OUT_MAX} = 3.6 kW
Kpz_v_Q15	2300	940
Kiz_v_Q15	500	400

11 AC line zero crossing synchronization

11.1 PLL loop control design

To track the frequency and phase of the AC line voltage, a phase-locked loop (PLL) is used. The block diagram of this loop is defined in Figure 56 by using a low pass filter and a PI controller implemented in the STM32 firmware. PLL is used to generate the current reference in phase with the AC line voltage to shape the input AC line current to the AC line voltage.

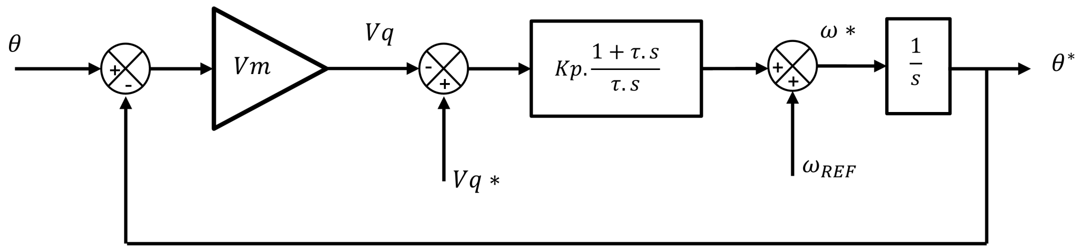
Figure 56. PLL diagram



The PLL is a closed loop system where the phase error between the PLL output phase and the reference is minimum. In steady state, the PLL output generates a sinusoidal wave close to the AC line voltage. A PI controller is used to reduce the error between the reference and the Vq value measured. Vq is defined thanks to the Park transformations of AC line voltage.

In steady state operation, the PLL and the grid frequency are closed. The simplified system for the PLL is defined by the following figure.

Figure 57. PLL loop PI controller



The input voltage sense gain is defined by

$$K_{VAC\_sense} = 0.003545 \tag{71}$$

The ADC STM32 transfer function is defined by

$$ADC = \frac{2^n}{V_{ref}} = \frac{2^{12}}{3.3} = 1241 \tag{72}$$

The full transfer function of open loop is defined by

$$T_{PLL}(s) = Vm \cdot Kp_{PLL} \cdot \frac{1 + \tau_{PLL} \cdot s}{\tau_{PLL} \cdot s} \cdot \frac{1}{s} \tag{73}$$

The current loop controller CPLL(s) is defined by the following equation with K_{p_PLL} and K_{i_PLL} as analog coefficients

$$C_{PLL}(s) = K_{p\_PLL} \times \left(\frac{1 + \tau_{PLL} \times s}{\tau_{PLL} \times s}\right) \tag{74}$$

with

$$\tau_{PLL} = \frac{K_{p\_PLL}}{K_{i\_PLL}} \tag{75}$$

The input voltage sense gain is defined by

$$K_{VAC\_sense} = 0.003545 \tag{76}$$

The ADC STM32 transfer function is defined by

$$ADC = \frac{2^n}{V_{ref}} = \frac{2^{12}}{3.3} = 1241 \tag{77}$$

Vm is defined by

$$V_m = VAC \cdot K_v \cdot ADC \tag{78}$$

11.2 Controller design

A good current loop performance needs the crossover frequency F_{C_PLL} to be fixed at 65 Hz. To ensure the stability of the loop, two criteria must be verified with PM_i phase margin fixed at 45°C.

$$20 \times \log(|T_{PLL}(s)|) = 1 \tag{79}$$

$$\arg(T_{PLL}(s)) = +180 + PM_i \tag{80}$$

According to the previous equations, τ_{PLL}, K_{p_PLL} and K_{i_PLL} are defined by

$$\tau_{PLL} = \frac{\tan(PM_{PLL})}{2 \times \pi \times F_{c\_PLL}} \tag{81}$$

$$K_{p\_PLL} = \frac{\tau_{PLL} \times (2 \times \pi \times F_{C\_PLL})^2}{V_{AC\_Peak} \times ADC \times K_{VAC\_Sense} \times \sqrt{1 + (\tau_{PLL} \times 2 \times \pi \times F_{C\_PLL})^2}} = 0.546 \tag{82}$$

$$K_{i\_PLL} = \frac{K_{p\_PLL}}{\tau_{PLL}} \tag{83}$$

In bilinear transformation, the formula below is used

$$s = \frac{2}{T_s} \times \frac{z - 1}{z + 1} \tag{84}$$

The current loop controller CPLL(z) is defined by

$$C_{PLL}(z) = \frac{\left(\frac{K_{p\_PLL} \cdot T_{s\_PLL}}{2 \cdot \tau_{PLL}} - K\right) + \left(\frac{K_{p\_PLL} \cdot T_{s\_PLL}}{2 \times \tau_{PLL}} + K_{p\_PLL}\right) \cdot z}{-1 + z} \tag{85}$$

$$\tau_v = \frac{K_{p\_v}}{K_{i\_v}} \tag{86}$$

According to the previous equations Kpz_i and Kiz_i are defined by

$$K_{pz\_PLL} = \left(K_{p\_PLL} - \frac{K_{p\_PLL}}{2 \times \tau_{PLL} \times F_{s\_PLL}}\right) \tag{87}$$

$$K_{iz\_PLL} = \frac{K_{p\_PLL}}{2 \times \tau_{PLL} \times F_{s\_PLL}} \tag{88}$$

Note: The PLL loop is executed at 9 kHz (Fs_PLL).

To thoroughly use MCU resources, the PI corrector coefficients are normalized to fixed-point decimal format (Q15 data format). The relation between the actual and normalized values is defined by

$$K_{pz\_PLL\_Q15} = K_{pz\_PLL} \times 2048 \quad (89)$$

$$K_{iz\_PLL\_Q15} = K_{iz\_PLL} \times 2048 \quad (90)$$

To optimize the HVDC regulation, the PI PLL loop coefficient has been defined according to the AC line voltage.

The table below defines the controller coefficient to be set in the MCU. In the firmware:

- the integral gain is defined by “PI_PLL_KI_230” and “PI_PLL_KI_110” according to the AC line voltage range
- the proportional gain is defined by “PI_PLL_KP_230” and “PI_PLL_KP_110” according to the AC line voltage range

Table 12. Integral and proportional gains of the current loop PI controller

Parameter	V_{AC} = 110 V_{RMS} P_{OUT_MAX} = 1.8 kW	V_{AC} = 230 V_{RMS} P_{OUT_MAX} = 3.6 kW
Kpz_PLL_Q15	1421	460
Kiz_PLL_Q15	30	10

12 Experimental results

12.1 Efficiency and THD

The figures below show the PFC totem pole efficiency and THD according to the output power (P_{out}).

Figure 58. **PFC efficiency and THD for V_{AC} = 230 V_{RMS}/50 Hz**

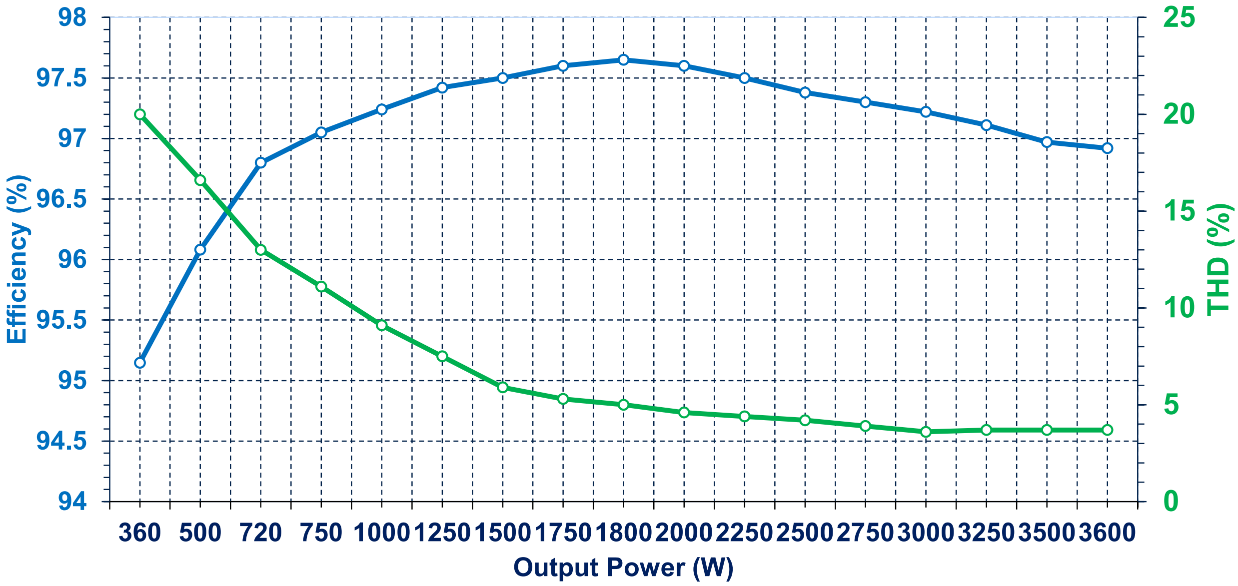
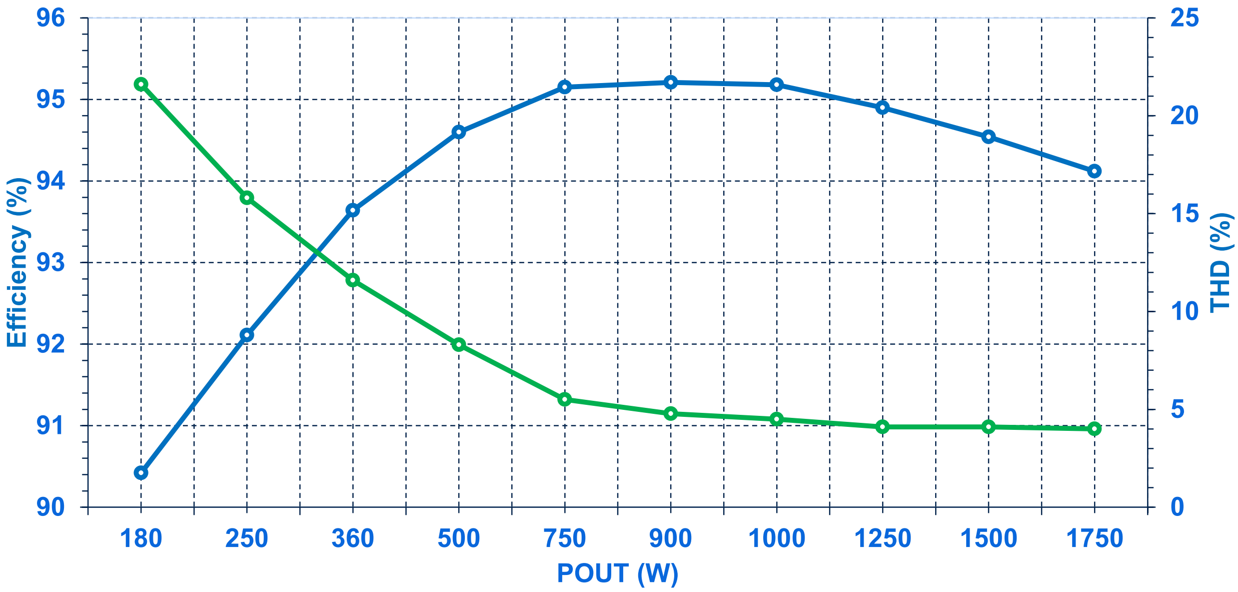


Figure 59. **PFC efficiency and THD for V_{AC} = 115 V_{RMS}/60 Hz**

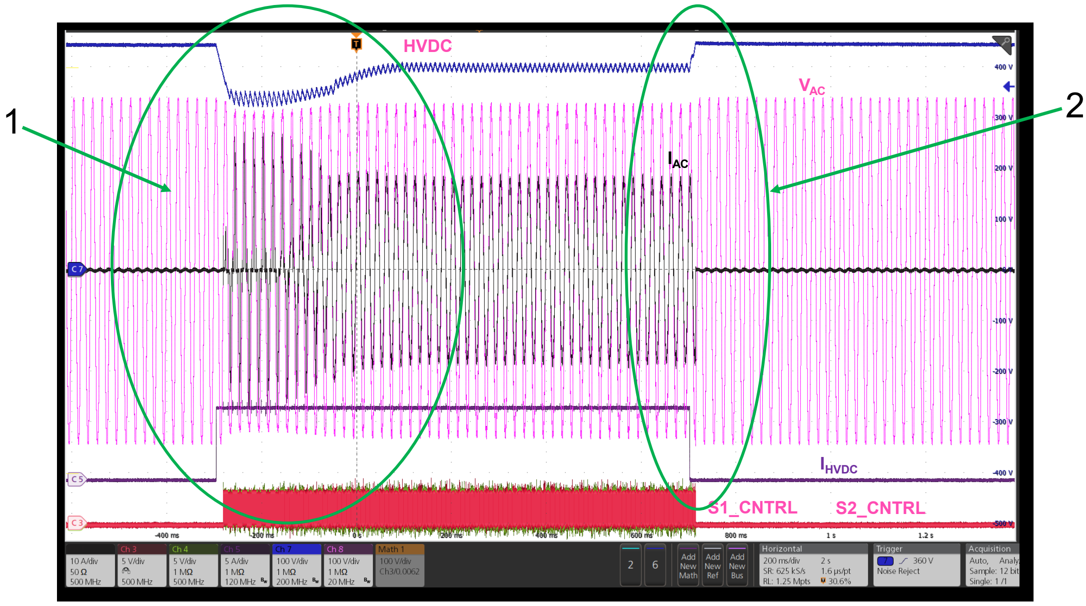


12.2 Load variation

The figure below shows the transient response of the PFC totem pole when the AC line voltage is 230 V_{rms} (V_{AC}) and the DC load current (IHVDC) is stepped up from 0 % to 100 % (see 1) and stepped down from 100 % to 0 % (see 2).

Figure 60. Load variation with V_{AC} = 230 V_{RMS}/50 Hz

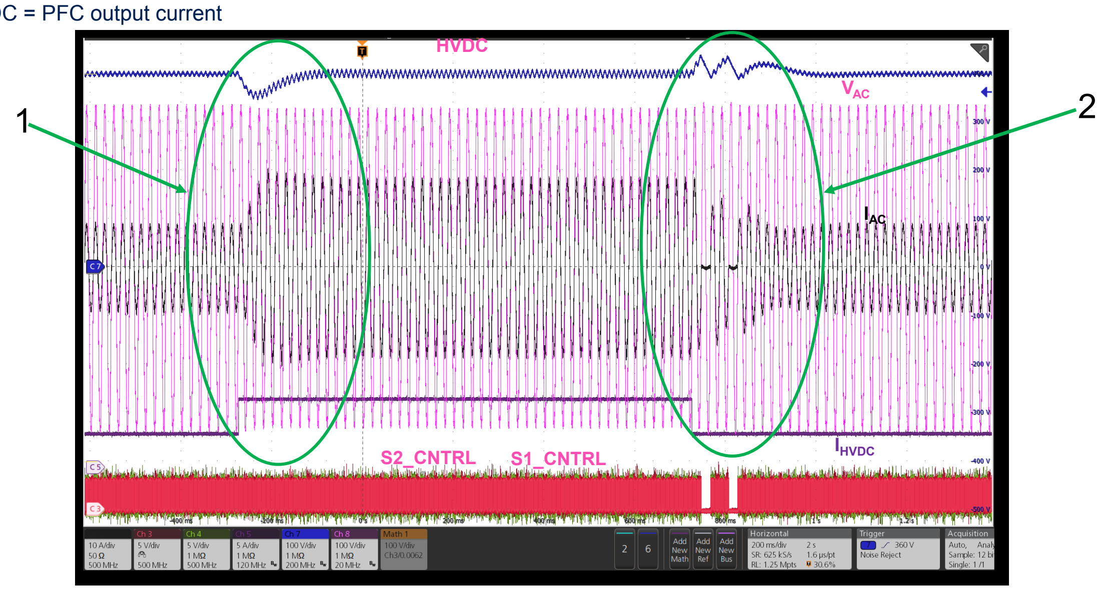
V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage
IHVDC = PFC output current



The figure below shows the transient response when the AC line voltage is 230 V_{rms} (V_{AC}) and the DC load current (IHVDC) is stepped up from 50 % to 100 % (see 1) and stepped down from 100 % to 50 % (see 2).

Figure 61. Load variation with V_{AC} = 230 V_{RMS}/50 Hz (stepped up/down to 50%)

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage
IHVDC = PFC output current

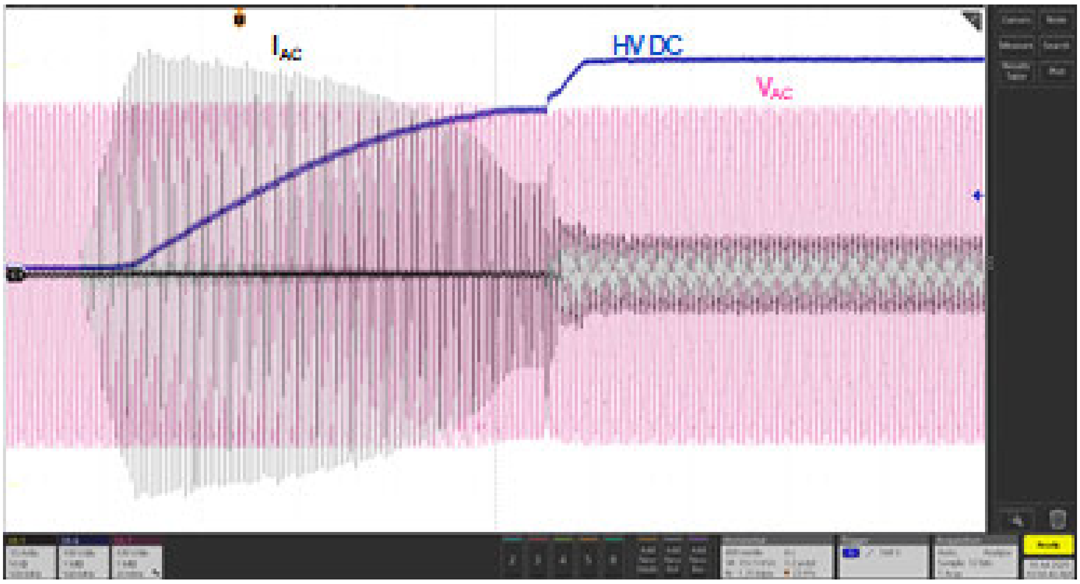


12.3 PFC totem pole startup

The figure below shows the startup sequence of the PFC totem pole with V_{AC} = 230 V_{rms}/50 Hz and with a 1 kW DC load.

Figure 62. **PFC startup with V_{AC} = 230 V_{RMS}/50 Hz and P_{out} = 1 kW**

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



The figure below shows the startup sequence of the PFC totem pole with V_{AC} = 110 V_{rms}/60 Hz and with a 1 kW DC load.

Figure 63. **PFC startup with V_{AC} = 110 V_{RMS}/60 Hz and P_{out} = 1 kW**

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage

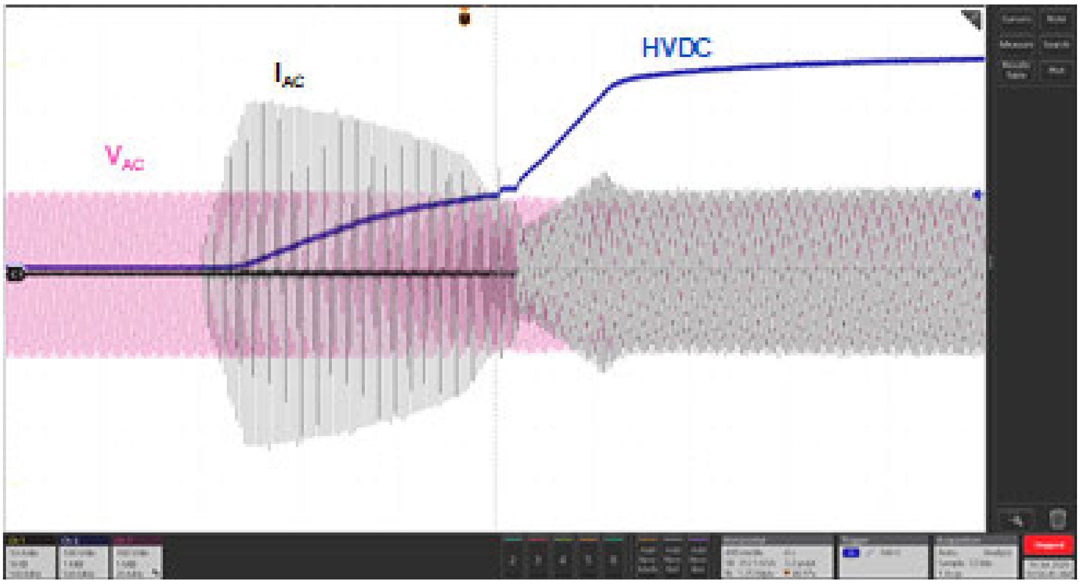
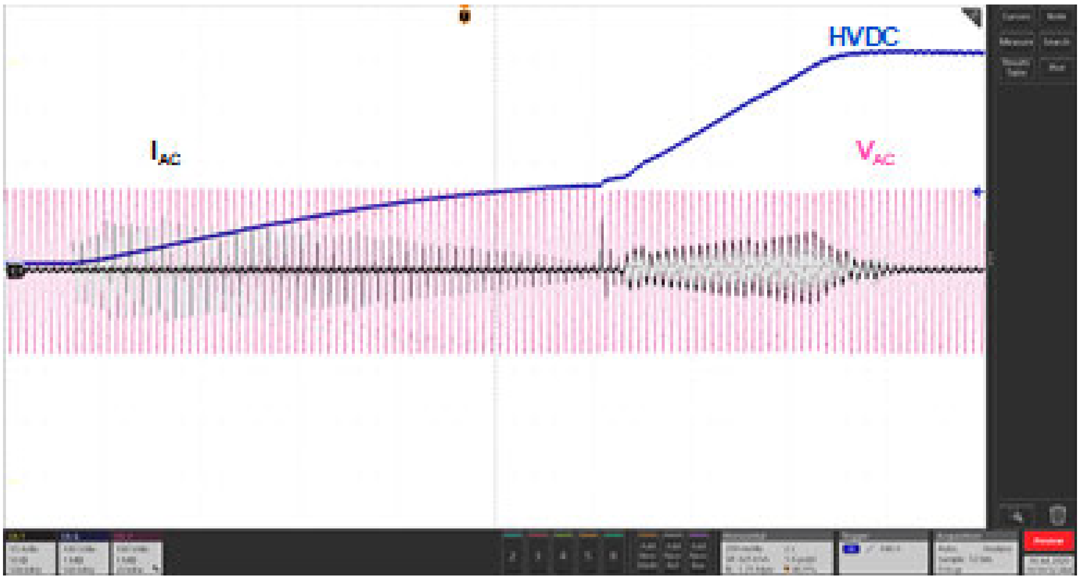


Figure 64. PFC startup with V_{AC} = 110 V_{RMS}/60 Hz and without DC load

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



12.4 Steady state operation

The figures below show the PFC steady state current waveform at different load conditions.

Figure 65. PFC steady state with V_{AC} = 230 V_{RMS}/50 Hz and Pout = 1 kW

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage

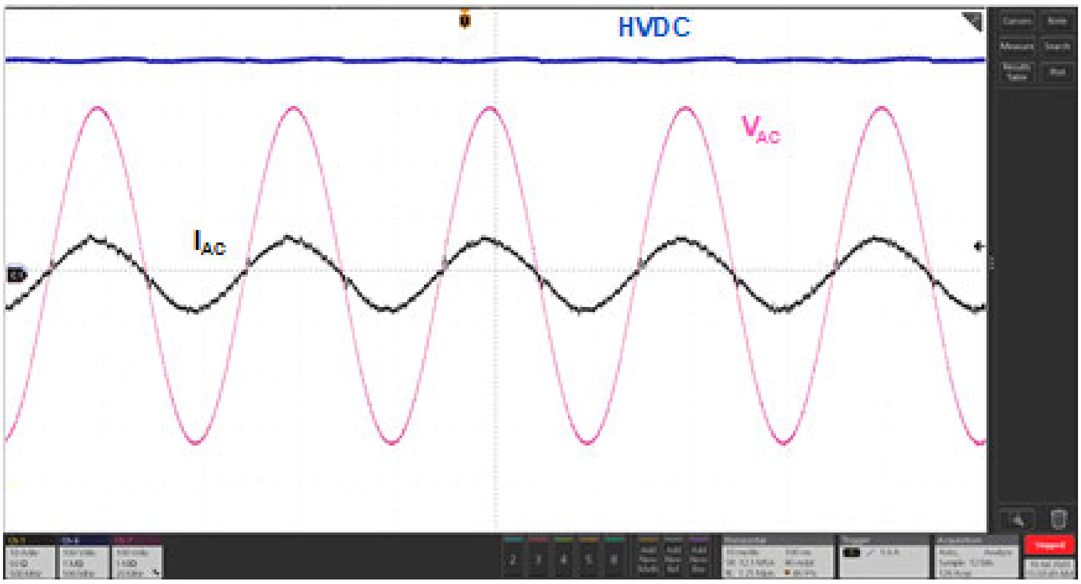


Figure 66. PFC steady state with V_{AC} = 230 V_{RMS}/50 Hz and Pout = 2 kW

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage

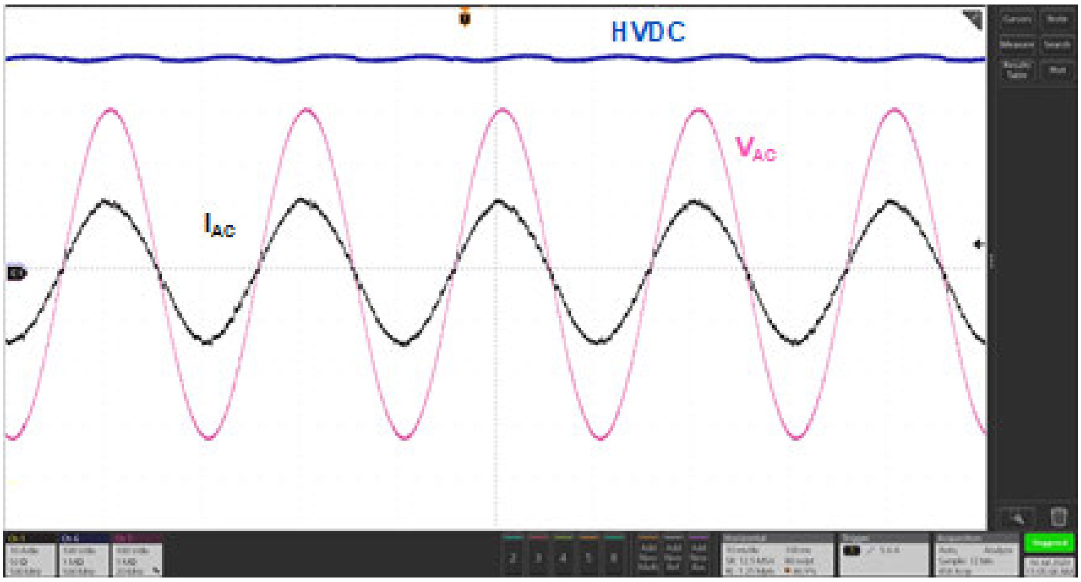
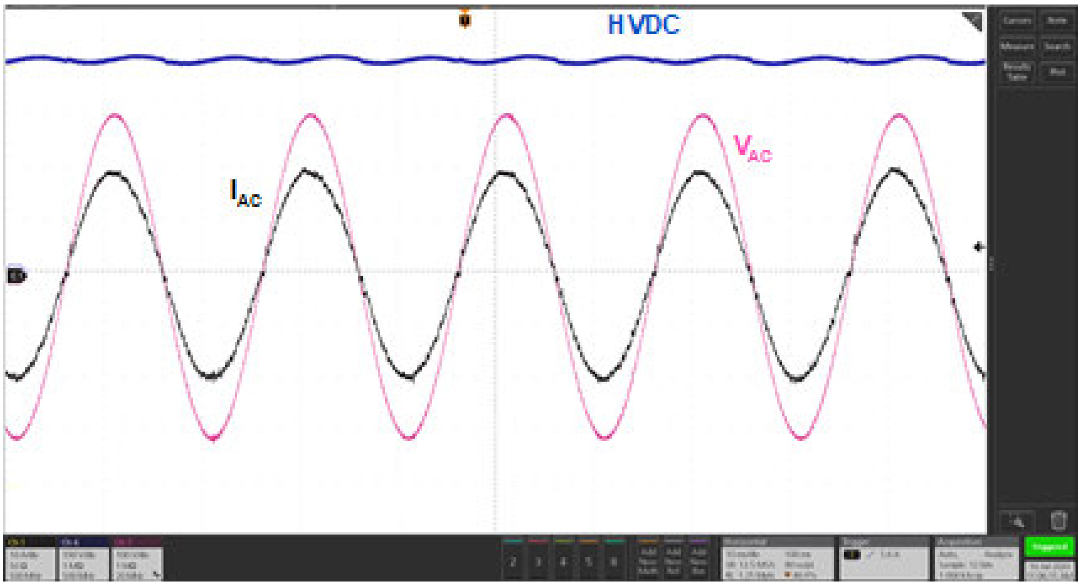


Figure 67. PFC steady state with V_{AC} = 230 V_{RMS}/50 Hz and Pout = 3 kW

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



12.5 Mains voltage dips and interruptions

12.5.1 IEC 61000-4-11 standard

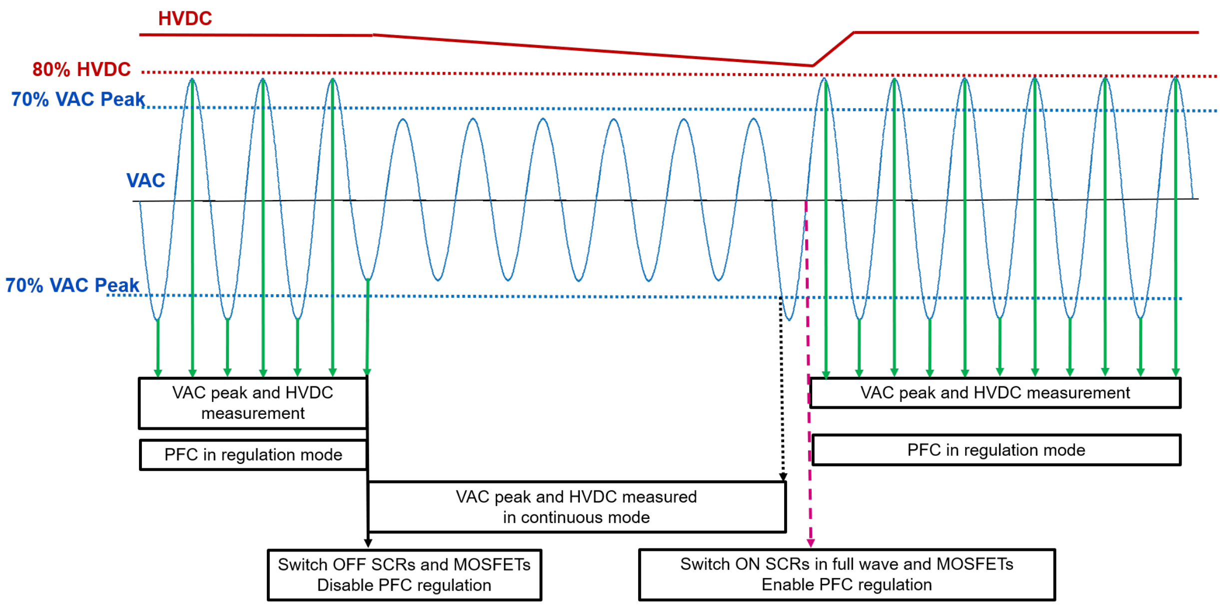
IEC 61000-4-11 standard defines the test conditions to evaluate the immunity of the equipment to a voltage dip or interrupt. As any appliance connected to the mains can be subject to line voltage dips or interruptions, a high input current may occur when the line voltage suddenly increases to its nominal value. This high current may damage the front-end circuit components such as the AC fuse for example.

12.5.2 PFC voltage dips

The STEVAL-DPSTPFC1 MCU firmware is programmed to comply with the IEC 61000-4-11 standard tests on the basis of the following strategy:

- if the peak AC line voltage falls below 70% of the AC line peak reference voltage, SCR1/SCR2 and MOSFET1/MOSFET2 are switched off. The DC bus voltage is discharged by its load current. When the line voltage is reapplied and if the HVDC voltage is higher than 80% of 400 V_{DC} (PFC output voltage), the SCRs are controlled back in full wave and MOSFET1/ MOSFET2 controlled in PWM.

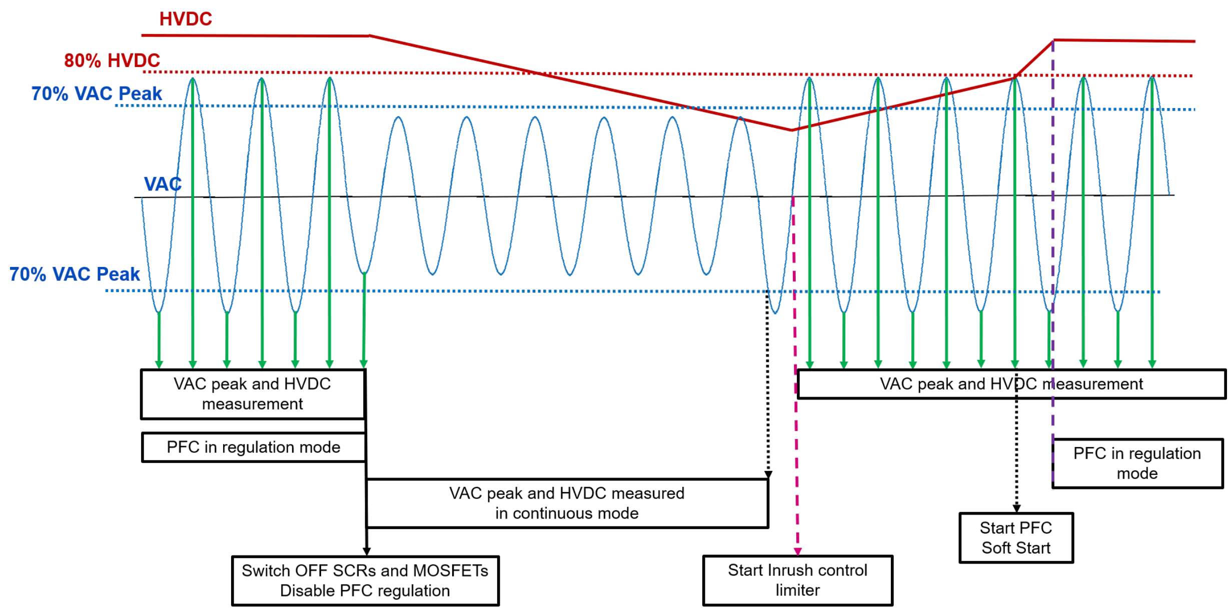
Figure 68. AC line drop principle (HVDC > 80% of 400 V_{DC})



Note: The SCR1/SCR2 and MOSFET1/MOSFET2 are switched on at the next zero cross of the AC line voltage when the line voltage is reapplied.

- if the peak AC line voltage falls below 70% of the AC line peak reference voltage, SCR1/SCR2 and MOSFET1/MOSFET2 are switched off. The DC bus voltage is discharged by its load current. When the line voltage is reapplied and if the HVDC voltage is lower than 80% of 400 V_{DC}, the SCRs are controlled back in soft-start to ensure the inrush current limitation

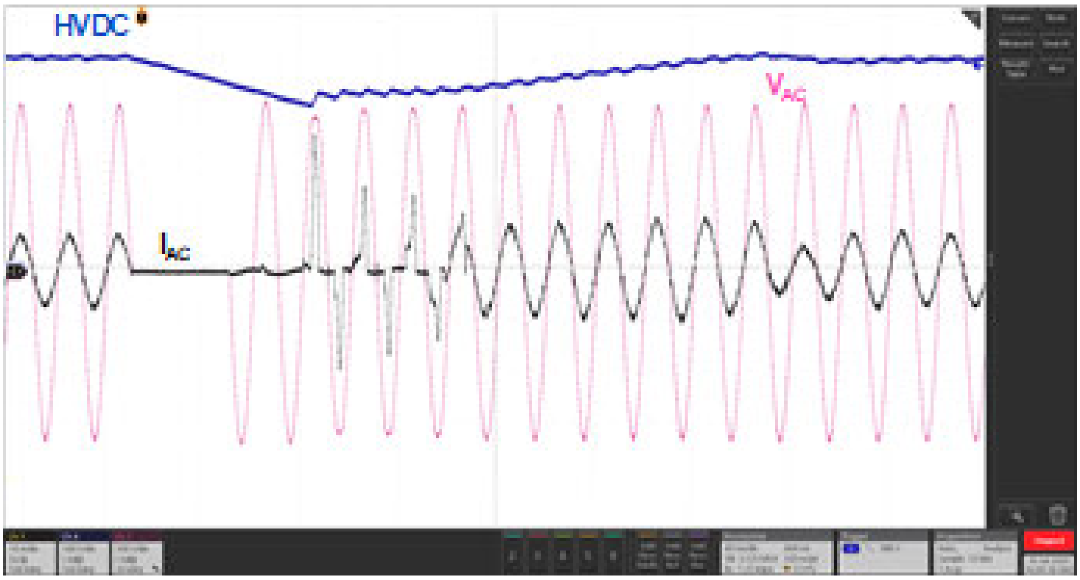
Figure 69. AC line drop principle (HVDC < 80% of 400 V_{DC})



The figure below shows the PFC totem pole board behavior, working at 230 V_{RMS} AC line voltage with a 1 kW DC load, for an AC line voltage dip with a 0% residual voltage applied for 40 ms. When the voltage is reapplied back and if HVDC voltage is higher than 80% of 400 V_{DC}, SCRs are controlled in full wave according to the AC line polarity and MOSFET1/ MOSFET2 controlled in PWM. The peak current is only 25 A as the DC voltage decreased by just 100 V during the lack of AC line voltage.

Figure 70. Mains voltage dips with V_{AC} = 230 V_{rms} and P_{out} = 1 kW(0% residual voltage applied for 40 ms)

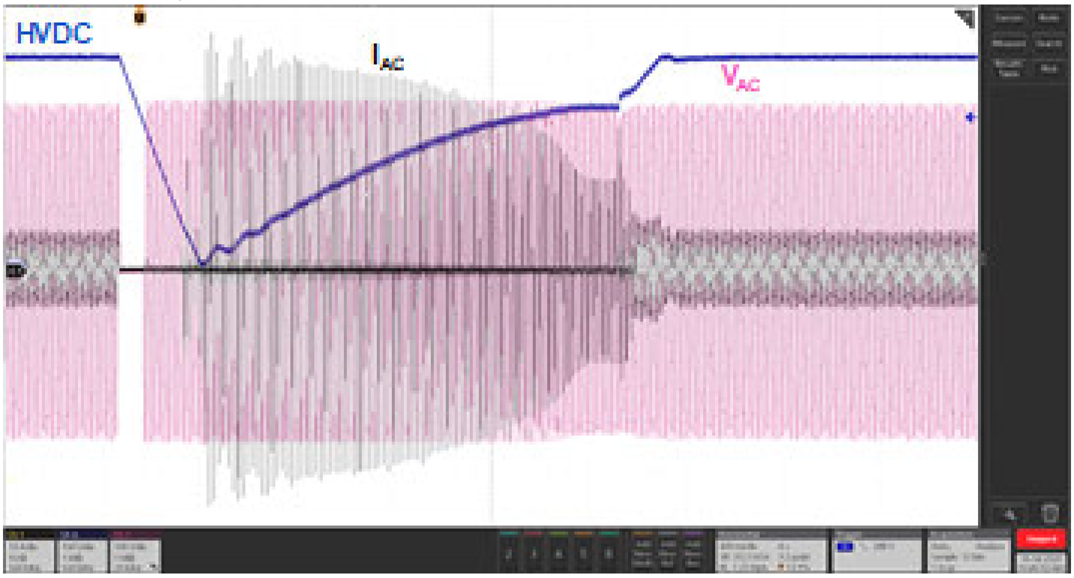
V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



The figure below shows the PFC totem pole board behavior, working at 230 V_{RMS} AC line voltage with a 1 kW DC load, for an AC line voltage dip with a 0% residual voltage applied for 100 ms. When the voltage is reapplied back and the HVDC voltage is lower than 80% of the 400 V_{DC}, SCRs are controlled in soft-start (as at any system startup) to avoid any component damage according to the AC line polarity.

Figure 71. Mains voltage dips with V_{AC} = 230 V_{rms} and P_{out} = 1 kW (0% residual voltage applied for 100 ms)

V_{AC} = AC line voltage
I_{AC} = AC line current
HVDC = PFC output voltage



12.5.3 Case temperature measurements

The figures below define the case temperature of each power switch with an ambient temperature of 30 °C, an AC line voltage of 230 V_{RMS} and a DC output load of 3.6 kW.

The maximum case temperature of the low side MOSFET1 is 82.7°C, the maximum case temperature of the high side MOSFET2 is 82.9°C and the maximum case temperature of the high side SCR is 71.2°C.

Figure 72. Low side SiC MOSFET1 case temperature measurement

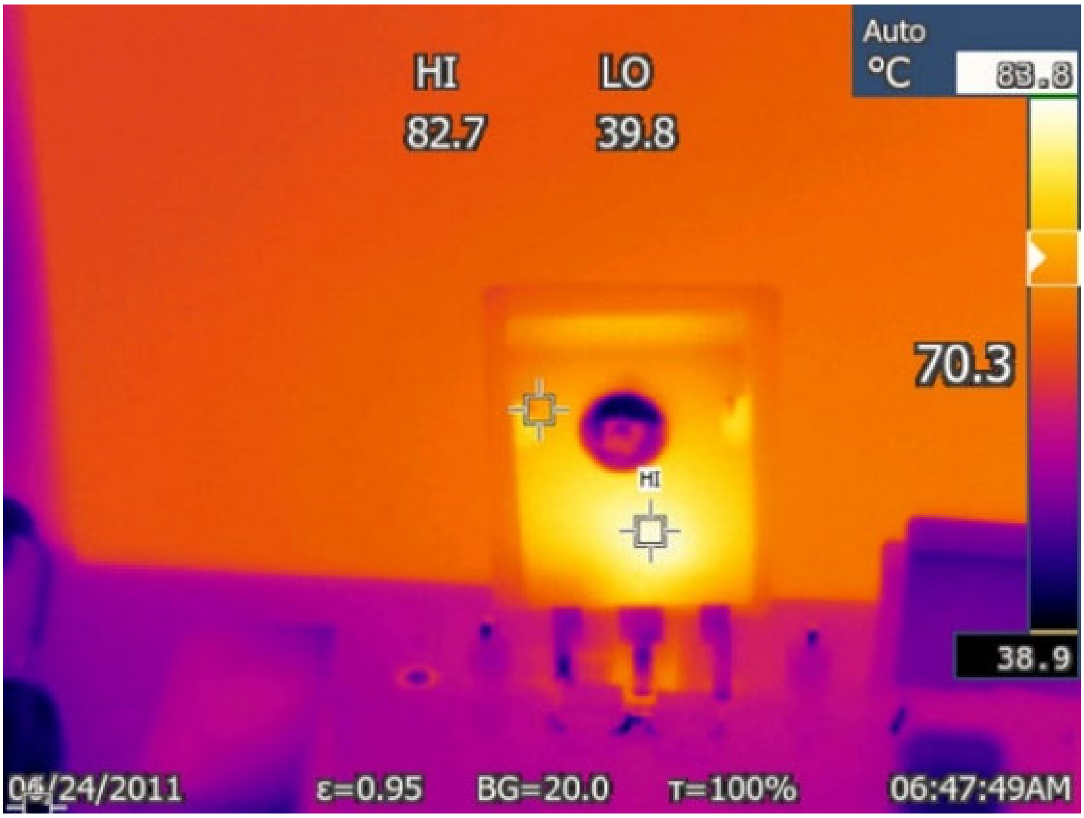
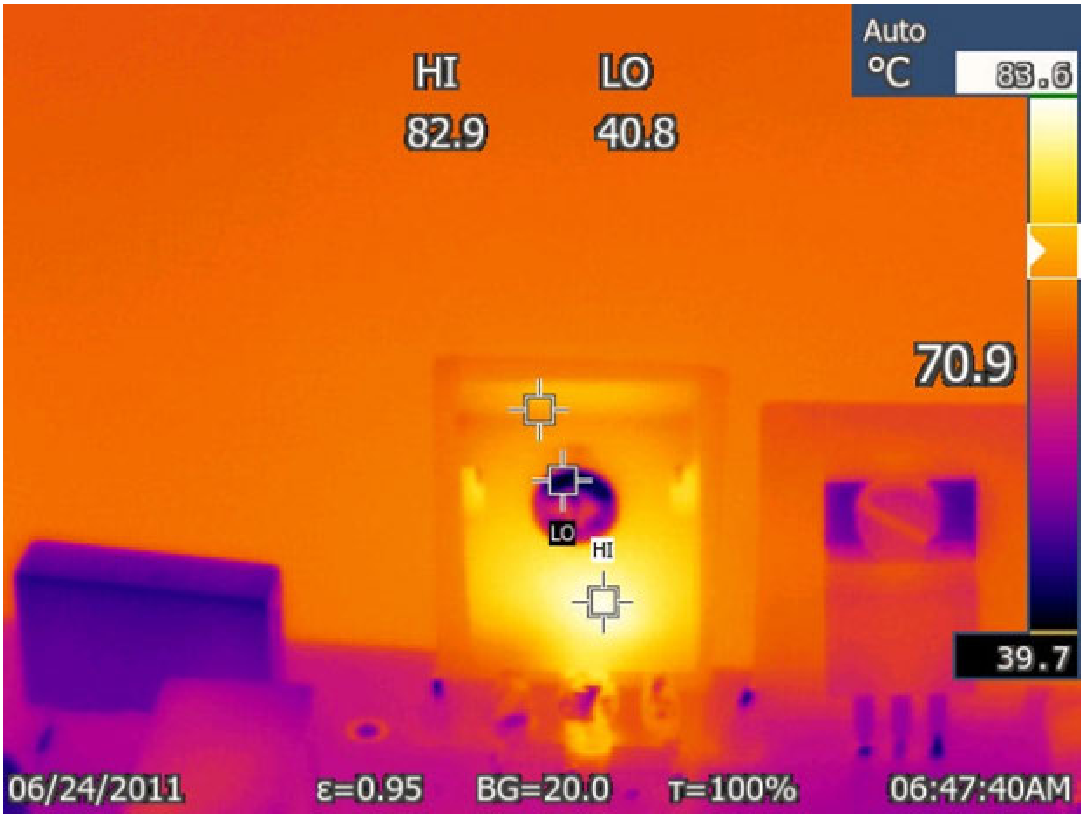


Figure 73. Low side SiC MOSFET2 case temperature measurement



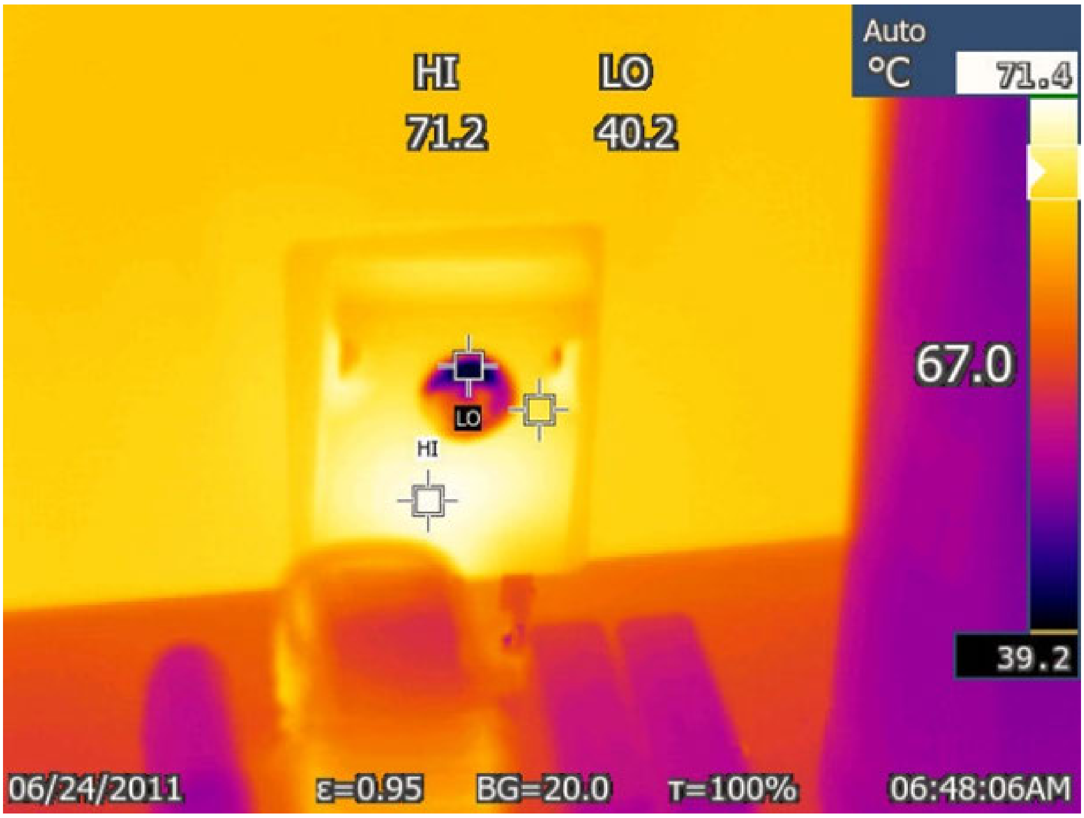


Figure 74. High side SCR case temperature measurement

13 PFC firmware description

13.1 Overview

The STSW-DPSTPFC1FW firmware source code for the STEVAL-DPSTPCF1 is provided on demand and is delivered free of charge only after explicit agreement with ST sales/marketing teams.

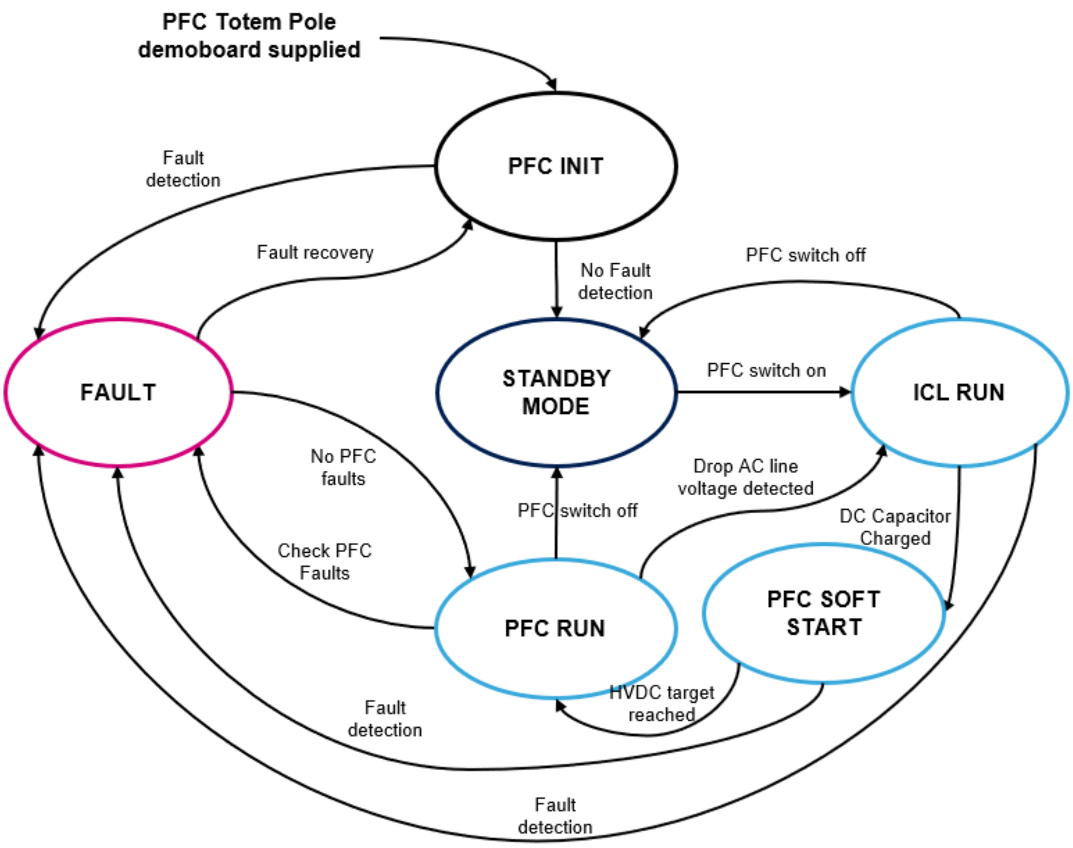
The firmware package is based on STM32CubeMX (v 4.22) and has been designed for IAR/EWARM workspace (version 7.70).

The firmware is ready to be used at first power on or immediately after a board reset event.

If a different parameter needs to be modified before the demo board starts running, refer to the "main.h" file. Once the modifications have been applied, the firmware must be re-built and downloaded into the STM32 microcontroller using your own development tool.

13.2 STEVAL-DPSTPFC1 PFC totem pole state machine

Figure 75. Digital PFC state machine

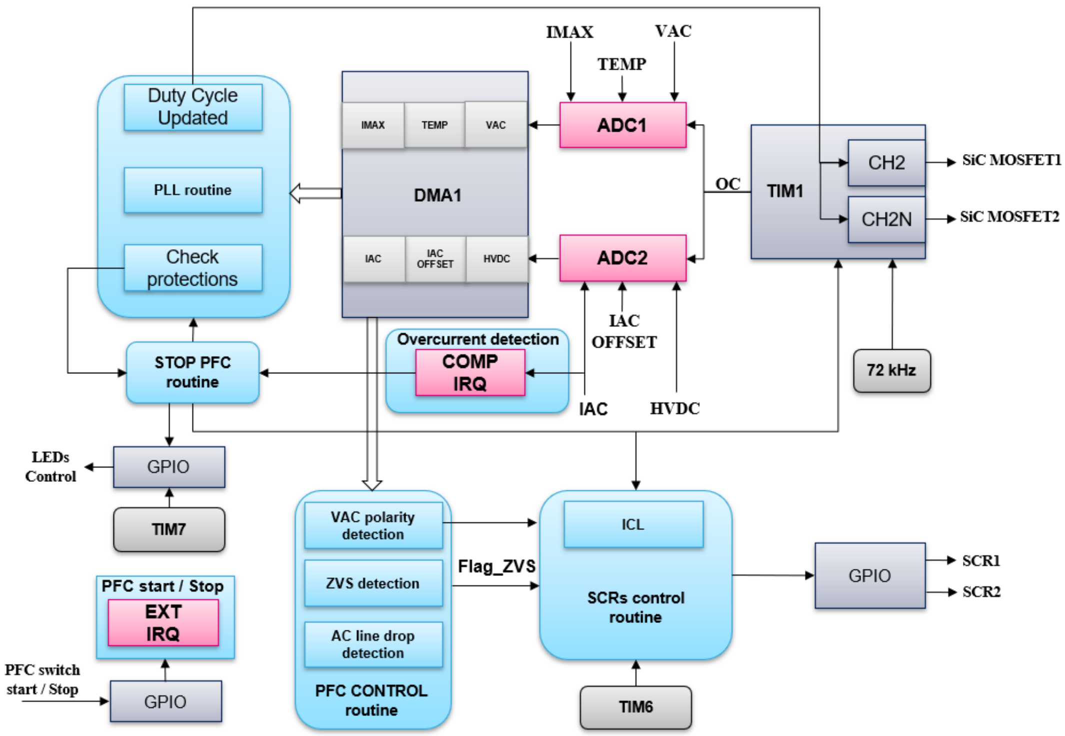


As shown in the figure above, the state machine is divided in the following states:

- **PFC INIT**: at board startup, the STM32 microcontroller is initialized. To switch from INIT to PFC OFF state, the AC line voltage has to be between 85 and 264 V_{AC} and the AC line frequency has to be between 45 and 65 Hz. If the AC line is out of range, the state machine goes from INIT to FAULT state.
- **PFC OFF**: SCRs and SiC MOSFETs are not controlled. SCRs allow PFC full disconnection at OFF state to avoid undesired losses by just turning them off . The bridgeless PFC totem pole board switches from PFC OFF to ICL RUN state when the user slides the PFC switch (SW1) to ON position.
- **ICL RUN**: to limit the inrush current, a resistor or NTC in series with DC capacitor is added. To limit the power losses during steady-state operation, the resistor has to be bypassed. Usually, a relay or a TRIAC is used for this purpose. On this board, a different startup procedure is implemented. With SCRs, the PFC output DC capacitor can be smoothly charged with a progressive phase control. To start charging the DC output capacitor, SCR1 and SCR2 have to be turned on according to the AC line voltage polarity in progressive phase control (SCR1 is turned on when the AC line polarity is negative and SCR2 is turned on when the AC line polarity is positive). When the output DC capacitor is charged to peak AC line voltage, the PFC control switches from ICL RUN to PFC SOFT START state.
- **PFC SOFT START**: the current and voltage loop are initialized. The DC output voltage (HVDC) is slowly incremented up to reference voltage target. Once the PFC output voltage reference is reached, the state machine goes from PFC SOFT START to PFC RUN state.
- **PFC RUN**: the PFC output DC voltage is regulated at 400 V_{dc} according to the output and the input conditions.
- **FAULTS**: if an out of range of the current (IAC), the voltage conditions or temperature occurs, the state machine activates PFC protection.

13.3 STM32 peripherals

Figure 76. STM32 MCU peripherals/registers used to control the PFC totem pole



- TIM1: its frequency is fixed at 72 kHz. CH2 is used to drive the PFC SiC MOSFET 1 and CH2N is used to drive the PFC SiC MOSFET 2
- TIM6: controls the inrush current by decreasing the SCR turn-on delay and used to detect the AC line frequency
- TIM7: is used to flash LEDs which define the PFC board status

- ADC1: reads the inrush current delay (I_{MAX}), the heat-sink temperature (TEMP) and the AC line voltage (V_{AC})
- ADC2: reads the inductor current (I_{AC}), the I_{AC} current offset (I_{AC} OFFSET) and the HVDC output PFC voltage (HVDC) alternatively
- DMA1: stores the converted values by ADC1 and ADC2. As soon as all values have been converted, an IRQ is generated and the PFC routine is executed
- COMP2/COMP4: retrieves overcurrent information from the power section. An IRQ is generated and the digital PFC is stopped if an overcurrent condition is detected
- EXTI_LINE3: defines the PFC start or stop. An IRQ is generated and the STM32 checks the PFC switch state to start or stop it.

13.4 MCU pins

Table 13. STM32 microcontroller MCU pins

MCU pin	Description	Comment
PC13	DC_DC_START	To enable/disable a DC-DC converter
PA0	IMAX	External potentiometer value to define the step to control SCRs in progressive phase control
PA1	FIX_VAR	External switch to control SCRs in progressive phase control or through a look-up table
PA2	TEMP	Heat sink temperature measurement
PA3	PFC_START	Switch to start or stop PFC
PA5	IAC_SENSE	AC line current measurement
PA6	IAC_OFFSET	OFFSET to measure the positive and negative AC line current
PA7	IAC_PROTECTION	I_{AC} value used to protect the PFC in case of I_{AC} overcurrent
PC4	LED1_STATUS	Control LED to determine if the I_{AC} flows
PC5	LED2_STATUS	Control LED to determine if the I_{AC} flows
PB0	TIM1_CH2N	High side MOSFET1 control
PB1	VAC_SENSE2	AC line voltage measurement
PB12	LED3_STATUS	Control LED to determine if the PFC output voltage is regulated
PB13	LED8_STATUS	Control LED to determine if the AC line voltage is detected
PB14	LED4_STATUS	Control LED to determine the if the PFC output voltage is regulated
PB15	HVDC_SENSE	PFC output DC voltage measurement
PC1	TIM1_CH2	Low side MOSFET2 control
PC6	LED6_STATUS	Control LED to determine if the AC line frequency is detected
PC8	LED10_STATUS	Control LED to determine heat sink temperature
PC9	LED5_STATUS	Control LED to determine if the AC line frequency is detected
PA8	SCR1	SCR1 control
PA9	SCR2	SCR2 control
PA10	ZVS	Zero cross of the AC line voltage (not used)
PA11	LED7_STATUS	Control LED to determine if the AC line voltage is detected
PA12	HV_DISCHARGE	To discharge the output DC capacitor
PC12	FAN_CTL	FAN control
PB4	LED9_STATUS	Control LED to determine heat sink temperature

13.5 IRQ priorities

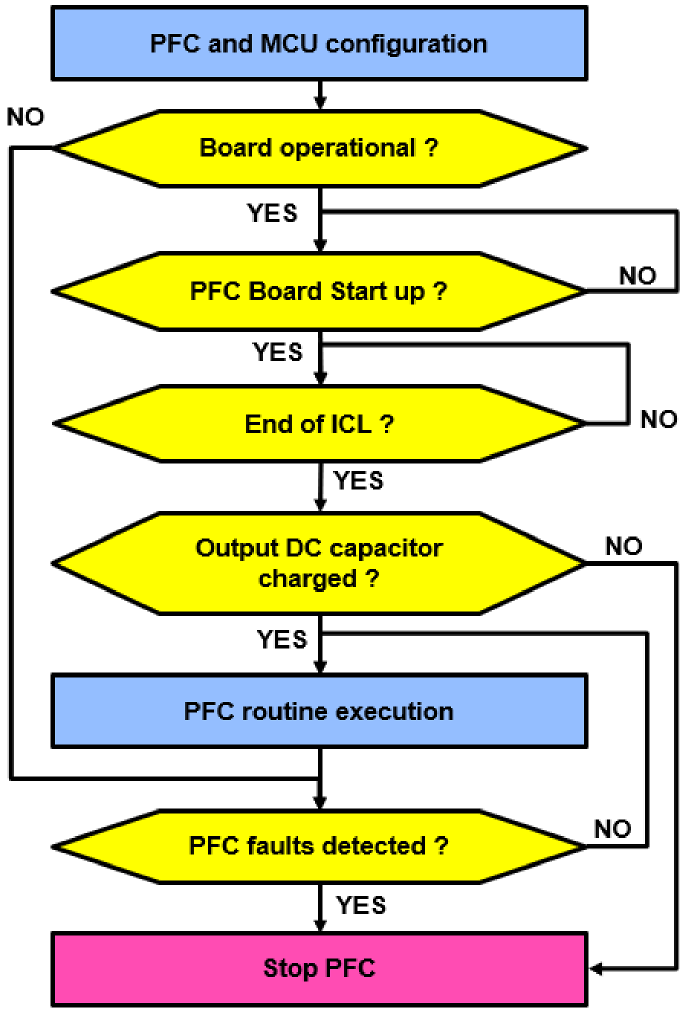
The table below shows the interrupts and their priorities for the integrated firmware, with 0 being the highest priority. Priority must be given to IRQs used to manage protection conditions or synchronizations.

Table 14. **MCU IRQ priorities**

Peripheral	IRQ use	Pre-emption priority	Sub priority
COMP2	Overcurrent protection (Positive IAC line cycle)	0	0
COMP4	Overcurrent protection (Negative IAC line cycle)	0	0
DMA1_CH1	PFC routine	1	0
EXTI3	PFC start	4	0
TIM3	PFC start	1	0
TIM6	ICL control	5	0
TIM7	LEDs control	8	0

13.6 Digital PFC firmware execution

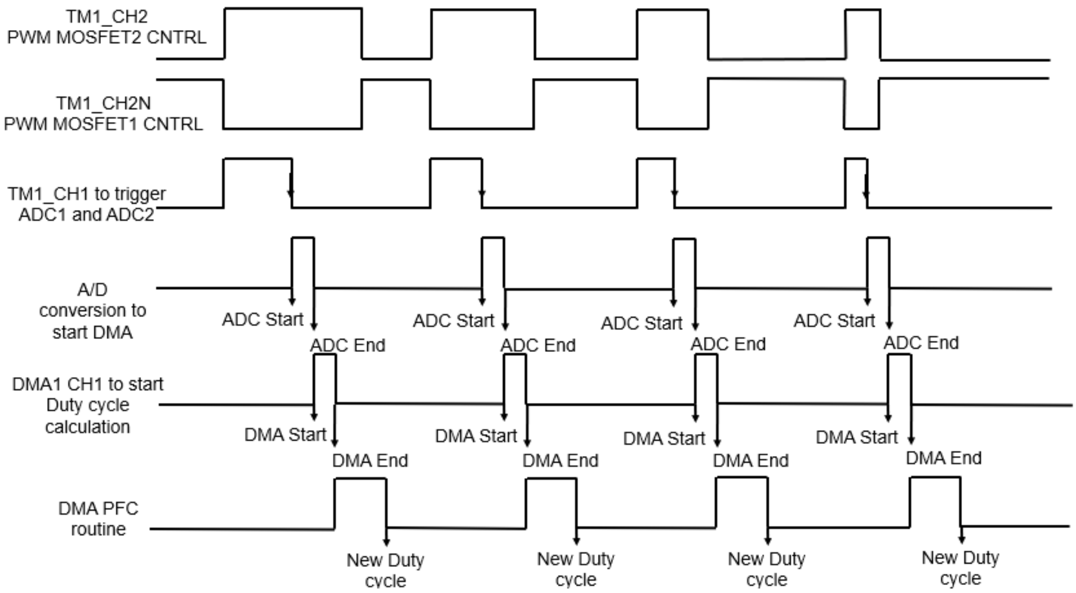
Figure 77. **PFC firmware event sequence flowchart**



13.7 PFC regulation

The signal output from TIM1_CH2 and from TIM1_CH2N are used to drive power MOSFET2 and MOSFET1, respectively. The frequency is fixed at 72 kHz and the duty cycle of the TIM1_CH2 and the TIM1_CH2N varies according to the PFC control strategy according to the current loop computation.

Figure 78. PFC management timing



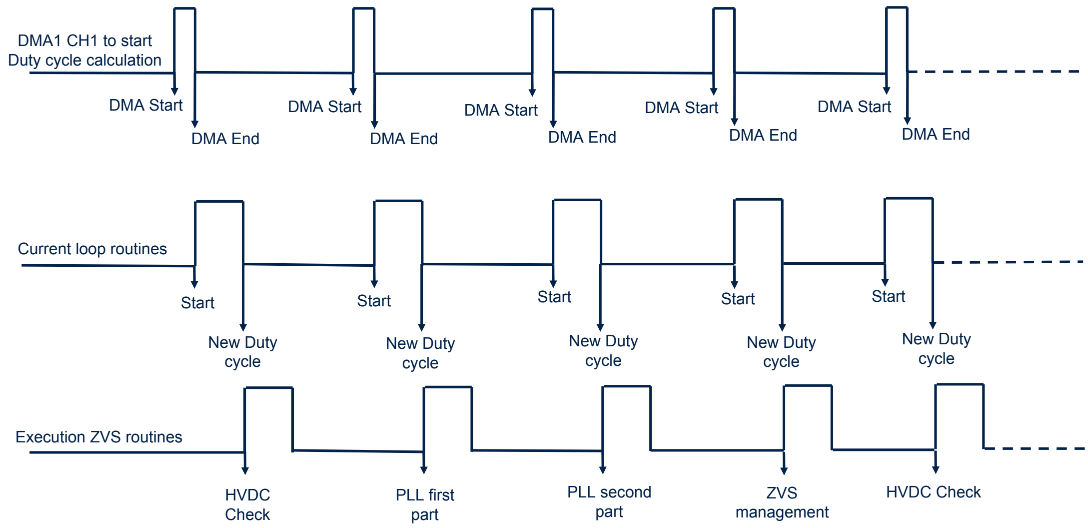
TIM1_CH1 is used to start ADC1 and ADC2 as detailed in the table below. The ADC conversion starts at the end of each TIM1_CH1 ON period. The duty cycle of TIM1_CH1 is equal to half the duty cycle of the TIM1_CH2 but no lower than 1.5 µs to avoid invalid conversions due to noise generated by the power MOSFET switching. For STM32 ADC the total conversion time is calculated as follows:

$$T_{ADCconv} = \frac{Sampling\ time + 12.5 cycles}{ADC_{CLK}} \tag{91}$$

Table 15. ADC conversion definition

ADC Rank	Signal measured	Sampling time
ADC1_Rank1	VAC	7.5 cycles
ADC1_Rank2	IMAX	4.5 cycles
ADC1_Rank3	TEMP	4.5 cycles
ADC2_Rank1	IAC	7.5 cycles
ADC2_Rank2	HVDC	4.5 cycles
ADC2_Rank4	IAC_OFFSET	4.5 cycles

Figure 79. PFC regulation and ZVS management timing



DMA_CH1 interruption calls current loop, feed forward and PLL routines.

Figure 80. Current loop and PLL execution flowchart

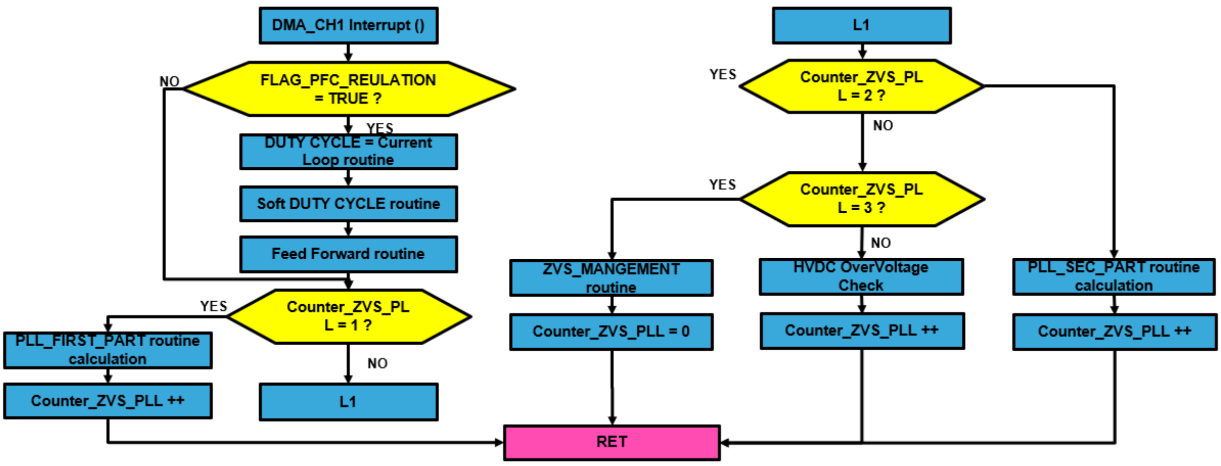


Table 16. Routine execution frequency

Routine name	Routine definition	Execution frequency
Current Loop	PFC regulation	72 KHz
Feed Forward	PFC regulation	72 kHz
PLL_FIRST_PART routine calculation	PLL calculation first part	18 kHz
PLL_SEC_PART routine calculation	PLL calculation second part	18 KHz
ZVS_MANGEMENT routine	Phase management and ZVS detection	18 KHz
HVDC Overvoltage Check	Check HVDC Overvoltage	18 KHz

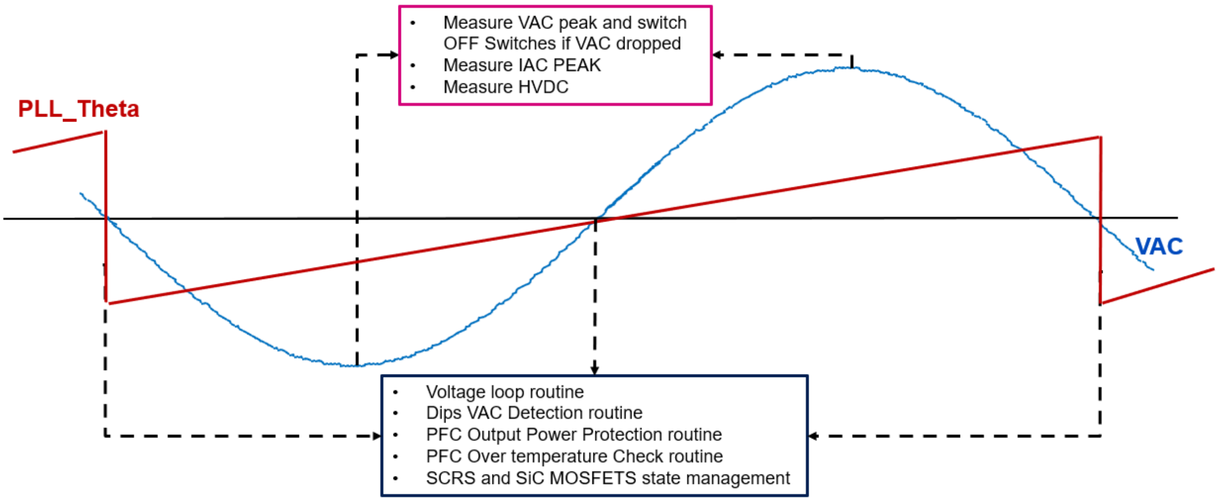
13.8 PFC synchronization with the AC line zero crossing

The PFC totem pole requires synchronization with the grid. To capture the phase information of single-phase power grids, a single-phase phase-locked loop (PLL) method is applied.

Thanks to the phase information from the PLL routine (`PLL_Theta`) information, `ZVS_Management` routine is called every 18 kHz and used to:

- manage the PFC, the voltage loop regulation at each AC line zero cross (twice the AC line frequency) and the AC line voltage dips
- control SCRs and SiC MOSFETS according the AC line voltage polarity
- switch SCRs and SiC MOSFETs off at each AC line zero cross
- check PFC totem pole board temperature

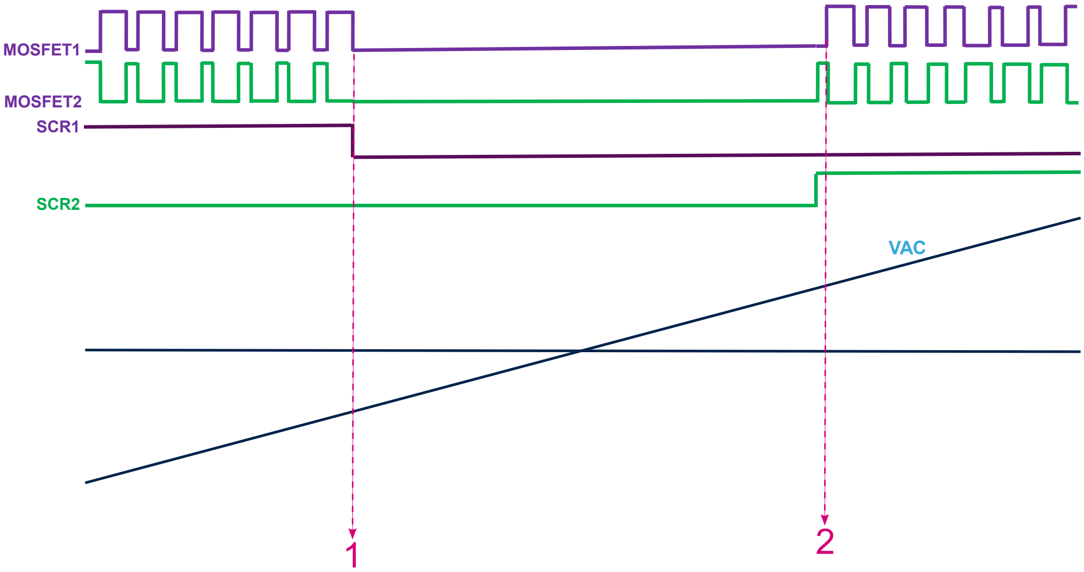
Figure 81. PFC synchronization with the AC line zero crossing



In the figure below:

- the dotted line with number 1 indicates:
  - SCRs turn off
  - MOSFETs turn off
  - Voltage loop communication routine
  - Dip V_{AC} detection routine
  - Heat-sink overtemperature check routine
  - PFC output power protection management routine
  - Test HVDC: if overvoltage is detected, SCRs and MOSFETs turn off on the next half AC line cycle
- the dotted line with number 2 indicates:
  - ZVS flag has been set (zero cross AC line voltage detected)
  - V_{AC} polarity has been saved
  - SCRs and MOSFETs are controlled if no HVDC overvoltage is detected

Figure 82. **PFC management at the AC line zero crossing**



13.9 PFC main files

The software for the digital PFC is composed of several files which contain all functions needed for the PFC operation. The main.h file contains the definitions of the system parameters. Assuming that the host application has the minimum necessary resources available (in terms of embedded peripherals, CPU load and code memory), it is sufficient to include these two files in the host application firmware and to appropriately call a function that initializes and starts the digital PFC.

13.9.1 ICL.c file

These routines manage the inrush current control at the board start up.

Get_Max_Inrush_Current_order () routine Reads the value of the external potentiometer (R30) to define the step value of the constant progressive phase control to control SCRs and therefore to control the peak inrush current.

ICL_Init () routine Initializes the timer used to reduce the SCR turn-on delay from half-cycle to half-cycle of the AC line cycle and read SW2 ICL PEAK switch state. The step of SCR turn-on delay reduction can be constant or variable (defined in the look up table) from one half-cycle to the following one according to SW2 switch.

ICL_Management () routine Manages the inrush current limiter at board startup and checks whether the output DC capacitor is charged

13.9.2 PI_Controller.c file

These routines manage the PFC.

PI_Regulator_IAC () routine PI controller implementation to shape the IAC line current on the AC line voltage

PI_Regulator_VDC () routine PI controller implementation to manage the PFC HVDC output voltage

CalcDutyFeedForward () routine To alleviate the feedback controller, a digital feed-forward control has been included in the current loop to calculate duty ratio

SET_KP_HVDC () routine Sets the proportional gain of the HVDC PI controller

SET_KI_HVDC () routine Sets the integral gain of the HVDC PI controller

SET_KP_IAC () routine Sets the proportional gain of the IAC PI controller

SET_KI_IAC () routine	Sets the integral gain of the IAC PI controller
SET_KP_PLL () routine	Sets the proportional gain of the PLL PI controller
SET_KI_PLL () routine	Sets the integral gain of the PLL PI controller
RST_uDigitalLowPassFilter () routine	Resets digital low pass filter
Sin_Wave_Reference () routine	Generates the AC line current sine wave reference
Soft_Duty_Cycle () routine	Manages the duty cycle at each AC line zero crossing to reduce the IAC current spike. SiC MOSFETs are controlled with a small pulse width. The pulse gradually increases to normal duty cycle
Soft_Start_PFC_Management () routine	During the board power-up, the internal voltage loop output increases from initial voltage under soft-start, reducing the current stress for all power switches. Once HVDC has reached 400 V_{DC}, the soft-start control is released to achieve regulation.
PFC_PI_Init_All () routine	Initializes HVDC, PLL and IAC PI controllers
PFC_PI_Init_REG () routine	Initializes HVDC and IAC PI controllers

13.9.3 PLL.c file

PLL_Zero_crossing_First_Part () routine	Tracks the frequency and phase of the AC line voltage (first part)
PLL_Zero_crossing_Second_Part () routine	Tracks the frequency and phase of the AC line voltage (second part)
Digital_LF () routine	Digital low pass Filter
uDigitalLowPassFilter () routine	Digital low pass Filter
Components DPSM_Trig_Functions () routine	Define cos and sin values according to the angle value
Park_Transformation () routine	Park transform
Rev_Park_Beta () routine	Reverses Park transform
Calc_Sin_Value_Ref () routine	Defines sin value
ShiftElectricAngle () routine	Shifts the phase angle of the current signal reference from the AC line voltage
PI_Regulator_PLL () routine	PI controller implementation to manage the PLL

13.9.4 System.c file

AC_Line_RMS_Detection ()	RMS and Peak AC line voltage measurement

AC_Line_Freq_Detection () routine AC line frequency measurement

Init_Switch_OFF_PFC () routine Switches PFC off and initializes MCU parameters

Get_Temp () routine Heat-sink temperature measurement

Get_Main_Voltage () routine AC line voltage measurement

Get_Main_Voltage_Rectifier () routine Absolute value of the AC line voltage measurement

Get_IAC_Current_uint32 () routine PFC chock current inductor measurement

Get_REF_IAC_Sensor_uint32 () routine Reference voltage of the current sensor measurement

Get_HVDC_output () routine PFC HVDC output voltage measurement

Board_Operational () routine Flashing LEDs indicating the board is operational

CLEAR_IT_DMA_TC () routine Clears IRQ DMA

PVD_Config () routine PVD configuration

Check_Board_StartUp () routine Checks AC line frequency, AC line RMS voltage, heat-sink temperature and current sensor

Init_MCU () routine Initializes all MCU parameters

PFC_TIMING_Management () routine Manages the zero crossing of the AC line voltage, the AC line drops and the heat-sink temperature

13.9.5 PFC_FAULT_DETECTION.c file

PFC_BusVoltageCheck () routine Checks PFC output HVDC voltage

PFC_OutputPowerProtection () routine Checks the PFC output power

PFC_OverCurrent_Check () routine Checks the PFC chock inductor overcurrent

PFC_IAC_Sensor_Check () routine Checks the current sensor

PFC_OverTemp_Check () routine Checks the heat-sink temperature

Dips_VAC_Detection () routine Detects the AC line drops

PFC_Statut_Led_Management () routine	Manages LED state
PFC_Statut_Faults_Management () routine	Manages PFC fault detection

14 Schematic diagrams

Figure 83. STEVAL-DPS334M1 circuit schematic (1 of 3)

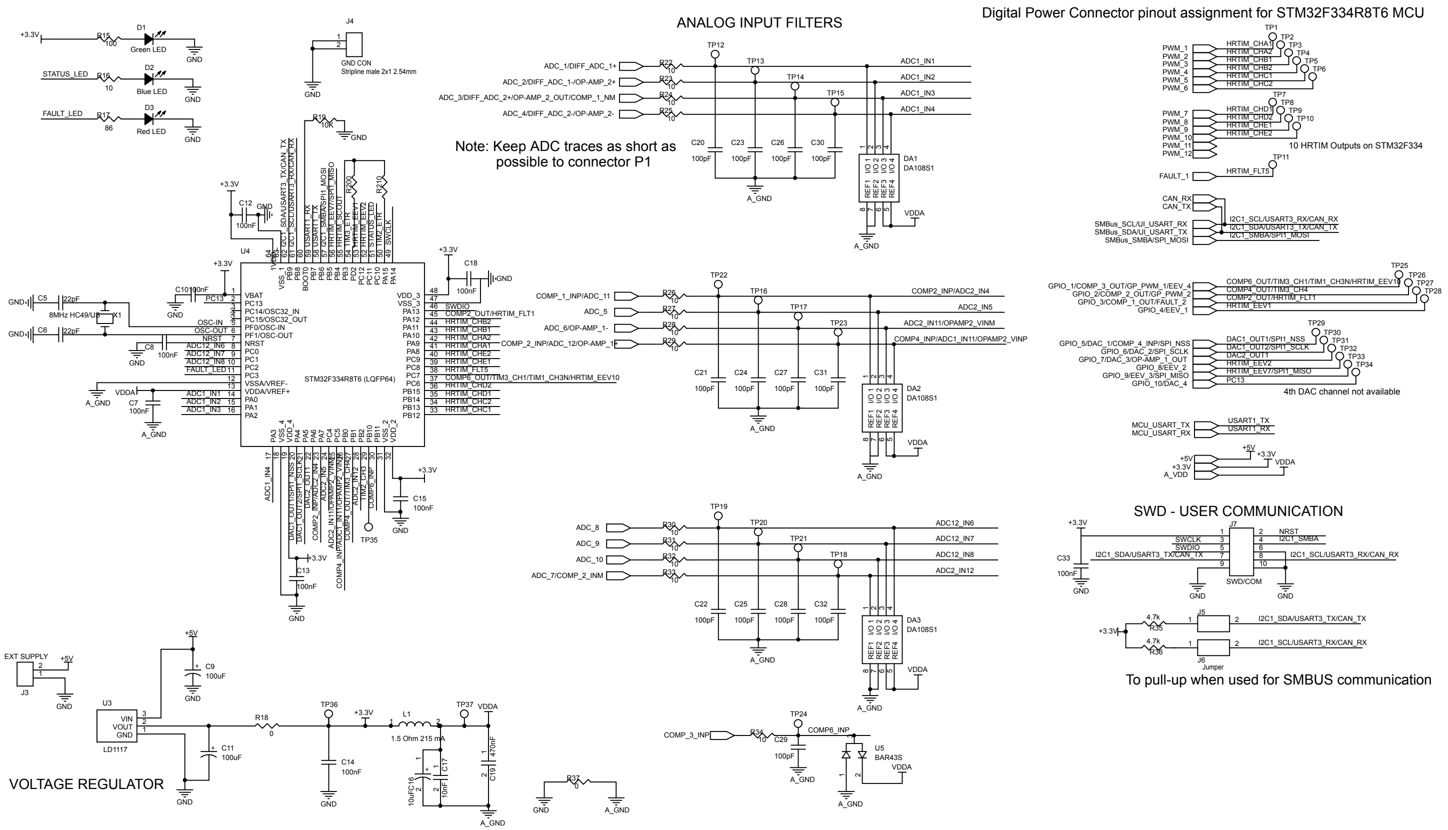


Figure 84. STEVAL-DPS334M1 circuit schematic (2 of 3)

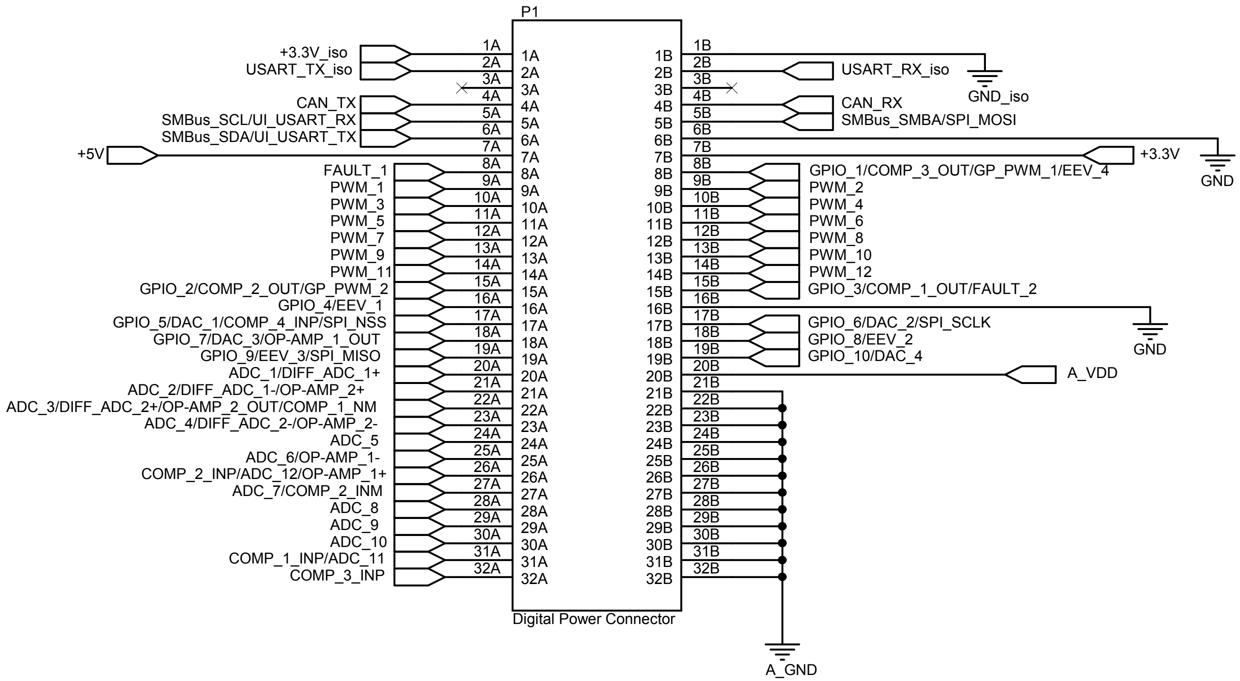


Figure 85. **STEVAL-DPS334M1 circuit schematic (3 of 3)**

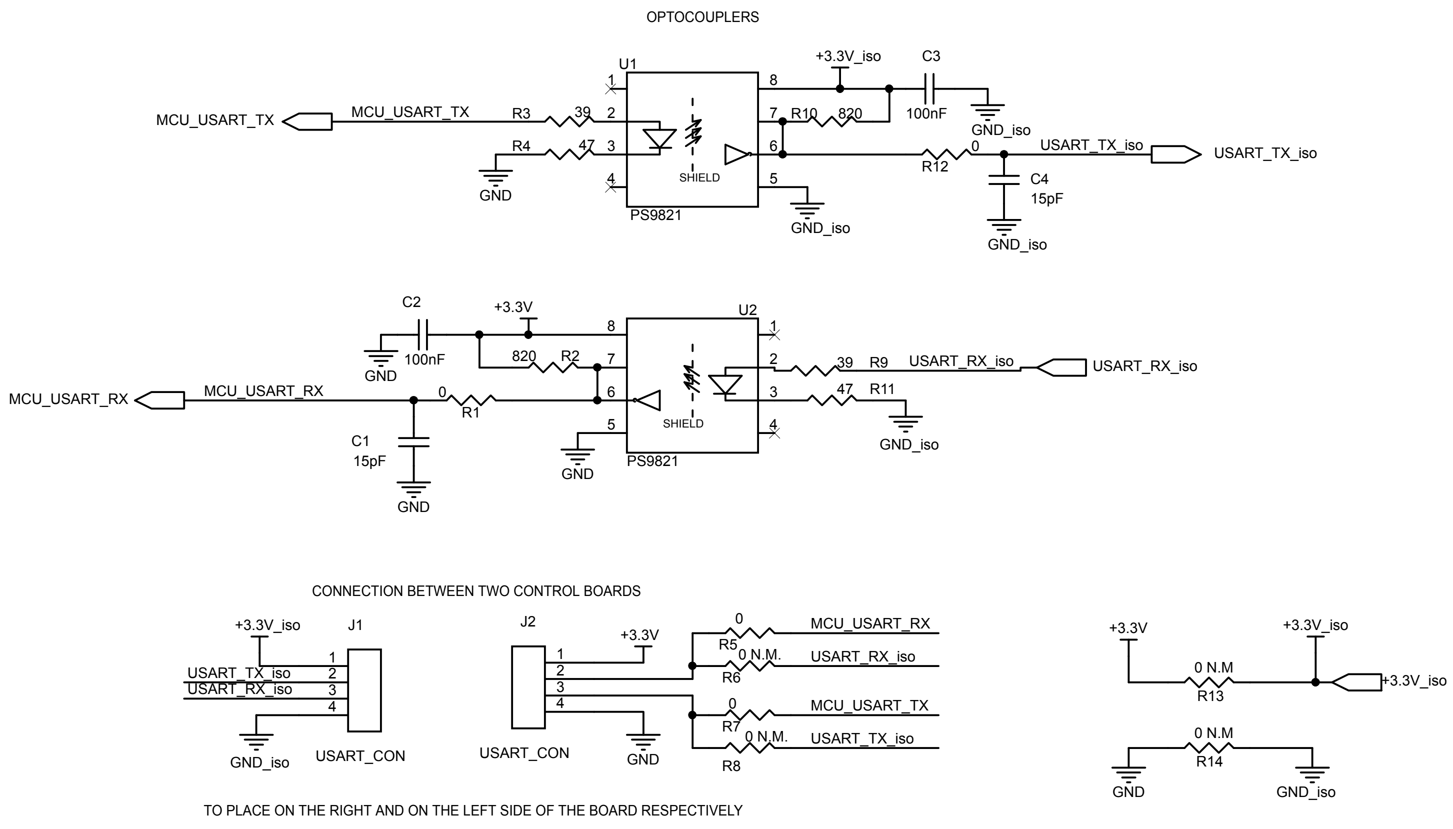


Figure 86. **STEVAL-DPSADP01 circuit schematic**

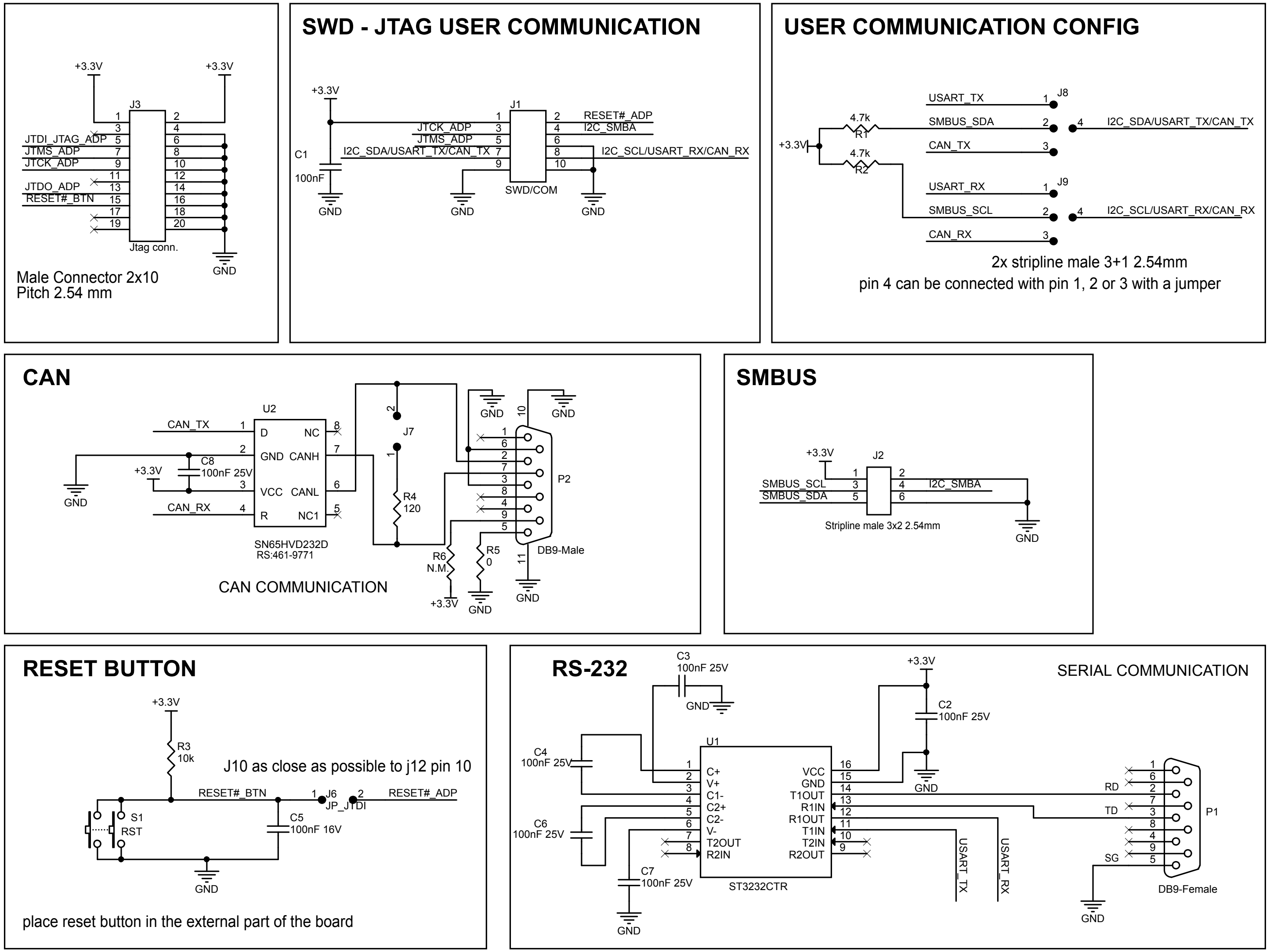
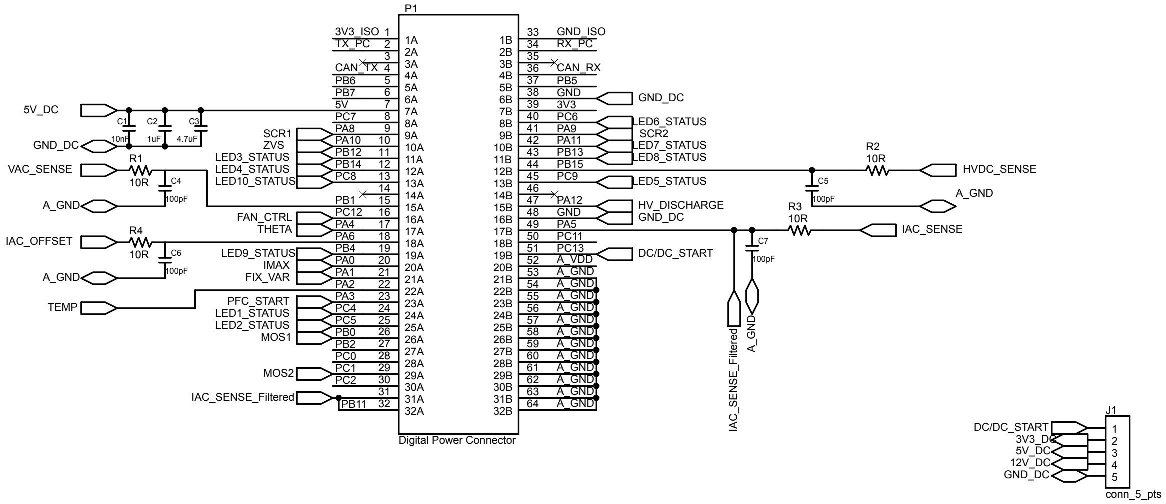


Figure 87. **STEVAL-DPSTPFC0 circuit schematic (1 of 4)**

EXTERNAL CONNECTORS



LED STATUS

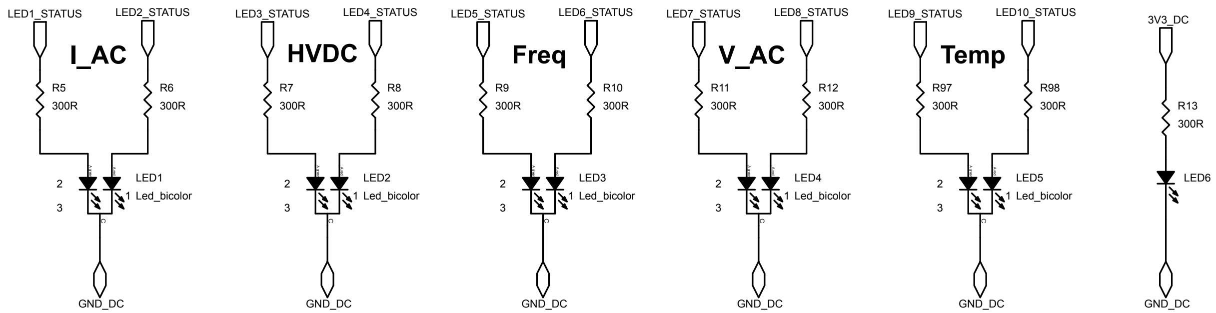
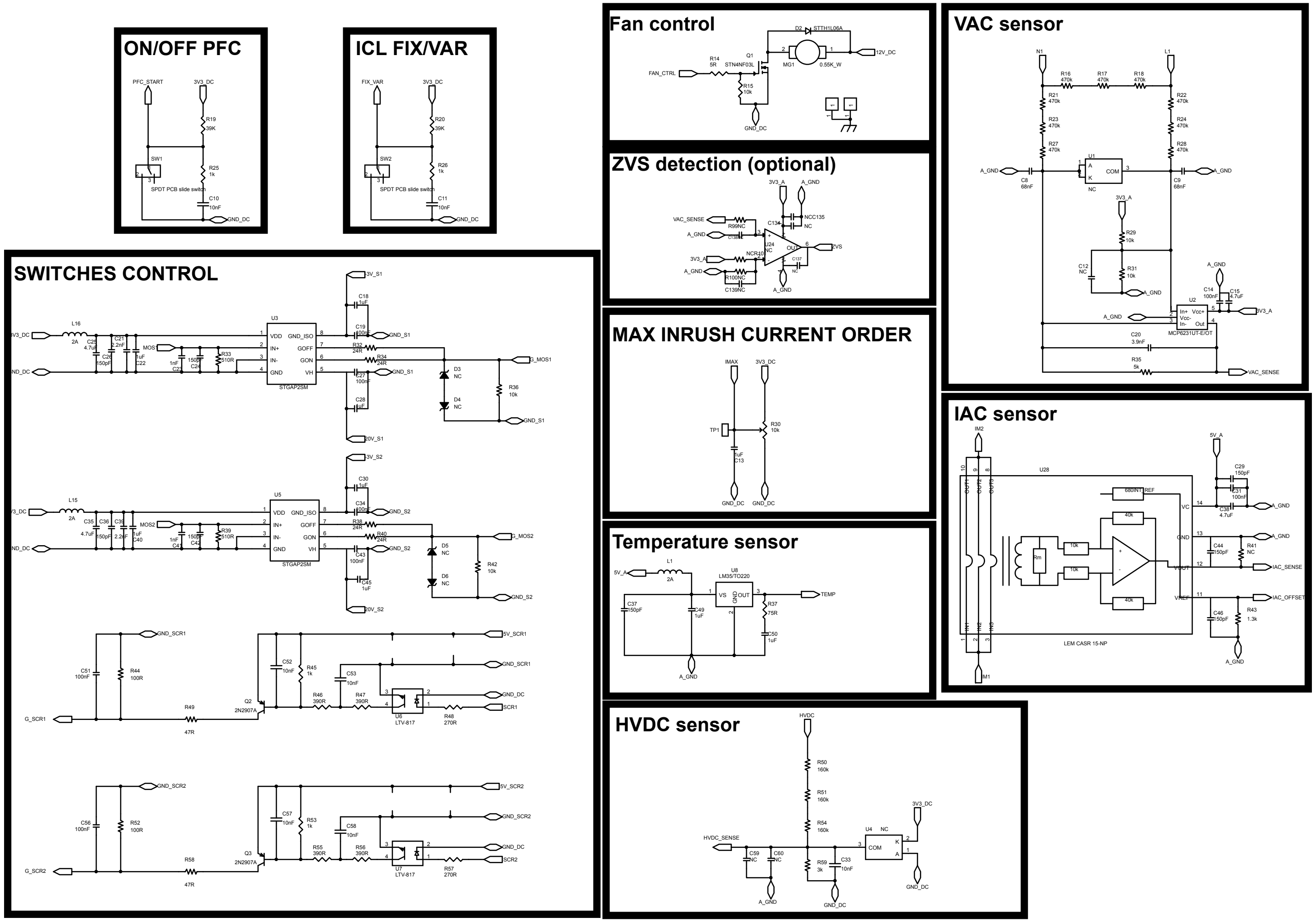


Figure 88. STEVAL-DPSTPFC0 circuit schematic (2 of 4)



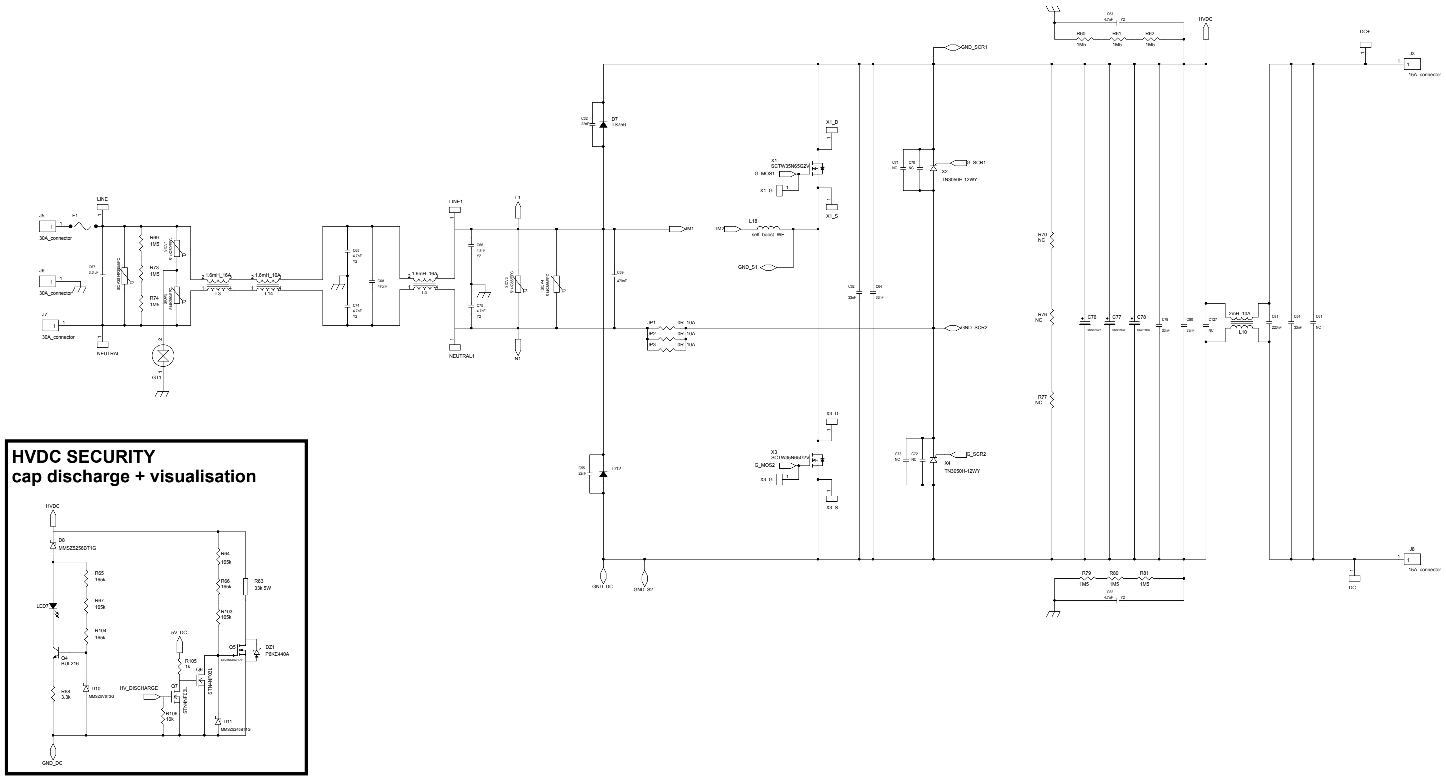
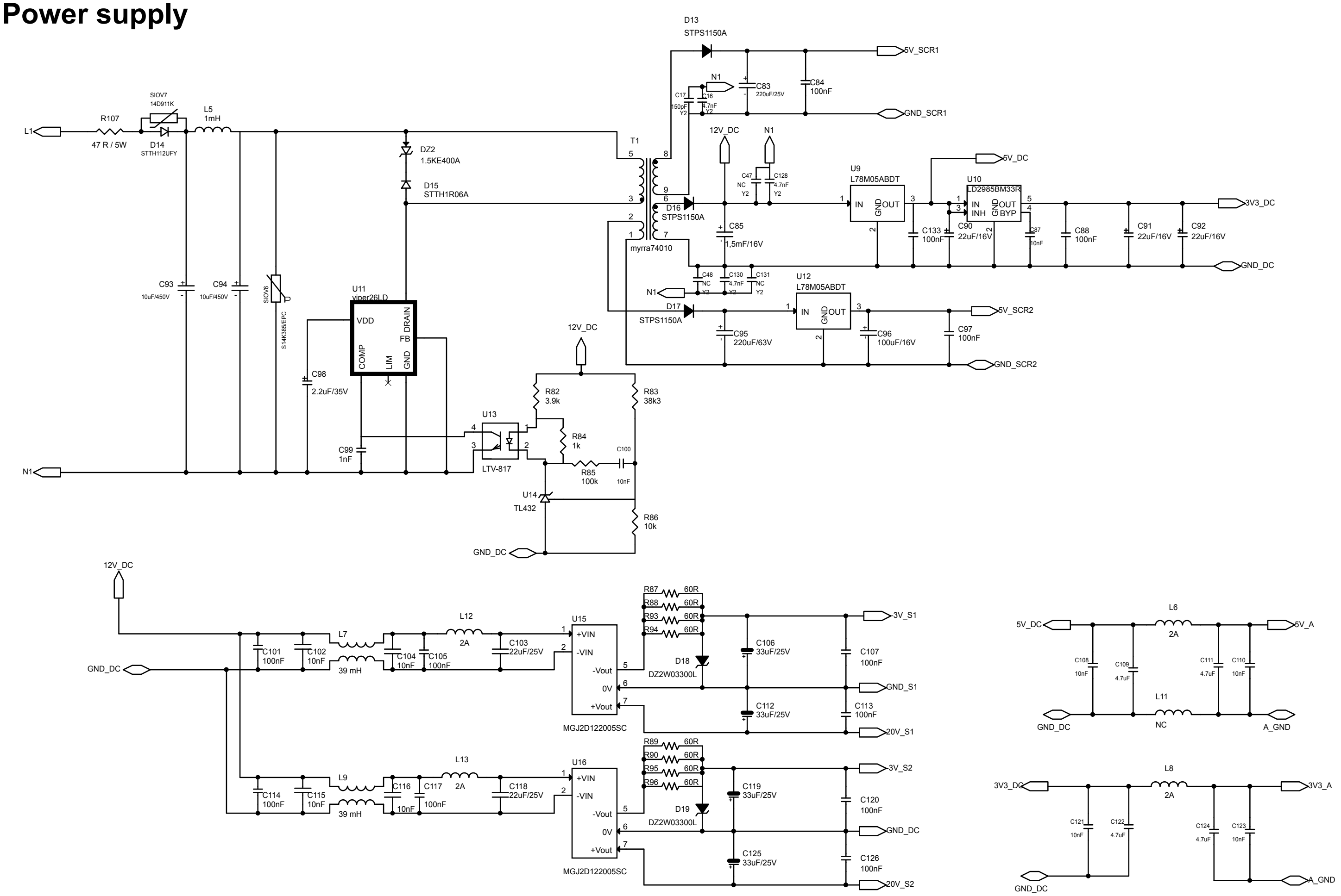


Figure 89. STEVAL-DPSTPFC0 circuit schematic (3 of 4)

Figure 90. **STEVAL-DPSTPFC0 circuit schematic (4 of 4)**

Power supply



15 Bill of materials

Table 17. STEVAL-DPSTPFC1 bill of materials

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	Table 18. STEVAL-DPS334C1		Digital power control board	ST	Not available for separate sale
2	1	Table 21. STEVAL-DPSTPFC0		PFC bridge-less totem pole	ST	Not available for separate sale

Table 18. STEVAL-DPS334C1 bill of materials

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	Table 19. STEVAL-DPS334M1		Digital power control module	ST	Not available for separate sale
2	1	Table 20. STEVAL-DPSADP01		DSMPS adapter	ST	Not available for separate sale

Table 19. STEVAL-DPS334M1 bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	2	C1, C4	15 pF 25 V ±10% smc0603 XR7	Ceramic capacitor	Any	
2	11	C2, C3, C7, C8, C10, C12, C13, C14, C15, C18, C33	100 nF 25 V ±10% smc0603 XR7	Ceramic capacitor	Any	
3	2	C5, C6	22 pF 25 V ±10% smc0603 XR7	Ceramic capacitor	Any	
4	2	C9, C11	100 μF 16 V ±20% capAluminumC	Electrolytic capacitor	PANASONIC	EEEFT1C101AR
5	1	C16	10 μF 16 V ±10% tantalioB	Tantalium capacitor	KEMET	T491B106K010AT
6	1	C17	10 nF 25 V ±10% smc0603 XR7	Ceramic capacitor	Any	
7	1	C19	470 nF 25 V ±10% smc0603 XR7	Ceramic capacitor	Any	
8	13	C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32	100 pF 25 V ±10% smc0603 XR7	Ceramic capacitor	Any	
9	3	DA1, DA2, DA3	DA108S1 sog0508wg244l200	Diode array	ST	DA108S1
10	1	D1	1.9 V smd0603	Green LED	KINGBRIGTH	KP-1608CGCK
11	1	D2	1.9 V smd0603	Blue LED	KINGBRIGTH	KP-1608QBC-D
12	1	D3	1.9 V smd0603	Red LED	KINGBRIGTH	KP-1608 SRC-PRV
13	2	J1, J2	USART_CON COn4TE215079	Ribbon cable connector	TE Connectivity	7-215079-4
14	1	J3	EXT SUPPLY MOR2X254	Terminal block	Phoenix Contact	1725656
15	3	J4, J5, J6	CON2A SIPTM2002	Strip Line Male 2X1 pitch 2, 54mm	Any	
16	1	J7	SWD/COM AMPMODE10	Connector header	HARTING	9185106324

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
17	1	L1	470 Ohm 100 MHz 250 mA sml0402	Ferrite beads	WURTH ELEKTRONIK	7427927141
18	1	P1	64 pin Conn64X254Harting09021646921	Male DIN 41612 through hole	Erni	533406
19	5	R1, R12, R20, R21, R37	0 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
20	2	R2, R10	820 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
21	2	R3, R9	39 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
22	2	R4, R11	47 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
23	2	R5, R7	0 750 mW ±5% SMR2010 SMD	Thick film resistor	VISHAY	CRCW20100000ZOEF
24	0	R6, R8	750 mW ±5% SMR2010 SMD	Thick film resistor (not mounted)	Any	
25	0	R13, R14	750 mW ±5% SMR2010 SMD	Thick film resistor (not mounted)	Any	
26	1	R15	100 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
27	14	R16, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34	10 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
28	1	R17	86.6 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
29	1	R18	0 1/4 W ±1% smr1206 SMD	Thick film resistor	Any	
30	1	R19	10 K 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
31	2	R35, R36	4.7 k 1/16 W ±1% smr0603 SMD	Thick film resistor	Any	
32	37	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37		Test point	Any	
33	2	U1, U2	PS9821 sog0508wg244l200	Optocoupler 1 chanel	NEC	PS9821-1-F3-AX
34	1	U3	LD1117 800 mA ±1% SMDPACK	Adjustable and fixed low drop positive voltage regulator	ST	LD1117DT33TR
35	1	U4	STM32F334R8T6 (LQFP64) quad50m64wg1200	Mainstream mixed signals MCU Arm Cortex-M4 core	ST	STM32F334R8T6

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
36	1	U5	BAR43S 30 V, 0.1 A smsot23123	General purpose signal Schottky diode	ST	BAR43SFILM
37	1	X1	8 MHz HC49/US	Crystal oscillator	EUROQUARTZ	8.000MHZ 49USMX/30/50/40/18PF /ATF
37	1		2.54 mm	Flat cable	Samtec Inc.	HCSD-05-D-11.40-01-N-G-R
38	1		Micro-Match 4 ways, 9.9"", 250mm, 1.27mm	AMP Micro-MaTch	TE Connectivity	1483350-3

Table 20. **STEVAL-DPSADP01 bill of materials**

Item	Q.ty	Ref.	Part	Description	Manufacturer	Order code
1	8	C1, C2, C3, C4, C5, C6, C7, C8	100 nF 25 V ± 10% smc0603	Capacitor Ceramic XR7	Any	
2	1	J2	CON6 blkcon100vhtm2oew2006	Stripline male 3x2 2.54mm	Any	
3	1	J3	Jtag conn. walcon100vhtm2oew32520	JTAG connector	TE-Connectivity	5103308-5
4	2	J6, J7	JP_JTDI siptm2002	Jumper pitch 2, 54 mm	Any	
5	1	J8	JP_JTDI siptm2002	Stripline Male 2X1 pitch 2, 54 mm	Any	
6	2	J9, J11	JP_JTDI siptm3003	Stripline Male 3X1 pitch 2, 54 mm	Any	
7	1	J10	SWD/COM AMPMODE10	Prog Connector	HARTING	9185106324
8	1	P1	DB9-Female dsubrs318tm9f	90° Through Hole	TE-Connectivity	1-1634584-2
9	1	P2	DB9-Male dsubrp318tm9mcon	90° Through Hole	RS-Pro	
10	2	R1, R2	4.7 k 1/16 W ± 1% smr0603 SMD	Thick film resistor	Any	
11	1	R3	10 k 1/16 W ± 1% smr0603 SMD	Thick film resistor	Any	
12	1	R4	120 1/16 W ± 1% smr0603 SMD	Thick film resistor	Any	
13	1	R5	0 1/16 W ± 1% smr0603 SMD	Thick film resistor	Any	
14	0	R6	N.M. 1/16W ± 1% smr0603 SMD	Thick film resistor (not mounted)	Any	
15	1	S1	RST puls4smd	Surface mount tactile switch	TE Connectivity	FSM4J
16	1	U1	ST3232CTR SOG65M16WG820L635	RS-232 driver and receiver	ST	ST3232CTR
17	1	U2	SN65HVD232D SOG0508WG244L200	CAN transceiver	TI	SN65HVD232D

Table 21. **STEVAL-DPSTPFC0 bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	18	C1, C10, C11, C33, C52, C53, C57, C58, C87, C100, C102, C104, C108, C110, C115, C116, C121, C123	10 nF cms0805 25 V ±10 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207066
2	10	C2, C13, C18, C22, C28, C30, C40, C45, C49, C50	1 µF cms0805 25 V ±10 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207078
3	9	C3, C15, C25, C35, C38, C109, C111, C122, C124	4.7 µF cms0805 16 V ±10 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207053
4	4	C4, C5, C6, C7	100 pF cms0805 25 V ±5 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207054
5	2	C8, C9	68 nF cms0805 25 V ±5 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207071
6	20	C14, C19, C27, C31, C34, C43, C51, C56, C84, C88, C97, C101, C105, C107, C113, C114, C117, C120, C126, C133	100 nF cms0805 25 V ±10 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207072
7	9	C16, C63, C82, C128, C130, C65, C66, C74, C75	4.7 nF capa_Y2_LS_7_5mm 400 VAC ±10 %	Capacitors	Kemet	C947U472MZVDAAWL45
8	1	C17	150 pF capa_Y2_LS_7_5mm 440 VAC ±10 %	Capacitors	Any	
9	1	C20	3.9 nF cms0805 25 V ±5 % SMD_0805	Capacitors	Any	
10	2	C21, C39	2.2 nF cms0805 25 V ±5 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207062
11	3	C23, C41, C99	1 nF cms0805 25 V ±10 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207060
12	8	C24, C26, C29, C36, C37, C42, C44, C46	150 pF cms0805 25 V ±10 % SMD_0805	Capacitors	WURTH ELEKTRONIK	885012207055
13	2	C32, C55	22 nF capa_x2_15mm 305 VAC ±10 % SMD_0805	Capacitors	Any	
14	5	C54, C62, C64, C79, C80	33 nF capa_x2_15mm 305 VAC ±10 %	Capacitors	WURTH ELEKTRONIK	890334025006
15	1	C67	3.3 µF capa_X2_27.5mm 275 VAC ±10 %	Capacitors	WURTH ELEKTRONIK	8324027025CS
16	2	C68, C69	470 nF capa_x2_22_5mm 305 VAC ±10 %	Capacitors	Any	
17	3	C76, C77, C78	680 µF/450V capa_680uf-450V 450 V ±20 %	Capacitors	WURTH ELEKTRONIK	861141486026

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
17	3	C76, C77, C78	680 µF/450V capa_680uf-450V 450 V ±20 %	Capacitors	WURTH ELEKTRONIK	B43649A5687M05
18	1	C81	220 nF capa_x2_15mm 305 VAC ±10 %	Capacitors	Any	
19	1	C83	220 µF/25 V capa_cms_16V_D 25 V ±20 %	Capacitors	Any	
20	1	C85	1.5 mF/16 V capa_cms_63v_H13 16 V ±20 %	Capacitors	WURTH ELEKTRONIK	865080362017
21	3	C90, C91, C92	22 µF/16V capa_cms_63V 16 V ±20 %	Capacitors	Any	
22	2	C93, C94	10 µF/450V capa_cms_450V_K16 450 V ±20 %	Capacitors	Any	
23	1	C95	220 µF/63V capa_cms_63v_H13 63 V ±20 %	Capacitors	Any	
24	1	C96	100 µF/16V capa_cms_16V_D 16 V ±20 %	Capacitors	WURTH ELEKTRONIK	865060343005
25	1	C98	2.2 µF/35V capa_cms_63V 35 V ±20 %	Capacitors	WURTH ELEKTRONIK	865250540001
26	2	C103, C118	22 µF/25V cms0805 25 V ±20 %	Capacitors	Any	
27	4	C106, C112, C119, C125	33 µF/25V capa_cms_35V_4_7uF 25 V ±20 %	Capacitors	Any	
28	13	DC-, DC+, LINE, X1_S, X1_G, X1_D, LINE1, X3_S, X3_G, X3_D, NEUTRAL, NEUTRAL1, TP1	HVDC, L1, L2, N1, N2	Test point	VERO	20-136
29	1	DZ1	P6KE440A do15 440 V 600 W	600 W TVS in DO-15	ST	P6KE440A
30	1	DZ2	1.5KE400A do201 400 V 600 W	1500 W TVS in DO-201	ST	1.5KE400A
31	1	D2	STTH1L06A sma 600 V 1 A	Low drop ultra fast diode	ST	STTH1L06
32	2	D7, D12	TS756 P600 600 V 6 A	TS756_diode_standard	Any	
33	1	D8	MMSZ5256BT1G SOD123 30 V 500 mW ±5 %	Zener diode	Any	
34	1	D10	MMSZ5V6T3G SOD123 5.6 V 500 mW ±5 %	Zener diode	Any	
35	1	D11	MMSZ5245BT1G SOD123 15 V 500 mW ±5 %	Zener diode	Any	
36	3	D13, D16, D17	STPS1150A sma 150 V 1 A	Power Schottky rectifier	ST	STPS1150
37	1	D14	STTH112UFY smbflat 1200 V 1 A	Ultra fast diode	ST	STTH112UFY
38	1	D15	STTH1R06A sma 600 V 1 A	Turbo 2 ultra fast diode	ST	STTH1R06A
39	2	D18, D19	DZ2W03300L SOD123 3.3 V 1 W	3V3_zener_diode_SOD-123	Any	
40	1	F1	FUSE support_fusible_6_3_32	Fuse holder	SCHURTER	0031.8231
41	1	GT1	GTD_EC600X GTD_EC600X 600 V 5 kA	Gas tube discharge	EPCOS	B88069X2830S102
42	3	JP1, JP2, JP3	0R_10A shunt_harwin_10A 10 A	SMD jumper	Any	

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
43	1	J1	conn_5_pts con_5pts_RS_pas3_5mm 300 V 10 A	Terminal block	Any	
44	2	J3, J8	15A_connector 15A_connector 15 A	Connector	KEYSTONE	7691
45	3	J5, J6, J7	30A_connector 30A_DC_connector 30 A	Connector	KEYSTONE	8197
46	5	LED1, LED2, LED3, LED4, LED5	Led_bicolor led_bicolor_small_pad	LED	VISHAY	VLMV3100-GS08
47	2	LED6, LED7	LED_RED_SMD1206 cms1206	LED	Any	
48	7	L1, L6, L8, L12, L13, L15, L16	2 A cms0805 2 A ±25 %	Ferrite bead	MURATA	BLM21PG221SN1D
49	3	L3, L4, L14	1.6 mH_16A WE_CMBH_1.6mH_16A 16.4 A	WE-CMBHV series	WURTH ELEKTRONIK	744831016164
50	1	L5	1 mH 1mH_WE_TI 300 mA ±5 %	Power inductor	WURTH ELEKTRONIK	744741102
51	2	L7, L9	39 mH filter_39mH_WE_CMB 300 mA ±2=30 %	Filter	WURTH ELEKTRONIK	744821039
52	1	L10	2 mH_10A filter_2mH_10A_WE_CMB 10 A	Filter	WURTH ELEKTRONIK	7448031002
53	1	L18	self_boost_WE self_boost_WE_toroid 360 μH 16 A	PFC boost inductor	WURTH ELEKTRONIK	750318545
54	1	P1	DIN41612_b_64	Digital power connector	Any	
55	3	Q1, Q6, Q7	STN4NF03L sot223 30 V 4 A	StripFET power MOSFET	ST	STN4NF03L
56	2	Q2, Q3	2N2907A to18 60 V 600 mA	60 V_PNP BJT	Any	
57	1	Q4	BUL216 to220ab 800 V 4 A	High voltage fast switching NPN power transistor	ST	BUL216
58	1	Q5	STQ1NK80ZR-AP to92am 800 V 300 mA	SuperMESH power MOSFET	ST	STQ1NK80ZR-AP
59	4	R1, R2, R3, R4	10 R cms0805 0.125 W ±1 %	Resistors	Any	
60	11	R5, R6, R7, R8, R9, R10, R11, R12, R13, R97, R98	300 R cms0805 0.125 W ±5 %	Resistors	Any	
61	1	R14	5 R cms0805 0.125 W ±1 %	Resistors	Any	
62	5	R15, R36, R42, R86, R106	10 k cms0805 0.125 W ±1 %	Resistors	Any	
63	9	R16, R17, R18, R21, R22, R23, R24, R27, R28	470 k cms1206 0.25 W ±1 %	Resistors	Any	
64	2	R19, R20	39 K cms0805 0.125 W ±5 %	Resistors	Any	
65	6	R25, R26, R45, R53, R84, R105	1 k cms0805 0.125 W ±5 %	Resistors	Any	
66	3	R29, R31	10 k cms0805 0.125 W ±1%	Resistors	Any	
67	1	R30	10 k potar_vertical_rotatif 0.05 W ±20 %	Resistors	Any	

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
68	4	R32, R38, R34, R40	24 R cms1206 0.25 W ±1 %	Resistors	Any	
69	2	R33, R39	510 R cms0805 0.125 W ±5 %	Resistors	Any	
70	1	R35	5 k cms0805 0.125 W ±0.1 %	Resistors	Any	
71	1	R37	75 R cms0805 0.125 W ±5 %	Resistors	Any	
72	1	R43	1.3 k cms0805 0.125 W ±1 %	Resistors	Any	
73	2	R44, R52	100 R cms0805 0.125 W ±1 %	Resistors	Any	
74	4	R46, R47, R55, R56	390 R cms0805 0.125 W ±5 %	Resistors	Any	
75	2	R48, R57	270 R cms0805 0.125 W ±5 %	Resistors	Any	
76	2	R49, R58	47 R r1w 2 W ±5 %	Resistors	Any	
77	3	R50, R51, R54	160 k cms1206 0.25 W ±0.1 %	Resistors	Any	
78	1	R59	3 k cms0805 0.125 W ±0.1 %	Resistors	Any	
79	9	R60, R61, R62, R69, R73, R74, R79, R80, R81	1M5 cms1206 0.25 W ±5 %	Resistors	Any	
80	1	R63	33 k 5 W res1000 5 W ±5 %	Resistors	VISHAY	CW00533K00JE12
81	6	R64, R65, R66, R67, R103, R104	165 k cms1206 0.125 W ±5 %	Resistors	Any	
82	1	R68	3.3 k cms0805 0.125 W ±5 %	Resistors	Any	
83	1	R82	3.9 k cms0805 0.125 W ±1 %	Resistors	Any	
84	1	R83	38k3 cms0805 0.125 W ±1 %	Resistors	Any	
85	1	R85	100 k cms0805 0.125 W ±1 %	Resistors	Any	
86	8	R87, R88, R89, R90, R93, R94, R95, R96	60R cms1206 0.25 W ±1 %	Resistors	Any	
87	1	R107	47R r5W 5W ±5 %	Resistors	Any	
88	2	SIOV1, SIOV5	S14K250/EPC NTC_S238_EPCOS 250 VAC	Varistors	Any	
89	5	SIOV2, SIOV3, SIOV4, SIOV6, SIOV7	S14K385/EPC NTC_S238_EPCOS 385 VAC	Varistors	Any	
90	2	SW1, SW2	switch_HVDC	SPDT PCB slide switch	Any	
91	1	T1	myrra74010 12 W	Flyback transformer	MYRRA	74010
92	1	U2	MCP6231UT-E/OT sot23_5	CMOS operational amplifier	MICROCHIP	MCP6231UT-E/OT
93	2	U3, U5	STGAP2SM so8	Galvanically isolated single gate driver	ST	STGAP2SM
94	3	U6, U7, U13	LTV-817 dip4	LTV-817_DIP4	Any	
95	1	U8	LM35/TO220 to220ab	Temperature sensor	TEXAS INSTRUMENTS	LM35DT/NOPB
96	2	U9, U12	L78M05ABDT LM2931_DPAK 5 V 0.5 A	Precision 500 mA regulator	ST	L78M05ABDT-TR
97	1	U10	LD2985BM33R sot23_5	Very low drop and low noise voltage regulator with inhibit function	ST	LD2985BM33R
98	1	U11	viper26LD SOIC16	High voltage converter with direct feedback	ST	VIPER26LD

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
99	1	U14	TL432 sot23	Voltage reference	TEXAS INSTRUMENTS	TL432BQDBZR
100	2	U15, U16	MGJ2D122005SC MGJ2_murata	DC-DC converter	MURATA	MGJ2D122005SC
101	1	U28	LEM CASR 15-NP LEM_CASR_15_NP 15 A	CASR 15-NP	LEM	CASR 15-NP
102	2	X1, X3	SCTW35N65G2V to247ae	Silicon carbide power MOSFET	ST	SCTW35N65G2V
103	2	X2, X4	TN3050H-12WY to247ae	Automotive grade AEC-Q101 SCR Thyristor	ST	TN3050H-12WY

Appendix A Inrush current limitation

The IEC 61000-3-3 standard gives the limitation of voltage changes and fluctuations for equipment with rated RMS current lower than 16 A connected to a low voltage grid. Voltage fluctuations are caused by the equipment in case a too high current is sunk from the grid. Then, a voltage drop occurs due to the line impedance.

As the mains voltage fluctuation might cause undesired brightness variation of lamps and displays (flicker phenomenon), the inrush current sunk by the equipment has to be kept lower than specific limits.

The following equation explains the link between the line current variation ΔI_{Input} (due to the equipment operation) and the relative mains voltage variation (ΔU) which has to be lower than the maximum allowed value (d_{max} given in %):

$$\Delta U = \Delta_{Input} \times Z_{ref} / U \times 100 < d_{\max} \quad (92)$$

where Z_{ref} is the normalized line impedance (0.6 W with 796 µH in series for a single-phase grid) and U is the nominal RMS line voltage.

The d_{max} level must not exceed 4%. A 6% or 7% limit is also allowed according to the way the equipment is switched (manually or automatically, delayed or not, etc.) or for specific appliances.

If the ΔU variation exceeds 3.3% during a single voltage change, this should not last more than 500 ms.

The table below details the associated maximum input current variation related to the different d_{max} levels. An appliance complies with the IEC 61000-3-3 limit at start-up if its RMS current remains below 16.1 A. The relative variation is then lower than 3.3% and so the compliance is ensured even if the start-up lasts more than 500 ms.

Table 22. Maximum input RMS current variation for 230 V single-phase grid according to IEC 61000-3-3

d_{max} (%)	ΔU (V)	ΔI_{Input} (A)
3.3	7.6	16.1
4	9.2	19.5
6	13.8	29.3
7	16.1	34.1

Appendix B Mains voltage dips and interruptions

IEC 61000-4-11 standard defines the test conditions to evaluate the immunity of equipment to a voltage dip or interrupt. This electromagnetic standard is given as a testing method reference by other standards. For example, product standards (like EN55014-2 for appliances or EN 55024 for IT equipment) which have to be fulfilled by products to be sold on the European open market, list tests to be performed according to IEC 61000-4-11 standard and the associated expected tests results.

If a product is not listed in a specific product standard, the general electromagnetic standard applies according to the environment of use (residential or industrial environment, for example).

As any appliance connected to the mains can be subject to line voltage dips or interruptions, a high input current may occur when the line voltage suddenly increases to its nominal value in rectifier circuits charging DC capacitors. This high current may damage the front-end circuit components (like the bridge diodes, the AC fuse, etc.).

The table below lists the different requirements for line voltage dips and interruptions according to different electromagnetic immunity standards. The worst cases to take into account are:

- voltage dips: 1 cycle with a 0% residual voltage and 50 cycles with a 70% residual voltage
- voltage interruptions: 0% residual voltage for 250 or 300 cycles for 50 and 60 Hz line frequency, respectively

Criterion B is requested for the 0% voltage test for one cycle, while the other tests require criterion C only.

Table 23. Required dip and interruption tests and STEVAL-DPSTPFC1 performance

Standard	Application	Test type	% residual voltage	Number of cycles	Required criterion by standard	STEVAL-DPSTPFC1 result
IEC 61000-6-1	Residential, commercial and light industrial environments	Dips	0	0.5	B	A
		Interruptions	0	1	B	A
			70	25[1]/30[2]	C	A
			0	250[1]/300[2]	C	A
IEC 61000-2-1	Industrial environments	Dips	0	1	B	A
			40	10[1]/12[2]	C	B
			70	25[1]/30[2]	C	A
		Interruptions	0	250[1]/300[2]	C	B
EN55024	Information technology equipment	Dips	<5	0.25	B	A
			70	25	C	A
		Interruptions	<5	250	C	B
EN55014-2	Appliances, electric tools, etc.	Dips	0	0.5	C	A
			40	10	C	B
			70	50	C	A

Revision history

Table 24. Document revision history

Date	Version	Changes
15-Jan-2021	1	Initial release.
22-Jun-2022	2	Updated introduction, Section 1.4 Totem pole PFC specifications, and Section 12.1 Efficiency and THD.
08-Nov-2022	3	Updated Section 1.4 Totem pole PFC specifications and Section 12.1 Efficiency and THD.

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