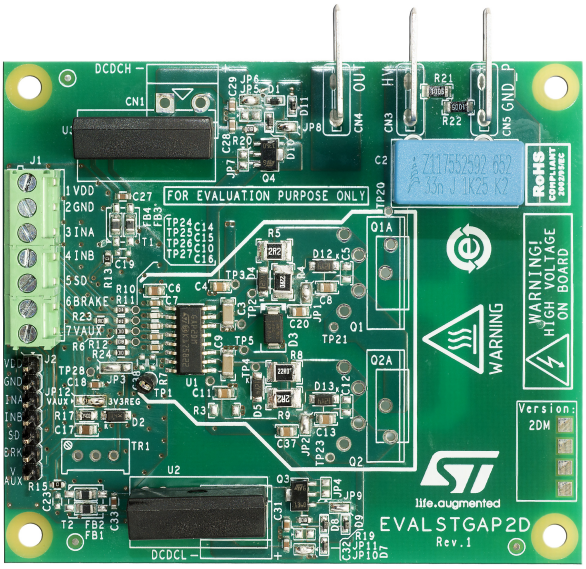
EVALSTGAP2DM: isolated 4 A single gate driver demonstration board

Introduction

The EVALSTGAP2DM board allows evaluating all the STGAP2DM features while driving a half-bridge power stage with voltage rating up to 1700 V in TO-220 or TO-247 package.

The board allows easily selecting and modifying the values of relevant external components in order to facilitate driver performance evaluation under different applicative conditions and fine pre-tuning of final application's components.

Figure 1. EVALSTGAP2DM demonstration board



1 Board description and configuration

The board allows tuning several design parameters, giving the possibility to evaluate and optimize the performance and switching characteristics of the power stage.

The user can select and mount the power switch of choice either in TO-220 or TO-247 package; the board also allows installing an optional heatsink.

The demonstration board can be populated with isolated DC-DC converters in the standard SIP7 package to supply the gate driving section, which significantly reduce the effort to supply the system and allows fast and easy evaluation of the gate driving performances.

With reference to the STGAP2DM datasheet, the high-side section is driven by the device's Channel A, while the low-side section by the device's Channel B.

Figure 2 shows the position of the main components and connectors on the board.

Figure 2. EVALSTGAP2DM – Main components and connectors position

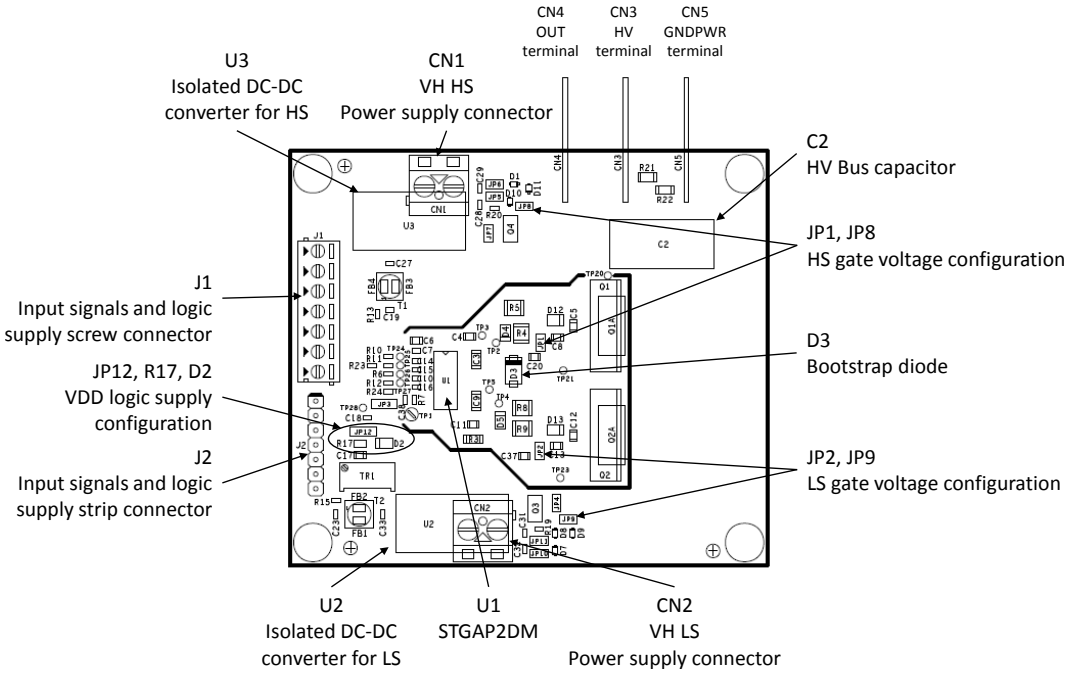


Table 1. Board connectors

Name	Pin	Label	Description
CN1	1 - 2	DCDCL	High-side VH supply voltage
CN2	1 - 2	DCDCH	Low-side VH supply voltage
J1 J2	1	VDD	Logic supply voltage
	2	GND	Logic ground
	3	INA	High-side driver logic input, active high
	4	INB	Low-side driver logic input, active high
	5	SD	Shutdown input, active low
	6	BRAKE	Brake input, active low
	7	VAUX	Auxiliary power supply
CN3	1 - 2	HV	High voltage power supply

Name	Pin	Label	Description
CN4	1 - 2	OUT	Power stage output
CN5	1 - 2	GNDPWR	Power ground

Table 2. Board jumpers setting

Jumper	Permitted configurations	Default condition
JP1	HS gate voltage configuration: selection of negative voltage (refer toTable 5)	Closed
JP2	LS gate voltage configuration: selection of negative voltage (refer to Table 5)	Closed
JP3	Must be left as is for default configuration, VDD2 connected to VDD	Closed
JP4	LS gate voltage configuration: direct connection of DCDCL+ to VH_B net	Open
JP5	HS gate voltage configuration: connection of DCDCH 0V output reference to OUT net	Open
JP6	HS gate voltage configuration: connection of DCDCH- to GNDISO_A net	Closed
JP7	HS gate voltage configuration: direct connection of DCDCH+ to VH_A net	Open
JP8	HS gate voltage configuration: selection of positive voltage (refer to Table 5)	Closed
JP9	LS gate voltage configuration: selection of positive voltage (refer to Table 5)	Closed
JP10	LS gate voltage configuration: connection of DCDCL- to GNDISO_B net	Closed
JP11	LS gate voltage configuration: connection of DCDCL 0V output reference to GNDPWR net	Open
JP12	VDD logic supply configuration (refer to Table 3)	Closed 2-3

1.1 Logic supply voltage (VDD)

It is possible to provide the gate driver with logic supply VDD in three alternative ways to match driver input threshold with the controlling signals' voltage swing:

- Using the on-board 3.3 V Zener D2 regulator to supply VDD. The Zener is supplied from DC-DC input voltage VAUX. So only the 5 V VAUX DC-DC supply input is powered to supply the whole system (default configuration).
- Supplying externally VDD net from J1 or J2 (pin 1) with a voltage between 3 V and 5.5 V.
- Supplying externally VDD and VAUX together (VDD max. 5.5 V).

In case the default option is not used, it is required to modify JP12 according to Table 3 and R17 according to Table 4 also to avoid damage to regulator components.

Table 3. Logic supply voltage selection (VDD)

VDD	JP12	Note
3.3 V, on-board (default)	2-3 closed	VDD generated from VAUX with Zener diode D2
3.3 V, external	Open	VDD directly supplied from J1 or J2 (pin 1)
VDD = VAUX, external	1-2 closed	VDD and VAUX (DC-DC supply) tied together by JP12

The R17 resistor value has been selected for using 5 V input DC-DC module. If a different VAUX input voltage is used, follow Table 4 to modify resistor R17 (which biases Zener D2) to avoid resistor overheating.

Table 4. **R17 value selection with a 3.3 V Zener diode D2 regulator**

DC-DC module supply input voltage VAUX	R17	JP12
3.3 V	Do not care	1-2 closed
5 V (default)	240 Ω	2-3 closed or JP12 open
12 V	1200 Ω	2-3 closed or JP12 open
15 V	1500 Ω	2-3 closed or JP12 open
24 V	2700 Ω	2-3 closed or JP12 open

1.2 Gate driver supply voltage (VH)

It is possible to provide the gate driver supply voltage VH in several alternative ways:

- Using isolated DC-DC converters in the standard SIP7 package (U2, U3)
- Using the bootstrap diode D3 by supplying the low-side driver via CN2 and mounting the resistor R3 (initial suggested value 10 Ω).
- Supplying directly CN1 and CN2 connectors (not mounted) with two separated isolated supplies.

The faster and safer way to supply the board is by using isolated DC-DC converters.

The bootstrap diode supplying method is much simpler and less expensive but does not allow evaluating negative gate driving voltage. The bootstrap diode is 1200 V rated; if a higher bus voltage is required the diode must be replaced accordingly.

Supplying externally via CN1 and CN2 is, in general, not recommended, unless using supplies specifically designed for this purpose (with high voltage isolation) or batteries.

Supplies provided from the optional DC-DC or from CN1 and CN2 connectors are post regulated in order to allow an easy modification of the gate driving voltages. Some predefined supply voltages can be selected through solder jumpers; further tuning can be made by changing the value of the relevant Zener diodes.

Table 5. **Gate driving voltage configuration (positive/negative)**

Gate driving voltage	JP1, JP2	JP8, JP9	Most suited for:
+15 V / 0 V (default)	Closed	Closed	MOSFET/ IGBT
+15 V / -2.7 V	Open	Closed	MOSFET/ IGBT
+19 V / 0 V	Closed	Open	SiC
+19 V / -2.7 V	Open	Open	SiC

The board has been designed for indifferently using 5 V input and 24 V single output or “12 + 12 V” dual output DC-DCs.

Other output voltage DC-DCs can be used by modifying the post regulation network.

Other input voltage DC-DCs can be used by modifying R17 (see Section 1.1)

DC-DC input voltage is connected to VAUX signal, available on J1 and J2.

DC-DCs with SIP7 footprint are available mostly with 1 W and 2 W output rated power. For most applications, 1 W power modules are enough.

Especially for high dV/dt applications, low input to output isolation capacitance (referred to as input to output coupling capacitance) regulators are recommended.

During applicative output transients (dV/dt), the potential noise generated by the isolation capacitance could make user measurements difficult and noisy. To simplify user' measurement tasks, DC-DC input supply is filtered with FB1, FB2, FB3 and FB4 ferrite beads. In the final application, beads are usually removed for cost reasons. On the other hand, if the user wants a more improved filter, it is suggested to replace the beads with a common mode filter (T1 and T2) like, for example, TDK ACM4520-142.

1.3 Drivers logic input signals

Drivers logic input signals can be applied through the dedicated pins of J1 or J2 connector (refer to Table 1 for details).

1.4 Drivers gate resistors

The gate resistors are chosen based on the selected power switch and application topology.

The power transistor's gate is charged through resistors R4 and R8, while the discharge phase is done through two resistors in parallel: R4//R5 and R8//R9 (considering negligible the diode static resistance).

1.5 Power stage decoupling

As for all switching applications, high voltage supply is properly decoupled and an appropriate decoupling capacitor is connected to the board to reduce bus ringing and power switch overvoltage spikes during operation.

The board is equipped with a small 1.25 kV DC rated film capacitor (C2) in a convenient position to operate more safely the power switches. Depending on the application, bus decoupling can be modified also by using the provided footprint and holes for bus capacitors C1, C2, C34, C35, C36.

Danger:

DANGER OF DEATH!

High voltage present on the board! Before operating the board, ensure that all capacitors are discharged.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
13-Aug-2021	1	Initial release.

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