How to integrate and configure the VD55G0 device from a hardware and software perspective

Introduction

This document is the user manual for the VD55G0 0.4 megapixel global shutter image sensor. It should be read with the VD55G0 datasheet. The aim of this document is to provide further technical details about the VD55G0 and guidance on how to configure it for different applications.

It is intended that this document primarily covers items not described in the datasheet. Therefore, to avoid repetition, references are made to the datasheet.

1 Acronyms and abbreviations

Table 1. Acronyms and abbreviations

Acronym/abbreviation	Definition
AE	auto exposure
AEC	automatic exposure control
CC	central correction
CSI	camera serial interface
DDC	digital gain and dark calibration
ECC	error correcting code
EV	exposure value
FW	firmware
FWP	firmware patch
FSM	firmware state machine
GPH	group parameter hold
ISL	intelligent status line
ISP	image signal processor
LSB	least significant byte
MCU	microcontroller unit
MSB	most significant byte
NVM	nonvolatile memory
PCB	printed circuit board
PLL	phase-locked loop
PWM	pulse-width modulation
RC	ring correction
RD	read
ROI	region of interest
SCL	serial clock line
SDA	serial data line
UI	user interface
ULPM	Ultralow power mode
VT	video timing
VTRAM	video timing memory

2 Application schematic

Information on the application schematic and the layout recommendations are provided in the product datasheet. This section explains the integration of the image sensor into a system from a hardware perspective.

2.1 Power supplies

To power on the device, all the external supplies (VCORE, VDDIO, and VANA) must be properly provided according to the device characteristics described in the electrical characteristics section of the datasheet. Each supply should be in the operating range for a standard application configuration, and compatible with the device power consumption (average and peak current).

Table 2. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDIO	Digital IO power supply	1.7	1.8	1.9	V
VANA	Analog power supply	2.65	2.8	2.95	
VCORE	Digital core power supply	1.08	1.15	1.26	
VIO	IO referenced to VDDIO	-0.3	—	VDDIO + 0.3	
Temperature					
T JF	Junction temperature (functional operation)	-30	—	85	°C
T STO	Storage temperature	-40	—	125	°C

2.2 Hardware reset (XSHUTDOWN)

Reset of the device is managed by the XSHUTDOWN pin.

- At low level, the device is in power down state
- At high level, the device is active if all the power supplies are present

See the device datasheet for the electrical specifications of the XSHUTDOWN pin.

2.3 Input clock

To operate correctly, the device needs to be provided with an input clock. Refer to the electrical characteristic section of the datasheet for the constraints of the input clock.

2.4 I²C interface

2.4.1 CCI protocol

The device is controlled via an I²C interface as defined by the MIPI CSI-2 specification (refer to *MIPI Alliance standard for camera serial interface 2)*. The device uses CCI protocol over I²C. Details of this interface can be found in the device datasheet.

The value of the pull-up resistors, on the SDA and SCL signals, must be chosen to ensure that the I²C bus constraints are met in fast mode+. If the device has to be used in fast mode, the correct pull-up resistors must be selected to support fast mode and fast mode+. The default configuration of the device is fast mode+. The switch to fast mode is only available in SW_STANDBY state.

2.4.2 Data aligned within registers

Registers larger than 8 bits wide are stored LSB (least significant byte) first, i.e. the LSB is placed in the location with the lowest index (little endian).

Note: This ordering of multibyte registers is contrary to the recommended byte ordering detailed in the MIPI CSI-2 specification which states that multibyte registers should be stored MSB (most significant byte) first.

2.5 MIPI CSI-2 transmitter interface

The device outputs a frame through a MIPI CSI-2 with the following characteristic:

- Data and clock polarity can be inverted

This configuration is detailed in Section 16: Output interface.

2.6 GPIO interfaces

The VD55G0 has four GPIOs which synchronize signals or act as in/out general purpose pins.

3 Control interface

3.1 Register default values

The register default values depend on the device state. The default values after device reset may differ from the register default values observed once the firmware is in SW_STANDBY state.

Without specific notice, the default values listed in this document are default values observed in the device SW_STANDBY state after the BOOT command is complete.

3.2 Register groups

The registers are grouped together based on their functional purpose.

Table 3. Register group descriptions

Group	Base address	Access	Description
STATUS	0x0000	RO	Device status
COMMAND	0x0200	R/W	Commands to control the device
SENSOR SETTINGS	0x0220	R/W	General settings of the device
STATIC	0x0300	R/W	Static configuration for streaming
DYNAMIC	0x0400	R/W	Dynamic configuration for streaming
CONTEXT 0	0x044C	R/W	Used to control the dynamic settings of the sensor. The sensor can be configured to automatically switch between these settings from frame to frame.
CONTEXT 1	0x047C	R/W	
CONTEXT 2	0x04AC	R/W	
CONTEXT 3	0x04DC	R/W	
NVM MIRROR	0x0640	R/W	Buffer for NVM operations
MISCELLANEOUS	0x0900	R/W	Additional configurations
FW PATCH	0x2000	R/W	Buffer to load a Firmware patch. Not accessible after boot

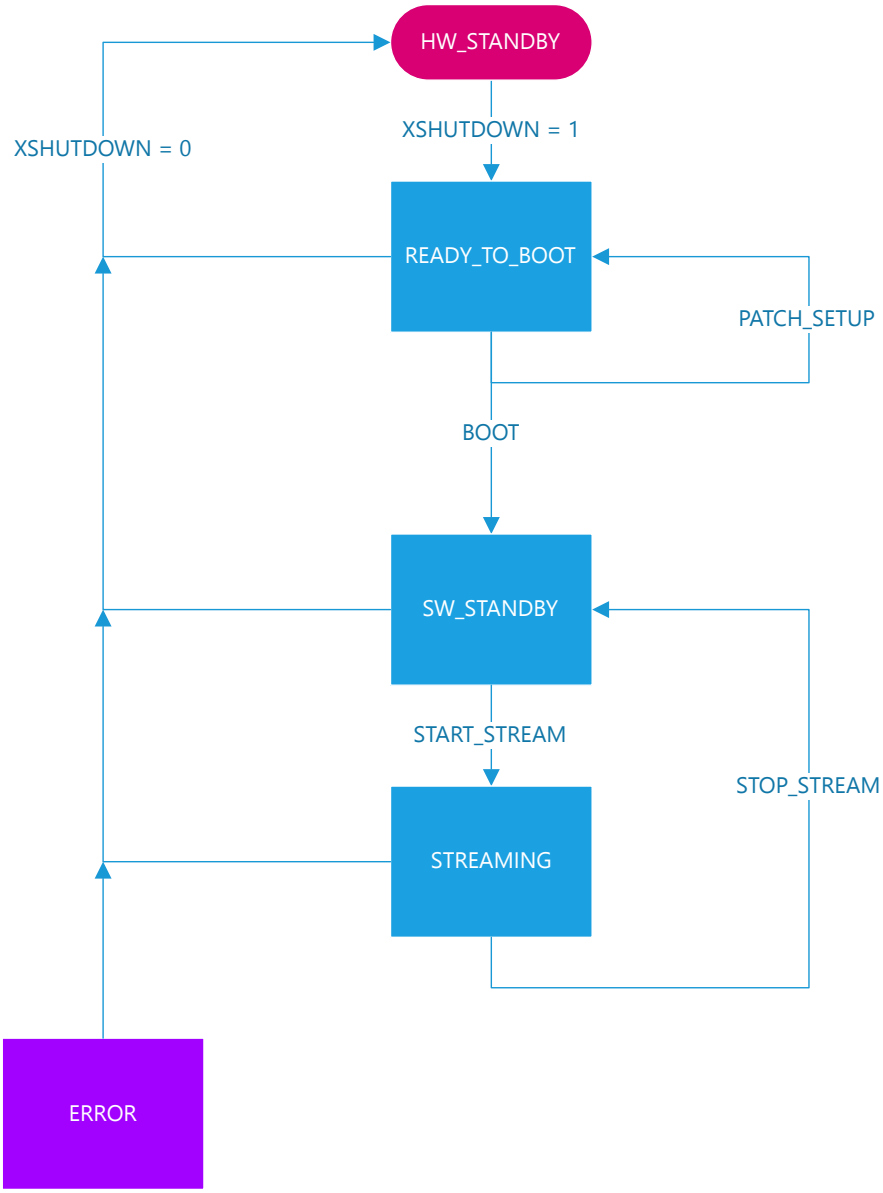
3.3 Register data types

Table 4. Data types description

Data type	Name	Description
UI	Unsigned integer	
SI	Signed integer	Two’s complement notation
C	Coded	This indicates that the value is coded to select one of several functions or modes
FP X.Y	Unsigned fixed point (FP)	Real value stored as unsigned, only for strictly positive value X.Y refers to the number of digits to store respectively the integer and decimal parts 3.75 <=> 0x03C0 in FP 8.8
SFP X.Y	Signed fixed point (SFP)	Real value stored as signed X.Y refers to the number of digits to store respectively the integer and decimal parts -3.75 <=> 0xFC40 in SFP 8.8
B	Bits	Each bit represents a specific function or mode (0 = disable, 1 = enable)

4 Firmware state machine

Figure 1. **Firmware state machine**



The SYSTEM_ FSM register in the STATUS group indicates the state of the device.

5 Steps from device power-up to sensor STREAMING state

This section describes the steps to be followed from device power-up to sensor STREAMING state. A power-up sequence diagram is provided in the product datasheet.

5.1 Device power-up sequence

To power on the device, all the external supplies (VCORE, VDDIO, VANA) must be properly provided according to the device characteristics described in the electrical characteristics section of the datasheet. XSHUTDOWN must stay low and the device should be in HW_STANDBY state.

5.2 Transition to READY_TO_BOOT

The CLKIN signal must be provided before the XSHUTDOWN pin can be set high. See the product datasheet for device signal specifications. The time between the release of the XSHUTDOWN pin and READY-TO-BOOT state depends on the external clock frequency due to firmware activity. The I²C interface is not operational before reaching the READY-TO-BOOT state.

5.3 READY_TO_BOOT

Once the device is in the READY-TO-BOOT state, the host can:

- Upload a firmware patch. The firmware patch upload procedure is described in Section 10: Firmware patch

Once these operations are complete, the host must issue a BOOT command to go to SW_STANDBY state.

5.4 SW_STANDBY

From the SW_STANDBY state, the host can perform the following actions:

- Configure the I2C interface regarding the device address and I2C protocol to be used for read and write operations.
- Perform all static, dynamic, and context configurations such as synchronization, ISP, output image, exposure, gain, and context chain.
- Perform a thermal sensor read (see Section 17: Temperature)
- Read/write into the NVM memory (see Section 12: NVM).

Once these operations have been completed, the host must issue a START_STREAMING command to go to STREAMING state.

5.5 STREAMING

In this state, the sensor streams frames according to the host configuration previously set in SW_STANDBY state.

Alternatively, from STREAMING state, the host can perform the following actions:

- Perform all “dynamic” configurations regarding image streaming through the DYNAMIC or CONTEXT register groups.
- Stop streaming by issuing a STOP_STREAM command. This makes the sensor go back to SW_STANDBY state.

6 Steps to power down device from sensor STREAMING state

This section describes the steps to be followed to power down the device starting from Sensor STREAMING state. A power down flow chart is available in the product datasheet. The power down steps are summarized as follows:

1. The host issues a STOP_STREAM command. This stops the current streaming and the device goes back to SW_STANDBY state.
2. In SW_STANDBY state, the external clock signal, CLKIN, must be disabled and the XSHUTDOWN pin must be set to low. This sets the device to HW_STANDBY state.
3. Finally, the power supplies (VCORE, VDDIO, and VANA) should be driven down which turns the device off.

See the product datasheet for device signal specifications.

7 I²C interface configuration

The I²C default configuration is fast mode+ (which is compatible with fast mode).

The I²C control interface supports different IDs for read and write operations. By default, these addresses are either loaded from the NVM memory content, or written to a default value by the firmware if the NVM is empty. Note that the NVM memory content is configured during device manufacturing test operations.

Without specific access, the I²C address does not change during device operations.

Once the device is in SW_STANDBY state, the I²C address can be updated by the host controller. The update sequence is as follows:

1. Ensure that the device is in SW_STANDBY state
2. The host writes the new configuration into the DEVICE_ID bit fields of the DEVICE_I2C_CTRL register.
3. The host issues an I2C_ADDR_UPDATE command

The new address is effective for the next I²C access until reset or power down.

Table 5. I²C interface configuration

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
DEVICE_I2C_CTRL	DEVICE_ID	7:1	UI	—
	MODE	8	C	0x0: FAST_MODE 0x1: FAST_MODE_PLUS

8 Commands

The host sends commands through the UI by writing into different registers (see table below). In Table 6. COMMAND registers, an interrupt is raised to inform the firmware that a command has been issued, then the command is processed in the FSM. Once a command has been executed, the same register is cleared to indicate that the command has been acknowledged. The host must wait for this command to be acknowledged to continue its sequence.

Table 6. COMMAND registers

COMMAND register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
BOOT	COMMAND	1:0	C	0x1: BOOT 0x2: PATCH_SETUP
SW_STANDBY	COMMAND	3:0	C	0x1: START_STREAM 0x2: NVM_READ 0x3: NVM_PROG 0x4: THSENS_READ 0x5: I2C_ADDR_UPDATE
STREAMING	COMMAND	3:0	C	0x1: STOP_STREAM 0x2: VT_FSYNC_IN_I2C

9 Error code

If a command cannot be achieved or an error occurs during STREAMING state, the device goes into ERROR state. In this case, streaming is stopped and the ERROR_CODE register is different from 0x0000. The device must be reset.

Table 7. Error codes

Error code	Error
FW PATCH ERRORS	
0x400	CODE_TOO_LARGE
0x401	TOO_MANY_PATCHES
0x402	TOO_MANY_HOOKS
0x403	BAD_CRC
EXCEPTIONS ERRORS	
0x500	PROTECT
0x501	OPCODE
0x502	GPRSIZE
0x503	PMISALIGN
0x504	POUTOFMEM
0x505	PEXECUTE
0x506	DMISALIGN
0x507	DOUTOFMEM
0x508	DREAD
0x509	DWRITE
0x50A	PSYSERR
0x50B	OVERFLOW
0x50C	UNKNOWN
VTIMING ERRORS	
0xa00	LONG_COARSE_MAX_ERROR
0xa01	LONG_COARSE_MIN_ERROR
0xa02	BAD_FRAME_LENGTH_ERROR
0xa03	ISB_LONG_PIPE_OVERFLOW
0xa04	Y_SIZE_SS_ERROR
0xa05	X_SIZE_SS_ERROR
0xa06	BGISON_LOW
0xa07	BGISON_HIGH
0xa08	TOKEN_NOT_FOUND_ERROR
ISP ERRORS	
0xb00	SDR_FIFO_FULL_ERROR
0xb01	OF_FIFO_FULL_ERROR
0xb02	ISLGEN_INVALID_CFG_ERROR
0xb03	ISLGEN_MEMORY_LOCKED_ERROR
0xb04	ISLGEN_MISSED_TRIGGER_ERROR

Error code	Error
0xb05	ISLGEN_TOO_MANY_ENTRIES_ERROR
0xb06	MULTICROP_NO_ROI_ERROR
0xb07	ISB2IDP_LINEBLANKING_ERROR
OIF ERRORS	
0xc00	CSI_LANE_DESYNC_ERROR
0xc01	CSI_PKT_TOO_LONG_ERROR
0xc02	CSI_PKT_TOO_SHORT_ERROR
0xc03	CSI_UNDERFLOW_ERROR
0xc04	MERGER_EXT_SYNC_MISSED_ERROR

10 Firmware patch

A firmware patch must be loaded in the sensor during READY_TO_BOOT state according to the following procedure:

1. Load the binary patch at address 0x2000.
2. Issue the PATCH_SETUP command to activate the code of the patch.
3. The firmware patch version immediately becomes available in the FWPATCH_REVISION register.

The patch number is available in the STATUS register FWPATCH_REVISION.

Table 8. Firmware patch revision register

STATUS register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
FWPATCH_REVISION	MINOR_REVISION	7:0	UI	—
	MAJOR_REVISION	15:8	UI	—

11 VT patch

The VT (video timing) patch must be loaded in the sensor during the SW_STANDBY state according to the following procedure:

1. Issue the START_VTRAM_UPDATE command.
2. Load the VT patch.
3. Issue the END_VTRAM_UPDATE command to activate the code of the VT patch.
4. The VT patch ID immediately becomes available in the VTPATCH_ID register.

STATUS register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
VTPATCH_ID	VALUE	63:0	UI	—

12 NVM

Several 32-bit words are available in the NVM for customer use. Below is the procedure to program one or more consecutive words. The sensor must be in SW_STANDBY.

1. Write the words in the NVM MIRROR register group (see Section 19.7: NVM MIRROR registers).
2. Set the NVM_START_ADDRESS (refer to the NVM operation address in the table below) and NVM_NB_OF_WORD.
3. Issue the NVM_PROG command (see Section 19.2: COMMAND registers).

An NVM_READ command can be executed to reload values from the NVM in the NVM MIRROR registers. This command also uses the values set in the NVM_START_ADDRESS and NVM_NB_OF_WORD.

The content of the NVM is automatically loaded at boot in the NVM mirror registers (see Section 19.7: NVM MIRROR registers).

The NVM customer area has a specific word: I2C_ADDRESS. This word controls the default I²C address at powerup. This feature is doubly protected as follows:

1. I²C address must be replicated in byte 0, byte 1 and byte 2
2. Security key 0xAA is set in byte 3 (MSB)

If the conditions are wrong, the I²C address is not updated.

Table 9. NVM MIRROR registers

NVM MIRROR register group					
Register name	**NVM operation address**	**Field name**	**Bits**	**Data type**	**Values**
RESERVED 0	0x000	VALUE	31:0	UI	First reserved word
LAST RESERVED	0x0074	VALUE	31:0	UI	Last reserved word
CUSTOMER_WORD_0	0x0078	VALUE	31:0	UI	First word available for customer
CUSTOMER_WORD_1	0x007C	VALUE	31:0	UI	—
CUSTOMER_WORD_2	0x0080	VALUE	31:0	UI	—
CUSTOMER_WORD_3	0x0084	VALUE	31:0	UI	—
CUSTOMER_WORD_4	0x0088	VALUE	31:0	UI	—
CUSTOMER_WORD_5	0x008C	VALUE	31:0	UI	—
CUSTOMER_WORD_6	0x0090	VALUE	31:0	UI	—
CUSTOMER_WORD_7	0x0094	VALUE	31:0	UI	—
CUSTOMER_WORD_8	0x0098	VALUE	31:0	UI	—
CUSTOMER_WORD_9	0x009C	VALUE	31:0	UI	—
CUSTOMER_WORD_10	0x00A0	VALUE	31:0	UI	—
CUSTOMER_WORD_11	0x00A4	VALUE	31:0	UI	—
CUSTOMER_WORD_12	0x00A8	VALUE	31:0	UI	—
CUSTOMER_WORD_13	0x00AC	VALUE	31:0	UI	—
CUSTOMER_WORD_14	0x00B0	VALUE	31:0	UI	—
CUSTOMER_WORD_15	0x00B4	VALUE	31:0	UI	—
CUSTOMER_WORD_16	0x00B8	VALUE	31:0	UI	—
CUSTOMER_WORD_17	0x00BC	VALUE	31:0	UI	—
CUSTOMER_WORD_18	0x00C0	VALUE	31:0	UI	—
CUSTOMER_WORD_19	0x00C4	VALUE	31:0	UI	—
CUSTOMER_WORD_20	0x00C8	VALUE	31:0	UI	—
I2C_ADDRESS	0x00CC	I2C_KEY	31:24	UI	Security key

NVM MIRROR register group					
Register name	NVM operation address	Field name	Bits	Data type	Values
I2C_ADDRESS	0x00CC	I2C_DEVICEID_2	22:16	UI	I²C address Device I²C address
		I2C_DEVICEID_1	14:8		
		I2C_DEVICEID_0	6:0		
CUSTOMER_WORD_21	0x00D0	VALUE	31:0	UI	—
CUSTOMER_WORD_22	0x00D4	VALUE	31:0	UI	—
CUSTOMER_WORD_23	0x00D8	VALUE	31:0	UI	—
CUSTOMER_WORD_24	0x00DC	VALUE	31:0	UI	—
CUSTOMER_WORD_25	0x00E0	VALUE	31:0	UI	—
CUSTOMER_WORD_26	0x00E4	VALUE	31:0	UI	—
CUSTOMER_WORD_27	0x00E8	VALUE	31:0	UI	—
CUSTOMER_WORD_28	0x00EC	VALUE	31:0	UI	—
CUSTOMER_WORD_29	0x00F0	VALUE	31:0	UI	—
CUSTOMER_WORD_30	0x00F4	VALUE	31:0	UI	—
CUSTOMER_WORD_31	0x00F8	VALUE	31:0	UI	Last word available for customer

The NVM STATUS register can be read to check if the write operation went well (refer to table below). Each NVM word is individually protected by the ECC. Therefore, only a single write operation is allowed for each NVM word.

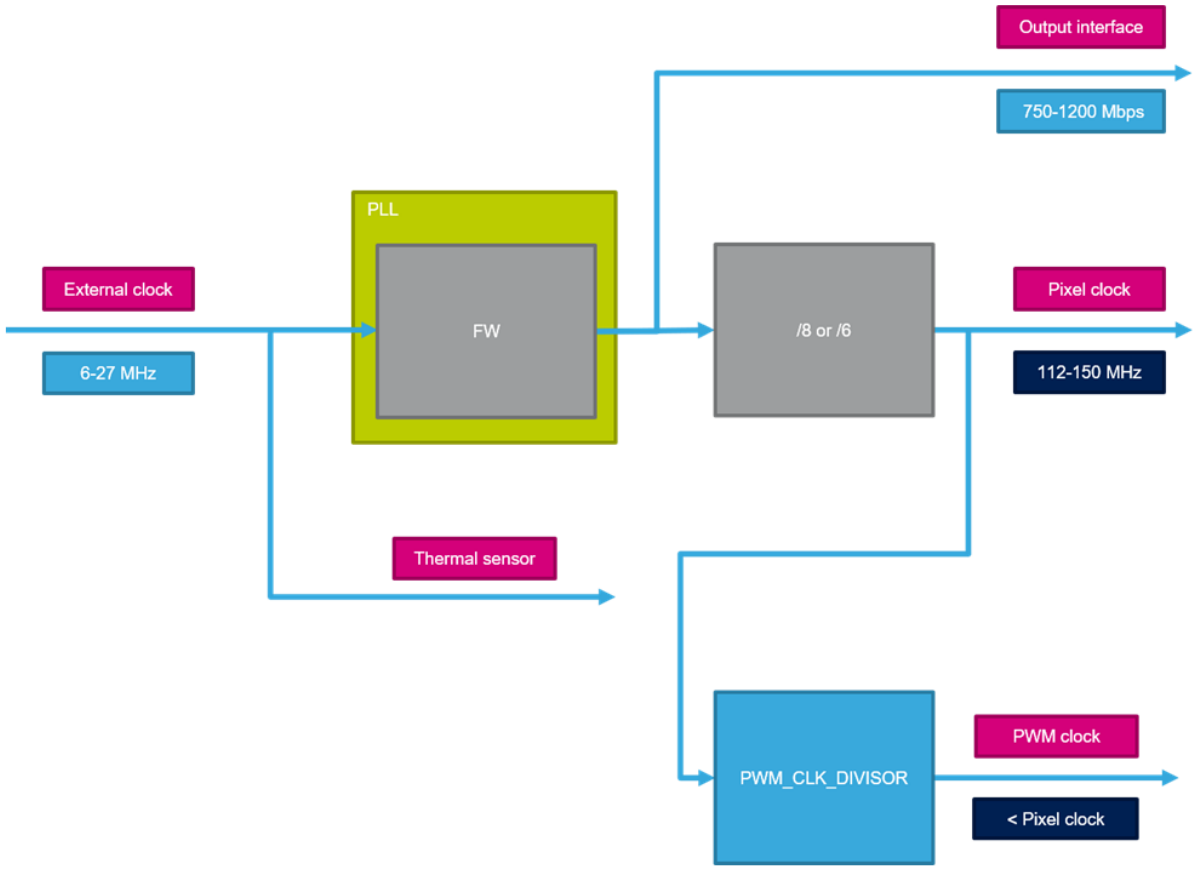
Table 10. NVM STATUS registers

STATUS register group				
Register name	Field name	Bits	Data type	Values
NVM	PROG_OK	0	B	0: False 1: True
	PROG_FAIL	1	B	0: False 1: True
	READ_OK	2	B	0: False 1: True
	READ_FAIL	3	B	0: False 1: True
	ECC_ERROR	5	B	0: NO_ERROR 1: ECC_ERROR
	DRIVER_FSM	7:6	C	0x0: IDLE 0x1: PROG_OP 0x2: READ_OP 0x3: ERROR

13 Timings

13.1 Clock tree

Figure 2. **Clock tree**



13.2 External clock source frequency configuration

The device supports a range of external clock source frequencies. Refer to the product datasheet for information on the range of clock sources supported.

Once the device is in SW_STANDBY state, the external clock frequency configuration can be updated by the host controller.

The new frequency configuration is used for internal PLL configurations. It is effective once the device is in STREAMING state, until the device reboots (power down or power up).

13.3 Pixel clock

The device has been designed to run with a pixel clock at 150 MHz. The register in the table below (from the STATIC register group) is used.

Table 11. Clock tree configuration registers

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
EXT_CLOCK	VALUE	31:0	UI	6–27 MHz

The pixel clock is available in the Section 19.1: STATUS registers (see PIXEL_CLK, register address 0x0040).

13.4 Line time

Line time is controlled by the LINE_LENGTH register (STATIC register group)

Table 12. Line length register

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
LINE_LENGTH	VALUE	15:0	UI	Length of line (in pixels)

Line time is computed using the following equation:

$$Line\ time = \frac{LINE\_LENGTH}{pixel\ clock}$$

The following table provides the minimum LINE_LENGTH according to ADC mode (see Table 16. Video timing control register).

Table 13. Minimum line length

ADC mode	Line length	Line time
10 bits	Clock > 900 MHz	1128
	Clock ≤ 900 MHz	1200
9 bits	Clock > 900 MHz	1024
	Clock ≤ 900 MHz	1200

Note: It is recommended to set the line length at the minimum value. Higher line lengths may decrease performance.

13.5 Frame rate

Frame rate is controlled by the FRAME_LENGTH register (CONTEXT register group).

Table 14. Frame rate register

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
FRAME_LENGTH	VALUE	15:0	UI	Length of frame (in lines)

The frame rate is computed as follows:

$$Frame_{rate} = \frac{1}{line_{time} * FRAME\_LENGTH}$$

The minimum FRAME_LENGTH is computed from the resolution of the VT output. The VT output is controlled by the Y_START/Y_END registers (see Section 14.1.1: ROIs) and subsampling factor (see Section 14.1.2: Subsampling and digital binning). Only subsampling has an impact on the minimum frame length.

The minimum FRAME_LENGTH equation must be set as follows:

$$Minimum\ FRAME\_LENGTH > \frac{Y\_END - Y\_START + 1}{subsampling factor} + FRAME\_LENGTH\_OFFSET$$

The FRAME_LENGTH_OFFSET is computed from the current line length and the minimum line length (see Section 13.4: Line time). The FRAME_LENGTH_OFFSET decreases when the line length has been increased. The default value is 76.

$$FRAME\_LENGTH\_OFFSET = 31 + READ\_OFFSET + roundUp\left(20 \times \frac{minimum\ \ line\ \ length}{current\ \ line\ \ length}\right)$$

Part of the frame length offset is linked to the time required by the FW to compute the current frame settings: the read offset. This value is controlled by two READ_OFFSET registers (STATIC register group) according to ADC mode. These registers are: READ_OFFSET_9BITS and READ_OFFSET_10BITS (see table below).

Table 15. READ_OFFSET register

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
READ_OFFSET_10BITS	VALUE	15:0	UI	Time to process image settings during interframe
READ_OFFSET_9BITS	VALUE	15:0	UI	

The read offset is set according to the following equation:

$$Read\ \ offset = roundUp\left(25 \times \frac{minimum\ \ line\ \ length}{current\ \ line\ \ length}\right)$$

The default values of both registers are 18 (0x12).

13.6 Output interface clock

The device is the follower of the output interface. Line length should be adapted based on this clock speed (see Section 13.4: Line time for more details). If the requested BIT_RATE is not obtainable, the FW sets the closest, lowest, achievable frequency. The host can check the frequency in the STATUS registers once the device is in STREAMING state.

13.7 Video timing control

The VT_CTRL register controls the synchronization mode (leader mode or follower mode) and ADC mode (normal or fast readout).

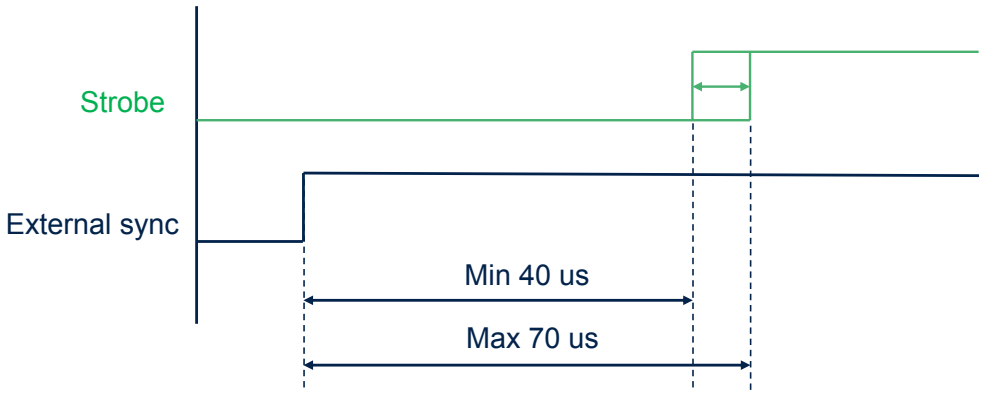
Table 16. Video timing control register

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
VT_CTRL	SYNC_MODE	1:0	C	0x0: MASTER 0x1: Follower mode on GPIO 0x2: Follower mode on I²C 0x3: Leader mode synchronization on GPIO (only for VDxxGxCCA)
	ADC_MODE	2	B	0: 10 bits (normal) 1: 9 bits (fast readout)
	RESERVED	7:3	—	0x0

The SYNC_MODE field controls synchronization mode, and sets the device either in leader mode or follower mode. There are two follower modes: External pulse or I²C command.

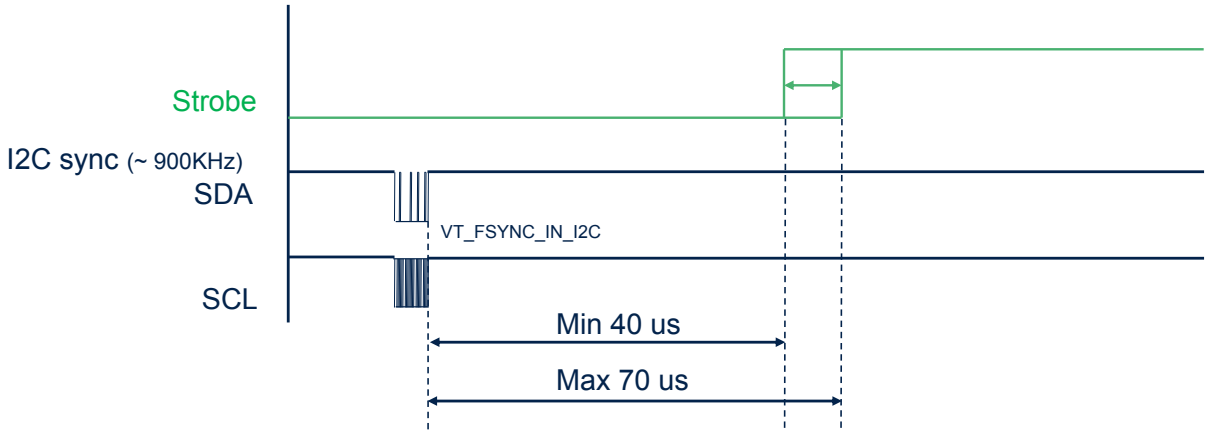
- MASTER
  - The device sends continuous frames
  - The FRAME_LENGTH register gives the frame rate
- EXTERNAL_SYNC (see Figure 3. EXTERNAL_SYNC timing)
  - The device starts to integrate a frame, then sends it each time the EXTERNAL_SYNC input pin is triggered.
  - Only GPIO_0 can be set as the EXTERNAL_SYNC pin
  - The maximum frame rate is defined by the FRAME_LENGTH register
- I2C_SYNC (see Figure 4. I2C_SYNC timing)
  - The device starts to integrate a frame, then sends it at each VT_FSYNC_IN_I2C command. Command is acknowledged once the frame is sent.
  - The maximum frame rate is defined by the FRAME_LENGTH register

Figure 3. EXTERNAL_SYNC timing



This delay varies from one frame to another

Figure 4. **I2C_SYNC timing**



This delay varies from one frame to another

The ADC_MODE field controls the ADC readout mode:

- 10 bits is the standard readout
- 9 bits is the fast readout

Because of a shorter line time, the 9-bit mode enables a higher frame rate. The drawback is lower image quality.

13.8 Video timing mode

Two different VT modes are available:

- Long Exposure mode (DEFAULT)
- Short Exposure mode

Short exposure mode allows a lower exposure time at the cost of a limited maximum exposure time. The exposure limits allowed for each VT mode are described in Table 19. Maximum exposure (in lines) and Table 21. Minimum exposure (in lines).

The following register must be written by the host in SW_STANDBY state to set the sensor in the required mode.

Table 17. USER_VT_VERSION register

Register name	Field name	Bits	Data type	values
USER_VT_VERSION	Value	7:0	B	0: Long exposure mode 1: Short exposure mode

Note: It is not possible to dynamically change VT mode. Once streaming has started, VT mode must be stopped if a change is required.

13.8.1 Exposure limits

Minimum and maximum exposure limits can be manually or automatically set according to the current use case.

To ensure the sensor is used in good conditions, a safety mechanism (involving exposure limits) is implemented.

By default, such exposure limits are automatically set based on Table 19. Maximum exposure (in lines) and Table 21. Minimum exposure (in lines).

To manually set the exposure limits, the following register is configured in SW_STANDBY state.

Table 18. MAX_EXPOSURE_LINES register

Register name	Field name	Bits	Data type	Values
MAX_EXPOSURE_LINES	Value	31:0	UI	—

The sensor sets the maximum exposure limit by computing the minimum value between the above control register and the theoretical value from Table 19. Maximum exposure (in lines). The maximum exposure possible is 32744 lines.

Table 19. Maximum exposure (in lines)

ADC 10 bits				ADC 9 bits			
VT long exposure mode		VT short exposure mode		VT long exposure mode		VT short exposure mode	
No low power	Full low power	No low power	Full low power	No low power	Full low power	No low power	Full low power
Frame_length - 64	Frame_length - 1507	Frame_length - VT Y size -62	Frame_length - 1507	Frame_length - 64	Frame_length - 1507	Frame_length - VT Y size - 64	Frame_length - 1507

For the minimum exposure limit, only one register (of two possible registers) is used based on ADC mode.

Table 20. MINIMUM_EXPOSURE registers

Register name	Field name	Bits	Data type	Values
MINIMUM_EXPOSURE_10BIT	Value	15:0	UI	—
MINIMUM_EXPOSURE_9BIT	Value	15:0	UI	—

The sensor sets the minimum exposure limit by computing the maximum value between these control registers and the theoretical value from Table 21. Minimum exposure (in lines).

Table 21. Minimum exposure (in lines)

ADC 10 bits				ADC 9 bits			
VT long exposure mode		VT short exposure mode		VT long exposure mode		VT short exposure mode	
No low power	Full low power	No low power	Full low power	No low power	Full low power	No low power	Full low power
19	19	9	9	21	21	10	10

In STREAMING state, two status registers are available to provide the current exposure limits.

Table 22. Exposure limit status registers

Register name	Field name	Bits	Data type	Values
MIN_EXPOSURE_IN_CURRENT_CONFIG	Value	15:0	UI	—
MAX_EXPOSURE_IN_CURRENT_CONFIG	Value	15:0	UI	—

Note: These limits remain identical whatever the exposure mode (Manual mode or Autoexposure mode).

13.9 Low power mode

A low power mode (called full low power mode) is available. It switches off the analog part of the sensor in interframe. This mode is only available if the blanking time is higher than 1500 lines (the default value). The following register must be configured in SW_STANDBY state.

Table 23. LOW_POWER_MODE register

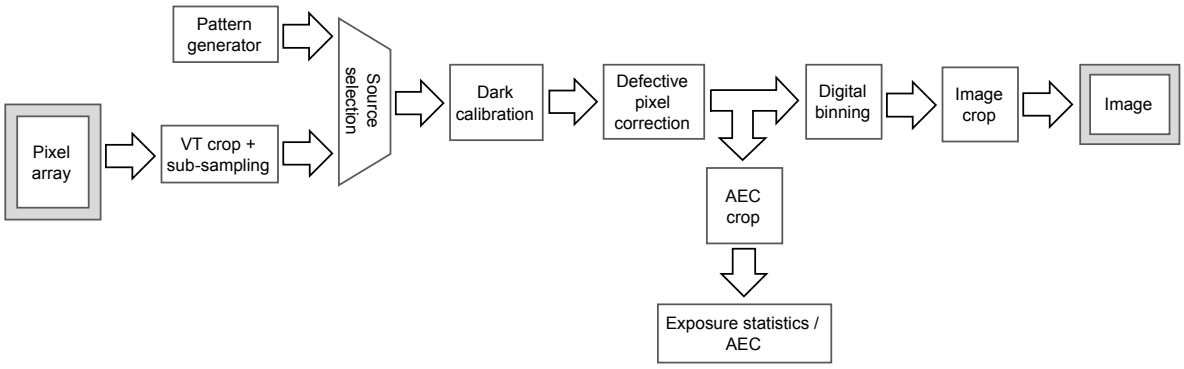
Register name	Field name	Bits	Data type	Values
LOW_POWER_MODE	Value	7:0	UI	0x0: Disable 0x5: Full low power mode

Full low power mode is on only if the blanking time is higher than a threshold of 1500 lines.

Note: When the full low power mode is enabled, the CONTEXT registers must be updated only in SW_STANDBY state.

14 Video pipe

Figure 5. **Video pipe**



14.1 Resolution and ROIs

The sensor has several features for configuring the resolution of the output image: crop, subsampling and digital binning.

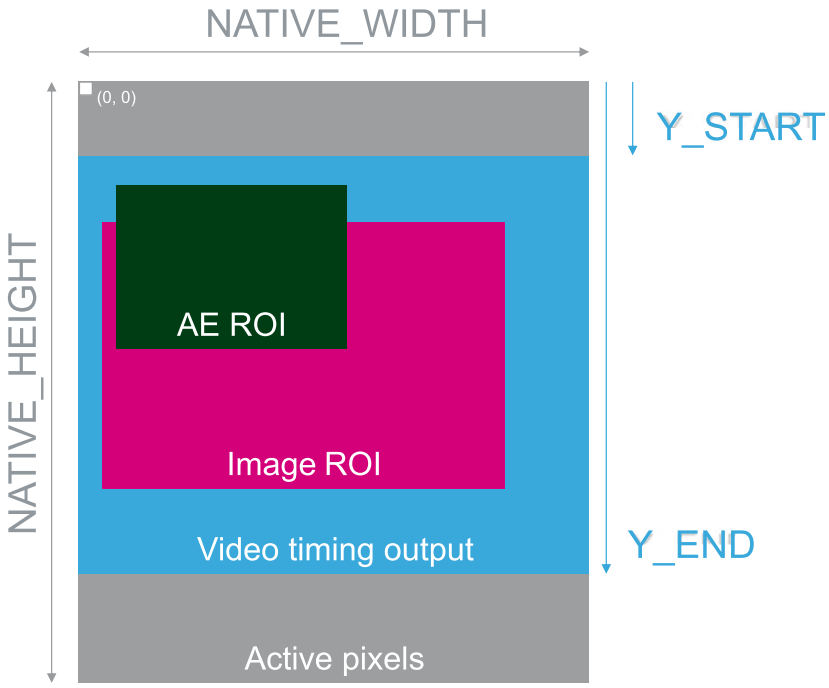
14.1.1 ROIs

There are three crop modules in the video processing pipeline:

- The first one crops the pixel array at the input of the ISP (VT crop)
- The second one crops the image at the output of the ISP (image crop). The image crop defines the image ROI.
- The third one crops at the input of the AEC module (AEC crop) for exposure statistics. The AEC crop defines the AEC ROI.

The VT crop feeds the processing data path so the output of the VT crop is the input of the ISP. Consequently, both image crop and AEC crop are configured according to the VT crop output (see figure below).

Figure 6. **Crops and ROIs**



The VT crop is controlled by two registers: Y_START and Y_END. They are respectively the first row and the last row of the pixel array read by the VT. When the orientation is normal, the VT processes the rows from the top of the pixel array to the bottom. Consequently, the reference of these registers is the top first row.

Table 24. **VT crop registers**

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
Y_START	VALUE	15:0	UI	First row read by the VT
Y_END	VALUE	15:0	UI	Last row read by the VT

Two other crop modules in the video pipe enable the selection of two different ROIs: one for the image, another one for the AEC. Both ROIs are strictly independent.

When the orientation is normal, the reference pixel of both ROIs is the top left corner of the VT output (see Figure 7. Image ROI configuration and Figure 8. AEC ROI configuration).

VT crop and image crop are defined in the CONTEXT register groups whereas AEC ROI is defined in the DYNAMIC register group, meaning the AEC ROI is shared across 4 contexts.

Figure 7. **Image ROI configuration**

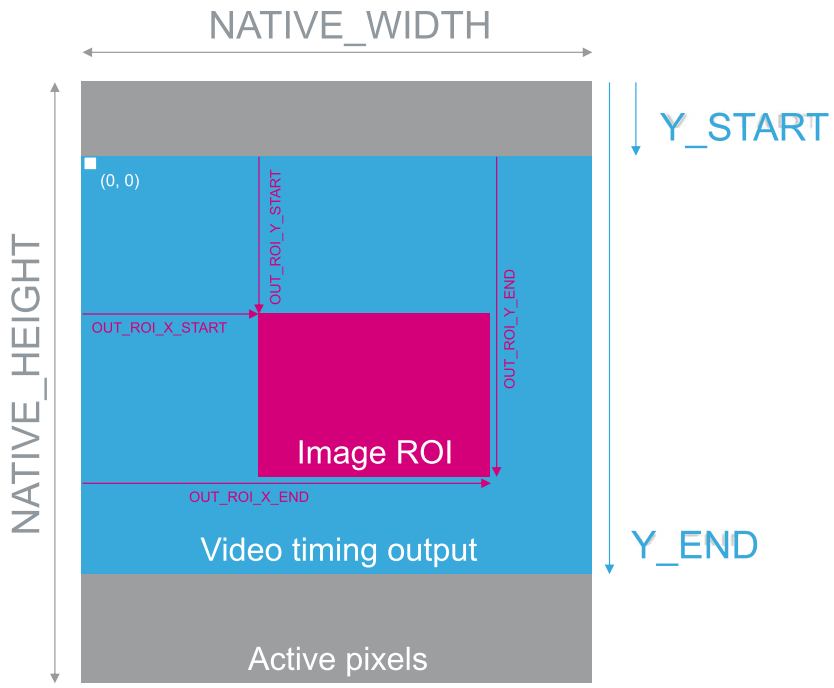


Table 25. **Image crop registers**

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
OUT_ROI_X_START	VALUE	15:0	UI	Image ROI
OUT_ROI_X_END	VALUE	15:0	UI	
OUT_ROI_Y_START	VALUE	15:0	UI	
OUT_ROI_Y_END	VALUE	15:0	UI	

The image resolution must comply with MIPI guidelines:

- Both width (OUT_ROI_X_END - OUT_ROI_X_END + 1) and height (OUT_ROI_Y_END - OUT_ROI_Y_END + 1) must be even.
- On top of this, when the output format is RAW10, the width must be a multiple of 4 pixels.
- Additional guidelines apply when subsampling or digital binning is enabled (refer to Table 28. ROI configurations versus decimation factor).

Figure 8. **AEC ROI configuration**

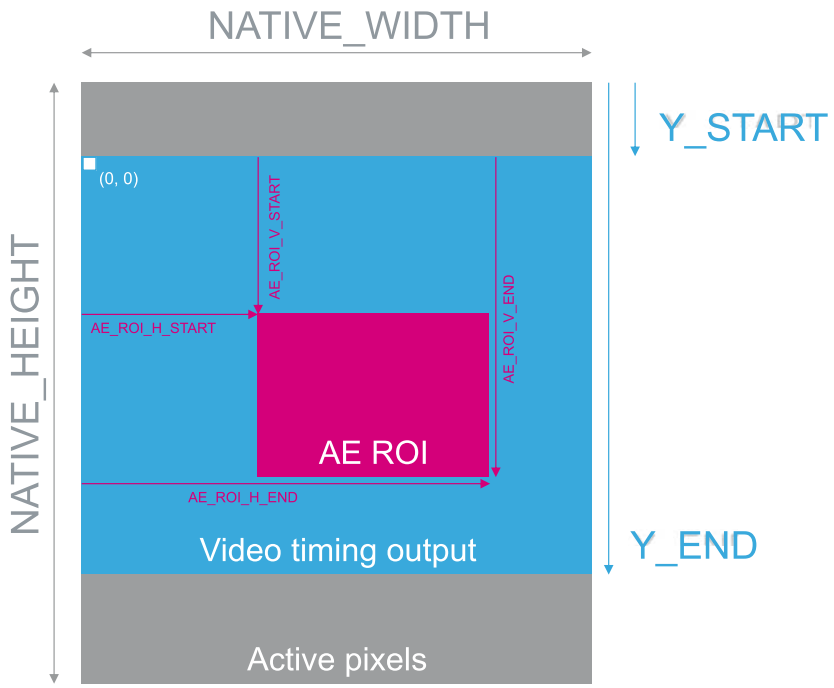


Table 26. **AEC crop registers**

DYNAMIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
AE_ROI_ START_H	VALUE	15:0	UI	AEC ROI
AE_ROI_ END_H	VALUE	15:0	UI	
AE_ROI_ START_V	VALUE	15:0	UI	
AE_ROI_END_V	VALUE	15:0	UI	

OUT_ROI_X_END and AE_ROI_END_H must be lower or equal to the native width (pixel array).
OUT_ROI_Y_END and AE_ROI_END_V must be lower or equal to the VT output width (Y_END – Y_START + 1).

14.1.2 Subsampling and digital binning

On top of the crop operations, the ISP has a subsampling and digital binning module. The available decimation factors are 2 and 4, nevertheless both modules cannot be enabled simultaneously. The decimation factor applies in X and Y directions.

Selection of the decimation method and factor is controlled by the READOUT_CTRL register. This register is part of the CONTEXT register group.

Table 27. Decimation control register

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
READOUT_CTRL	CFG	2:0	C	0: Normal 1: Digital binning x2 2: Digital binning x4 3: Subsampling x2 4: Subsampling x4

Whatever the decimation factor, the configuration of the ROIs is always based on the normal resolution (x1). However, the decimation operation introduces constraints on ROI configuration. Indeed, some register values must be multiples of powers of two. Refer to table below to determine which is the multiple that applies for each register or couple of registers.

Table 28. ROI configurations versus decimation factor

		RAW8			RAW10		
	Decimation factor	**Normal**	**x2**	**x4**	**Normal**	**x2**	**x4**
Y_START	—	1	2	4	1	2	4
Y_END + 1	—	1	2	4	1	2	4
OUT_ROI_X_END - OUT_ROI_X_START + 1	—	2	4	8	4	8	16
OUT_ROI_Y_END - OUT_ROI_Y_START + 1	—	2	4	8	2	4	8

14.1.3 Status registers of the image ROI

Confirmation of the image ROI is available in the STATUS register group. OUT_ROI_X_SIZE and OUT_ROI_Y_SIZE are the final resolution of the image including potentially the digital binning or the subsampling.

$$OUT\_ROI\_X\_SIZE = \frac{OUT\_ROI\_X\_END - OUT\_ROI\_X\_START + 1}{Decimation\ factor}$$

$$OUT\_ROI\_Y\_SIZE = \frac{OUT\_ROI\_Y\_END - OUT\_ROI\_Y\_START + 1}{Decimation\ factor}$$

Table 29. Image status registers

STATUS register group				
Register name	**Field name**	**Bits**	**Data type**	**values**
Y_START	VALUE	15:0	UI	First row read by the VT
Y_END	VALUE	15:0	UI	Last row read by the VT
OUT_ROI_X_START	VALUE	15:0	UI	Image ROI
OUT_ROI_X_END	VALUE	15:0	UI	
OUT_ROI_Y_START	VALUE	15:0	UI	
OUT_ROI_Y_END	VALUE	15:0	UI	
OUT_ROI_X_SIZE	VALUE	15:0	UI	Width of the image
OUT_ROI_Y_SIZE	VALUE	15:0	UI	Height of the image
READOUT_CTRL	CFG	2:0	C	Decimation

14.2 Group parameter hold

The host can prevent the firmware from applying some dynamic parameters (DYNAMIC and CONTEXT registers). This allows the sensor to be updated with a new configuration without timing constraints. To do this, the host controls the GROUP_PARAM_HOLD register (DYNAMIC register group). This register must be updated in STREAMING state.

Table 30. Group parameter hold (GPH) register

DYNAMIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
GROUP_PARAM_HOLD	HOLD	0	B	0: Hold disable 1: Hold enable

First, the hold must be enabled, then the host can update the following registers:

Table 31. Registers controlled by GPH

Feature	Register name	Register group
Dark calibration	DARKCAL_PEDESTAL	CONTEXT
Exposure	AE_COMPENSATION	DYNAMIC
	AE_TARGET_PERCENTAGE	
	AE_STEP_PROPORTION	
	AE_LEAK_PROPORTION	
	EXP_MODE	CONTEXT
	MANUAL_ANALOG_GAIN	
	MANUAL_COARSE_EXPOSURE	
	MANUAL_DIGITAL_GAIN	
Image ROI	OUT_ROI_X_START	CONTEXT
	OUT_ROI_X_END	
	OUT_ROI_Y_START	
	OUT_ROI_Y_END	
AEC ROI	AE_ROI_START_H	DYNAMIC
	AE_ROI_START_V	
	AE_ROI_END_H	
	AE_ROI_END_V	
Pattern generator	PATGEN_CTRL	DYNAMIC

Once the new configuration is set, the host disables the hold. Updated registers are then considered by the firmware.

Note: When GPH is enabled, automatic exposure control is frozen.

14.3 Orientation

Device orientation can be set using the Orientation register in the STATIC register group.

Table 32. Orientation register

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
ORIENTATION	MODE	15:0	C	0x0: No flip 0x1: X flip 0x2: Y flip 0x3: XY flip

Figure 9. Device orientation

No flip X flip Y flip XY flip

14.4 Pattern generator

The device can generate patterns for debugging purposes. Active pixel values are overridden when the register PATGEN_CTRL is different than 0.

Table 33. Pattern generator register

DYNAMIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
PATGEN_CTRL	ENABLE	1:0	C	0x0: BYPASS 0x1: PATGEN
	TYPE	9:4	C	See table below

Table 34. Pattern configuration

Pattern	Value
Solid color	0x00
Vertical color bars	0x08
Horizontal gray scale	0x20
Vertical gray scale	0x21
Diagonal gray scale	0x22
Pseudo random (PN28)	0x28

14.5 Dark calibration

The device embeds an automatic dark calibration mechanism. The dark calibration target value can be set with the dynamic register DARKCAL_PEDESTAL. This is a 10-bit value and is set regardless of the output format (RAW8 or RAW10). However, when the device outputs an 8-bit image, the dark calibration mechanism uses the register value right-shifted by two bits to automatically align the pedestal value according to the output format dynamic.

For instance, with the default value 64 set in the register DARKCAL_PEDESTAL:

- The pedestal is 64 in RAW10
- The pedestal is 16 in RAW8

Table 35. Dark calibration register

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
DARKCAL_PEDESTAL	VALUE	7:0	UI	[0:1023]

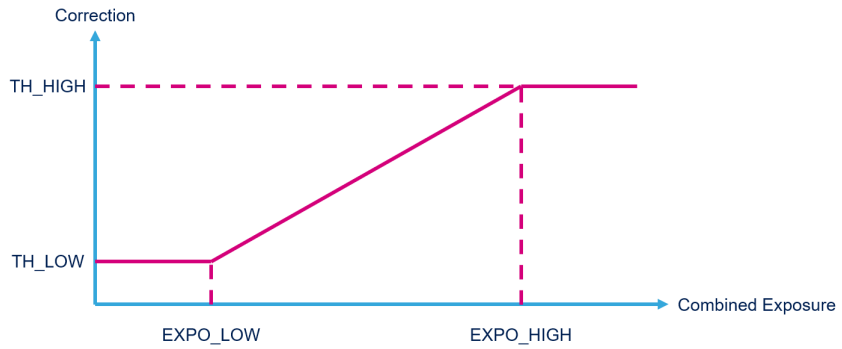
14.6 Defect correction

The device embeds an automatic defect correction algorithm allowing defective pixels to be replaced. CC_SIGMA and RC_TH are criteria to define if a pixel is defective or not. Measurements are damped based on exposure values

Table 36. Defect correction registers

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
DUSTER_CTRL	ENABLE	0	C	0x0: DISABLE 0x1: ENABLE
	DYN_ENABLE	2:1	C	0x0: DISABLE 0x1: ENABLE_SINGLET_COUPLET 0x2: ENABLE_ONLY_COUPLET
	MAP_ENABLE	3	C	0x0: DISABLE 0x1: ENABLE
	RING_ENABLE	4	C	0x0: DISABLE 0x1: ENABLE
DUSTER_DMP_CC_SIGMA_X	EXPO_LOW	15:0	UI	—
	EXPO_HIGH	31:16	UI	—
DUSTER_DMP_CC_SIGMA_Y	TH_LOW	15:0	UI	—
	TH_HIGH	31:16	UI	—
DUSTER_DMP_RC_TH_X	EXPO_LOW	15:0	UI	—
	EXPO_HIGH	31:16	UI	—
DUSTER_DMP_RC_TH_Y	TH_LOW	15:0	UI	—
	TH_HIGH	31:16	UI	—

Figure 10. Damper curve



14.7 Exposure

The exposure settings are either automatically controlled by the firmware (AEC), or directly controlled by the host (MANUAL). A third mode is to freeze the current settings of the AEC algorithm. Whatever the mode, analog and digital gains are respectively limited to 4 and 8.

14.7.1 Exposure mode control

Exposure mode is controlled by the EXP_MODE register in the CONTEXT register group. Each context has its own exposure mode.

Table 37. Exposure control register

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
EXP_MODE	MODE	1:0	C	0x0: Automatic mode 0x1: Freeze AE with current settings 0x2: Manual setting mode

14.7.2 Manual exposure

When manual setting mode is selected, the user takes full control of the exposure settings: integration time and analog and digital gains. Each context has its own manual exposure settings.

- Analog gain is controlled by the MANUAL_ANALOG_GAIN register. The gain is computed with the following formula: $analog\ gain = \frac{32}{32 - MANUAL\_ANALOG\_GAIN}$. The value of the register is in the range [0:24] that is, a gain from 1 to 4.
- Integration time is controlled by the MANUAL_COARSE_EXPOSURE register. The value is expressed in line equivalent. Minimum and maximum limits are based on several criteria like the VT, the ADC mode, etc. The integration time is also limited by the frame length. Exposure limits are described in Section 13.8.1: Exposure limits
- Digital gain is controlled by the MANUAL_DIGITAL_GAIN register. This register is coded as a Fixed Point 5.8 and the value is in the range [1.00, 8.00].

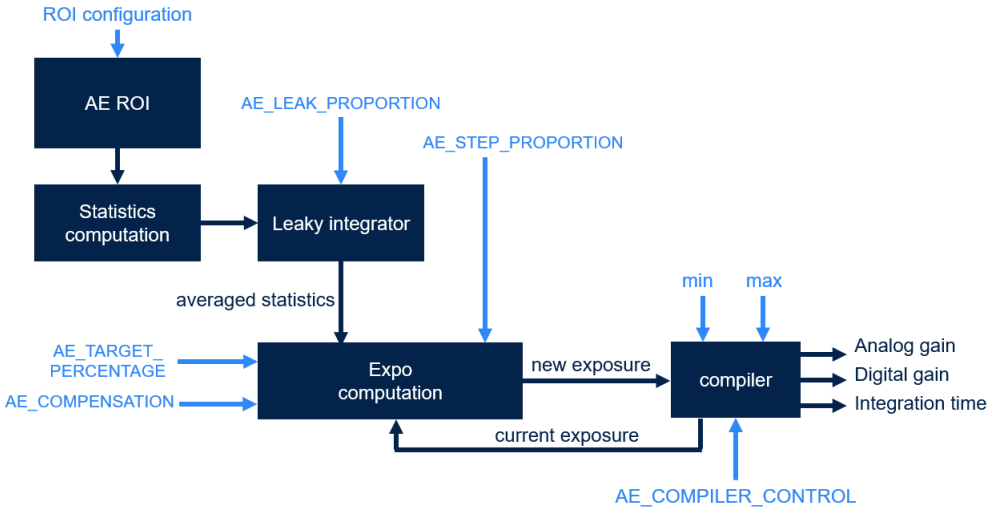
Refer to Exposure settings range to set the limits of each parameter.

Table 38. Manual exposure setting registers

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
MANUAL_ANALOG_GAIN	VALUE	4:0	C	Analog gain to be set
MANUAL_COARSE_EXPOSURE	VALUE	15:0	UI	Integration time in line to be set
MANUAL_DIGITAL_GAIN	VALUE	12:0	FP 5.8	Digital gain to be set

14.7.3 Automatic exposure

Figure 11. **AEC overview**



In automatic mode, the AEC targets a level of luminance as a percent of the saturation level (that is, 100 means saturated image). The exposure can also be adjusted through the compensation factor (expressed in EV) added on top of the target. From the image statistics and the current exposure, the AEC updates gains and the integration time on a frame basis.

- The target is set by the AE_TARGET_PERCENTAGE register
- The compensation factor is controlled by the AE_COMPENSATION register

Image statistics (luminance evaluation) are computed over a configurable area (ROI). Information regarding the configuration of the AE ROI is available in Section 14.1.1: ROIs.

Two AEC modes are available. The mode is selected by bit[0] of the AE_COMPILER_CONTROL register.

- 0 sets the priority to minimum gains. The AEC minimizes both digital and analog gains, then adjusts the integration time.
- 1 sets the priority to flicker free exposure. The AEC prioritizes the integration time in multiples of half the flicker period.

Two frequencies are available for flicker free mode (see above). The frequency is selected by bit[1] of the AE_COMPILER_CONTROL register:

- 0 is 50 Hz, the AEC tries to set the integration time to a multiple of 10 ms
- 1 is 60 Hz, the AEC tries to set the integration time to a multiple of 8.33 ms
- For lower integration times, the flicker free condition is not respected

The main solution to making the sensor insensitive to LED flicker is to adjust the frame length to a multiple of half the flicker period.

Two registers control the convergence loop of the AEC:

- AE_LEAK_PROPORTION register controls reactivity. It is the leak of a leaky integrator fed by the image statistics. The leaky integrator averages the image statistics over time and smoothes the luminance transition.
  - When AE_LEAK_PROPORTION = 0.0, statistics are frozen at the previous value
  - When AE_LEAK_PROPORTION = 1.0, statistics are forced to the current frame statistic
- AE_STEP_PROPORTION register controls the speed. It is the damping factor for the exposure variation.
  - When AE_STEP_PROPORTION = 0.0, the exposure is frozen
  - When AE_STEP_PROPORTION = 0.5, operation is at half speed
  - When AE_STEP_PROPORTION = 1.0, operation is at full speed (not recommended)

Table 39. **Automatic exposure mode registers**

DYNAMIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
AE_COMPILER_CONTROL	MODE	0	C	0: Priotity to smallest gains 1: Priority to flicker free
	FLICKER_FREQUENCY	1	C	0: 50 Hz 1: 60 Hz
AE_COMPENSATION	VALUE	15:0	SFP 8.8	Compensation in EV
AE_TARGET_PERCENTAGE	VALUE	15:0	UI	Percentage relative to saturation
AE_STEP_PROPORTION	VALUE	8:0	FP 1.8	Damping factor of the exposure
AE_LEAK_PROPORTION	VALUE	15:0	FP 1.15	Leaky integrator of the statistics

14.7.4 AEC cold start

It is possible to force the initial values of the AEC output. This feature is controlled by bit[0] of the AE_FORCE_COLDSTART register. If the feature is enabled, the AEC applies the following exposure settings at the next start STREAMING command:

- AE_COLDSTART_COARSE_EXPOSURE register
- AE_COLDSTART_ANALOG_GAIN register
- AE_COLDSTART_DIGITAL_GAIN register

If this feature is disabled, the AEC starts with the current values at the next START STREAMING command.

Table 40. **AEC cold start registers**

DYNAMIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
AE_FORCE_COLDSTART	VALUE	0	B	0: Disable 1: Enable
AE_COLDSTART_COARSE_EXPOSURE	VALUE	15:0	UI	See manual exposure mode for configuration
AE_COLDSTART_ANALOG_GAIN	VALUE	4:0	UI	
AE_COLDSTART_DIGITAL_GAIN	VALUE	12:0	FP 5.8	

14.7.5 Exposure settings status

Whatever the exposure mode, the settings currently applied are available in the STATUS registers group.

- Exposure control mode is available in EXPOSURE_MODE register
- Coarse exposure time is available in APPLIED_COARSE_EXPOSURE register. The value is expressed in line equivalent.
- Analog gain is available in the APPLIED_ANALOG_GAIN register
- Digital gain is available in the APPLIED_DIGITAL_GAIN register
- Status of the AEC is available in the AE_STATUS register

15 Context management

Four contexts are available to change the settings during STREAMING. The host configures the sequence to switch from one context to another one. The sensor sends CONTEXT_REPEAT_COUNT frames, then switches to the context number stored in NEXT_CONTEXT.

The first frame output by the sensor is based on context 0 parameters. If CONTEXT_REPEAT_COUNT is set to 0, the sensor remains on the current context.

Warning: *The current context parameters (CONTEXT_REPEAT_COUNT and NEXT_CONTEXT) must not be changed during STREAMING. If the NEXT_CONTEXT value is higher than 3, the sensor automatically goes to SW_STANDBY after CONTEXT_REPEAT_COUNT frames.*

The following values are available in the STATUS register group (also see table below).

- FRAME_COUNTER
- CONTEXT_FRAME_COUNTER
- CONTEXT_REPEAT_COUNT
- CURRENT_CONTEXT
- NEXT_CONTEXT

Table 41. Context management registers

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
CONTEXT_REPEAT_COUNT	VALUE	15:0	UI	—
NEXT_CONTEXT	VALUE	15:0	C	0, 1, 2, 3, 0xFF

16 Output interface

The output interface of the device embeds a single lane MIPI DPHY interface. It supports up to 1.2 Gb/s of data rate.

Data are transferred through the CSI2 as follows:

- Status lines coded on RAW8 SMIA format
- RAW10 or RAW8 image data

By default, the MIPI clock is continuous, meaning that the clock lanes are always in high-speed state. It is possible to disable this continuous mode, by setting the register below in SW_STANDBY. In non-continuous mode, the MIPI clock lanes are set in Low power state during the interframe.

Miscellaneous registers					
Register name	**Field name**	**Bits**	**Data type**	**Default**	**Values**
DPHYTX_CTRL	VALUE	[7:0]	CODE	0x18	0x08: Disable continuous mode 0x18: Enable continuous mode

16.1 Configuration

All data (active image and ISL) can be output on different virtual channels and/or data types by using the OIF_VC_CTRL and OIF_XXX_CTRL registers.

Table 42. Output interface configuration registers

STATIC register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
FORMAT_CTRL	OUT_FORMAT	4:0	C	0x8: RAW8 0xa: RAW10
OIF_CTRL	RESERVED	2:0	C	RESERVED
	CLKLANE_SWAP	3	C	0x0: NO_SWAP 0x1: LANE_SWAP
	RESERVED	5:4	C	RESERVED
	DATALANE0_SWAP	6	C	0x0: NO_SWAP 0x1: LANE_SWAP
	RESERVED	7	C	RESERVED
OIF_VC_CTRL	ACTIVE_PIX	1:0	UI	Virtual channel of the image
	ISL	3:2	UI	Virtual channel of the embedded status lines
OIF_IMG_CTRL	DATA_TYPE	5:0	UI	Data type of the image
OIF_ISL_CTRL	DATA_TYPE	5:0	UI	Data type of the embedded status lines
ISL_ENABLE	VALUE	0	B	0: Disable status lines 1: Enable status lines

16.2 Frame format

The frame is made of two status lines (each line is the same size) followed by the image content.

Figure 12. Image content

16.3 Status lines

Status lines are composed of two lines. The line width is the same as the active image output in bytes, with a minimum of 256 bytes. The lines contain status register values for the current frame. Data are coded in SMIA RAW8 format. Content is defined in Section 19.1: STATUS registers.

The default data type of the embedded status lines is 0x12. The default virtual channel of the embedded status lines is 0x0.

Figure 13. Structure of the ISL lines

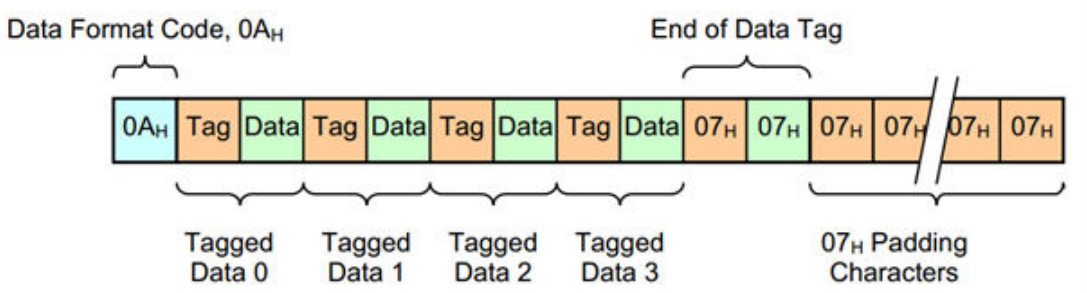


Table 43. List of used SMIA++ tags

Tag	Data byte description
07_H	End of data tdata byte value = 07_H)
AA_H	CCI register index MSB [15:8]
$A5_H$	CCI register index LSB [7:0]
$5A_H$	Auto-increment the CCI index after the data byte - valid data byte The data byte contains valid CCI register data

Although an SMIA encoding rule is used, the ISL structure is frame-to-frame identical. The first tags are used to set the MSB and LSB addresses (0xaa and 0xa5 respectively) of the CCI register. All subsequent tags are auto-increment tags. Consequently, the ISL content may be decoded using an SMIA compatible decoder. More simply, the ISL content can be decoded by reading every other byte of the ISL.

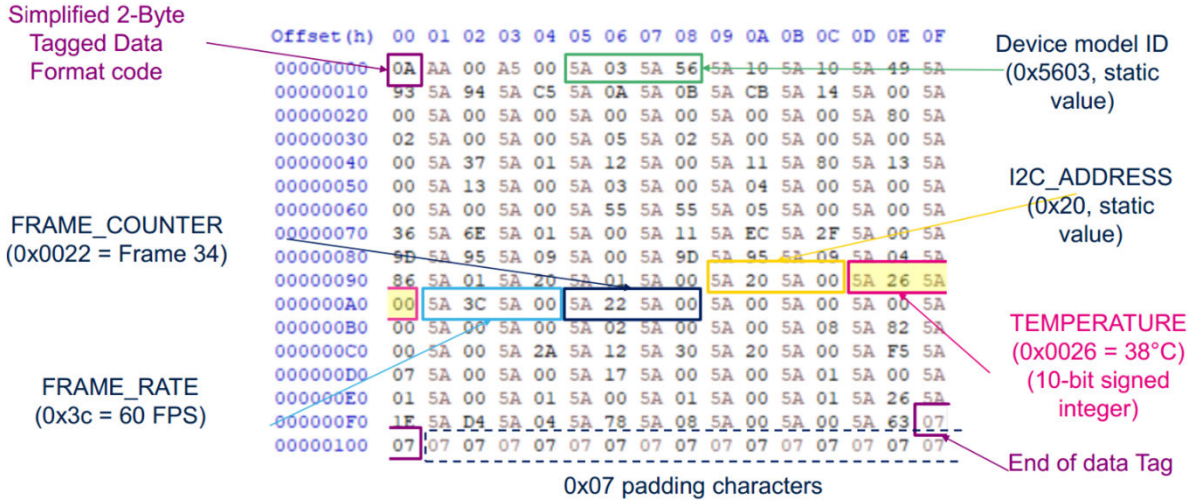
Example for the first ISL line

Status_register_address_N value [0:124] = (content of ISL byte) (2*N + 6).

Example for the second ISL line

Status_register_address_N value [125:249] = (content of ISL byte) (2*(N-125)+6).

Figure 14. **Example of ISL content and informative locations**



16.4 Image data

Image data contain pixel values based on different crop and binning sets. Values can be coded in RAW10 or RAW8 depending on the register settings. Image width and height should be even. For RAW10 data, the image width should be a multiple of 4 pixels.

The data type of the image is set by the OIF_ISL_CTRL register. The default value is 0x2B (RAW10). To comply with CSI-2 specifications, the host must update the OIF_ISL_CTRL register to 0x2A when the output format is RAW8. The default virtual channel of the image is 0x0.

17 Temperature

The device embeds a thermal sensor. Temperature is read at each frame in STREAMING state or in SW_STANDBY state if a THSENS_READ command is sent. The result is stored in the TEMPERATURE status register.

18 GPIOs

The device has four configurable GPIOs. GPIO settings are part of the CONTEXT register group (see table below) and consequently they can differ from one context to another.

GPIO settings are part of the CONTEXT register group (see table below) and consequently they can be configured differently from one context to another.

The GPIOs can be configured with the following modes:

- GPIO_IN: Standard input
- STROBE_MODE: Envelope of the integration time
- PWM_STROBE: Envelope of the integration time multiplied by the PWM
- PWM: Continuous PWM
- GPIO_OUT: Register control level
- VSYNC_OUT_MODE0: Image readout envelope
- VSYNC_OUT_MODE1: Image readout start
- VSYNC_OUT_MODE2: Image readout end
- VT_SLAVE_MODE: Input to trigger follower mode (only valid for GPIO 0)

The GPIOs are active only during STREAMING state, although configuration is also possible during SW_STANDBY state.

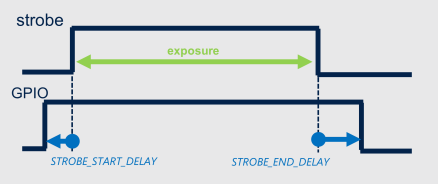
18.1 GPIO out control

When the GPIOs are set to GPIO_OUT, the polarity and value are set with the fields VALUE and POLARITY of the GPIO_X_CTRL register (refer to Section 18.4: GPIO control registers).

18.2 Strobe mode control

When GPIO is set to STROBE_MODE, it is possible to adjust the shift of the rising and falling edges of the output signal relative to the internal strobe. The STROBE_START_DELAY and STROBE_END_DELAY registers respectively control the shift of the rising and falling edges. The values are signed and expressed in line (refer to Section 18: GPIOs). The figure below shows an example with negative STROBE_START_DELAY and positive STROBE_END_DELAY.

Figure 15. Strobe signal control



18.3 PWM mode control

When the GPIOs are set to PWM or PWM_STROBE modes, the PWM frequency and duty cycle are set with the fields DUTY_CYCLE and CLK_DIVISOR of PWM_CTRL register as follows:

$$PWM\ \ frequency\ = \frac{PWM\_CLOCK}{CLK\_DIVISOR\ + 1}$$

$$PWM\ \ \text{duty cycle}\ = \frac{16\ - DUTY\_CYCLE}{16}$$

18.4 GPIO control registers

The following table details the registers used to control the GPIOs.

Table 44. GPIO registers

CONTEXT register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
GPIO_0_CTRL	MODE	3:0	C	0x0: RESERVED 0x1: GPIO_IN 0x2: STROBE_MODE 0x3: PWM_STROBE 0x4: PWM 0x5: GPIO_OUT 0x6: VSYNC_OUT_MODE0 0x7: VSYNC_OUT_MODE1 0x8: VSYNC_OUT_MODE2 0xa: VT_SLAVE_MODE
	VALUE	4	B	0x0: GPIO_LOW 0x1: GPIO_HIGH
	POLARITY	5	B	0x0: NO_INVERSION 0x1: INVERTED
GPIO_1_CTRL	Same as for GPIO_0_CTRL except default mode			Same as for GPIO_0_CTRL except default mode
GPIO_2_CTRL				
GPIO_3_CTRL				
VSYNC_START_DELAY	VALUE	7:0	SI	[0:127]
VSYNC_END_DELAY	VALUE	7:0	SI	[-128:127]
STROBE_START_DELAY	VALUE	7:0	SI	[-128:127]
STROBE_END_DELAY	VALUE	7:0	SI	[-128:127]
PWM_CTRL	DUTY_CYCLE	3:0	UI	[1:15]
	CLK_DIVISOR	31:16	UI	[7:65535]

18.5 GPIO status registers

When a GPIO is set to GPIO_IN mode, its current value can be retrieved using the GPIO status registers as follows:

Table 45. GPIO status registers

STATUS register group				
Register name	**Field name**	**Bits**	**Data type**	**Values**
GPIO_0_STATUS	VALUE	0	B	Input value of GPIO 0 when set to GPIO_IN
GPIO_1_ STATUS	VALUE	0	B	Input value of GPIO 1 when set to GPIO_IN
GPIO_2_ STATUS	VALUE	0	B	Input value of GPIO 2 when set to GPIO_IN
GPIO_3_ STATUS	VALUE	0	B	Input value of GPIO 3 when set to GPIO_IN

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19.1 STATUS registers

Register group range: 0x0000 to 0x0138

Table 46. STATUS registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0000	DEVICE_MODEL_ID	VALUE	31:0	UI	0x5335 4730	Device name
0x0004	DEVICE_REVISION	TOP_DIE	15:8	UI	0x11	Top die mask code (HW)
		BOTTOM_DIE	7:0	UI	0x11	Bottom die mask code (HW)
0x0008	DEVICE_NUMBER_1	VALUE	31:0	UI	—	Device number from traceability
0x000C	DEVICE_NUMBER_2	VALUE	31:0	UI	—	Device number from traceability
0x0010	DEVICE_NUMBER_3	VALUE	31:0	UI	—	Device number from traceability
0x0014	DEVICE_NUMBER_4	VALUE	31:0	UI	—	Device number from traceability
0x0018	ROM_REVISION	MAJOR_REVISION	11:8	UI	0x2	Major ROM code revision
		MINOR_REVISION	7:4	UI	0x1	Minor ROM code revision
		MICRO_REVISION	3:0	UI	0x1	Micro ROM revision
0x001C	UI_REVISION	MAJOR_REVISION	15:8	UI	0x02	Major UI revision
		MINOR_REVISION	7:0	UI	0x12	Minor UI revision
0x001E	OPTICAL_REVISION	VALUE	15:0	UI	0x0	Optical revision
0x0020	VTPATCH_ID	VALUE	63:0	UI	0x0009 0009 8011 0009	VTPATCH_ID
0x0022	FWPATCH_REVISION	MAJOR_REVISION	15:8	UI	0x0	Major FWP revision
		MINOR_REVISION	7:0	UI	0x0	Minor FWP revision
0x0024	VTIMING_RD_REVISION	VTRAM_UPDATED	31	UI	0x0	VTRAM update status in case of manual update
		LDEC	23:16	UI	0x0	Line decoder timing version
		RESERVED	15:8	UI	0x0	RESERVED
		PATTERN	7:0	UI	0x0	RD pattern timing version
0x0028	VTIMING_GR_REVISION	RESERVED	15:8	UI	0x0	RESERVED
		PATTERN	7:0	UI	0x0	GR pattern timing version
0x002A	VTIMING_GT_REVISION	RESERVED	15:8	UI	0x0	RESERVED
		PATTERN	7:0	UI	0x0	GT pattern timing version
0x002C	SYSTEM_FSM	VALUE	7:0	C	0x01	Sensor system FSM status: 0x00: HW_STBY 0x01: READY_TO_BOOT

Register address	Register name	Field name	Bits	Data type	Default	Values
						0x02: SW_STBY 0x03: STREAMING 0xFF: ERROR
0x002E	NVM	DRIVER_FSM	7:6	C	0x0	NVM driver FSM: 0x00: IDLE 0x01: PROG_OP 0x02: READ_OP 0x03: ERROR
		ECC_ERROR	5	UI	0x0	ECC error detection: 0x0: NO_ERROR 0x1: ECC_ERROR
		READ_FAIL	3	UI	0x0	Error during read operation
		READ_OK	2	UI	0x1	Read with success
		PROG_FAIL	1	UI	0x0	Error during program operation
		PROG_OK	0	UI	0x0	Program with success
0x0038	EXT_CLOCK	VALUE	31:0	UI	0x0	Integer part of EXT clock frequency in Hz
0x003C	SYSTEM_PLL_CLK	VALUE	31:0	UI	0x0	PLL output frequency in Hz
0x0040	PIXEL_CLK	VALUE	31:0	UI	0x0	Pixel clock frequency in Hz
0x0044	MCU_CLK	VALUE	31:0	UI	0x0	MCU clock frequency in Hz
0x0048	CLK_PLL_MULT	VALUE	7:0	UI	0x0	PLL multiplier value
0x004A	I2C_ADDRESS	DEVICE_ID	15:1	UI	0x10	Device I²C address
0x004C	TEMPERATURE	TH_DEG_INT	15:0	SI	0x0	Temperature in celsius
0x004E	FRAME_RATE	VALUE	15:0	UI	0x0	Frame rate x16
0x0050	FRAME_COUNTER	VALUE	15:0	UI	0x0	Global frame counter
0x0052	CONTEXT_FRAME_COUNTER	VALUE	15:0	UI	0x0	Context frame counter
0x0054	CONTEXT_REPEAT_COUNT	VALUE	15:0	UI	0x0	Number of frames per context
0x0056	CURRENT_CONTEXT	VALUE	7:0	UI	0x0	Current context
0x0057	NEXT_CONTEXT	VALUE	7:0	UI	0x0	Next context target, if >3 STOP STREAMING occurs after repeat count
0x0058	ORIENTATION	MODE	1:0	C	0x0	Image orientation mode control: 0x0: NORMAL no flip 0x1: X_FLIP X flip 0x2: Y_FLIP Y flip 0x3: XY_FLIP XY flip
0x005A	VT_CTRL	Reserved	4:3	UI	0x0	RESERVED
		ADC_MODE	2	B	0x0	Video timing ADC mode 9 or 10 bits: 0x0: STD_10 standard mode 10 bits 0x1: FAST_09, fast mode with 9 bits
		SYNC_MODE	1:0	C	0x0	Video timing synchronization mode: 0x0: MASTER 0x1: SLAVE_MODE STREAMING on EXTSYNC pulses

Register address	Register name	Field name	Bits	Data type	Default	Values
0x005A	VT_CTRL					0x2: SLAVE_I2C STREAMING on I²C pulses
0x005B	FORMAT_CTRL	OUT_FORMAT	4:0	UI	0x0	Frame output format control: 0x8: RAW8 0xA: RAW10
0x005C	OIF_CTRL	Reserved2	9	UI	0x0	RESERVED
		Reserved1	8:7	UI	0	RESERVED
		DATALANE0_SWAP	6	UI	0x0	Lane swapping: 0x0: NO_SWAP 0x1: LANE_SWAP
		Reserved0	5:4	UI	0x0	RESERVED
		CLKLANE_SWAP	3	UI	0x0	ClkLane swapping: 0x0: NO_SWAP 0x1: LANE_SWAP
		Reserved	2:0	UI	0x0	RESERVED
0x005E	OIF_VC_CTRL	ISL	3:2	UI	0x0	Virtual channel selection for ISL
		ACTIVE_PIX	1:0	UI	0x0	Virtual channel selection for image
0x005F	OIF_IMG_CTRL	DATA_TYPE	5:0	UI	0x0	Data type selection aligned with RAW format
0x0060	OIF_ISL_CTRL	DATA_TYPE	5:0	UI	0x0	Data type selection
0x0062	PATGEN_CTRL	TYPE	9:4	C	0x0	0x00: SOLID, solid color 0x08: COLORBAR, vertical color bars 0x10: GRADBAR, fade-to-gray vertical color bars 0x19: SMEAR, rectangle over the input image 0x20: HGREY, horizontal gray scale 0x21: VGREY, vertical gray scale 0x22: DGREY, diagonal gray scale 0x28: PN28, pseudo random
		ENABLE	1:0	UI	0x0	Patgen configuration 0x0: BYPASS 0x1: PATGEN_NORMAL
0x0064	APPLIED_COARSE_EXPOSURE	VALUE	15:0	UI	0x0	Coarse exposure time in line
0x0066	APPLIED_ANALOG_GAIN	VALUE	4:0	C	0x0	0x00: AnalogGain_AGAIN_1 0x01: AnalogGain_AGAIN_1_03 0x02: AnalogGain_AGAIN_1_07 0x03: AnalogGain_AGAIN_1_1 0x04: AnalogGain_AGAIN_1_14 0x05: AnalogGain_AGAIN_1_19 0x06: AnalogGain_AGAIN_1_23 0x07: AnalogGain_AGAIN_1_28 0x08: AnalogGain_AGAIN_1_33 0x09: AnalogGain_AGAIN_1_39

Register address	Register name	Field name	Bits	Data type	Default	Values
						0x0A: AnalogGain_AGAIN_1_45 0x0B: AnalogGain_AGAIN_1_52 0x0C: AnalogGain_AGAIN_1_6 0x0D: AnalogGain_AGAIN_1_68 0x0E: AnalogGain_AGAIN_1_78 0x0F: AnalogGain_AGAIN_1_88 0x10: AnalogGain_AGAIN_2 0x11: AnalogGain_AGAIN_2_13 0x12: AnalogGain_AGAIN_2_29 0x13: AnalogGain_AGAIN_2_46 0x14: AnalogGain_AGAIN_2_67 0x15: AnalogGain_AGAIN_2_91 0x16: AnalogGain_AGAIN_3_2 0x17: AnalogGain_AGAIN_3_56 0x18: AnalogGain_AGAIN_4
0x0068	APPLIED_DIGITAL_GAIN	INTEGER	12:8	UI	0x0	Digital gain applied from exposure algorithm Channel 0 (integer part)
		FRACT	7:0	UI	0x0	Digital gain applied from exposure algorithm Channel 0 (fractional part)
0x0070	AE_MODE	MODE	1:0	C	0x0	Mode control 0x0: AUTO, automatic mode 0x1: FREEZE, freeze AutoExposure algorithm 0x2: MANUAL, manual setting mode
0x0071	AE_STATUS	STATUS	0	UI	0x0	0x0: UNSTABLE 0x1: STABLE
0x0072	AE_MEAN_ENERGY	INTEGER	15:8	UI	0x0	Mean energy of input image (integer part)
		FRACT	7:0	UI	0x0	Mean energy of input image (fractional part)
0x0074	LINE_LENGTH	VALUE	15:0	UI	0x0	Line length output from sensor (including line blanking)
0x0076	FRAME_LENGTH	VALUE	15:0	UI	0x0	Frame length as programmed in the sensor (in fixed point 12.4)
0x0078	X_START	VALUE	15:0	UI	0x0	First row read by the VT
0x007A	X_END	VALUE	15:0	UI	0x0	Last row read by the VT
0x007C	Y_START	VALUE	15:0	UI	0x0	Image Y start from CAB
0x007E	Y_END	VALUE	15:0	UI	0x0	Image Y end from CAB
0x0080	X_SIZE	VALUE	15:0	UI	0x0	ImageX size
0x0082	Y_SIZE	VALUE	15:0	UI	0x0	Image Y size
0x0084	READOUT_CTRL	CFG	2:0	C	0x0	STREAMING readout mode control: 0x0: NORMAL, normal STREAMING 0x1: DBIN_X2, digital binning x2 0x2: DBIN_X4, digital binning x4 0x3: SS_X2, subsampling x2

Register address	Register name	Field name	Bits	Data type	Default	Values
						0x4: SS_X4, subsampling x4
0x0086	WAIT_DELAY	VALUE	15:0	UI	0x0	Wait time before the next frame in addition to blanking in lines
0x0088	OUT_ROI_X_START	VALUE	15:0	UI	0x0	Crop/ROI X start
0x008A	OUT_ROI_X_END	VALUE	15:0	UI	0x0	Crop/ROI X end
0x008C	OUT_ROI_Y_START	VALUE	15:0	UI	0x0	Crop/ROI Y start
0x008E	OUT_ROI_Y_END	VALUE	15:0	UI	0x0	Crop/ROI Y end
0x0090	OUT_ROI_X_SIZE	VALUE	15:0	UI	0x0	ROI X size
0x0092	OUT_ROI_Y_SIZE	VALUE	15:0	UI	0x0	ROI Y size
0x009D	GPIO_0_CTRL	VALUE	7:0	B	0x0	Input GPIO value in case of input mode
0x009E	GPIO_1_CTRL	VALUE	7:0	B	0x0	Input GPIO value in case of input mode
0x009F	GPIO_2_CTRL	VALUE	7:0	B	0x0	Input GPIO value in case of input mode
0x00A0	GPIO_3_CTRL	VALUE	7:0	B	0x0	Input GPIO value in case of input mode
0x00A1	DARKCAL_PEDESTAL	VALUE	7:0	UI	0x0	Pedestal value used for dark calibration
0x012E	MIN_EXPOSURE_IN_CURRENT_CONFIG	VALUE	15:0	UI	0x0	Minimum exposure allowed with the current configuration
0x0138	MAX_EXPOSURE_IN_CURRENT_CONFIG	VALUE	31:0	UI	0x0	Maximum exposure allowed with the current configuration

19.2 COMMAND registers

Register group range: 0x0200 to 0x0202

The command registers are the only registers able to trigger an action from the device (see Section 8: Commands.)

Table 47. COMMAND registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x200	BOOT	COMMAND	1:0	C	0x0	0x1: BOOT 0x2: PATCH_SETUP
0x201	SW_STANDBY	COMMAND	3:0	C	0x0	0x1: START_STREAM 0x2: NVM_READ 0x3: NVM_PROG 0x4: THSENS_READ 0x5: I2C_ADDR_UPDATE 0x6: START_VTRAM_UPDATE 0x7: END_VTRAM_UPDATE
0x202	STREAMING	COMMAND	3:0	C	0x0	0x1: STOP_STREAM 0x2: VT_FSYNC_IN_I2C

19.3 SENSOR SETTINGS registers

Register group range: 0x0220 to 0x0230

The SENSOR_SETTINGS registers must be set in the SW_STANDBY state. Any changes made in the STREAMING state are not considered before the next START_STREAM command.

Table 48. SENSOR SETTINGS registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0220	EXT_CLOCK	VALUE	31:0	UI	0xb71b00	External clock frequency in Hz
0x0224	CLK_PLL_MIPI	VALUE	31:0	UI	0x47868C00	PLL MIPI clock frequency in Hz
0x0229	NVM_NB_OF_WORDS	VALUE	7:0	UI	0x0	Number of 32-bit words for read/write operation
0x022A	NVM_START_ADDRESS	VALUE	8:0	UI	0x0	Start address in NVM for read/write operation
0x0230	DEVICE_I2C_CTRL	MODE	8	C	0x1	I²C mode 0x0: FAST_MODE 0x1: FAST_MODE_PLUS
		DEVICE_ID	7:1	UI	0x10	Device I²C address

19.4 STATIC registers

Register group range: 0x0300 to 0x032E

The STATIC registers must be set in SW_STANDBY state. Any changes made in STREAMING state are not considered before the next START_STREAM command.

Table 49. STATIC registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0300	LINE_LENGTH	VALUE	15:0	UI	0x468	Line length configuration
0x0302	ORIENTATION	MODE	1:0	C	0x0	Image orientation mode control: 0x0: NORMAL no flip 0x1: X_FLIP X flip 0x2: Y_FLIP Y flip 0x3: XY_FLIP XY flip
0x0309	VT_CTRL	RESERVED	4:3	UI	0x0	RESERVED
		ADC_MODE	2	B	0x0	Video timing ADC mode 9 or 10 bits: 0x0: STD_10 standard mode 10 bits 0x1: FAST_09 fast mode with 9 bits
		SYNC_MODE	1:0	C	0x0	Video timing synchronization mode: 0x0: MASTER 0x1: SLAVE STREAMING on EXTSYNC pulses
0x030A	FORMAT_CTRL	OUT_FORMAT	4:0	UI	0xA	Frame output format control: 0x8: RAW8 0xA: RAW10
0x030C	OIF_CTRL	DATALANE0_SWAP	6	C	0x0	CSI lane 0 swapping: 0x0: NO_SWAP 0x1: LANE_SWAP
		RESERVED	5:4	UI	0x0	RESERVED
		CLKLANE_SWAP	3	C	0x0	CSI clock lane swapping: 0x0: NO_SWAP 0x1: LANE_SWAP
		RESERVED2	2:0	UI	0x0	RESERVED
0x030E	OIF_VC_CTRL	ISL	3:2	UI	0x0	Virtual channel selection for ISL
		ACTIVE_PIX	1:0	UI	0x0	Virtual channel selection is common for output image
0x030F	OIF_IMG_CTRL	DATA_TYPE	5:0	UI	0x2B	Data type selection for RAW image format
0x0310	OIF_ISL_CTRL	DATA_TYPE	5:0	UI	0x12	Data type selection for status line
0x0311	OIF_ULPM	ENABLE	0	UI	0	ULPM enable 0x0: DISABLE 0x1: ENABLE
0x0316	DUSTER_CTRL	RING_ENABLE	4	UI	0x1	Duster ring correction control: 0x0: DISABLE disable duster ring correction 0x1: ENABLE enables duster ring correction

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0316	DUSTER_CTRL	MAP_ENABLE	3	UI	0x0	Duster mode control: 0x0: DISABLE disable duster map correction 0x1: ENABLE enables duster map correction
		DYN_ENABLE	2:1	C	0x1	Duster mode control: 0x0: BYPASS disable duster dynamic correction 0x1: AUTO duster corrects singlets and couplets
		ENABLE	0	UI	0x1	Duster mode control: 0x0: BYPASS fully disable duster 0x1: ENABLE enables duster modules
0x0318	DUSTER_DMP_CC_SIGMA_X	EXPO_HIGH	31:16	UI	0x9c40	2 point damper for CC sigma (high exposure value used)
		EXPO_LOW	15:0	UI	0x3e8	2 point damper for CC sigma (low exposure value used)
0x031C	DUSTER_DMP_CC_SIGMA_Y	TH_HIGH	31:16	UI	0x8	2 point damper for CC sigma (maximum threshold value)
		TH_LOW	15:0	UI	0x8	2 point damper for CC sigma (minimum threshold value)
0x0320	DUSTER_DMP_RC_TH_X	EXPO_HIGH	31:16	UI	0xAFC8	2 point damper for ring correction (high exposure value used)
		EXPO_LOW	15:0	UI	0x9c4	2 point damper for ring correction (low exposure value used)
0x0324	DUSTER_DMP_RC_TH_Y	TH_HIGH	31:16	UI	0xdc	2 point damper for ring correction (maximum threshold value)
		TH_LOW	15:0	UI	0xdc	2 point damper for ring correction (minimum threshold value)
0x0329	ISL_ENABLE	VALUE	0	C	0x1	Output ISL 0x0: Disable 0x1: Enable
0x032A	STATUSLINE_PKT_EQ_ACTIVELINE	ENABLE	7:0	UI	0x1	0: DISABLED 1: ENABLED
0x032C	DARKCAL_CTRL	ENABLE	1:0	C	0x1	DarkCal mode control: 0x0: BYPASS disable Darkcal is disabled 0x1: AUTO enable Darkcal in automatic mode 0x2: BYPASS_DARKAVG bypass Darkcal average
0x032E	FSYNC_IN_DELAY	VALUE	15:0	UI	0x0	Tunable single shot controlled mode delay in lines

19.5 DYNAMIC registers

Register group range: 0x0400 to 0x0444

The DYNAMIC register settings can be set either in SW_STANDBY or STREAMING state. These settings are common to all contexts. The table below shows the DYNAMIC parameters.

Table 50. DYNAMIC registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0400	PATGEN_CTRL	TYPE	9:4	C	0x8	0x00: SOLID solid color 0x08: COLORBAR vertical color bars 0x10: GRADBAR fade-to-gray vertical color bars 0x19: SMEAR rectangle over the input image 0x20: HGREY horizontal gray scale 0x21: VGREY vertical gray scale 0x22: DGREY diagonal gray scale 0x28: PN28 pseudo random
		ENABLE	1:0	UI	0x0	Patgen configuration 0x0: BYPASS 0x1: PATGEN_NORMAL
0x0416	DARKCAL_PEDESTAL	VALUE	7:0	UI	0x40	Pedestal value used in DDC block
0x0418	DARKCAL_CH0_OFFSET	INTEGER	18:7	UI	0x0	DarkCal channel 0 offset (integer part)
		FRACT	6:0	UI	0x0	DarkCal channel 0 offset (fractional part)
0x041C	DARKCAL_CH1_OFFSET	INTEGER	18:7	UI	0x0	DarkCal channel 1 offset (integer part)
		FRACT	6:0	UI	0x0	DarkCal channel 1 offset (fractional part)
0x0420	DARKCAL_CH2_OFFSET	INTEGER	18:7	UI	0x0	DarkCal channel 2 offset (integer part)
		FRACT	6:0	UI	0x0	DarkCal channel 2 offset (fractional part)
0x0424	DARKCAL_CH3_OFFSET	INTEGER	18:7	UI	0x0	DarkCal channel 3 offset (integer part)
		FRACT	6:0	UI	0x0	DarkCal channel 3 offset (fractional part)
0x042C	AE_FORCE_COLDSTART	VALUE	0	B	0x1	Force the exposure to start from a cold start 0x0: Disable 0x1: Enable
0x042E	AE_COLDSTART_COARSE_EXPOSURE	VALUE	15:0	UI	0x32	Coarse exposure time in line
0x0430	AE_COLDSTART_ANALOG_GAIN	VALUE	4:0	C	0x0	0x00: AnalogGain_AGAIN_1 0x01: AnalogGain_AGAIN_1_03 0x02: AnalogGain_AGAIN_1_07 0x03: AnalogGain_AGAIN_1_1 0x04: AnalogGain_AGAIN_1_14 0x05: AnalogGain_AGAIN_1_19 0x06: AnalogGain_AGAIN_1_23 0x07: AnalogGain_AGAIN_1_28 0x08: AnalogGain_AGAIN_1_33 0x09: AnalogGain_AGAIN_1_39 0x0A: AnalogGain_AGAIN_1_45

Register address	Register name	Field name	Bits	Data type	Default	Values
						0x0B: AnalogGain_AGAIN_1_52 0x0C: AnalogGain_AGAIN_1_6 0x0D: AnalogGain_AGAIN_1_68 0x0E: AnalogGain_AGAIN_1_78 0x0F: AnalogGain_AGAIN_1_88 0x10: AnalogGain_AGAIN_2 0x11: AnalogGain_AGAIN_2_13 0x12: AnalogGain_AGAIN_2_29 0x13: AnalogGain_AGAIN_2_46 0x14: (AnalogGain_AGAIN_2_67) 0x15: AnalogGain_AGAIN_2_91 0x16: AnalogGain_AGAIN_3_2 0x17: AnalogGain_AGAIN_3_56 0x18: AnalogGain_AGAIN_4
0x0432	AE_COLDSTART_DIGITAL_GAIN	INTEGER	12:8	UI	0x1	Digital gain (integer part) for cold start
		FRACT	7:0	UI	0x00	Digital gain (fractional part) for cold start
0x0434	AE_COMPILER_CONTROL	FLICKER_FREQUENCY	1	C	0x0	0x0: DEF_50Hz 0x1: DEF_60Hz
		MODE	0	C	0x0	0x0: MINIMUM_GAIN 0x1: FLICKER_FREE
0x0436	AE_ROI_START_H	VALUE	15:0	UI	0x0	Definition of exposure ROI according to CAB output coordinates
0x0438	AE_ROI_START_V	VALUE	15:0	UI	0x0	Definition of exposure ROI according to CAB output coordinates
0x043A	AE_ROI_END_H	VALUE	15:0	UI	0x283	Definition of exposure ROI according to CAB output coordinates
0x043C	AE_ROI_END_V	VALUE	15:0	UI	0x25b	Definition of exposure ROI according to CAB output coordinates
0x043E	AE_COMPENSATION	VALUE	15:0	SFP 8.8	0x0	Change the target exposure in stops by increasing or decreasing this value
0x0440	AE_TARGET_PERCENTAGE	VALUE	15:0	UI	0x1B	Exposure target of the AEC algorithm
0x0442	AE_STEP_PROPORTION	VALUE	15:0	FP 1.8	0x80	Fixed point step proportion (8.8)
0x0444	AE_LEAK_PROPORTION	VALUE	15:0	FP 1.15	0x666	Fixed point step proportion (1.15)
0x0448	GROUP_PARAM_HOLD	HOLD	0	B	0x0	0x0: Hold disable 0x1: Hold enable

19.6 CONTEXT 0 registers

Register group range: 0x044C to 0x047A

The CONTEXT 0 registers can be set either in SW_STANDBY or STREAMING state.

Table 51. CONTEXT 0 registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x044C	EXP_MODE	MODE	1:0	C	0x2	Exposure mode control 0x0: AUTO automatic mode 0x1: FREEZE Freeze AE with current settings 0x2: MANUAL manual settings mode
0x044D	MANUAL_ANALOG_GAIN	VALUE	4:0	C	0x0	0x00: AnalogGain_AGAIN_1 0x01: AnalogGain_AGAIN_1_03 0x02: AnalogGain_AGAIN_1_07 0x03: AnalogGain_AGAIN_1_1 0x04: AnalogGain_AGAIN_1_14 0x05: AnalogGain_AGAIN_1_19 0x06: AnalogGain_AGAIN_1_23 0x07: AnalogGain_AGAIN_1_28 0x08: AnalogGain_AGAIN_1_33 0x09: AnalogGain_AGAIN_1_39 0x0A: AnalogGain_AGAIN_1_45 0x0B: AnalogGain_AGAIN_1_52 0x0C: AnalogGain_AGAIN_1_6 0x0D: AnalogGain_AGAIN_1_68 0x0E: AnalogGain_AGAIN_1_78 0x0F: AnalogGain_AGAIN_1_88 0x10: AnalogGain_AGAIN_2 0x11: AnalogGain_AGAIN_2_13 0x12: AnalogGain_AGAIN_2_29 0x13: AnalogGain_AGAIN_2_46 0x14: AnalogGain_AGAIN_2_67 0x15: AnalogGain_AGAIN_2_91 0x16: AnalogGain_AGAIN_3_2 0x17: AnalogGain_AGAIN_3_56 0x18: AnalogGain_AGAIN_4
0x044E	MANUAL_COARSE_EXPOSURE	VALUE	15:0	UI	0x32	Coarse exposure time in line
0x0450	MANUAL_DIGITAL_GAIN	INTEGER	12:8	UI	0x1	Digital gain (integer part) for Channel 0 in manual mode
		FRACT	7:0	UI	0x00	Digital gain (fractional part) for Channel 0 in manual mode
0x0458	FRAME_LENGTH	VALUE	15:0	UI	0x2c8	Length of the frame including blanking in lines
0x045A	Y_START	VALUE	15:0	UI	0	Y start for image output
0x045C	Y_END	VALUE	15:0	UI	0x25b	Y end for image output
0x045E	OUT_ROI_X_START	VALUE	15:0	UI	0x0	Crop/ROI X start

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0460	OUT_ROI_X_END	VALUE	15:0	UI	0x283	Crop/ROI X size
0x0462	OUT_ROI_Y_START	VALUE	15:0	UI	0x0	Crop/ROI Y start
0x0464	OUT_ROI_Y_END	VALUE	15:0	UI	0x25b	Crop/ROI Y size
0x0467	GPIO_0_CTRL	Polarity	5	C	0x0	Polarity_Value: 0x0: NO_INVERSION 0x1: INVERTED
		VALUE	4	UI	0x0	GPIO_VALUE: 0x0: GPIO_LOW 0x1: GPIO_HIGH
		Mode	3:0	C	0x1	GPIO mode: 0x0: RESERVED 0x1: GPIO_IN 0x2: STROBE_MODE 0x3: PWM_STROBE 0x4: PWM 0x5: GPIO_OUT 0x6: VSYNC_OUT_MODE0 0x7: VSYNC_OUT_MODE1 0x8: VSYNC_OUT_MODE2 0xA: VT_SLAVE_MODE
0x0468	GPIO_1_CTRL	Polarity	5	C	0x0	Polarity_Value: 0x0: NO_INVERSION 0x1: INVERTED
		VALUE	4	UI	0x0	GPIO_VALUE: 0x0: GPIO_LOW 0x1: GPIO_HIGH
		Mode	3:0	C	0x2	GPIO mode: 0x0: RESERVED 0x1: GPIO_IN 0x2: STROBE_MODE 0x3: PWM_STROBE 0x4: PWM 0x5: GPIO_OUT 0x6: VSYNC_OUT_MODE0 0x7: VSYNC_OUT_MODE1 0x8: VSYNC_OUT_MODE2
0x0469	GPIO_2_CTRL	Polarity	5	C	0x0	Polarity_Value: 0x0: NO_INVERSION 0x1: INVERTED
		VALUE	4	UI	0x0	GPIO_VALUE: 0x0: GPIO_LOW 0x1: GPIO_HIGH
		Mode	3:0	C	0x6	GPIO mode:

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0469	GPIO_2_CTRL					0x0: RESERVED 0x1: GPIO_IN 0x2: STROBE_MODE 0x3: PWM_STROBE 0x4: PWM 0x5: GPIO_OUT 0x6: VSYNC_OUT_MODE0 0x7: VSYNC_OUT_MODE1 0x8: VSYNC_OUT_MODE2
0x046A	GPIO_3_CTRL	Polarity	5	C	0x0	Polarity_Value: 0: NO_INVERSION 1: INVERTED
		VALUE	4	UI	0x0	GPIO_VALUE: 0: GPIO_LOW 1: GPIO_HIGH
		Mode	3:0	C	0x2	GPIO mode: 0x0: RESERVED 0x1: GPIO_IN 0x2: STROBE_MODE 0x3: PWM_STROBE 0x4: PWM 0x5: GPIO_OUT 0x6: VSYNC_OUT_MODE0 0x7: VSYNC_OUT_MODE1 0x8: VSYNC_OUT_MODE2
0x046B	VSYNC_START_DELAY	DELAY_L	7:0	SI	0x0	Signed value of delay to apply in line
0x046C	VSYNC_END_DELAY	DELAY_L	7:0	SI	0x0	Signed value of delay to apply in line
0x046D	STROBE_START_DELAY	DELAY_L	7:0	SI	0x0	Signed value of delay to apply in line
0x046E	STROBE_END_DELAY	DELAY_L	7:0	SI	0x0	Signed value of delay to apply in line
0x0470	PWM_CTRL	CLkDivisor	31:16	UI	0x64	No. of pulses to be sent out
		DutyCycle	3:0	UI	0x7	Duty cycle in percentage
0x0474	WAIT_DELAY	VALUE	15:0	UI	0x0	Wait time before the next frame in addition to blanking in line
0x0476	CONTEXT_REPEAT_COUNT	VALUE	15:0	UI	0x0	Number of frames per context
0x0478	NEXT_CONTEXT	VALUE	15:0	UI	0x1	Next context target, if > 3 STOP_STREAMING occurs after repeat count
0x047A	READOUT_CTRL	CFG	2:0	C	0x0	STREAMINF readout mode control: 0x0: NORMAL normal STREAMING 0x1: DBIN_X2 digital binning x2 0x2: DBIN_X4 digital binning x4 0x3: SSAMP_X2 subsampling x2 0x4: SSAMP_X4 subsampling x4

19.7 NVM MIRROR registers

Register group range: 0x0640 to 0x0738

Table 52. NVM MIRROR registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x0640	RESERVED 0	VALUE	31:0	UI	0x00	First reserved word
0x06b4	LAST RESERVED	VALUE	31:0	UI	0x00	Last reserved word
0x06b8	CUSTOMER_WORD_0	VALUE	31:0	UI	0x00	First word available for customer
0x0708	CUSTOMER_WORD_20	VALUE	31:0	UI	0x00	—
0x070c	I2C_ADDRESS	I2C_KEY	31:24	UI	0x00	Security key
		I2C_DEVICEID_2	22:16			Device I²C address
		I2C_DEVICEID_1	14:8			
		I2C_DEVICEID_0	6:0			
0x0710	CUSTOMER_WORD_21	VALUE	31:0	UI	0x00	—
0x0738	CUSTOMER_WORD_31	VALUE	31:0	UI	0x00	Last word available for customer

19.8 Miscellaneous registers

Register group range: 0x93a to 0x957

The miscellaneous registers must be set in SW_STANDBY state.

Table 53. Miscellaneous registers

Register address	Register name	Field name	Bits	Data type	Default	Values
0x093A	DPHYTX_CTRL	VALUE	7:0	C	0x18	0x08: Disable Continuous mode 0x18: Enable Continuous mode
0x094E	FULL_READ_OFFSET	VALUE	15:0	UI	0x12	READOUT OFFSET
0x0950	FULL_READ_OFFSET_9BIT	VALUE	15:0	UI	0x12	READOUT OFFSET
0x0957	LOW_POWER_MODE	ENABLE	7:0	C	0x0	0x0: Disable 0x5: Full Low power mode
0x095c	MINIMUM_EXPOSURE_10BIT	VALUE	15:0	UI	0x9	Set manual minimum exposure limit in ADC 10 bits
0x095e	MINIMUM_EXPOSURE_9BIT	VALUE	15:0	UI	0xa	Set manual minimum exposure limit in ADC 9 bits
0x096c	MAX_EXPOSURE_LINES	VALUE	15:0	UI	0x7fe8	Set manual maximum exposure limit
0x0942	MAX_DG	VALUE	15:0	UI	0x0800	Set manual maximum digital gain limit
0x0944	MAX_AG_CODED	VALUE	7:0	UI	0x18	Set manual maximum analog gain coded limit (see MANUAL_ANALOG_GAIN LUT)
0x0970	USER_VT_VERSION	VALUE	1:0	C	0x0	0x0: Long exposure mode 0x1: Short exposure mode

Revision history

Table 54. **Document revision history**

Date	Version	Changes
21-May-2021	1	Initial release
07-May-2024	2	First public release Modified the read offset default values in Section 13.5: Frame rate. Updated Section 16.3: Status lines Modified DARKCAL_PEDESTAL register address in Section 19.5: DYNAMIC registers. Added MAX_DG and MAX_AG_CODED to Section 19.8: Miscellaneous registers.

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