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## STNRG012: How to set Non-Volatile Memory (NVM) parameters

### Introduction

This user manual provides information for developing applications with the STNRG012 digital combo multi-mode PFC and time shift LLC resonant controller.

The STNRG012 is an STMicroelectronics® digital device tailored for SMPS applications in which input DC management is required. It embodies a multi-mode (transition mode and DCM) PFC controller, a high voltage double-ended controller for the LLC resonant half-bridge, an 800 V-rated start-up generator and a sophisticated digital engine, that manages optimal operation of the three blocks.

All the key application parameters of the device are stored in an internal NVM (non-volatile memory), allowing wide configurability and calibration.

This user manual details all the NVM parameters and explains how to set them in a real application. For any other information about the STNRG012 product, please refer to the STNRG012 datasheet.

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## 1 Notes

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### 1.1 Parameters packing

The parameters in the NVM are packed starting from the first one at the address 0x00, going through to the boundaries between bytes if required.

### 1.2 NVM configuration

The NVM is divided into 4 parts called bank0, bank1, bank2 and bank3. Each bank size is 8 bytes:

- Bank0 contains mainly trimming and traceability information. For this reason, users cannot modify it.
- Bank1, 2 and 3 contain the parameters described in this document. The user can modify them to adapt the STNRG012 algorithms to its application.

### 1.3 GUI application

In order to easily program the NVM during the development of a new application, a graphical user interface (GUI) has been developed. The GUI works strictly with a communication interface board and allows real-time monitoring of the device as well as NVM and EEPROM content checking and programming. For more information about the GUI and the interface board, please refer to the UM2342 - user manual: Getting started with the STEVAL-PCC020V1: USB to I<sup>2</sup>C UART interface board and associated GUI for STNRG products.

## 2 Equations to set the parameters

### 2.1 PFC

#### 2.1.1 PFC power calculation

The device uses an internal numerical representation of the power delivered. The relationship between the internal value and the true power is as follows:

$$p_{inn} = P \frac{L}{128 \cdot LSBVin^2 \cdot Tck} \quad (1)$$

where:

- $p_{inn}$  is the internal numerical power estimation
- $P$  is the real power level
- $L$  is the PFC choke inductance value
- $LSBVin = 1.89$  V
- $Tck = 16.66$  ns

Note that this relation is a loose approximation due to the PFC parasitics, which offset the true power level.

#### 2.1.2 PFC compensation parameters

The PFC compensation is calculated at each line valley (i.e. input mains zero crossing). The device uses the following formula to calculate the power:

$$p_{inn} = \left( 2 \cdot Kp + Ki \frac{1}{1-z^{-1}} \right) err \quad (2)$$

where  $err$  is equal to the voltage error (target output voltage - real output voltage) divided by  $Verr_{LSB} = 0.473$  V (in case standard bulk partitioning resistors are used).

### 2.2 LLC

The LLC compensation is based on analog circuitry at the secondary side.

The time shift value applied by the controller is calculated using the sampled value on the LLC\_FB pin.

$$TS = K \cdot \left( \frac{V_{FB}}{LSBV_{FB}} - FBos \right) \quad (3)$$

where:

- $TS$  = time shift value applied to LLC SMEDs (in 60 MHz clock ticks)
- $K$  is a coefficient that changes according to the LLC switching frequency range used (see [Section 3.4.1 LLC low frequency range](#))
  - $K = 0.5$  for standard range
  - $K = 1$  for low frequency range
- $V_{FB}$  = voltage on the LLC\_FB pin
- $LSBV_{FB} = 2.44$  mV (used to convert the LLC\_FB voltage value in the internal numerical format)
- $FBos$  = fixed offset (68)

## 3 Parameters description

### 3.1 General system configuration

#### 3.1.1 Shutdown feature

Size: 1 bit

Enables / disables the shutdown comparator connected to the LLC\_FB pin.

Available values are:

- . Disabled
- . Enabled

The shutdown comparator is connected to the LLC\_FB pin. Its threshold is 125 mV. If the pin is brought below this threshold and the comparator is enabled, then the system shuts down as long as the pin voltage remains below this threshold.

This feature can be used to realize extra protection (e.g. OTP protection for power stage).

#### Use

It is suggested to disable the feature if the shutdown comparator is not used.

#### 3.1.2 Non latched faults timer

Size: 2 bits

Sets the time between retries in the non-latched (auto restart) mode.

Available values are:

- . 546 ms
- . 1.09 s
- . 2.18 s
- . 4.37 s

#### 3.1.3 ATE mode

Size: 1 bit

Enables / disables the ATE mode.

Available values are:

- . Enabled
- . Disabled

#### Use

ATE mode is required to read / write the NVM. Therefore, this parameter should be set to "Enabled".

In case, after the correct programming of all NVM parameters, the user wants to keep such information protected, they can disable the ATE mode.

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**Warning:** *Once the bit is set to disabled, it is impossible to access the NVM.*

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### 3.1.4 Patch upload from EEPROM

Size: 1 bit

Enables / disables the patching feature.

Available values are:

- . Disabled
- . Enabled

If patching is disabled, the STNRG012 does not upload the patch from the external EEPROM.

#### Use

The default value is enabled (i.e. patching enabled). The user has to disable the patching feature if no EEPROM is installed on the application.

### 3.1.5 System monitoring

Size: 1 bit

Enables / disables the system monitoring.

Available values are:

- . Enabled
- . Disabled

Monitoring is the periodic unidirectional communication through the UART interface used by the STNRG012 to send out information (including the power estimation, PFC operating mode, etc.). If this feature is not requested, the user can disable it.

### 3.1.6 VAC reading improvement

Size: 1 bit

Enables / disables the VAC reading improvement feature.

Available values are:

- . Disabled
- . Enabled

If the feature is enabled, the IC sinks from the VAC pin  $I_{VAC\_HV\_SINK}$  current during line synchronization at the startup and  $I_{XCD}$  current for about 3 ms in case of the brownout event, to avoid false brown-in. This ensures that voltage on the VAC/VDC pin has a regular waveform and compensates for the effect of an unbalanced Y-cap on the AC input (such unbalance generates a charge pump effect that increases the VAC voltage).

#### Use

It is suggested to keep the feature enabled.

## 3.2 Faults parameters

### 3.2.1 LLC OVP detection

Size: 1 bit

Enables / disables the LLC OVP comparator.

Available values are:

. Disabled

. Enabled

The LLC OVP comparator is connected to the LLC\_AUX pin and its threshold is 2.5 V.

### 3.2.2 Surge detection

Size: 1 bit

Enables / disables the surge comparator.

Available values are:

. Disabled

. Enabled

The surge comparator is connected to the VAC pin and its threshold is 430 V.

### 3.2.3 PFC OC2 detection

Size: 1 bit

Enables / disables the PFC OC2 comparator.

Available values are:

. Disabled

. Enabled

The PFC OC2 comparator is connected to the PFC\_CS pin and its threshold is 900 mV.

### 3.2.4 Max number of PFC OC2

Size: 2 bits

Sets the number of consecutive PFC OC2 events before shutting down.

Available values are:

. 1

. 2

. 3

. 4

**Use**

The suggested value is “2”, since it is a good compromise between the noise rejection and protection reactivity.

The value “1” can be used if minimum intervention time is required; in this case, be aware that noise could trigger the protection.

Higher values can be used in case of noisy boards (in this case, the reaction to real OCP2 events is slower).

**3.2.5 LLC OC2 detection**

Size: 1 bit

Enables / disables the LLC OC2 comparator.

Available values are:

- . Disabled
- . Enabled

The LLC OC2 comparator is connected to the LLC\_CS pin and its threshold is 700 mV.

**3.2.6 Max number of LLC OC2**

Size: 2 bits

Sets the number of consecutive LLC OC2 events before shutting down.

Available values are:

- . 1
- . 2
- . 4
- . 8

**Use**

The suggested value is “2”, since it is a good compromise between the noise rejection and protection reactivity.

The value “1” can be used if minimum intervention time is required; in this case, pay attention because some noise could trigger the protection.

**3.2.7 PFC HW OVP detection**

Size: 1 bit

Enables / disables the hardware PFC OVP comparator.

Available values are:

- . Disabled
- . Enabled

The PFC OVP comparator is the hardware protection against bulk overvoltage. It is connected to the PFC\_FB pin and its threshold is set at 2.3 V.

If the PFC HW OVP protection is triggered during the running state of the PFC, the device turns off the PFC until the next line valley. The device shuts down for PFC HW OVP (not latched fault) only if each of the following three conditions are triggered:

- the PFC\_OVP HW comparator is triggered during the PFC startup

- the feedback disconnection faults are enabled
- PFC\_CS comparator is not triggered during PFC start-up phase

Please consider that in all other cases the device does not enter fault state so the half-bridge input voltage could be higher than the PFC\_OVP HW threshold with the output still in regulation.

**Use**

It is suggested to leave the PFC OVP comparator enabled.

### 3.2.8 Disconnection faults detection

Size: 1 bit

Enables / disables the feedback disconnection faults detection.

Available values are:

- . Disabled
- . Enabled

**Use**

It is suggested to enable the feedback disconnection faults detection.

*Note:* Disconnection faults have always “latched” behavior with the exception of LLC\_CS disconnection.

### 3.2.9 PFC OC2 behavior

Size: 1 bit

Sets the behavior of PFC OC2 protection.

Available values are:

- . Not latched
- . Latched

If the fault is set as “Not latched” the system tries to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity remains off and the  $V_{CC}$  remains between 15 V and 17 V using the HV start-up generator (as long as the mains is connected).

### 3.2.10 PFC UVP behavior

Size: 1 bit

Sets the behavior of the PFC UVP.

Available values are:

- . RESERVED
- . Immediate

The PFC UVP shall be set to “Immediate”: the device shuts down the power supply if the PFC UVP is triggered. In this case the un-latch timer depends on the NVM parameter PFC UVP auto-restart timer (see 3.2.11).

Please remember that because of the LLC OC2 protection and the ACP feature that the system is still protected against overstresses.



### 3.2.11 PFC UVP auto-restart timer

Size: 1 bit

Sets the auto-restart timer of the PFC UVP in case the fault is triggered during LLC running phase (i.e. not at soft-start phase, ACP phase and burst phase).

Available values are:

- . Non latched faults timer (see 3.1.2)
- . 100 ms

In case the PFC UVP is not triggered during LLC running phase the auto-restart timer is the non latched fault timer (see 3.1.2).

### 3.2.12 LLC SS timeout behavior

Size: 1 bit

Sets the behavior of the LLC soft-start timeout protection.

Available values are:

- . Not latched
- . Latched

If the fault is set as “Not latched” the system tries to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity remains off and the  $V_{CC}$  remains between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

### 3.2.13 LLC ACP behavior

Size: 1 bit

Sets the behavior of the LLC ACP (both “Soft” and “Hard”).

Available values are:

- . Not latched
- . Latched

If the fault is set as “Not latched” the system tries to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity remains off and the  $V_{CC}$  remains between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

### 3.2.14 LLC OC2 behavior

Size: 1 bit

Sets the behavior of the LLC OC2 protection.

Available values are:

- . Not latched
- . Latched

If the fault is set as “Not latched” the system tries to restart after the time defined by the “Non latched faults timer” parameter.

If the fault is set as “Latched” the switching activity remains off and the  $V_{CC}$  remains between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

### 3.2.15 LLC OLP behavior

Size: 1 bit

Sets the behavior of the LLC overload protection (OLP).

Available values are:

- . Not latched
- . Latched

If the fault is set as “Not latched” the system tries to restart after the time defined by the “Non latched faults timer”.

If the fault is set as “Latched” the switching activity remains off and the  $V_{CC}$  remains between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

### 3.2.16 LLC OVP behavior

Size: 1 bit

Sets the behavior of the LLC OVP.

Available values are:

- . Not latched
- . Latched

If the fault is set as “Not latched” the system tries to restart after about 34 ms.

If the fault is set as “Latched” the switching activity remains off and the  $V_{CC}$  remains between 15 V and 17 V using the HV start-up generator (as long as there is the mains connected).

### 3.3 PFC parameters

#### 3.3.1 PFC Ki

Size: 3 bits

Sets the integral constant of the PFC compensation filter.

Available values are:

. 4  
. 6  
. 8  
. 12  
. 16  
. 24  
. 32  
. 48

#### 3.3.2 PFC Kp

Size: 3 bits

Sets the proportional constant of the PFC compensation filter.

Available values are:

. 8  
. 12  
. 16  
. 24  
. 32  
. 48  
. 64  
. 96

*Note:* The device uses  $2 * Kp$  for calculations (see Section 2.1.2 ,PFC compensation parameters).

#### 3.3.3 PFC boost exiting burst

Size: 1 bit

Enables / disables the PFC improved dynamic response exiting burst mode.

Available values are:

. Disabled  
. Enabled

#### Use

This feature prevents bulk voltage undershoots in the case of a high load transient from the burst mode.

It is suggested to disable or enable the PFC SW OVP if the feature is disabled or enabled (see Section 3.3.22 PFC SW OVP threshold (delta) for details).

### 3.3.4 PFC MOSFET LEB

Size: 2 bits

Sets the PFC MOSFET minimum on-time (also called LEB, i.e. "Leading Edge Blanking").

Available values are:

- . 133 ns
- . 200 ns
- . 267 ns
- . 400 ns

This time is used to filter the spike on the PFC\_CS pin at the PFC MOSFET turn-on. During this time the PFC\_CS comparator output (THD improver) is ignored.

#### Use

Adjust the blanking time according to design requirements.

The middle value 267 ns can be used as a starting point and then, after looking at the PFC\_CS waveform during the PFC operation, it can be adjusted.

### 3.3.5 PFC THD improver base

Size: 3 bits

Sets the base value for the ReCOT functionality (THD improver).

Available values are:

- . 0 mV
- . 2 mV
- . 4 mV
- . 6 mV
- . 8 mV
- . 10 mV
- . 12 mV
- . 14 mV

The parameter sets the PFC\_CS comparator threshold.

#### Use

This parameter can be tuned to improve the THD of the system. Together with the "PFC THD improver gain", this parameter can be used to improve the distortion and power factor of the PFC observing the current waveform and THD/PF measurements.

If "THD optimizer" is enabled the suggestion is to decrement by 1 the "PFC THD improver base".

### 3.3.6 PFC THD optimizer

Size: 1 bit

Enables / disables the PFC THD optimizer algorithm (see 3.3.7, PFC THD improver gain for details).

Available values are:

- . Disabled
- . Enabled

### 3.3.7 PFC THD improver gain

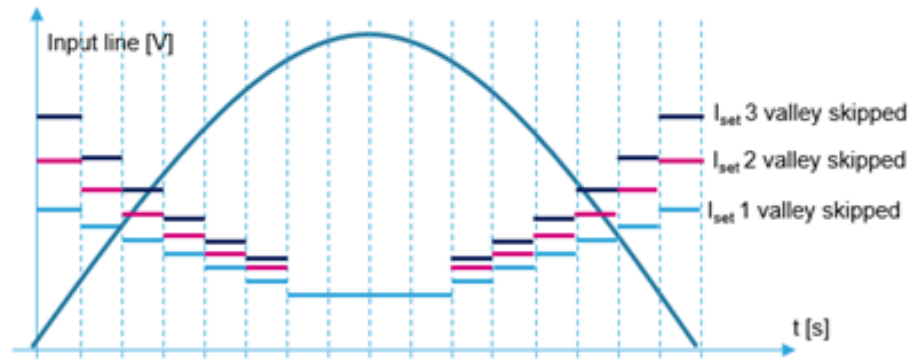
Size: 3 bits

If the THD optimizer is disabled, this parameter sets the slope of the ReCOT functionality (THD improver) to compensate for the current in the input capacitors.

If the THD optimizer is enabled, this parameter sets the parameter for the THD optimizer algorithm.

The standard eCOT uses the same current threshold (THD improver base parameter) during all the half-cycle. The solution modifies the current threshold during the half-cycle. In particular, the THD optimizer algorithm increases the current level near the valley and decreases near the peak. Moreover, the modulation emphasizes increasing the valleys skipped. The algorithm is used in DCM too.

Figure 1. THD Optimizer algorithm example



Available values for THD optimizer disable are:

- . 0 - gain disabled
- . 1
- . 2
- . 3
- . 4
- . 5
- . 6
- . 7

The threshold level difference between the beginning and the end of the line cycle is:

$$V_{ramp} = \frac{igain \cdot \sqrt{2} V_{in} \cdot 3 \cdot 9mV}{256 \cdot 484.5V / 256} \quad (4)$$

i.e.

$$V_{ramp} = igain \cdot V_{in} \cdot 11.38 \cdot 10^{-6} \quad (5)$$

Which acts as a negative capacitance of the value

$$C_{neg} = 2 \cdot 10^{-6} \frac{gain}{\pi f_{line} R_{sense}} \quad (6)$$

**Use** – THD optimizer disabled

Together with the “PFC THD improver base”, this parameter can be used to improve the distortion and power factor of the PFC.

The value can be initially calculated with Eq. (6) to compensate for the capacitance at the PFC input and EMI filter and then tune it by observing the current waveform at the converter input and THD/PF measurements to find the optimum point.

**Use** – THD optimizer enabled

Together with the “PFC THD improver base” and “THD optimizer”, this parameter can be used to improve the distortion of the PFC over all the range.

We suggest tuning this parameter starting from 0 to 7.

### 3.3.8 PFC maximum power

Size: 5 bits

Sets the upper clamp of the PI filter, i.e. the maximum power that the PFC can provide.

Available values are:

·4096	· 8192
·4352	· 8704
·4608	· 9216
·4864	· 9728
·5120	·10240
·5376	·10752
·5632	·11264
·5888	·11776
·6144	·12288
·6400	·12800
·6656	·13312
·6912	·13824
·7168	·14336
·7424	·14848
·7680	·15360
·7936	·15872

#### Use

Select a value higher than the nominal power, in order to be able to respond to transients.

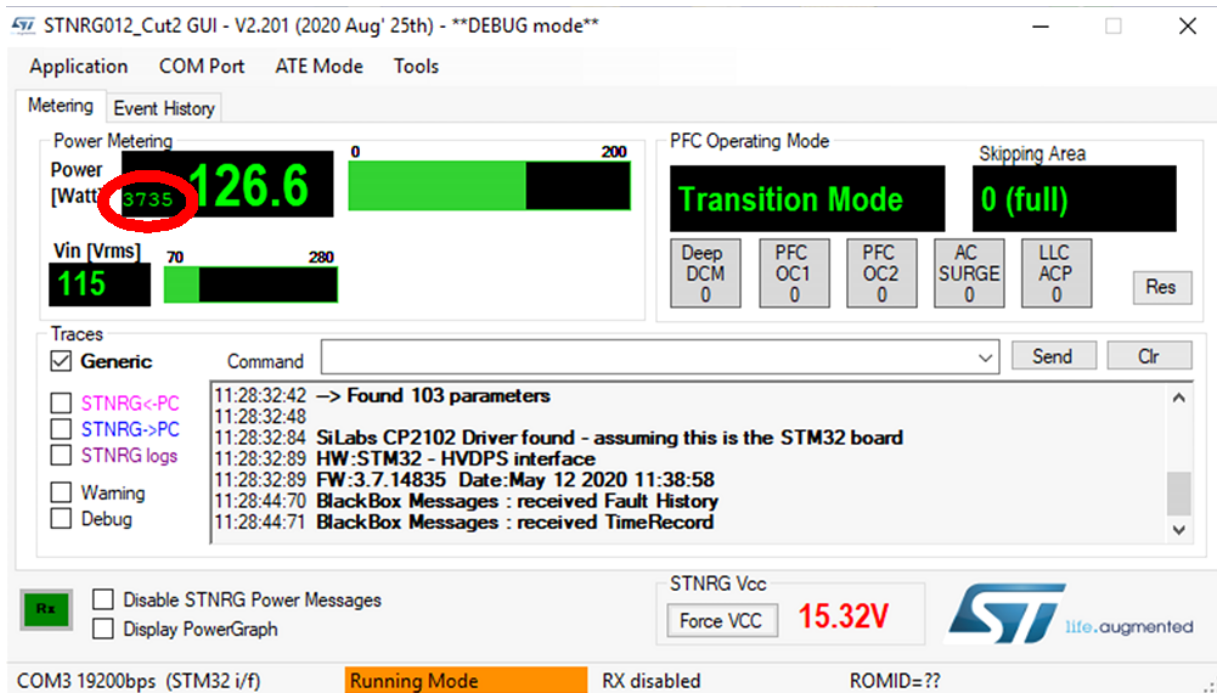
To initially set up this value, set it to twice the maximum power estimation using [Section 2.1.1 PFC power calculation](#).

Then fine-tune it by:

- Turning on the board with the maximum load
- Reading the input power raw value using the GUI (see [Fig. 2](#) for details)
- Setting the parameter to input power raw value + 30%

The value can be further adjusted by looking at the PFC stage transient response.

Figure 2. STNRG012 GUI; circled in red the raw value of the input power



### 3.3.9 PFC pss

Size: 3 bits

Sets the PFC power during the soft-start.

Available values are:

- . 640
- . 1280
- . 1920
- . 2560
- . 3200
- . 3840
- . 4480
- . 5120

The higher the value, the higher the on-time of the PFC MOSFET during the soft-start phase.

#### Use

Choose the value that allows reaching the required PFC soft-start time.

The faster the soft-start time required, the higher the PFC current is.

Using a high value can lead to overshoots (the bulk voltage increases at every line cycle).



### 3.3.10 PFC pcc

Size: 2 bits

Sets the PFC reference power during burst mode operation.

Available values are:

- 3218
- 5558
- 7898
- 10238

The higher the value, the higher the maximum on-time of the PFC MOSFET during the burst mode operation. This means that the transferred power is also higher.

The algorithm adjusts the on-time of the PFC MOSFET according to the required power, in order to reduce the acoustic noise.

#### Use

Select the lowest value that allows correct bulk voltage regulation at the no-load and minimum AC voltage condition.

### 3.3.11 PFC min pin vskip

Size: 5 bits

Sets the internal power threshold at which the mode is changed towards DCM (i.e. one more valley is skipped).

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
· 1280	· 2304
· 1344	· 2368
· 1408	· 2432
· 1472	· 2496
· 1536	· 2560
· 1600	· 2624
· 1664	· 2688
· 1728	· 2752
· 1792	· 2816
· 1856	· 2880
· 1920	· 2944
· 1984	· 3008
· 2048	· 3072
· 2112	· 3136
· 2176	· 3200
· 2240	· 3264

**Use**

This parameter is mainly used to guarantee a fast reaction to transients, forcing the PFC to increase the number of valleys or to switch to DCM when the internal power value plus nValleys \* "PFC Delta Pin Vskip" is lower than this parameter.

The frequency based mode change measures the frequency at each half-line cycle, then, if the frequency is out of the "PFC Min Tsw Vskip" or "PFC Max Tsw Vskip" value range, it increments or decrements the number of valleys by one. By only relying on the frequency it would require 4 half-line cycles to change from TM to DCM, potentially causing an overshoot on the Vbus.

The threshold should be kept low enough so that in steady-state the frequency dominates the mode change.

**3.3.12 PFC max pin vskip (delta)**

Size: 5 bits

Sets the internal power threshold at which the mode is changed toward TM (i.e. one less valley is skipped).

Available values are:

"LLC low frequency range" = disabled	"LLC low frequency range" = enabled
·1280	·3328
·1408	·3456
·1536	·3584
·1664	·3712
·1792	·3840
·1920	·3968
·2048	·4096
·2176	·4224
·2304	·4352
·2432	·4480
·2560	·4608
·2688	·4736
·2816	·4864
·2944	·4992
·3072	·5120
·3200	·5248

The parameter in the NVM is a positive delta with respect to the "PFC Min Tsw Vskip". The real value used during the code execution is therefore

$$"PFC Max Pin Vskip" = "PFC Min Pin Vskip" + "PFC Max Pin Vskip (delta)" \tag{7}$$

**Use**

This parameter is mainly used to guarantee a fast reaction to transients, forcing the PFC to reduce the number of valleys or to switch to the transition mode when the internal power value plus nValleys \* "PFC Delta Pin Vskip" is greater than this parameter.

The frequency based mode change measures the frequency at each half-line cycle, then, if the frequency is out of the "PFC Min Tsw Vskip" or "PFC Max Tsw Vskip" values, it increments or decrements the number of valleys by one. By only relying on frequency it would require 4 half-line cycles to change from DCM to TM, potentially causing a dip on the Vbus.

The threshold should be kept high enough so that in the steady-state the frequency dominates the mode change.

### 3.3.13 PFC delta pin vskip

Size: 5 bits

Sets a correction factor used when switching between valley-skipping modes.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
·160	· 416
·176	· 432
·192	· 448
·208	· 464
·224	·480
·240	·496
·252	·512
·272	·528
·288	·544
·304	·560
·320	·576
·336	·592
·352	·608
·368	·624
·384	·640
·400	·656

#### Use

This parameter should be approximately set to the reduction of output power determined by the addition of one valley.

The device uses this parameter to reduce the discontinuity on the output power when changing the number of valleys skipped.

### 3.3.14 PFC maximum DCM power

Size: 5 bits

Sets the power threshold to switch from the DCM to the valley-skipping mode. Sets also the on-time duration of the PFC gate drive while in the DCM mode.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
·1024	· 2560
·1088	· 2816
·1152	· 3072
·1216	· 3328
·1280	·3584
·1344	·3840
·1408	·4096
·1472	·4352
·1536	·4608
·1664	·5120
·1792	·5632
·1920	·6144
·2048	·6656
·2176	·7168
·2304	·7680
·2432	·8192

In DCM mode, the MOSFET on-time is calculated with the following formula:

$$T_{on} = \frac{\text{"PFC Maximum DCM power"} \cdot 2}{V_{in}^2} \quad (8)$$

### 3.3.15 PFC min tsw VSKIP

Size: 5 bits

Sets the minimum switching period (i.e. the maximum switching frequency) for the valley-skipping mode.

Available values are:

·234 kHz	·117 kHz
·221 kHz	·110 kHz
·208 kHz	·104 kHz
·197 kHz	·99 kHz
·188 kHz	·94 kHz
·179 kHz	·89 kHz
·170 kHz	·85 kHz
·163 kHz	·82 kHz
·156 kHz	·78 kHz
·150 kHz	·75 kHz
·144 kHz	·72 kHz
·139 kHz	·69 kHz
·134 kHz	·67 kHz
·129 kHz	·65 kHz
·125 kHz	·63 kHz
·121 kHz	·60 kHz

The period is measured at the peak of the mains sinusoidal voltage. If the measured period is lower than this value, the system increases the number of valleys, towards DCM.

The corresponding frequency values are shown above.

#### Use

This value, together with the "PFC Max Tsw Vskip", is used to set the range of PFC switching frequency; therefore, it is important to optimize the efficiency of the PFC.

The max. value should be at least 1.5 times the min. value to avoid the system continuously switching between different modes.

### 3.3.16 PFC max tsw vskip

Size: 5 bits

Sets the maximum switching period (i.e. the minimum switching frequency) for the valley-skipping mode.

Available values are:

·101 kHz	·54 kHz
·96 kHz	·51 kHz
·91 kHz	·49 kHz
·87 kHz	·46 kHz
·83 kHz	·44 kHz
·80 kHz	·42 kHz
·77 kHz	·40 kHz
·74 kHz	·39 kHz
·71 kHz	·37 kHz
·68 kHz	·36 kHz
·66 kHz	·34 kHz
·64 kHz	·33 kHz
·61 kHz	·32 kHz
·60 kHz	·31 kHz
·58 kHz	·30 kHz
·56 kHz	·29 kHz

The period is measured at the peak of the mains sinusoidal voltage. If the measured period is higher than this value, the system decreases the number of valleys, towards TM.

The corresponding frequency values are shown above.

#### Use

This value, together with the “PFC Min Tsw Vskip”, is used to set the range of PFC switching frequency; therefore, it is important to optimize the efficiency of the PFC.

The max. value should be at least 1.5 times the min. value to avoid the system continuously switching between different modes.

Please note that PFC Max Tsw Vskip and PFC Min Tsw Vskip are used only for AC input voltage below 245 Vac (if PFC High Voltage Range is set to 0), or AC input voltage below 290 Vac (if PFC High Voltage Range is set to 1).

### 3.3.17 Skipping area setting

Size: 3 bits

Sets the allowed skipping area levels and, consequently, the power level at which the PFC starts reducing the conduction phase to a part of the AC line half-cycle (skipping area feature).

Available values are:

- . 0 Skipping area enabled level from 1 to 6 (6 is the deepest skipping area level)
- . 1 Skipping area enabled level from 2 to 6
- . 2 Skipping area enabled level from 3 to 6
- . 3 Skipping area enabled level from 4 to 6
- . 4 Skipping area enabled level from 5 to 6
- . 5 Skipping area enabled level from 6 to 6
- . 6 no skipping area
- . 7 no skipping area

Related skipping area input thresholds:

- . 0 1792
- . 1 1568
- . 2 1288
- . 3 960
- . 4 584
- . 5 320
- . 6 no skipping area
- . 7 no skipping area

#### Use

This parameter can be used to:

- improve efficiency at the power levels at which harmonic contents are not subject to regulation (e.g. below 75 W)
- avoid a high ripple of bulk voltage when working at high mains; it is suggested to set this value to “5” enabling only the lower skipping area level.

It is suggested to keep a 20% margin to take into account variations from unit to unit (e.g. set the threshold to 60 W to assure it is out of this mode at 75 W).

Test the exit point from the skipping area mode at the nominal mains voltages to check that the system returns to the continuous switching mode below 75 W.

Setting this parameter to “7” or “6” disables the skipping area feature, in case good THD and PF are required even at very low loads.

### 3.3.18 PFC high voltage range

Size: 2 bits

Sets the percentage increasing of PFC output voltage.

Available values are:

- . 0 – PFC High Voltage Range disabled
- . 1 – +11%
- . 2 – RESERVED
- . 3 – RESERVED

This is the percentage level to add to the nominal PFC output voltage set by the parameter (see [Section 3.3.19 PFC vout target](#) for details).

#### Use

The parameter at [Section 3.3.19 PFC vout target](#) is set considering the resistor partition value such as the standard application working at 400 V. In case the partition is changed the user should change this parameter as a consequence. If the partition is changed in order to have the nominal voltage at around 444 V the parameter shall be set to 1. Considering the 400 V as reference:

$$. 1 - +11\% \Rightarrow 400V \cdot 1.1 = 444V$$

### 3.3.19 PFC vout target

Size: 3 bits

Sets the nominal PFC output voltage.

Available values are:

- . 1.946 V - 377 V
- . 1.965 V - 381 V
- . 1.985 V - 385 V
- . 2.004 V - 388 V
- . 2.024 V - 392 V
- . 2.063 V - 400 V
- . 2.102 V - 407 V
- . 2.141 V - 415 V

This is the voltage level at which the PFC stage regulates its output, in all operating conditions.

#### Use

Set the PFC output voltage according to the application specs.

The values on the left refer to the PFC\_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio  $k = 5.16 \cdot 10^{-3}$  (i.e. 484.5 V on the bulk voltage corresponds to 2.5 V on the PFC\_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage. In this case, consider that the PFC HW OVP comparator has a fixed threshold of 2.3 V.

### 3.3.20 PFC vout SS end (delta)

Size: 2 bits



Sets the voltage at which the PFC terminates the soft-start and the system begins the LLC soft-start.

Available values are:

- . 19.5 mV - 3.8 V
- . 29.3 mV - 5.7 V
- . 39.1 mV - 7.6 V
- . 58.6 mV - 11.4 V

#### Use

The above values are intended as a negative delta with respect to the “PFC Vout target” parameter.

The PFC soft-start end voltage is therefore:

$$"PFC\ Vout\ SS\ end" = "PFC\ Vout\ target" - "PFC\ Vout\ SS\ end\ (delta)" \quad (9)$$

The values on the left refer to the PFC\_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio  $k = 5.16 \cdot 10^{-3}$  (i.e. 484.5 V on the bulk voltage corresponds to 2.5 V on the PFC\_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage.

### 3.3.21 PFC UVP threshold (delta)

Bits: 3

Sets the UVP level for PFC output voltage.

Available values are:

- . 0.156 V - 30 V
- . 0.234 V - 45 V
- . 0.313 V - 61 V
- . 0.391 V - 76 V
- . 0.469 V - 91 V
- . 0.547 V - 106 V
- . 0.625 V - 121 V
- . 0.703 V - 136 V

#### Use

The above values are intended as a negative delta with respect to the “PFC Vout target” parameter.

In fact, the UVP threshold is defined as

$$"PFC\ UVP\ threshold" = "PFC\ Vout\ target" - "PFC\ UVP\ threshold\ (delta)" \quad (10)$$

The values on the left refer to the PFC\_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio  $k = 5.16 \cdot 10^{-3}$  (i.e. 484.5 V on the bulk voltage corresponds to 2.5 V on the PFC\_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage.

### 3.3.22 PFC SW OVP threshold (delta)

Size: 2 bits

Sets the PFC SW OVP level.

Available values are:

- . 51.3 mV - 10 V
- . 78.1 mV - 15 V
- . 105 mV - 20 V
- . SW OVP disabled

#### Use

The above values are intended as a positive delta with respect to the “PFC Vout target” parameter. In fact, the SW OVP threshold is defined as

$$\text{"PFC SW OVP threshold"} = \text{"PFC Vout target"} - \text{"PFC SW OVP threshold (delta)"} \quad (11)$$

The values on the left refer to the PFC\_FB pin, that corresponds to values on the right if the bulk voltage divider is designed with the standard ratio  $k = 5.16 \cdot 10^{-3}$  (i.e. 484.5 V on the bulk voltage corresponds to 2.5 V on the PFC\_FB pin).

If other bulk voltage dividers are used, the values on the left can be used to set the output voltage.

It is suggested to keep the SW OVP enabled with the maximum value 105 mV - 20 V, especially if the “PFC boost exiting burst” feature is enabled.

## 3.4 LLC parameters

### 3.4.1 LLC low frequency range

Size: 1 bit

Enables / disables the low LLC switching frequency range selection.

Available values are:

- . Enabled
- . Disabled

This parameter is used to select the operating frequency range for the LLC. In more detail, if it is set as disabled the frequency range is the standard one.

In case an application is designed for a low operating switching frequency range, setting this parameter to “Enable” allows using an appropriate range for some of the timing parameters.

#### Use

As a rule of thumb, considering a system designed to work near resonance in nominal condition, if the resonance frequency is greater than 70 kHz the standard range can be used.

In case the resonance frequency is lower than 60 kHz, the low frequency range is suggested.

### 3.4.2 LLC HVG first ton

Size: 4 bits

Sets the total on-time of the first LLC HVG.

Available values are:

- . 133.3 ns
- . 200 ns

- . 266.7 ns
- . 333.3 ns
- . 400 ns
- . 466.7 ns
- . 533.3 ns
- . 600 ns
- . 666.7 ns
- . 800 ns
- . 933.3 ns
- . 1067 ns
- . 1200 ns
- . 1333 ns
- . 1467 ns
- . 1600 ns

At the LLC turn-on, during the safe-start phase, this is the total on-time of the first pulse of the high-side gate drive. Typically, higher values have to be used with high  $L_{lk}$  resonant tanks.

### 3.4.3 LLC LVG first ts

Size: 4 bits

Sets the time shift value of the first LLC LVG.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
.166.7 ns	.333.3 ns
.200 ns	.366.7 ns
.233.3 ns	.400 ns
.266.7 ns	.433.3 ns
.300 ns	.466.7 ns
.333.3 ns	.500 ns
.366.7 ns	.533.3 ns
.400 ns	.566.7 ns
.433.3 ns	.600 ns
.500 ns	.666.7 ns
.566.7 ns	.733.3 ns
.633.3 ns	.800 ns
.700 ns	.866.7 ns
.766.7 ns	.933.3 ns
.833.3 ns	.1000 ns
.900 ns	.1067 ns

This parameter defines the time shift for the first low-side gate drive pulse, during the safe-start.

Such time shift value is then used as the first one for the LLC soft-start.

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

### 3.4.4 LLC deadtime

Size: 2 bits

Sets the LLC half-bridge deadtime.

Available values are:

- . 266.7 ns
- . 333.3 ns
- . 400 ns
- . 466.7 ns

Use this parameter to select the deadtime duration (for both transitions) according to resonant tank needs.

### 3.4.5 LLC soft-start speed

Size: 3 bits

Sets the speed of the LLC soft-start.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
·8.3 ns	·16.7 ns
·16.7 ns	·33.3 ns
·25 ns	·50 ns
·33.3 ns	·66.7 ns
·41.7 ns	·83.3 ns
·50 ns	·100 ns
· 58.3 ns	·117 ns
·66.7 ns	·133 ns

This parameter is the time shift increment applied every 30  $\mu$ s during the LLC soft-start. The smaller the value, the slower the output voltage rise and the LLC tank current.

It is suggested to start with the minimum value (usually OK for most applications) and increase it in case a faster Vout rise time is required.

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

### 3.4.6 Minimum time shift

Size: 4 bits

Sets the minimum value for the time shift during the normal operation.

Available values are:

“LLC low frequency range”

= disabled

- 125 ns
- 158.3 ns
- 191.7 ns
- 225 ns
- 258.3 ns
- 291.7 ns
- 325 ns
- 358.3 ns
- 391.7 ns
- 425 ns
- 458.3 ns
- 491.7 ns
- 525 ns
- 558.3 ns
- 591.7 ns
- 625 ns

“LLC low frequency range”

= enabled

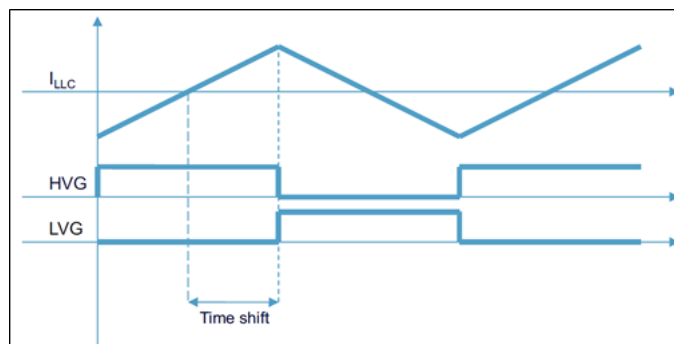
- 250 ns
- 316.7 ns
- 383.3 ns
- 450 ns
- 516.7 ns
- 583.3 ns
- 650 ns
- 716.7 ns
- 783.3 ns
- 850 ns
- 916.7 ns
- 983.3 ns
- 1050 ns
- 1116 ns
- 1183 ns
- 1250 ns

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

**Use**

The minimum time shift value is used to set the maximum LLC switching frequency. The relationship between the time shift and switching period is complex. Anyway, for this limit condition and by looking at Fig. 3 , a good approximation can be found.

Figure 3. LLC operation at  $f_{sw} \gg f_{RES}$



When the operating frequency is much higher than the resonance frequency, the resonant tank current  $I_{LLC}$  becomes a triangular waveform, because the current provided to the secondary side becomes negligible with respect to the magnetizing current.

Approximating the current triangular and neglecting the deadtimes, the time shift value (i.e. the time between zero crossing and MOS turn-off) becomes half of each MOSFET on-time.

Therefore:

$$f_{sw \max} = \frac{1}{4 \cdot (TS_{\min} + ZCD_{\text{delay}})} \tag{12}$$

where  $TS_{\min}$  is the minimum time shift value and  $ZCD_{\text{delay}}$  is the delay given by the ZCD comparator and digital filtering:

$$ZCD_{\text{delay}} = ZCD_{\text{compdel}} + LLC \text{ ZCD comp digital filtering} \quad (13)$$

$ZCD_{\text{compdel}}$  is the comparator delay, estimated in 150 ns. "LLC ZCD comp digital filtering" is the digital filtering of the ZCD comparator.

Even if the deadtimes are not negligible (since we are working at high frequency), the above relationship is still valid if the system is well designed and guarantees the ZVS operation.

### 3.4.7 Maximum time shift

Size: 4 bits

Sets the maximum value for the time shift during the normal operation.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
·3.96 μs	·7.92 μs
·4.22 μs	·8.45 μs
·4.49 μs	·8.98 μs
·4.76 μs	·9.52 μs
·5.02 μs	·10.05 μs
·5.29 μs	·10.58 μs
·5.56 μs	·11.12 μs
·5.82 μs	·11.65 μs
·6.09 μs	·12.18 μs
·6.36 μs	·12.72 μs
·6.62 μs	·13.25 μs
·6.89 μs	·13.78 μs
·7.16 μs	·14.32 μs
·7.42 μs	·14.85 μs
·7.69 μs	·15.38 μs
·7.96 μs	·15.92 μs

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

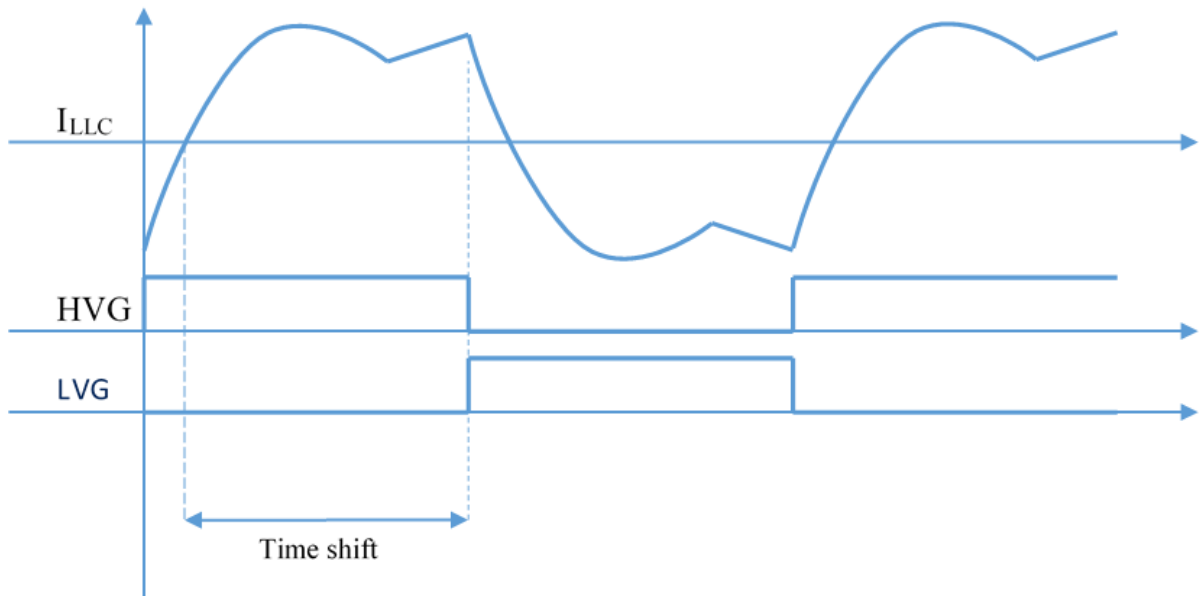
#### Use

The maximum time shift value is used to set the minimum LLC switching frequency. The relationship is not as easy as for the maximum frequency but it is possible to find a simple relationship to set the parameter.



Minimum frequency typically means working in the below resonance region. The key waveform is shown in Fig. 4.

Figure 4. LLC operation at  $f_{SW} < f_{RES}$



Looking at Fig. 4 it is possible to see that, when working below resonance, the time shift duration and the half period become quite similar. As a limit case, when working on the boundary between inductive and capacitive regions, the time shift is exactly half of the switching cycle.

The above information can be used to estimate a first value for the maximum time shift

$$f_{SW\ min} \cong \frac{1}{2 \cdot (TS_{max} + ZCD_{delay})} \quad (14)$$

where  $TS_{max}$  is the maximum time shift value and  $ZCD_{delay}$  is the delay given by the ZCD comparator and digital filtering

$$ZCD_{delay} = ZCD_{comp_{del}} + \text{"LLC ZCD comp digital filtering"} \quad (15)$$

$ZCD_{comp_{del}}$  is the comparator delay, estimated in 150 ns. "LLC ZCD comp digital filtering" is the digital filtering of the ZCD comparator.

This formula can be used to start the design and the value can be fine-tuned at the bench, running the real application prototype.

Remember that the STNRG012 provides anti-capacitive protection (ACP), so, even if the user puts a large value there is no risk of damaging the board components.

### 3.4.8 LLC OLP threshold

Size: 4 bits

Sets the threshold of the LLC OC1 comparator on the LLC\_CS pin for OLP functionality.

Available values are:

- . 23.87 mV
- . 55.61 mV
- . 87.35 mV
- . 119.1 mV
- . 150.84 mV

. 182.58 mV  
 . 214.32 mV  
 . 246.06 mV  
 . 277.81 mV  
 . 309.55 mV  
 . 341.29 mV  
 . 373.03 mV  
 . 404.77 mV  
 . 436.52 mV  
 . 468.26 mV  
 . 500 mV

**Use**

The LLC OC1 comparator is used to manage overload conditions (OLP). This parameter defines the threshold of the current sense level of the application at which the system has to enter the OLP fault, after a timeout defined by the “LLC OLP timeout”.

**3.4.9 LLC OLP timeout**

Size: 2 bits

Sets the duration of the OLP management.

Available values are:

. 10 ms  
 . 200 ms  
 . 400 ms  
 . 1 s

**Use**

The LLC OC1 comparator is used to manage overload conditions (OLP). This parameter defines how long an overload condition can be sustained.

If the load is high enough to continuously trigger the LLC OC1 comparator, set with the “LLC OLP threshold” parameter, the system shuts down after the timeout defined by this parameter.

**3.4.10 ACP sensitivity**

Size: 1 bit

Sets the sensitivity on detection ACP condition.

Available values are:

. Low  
 . High

The ACP sensitivity applies either for hard and soft ACP features. Please note that the accuracy of this parameter depends on the main clock accuracy.

**3.4.11 Hard ACP detection**

Size: 1 bit

Enables / disables the hard ACP detection.

Available values are:

- . Disabled
- . Enabled

Hard ACP is the protection that is triggered when the system reaches the capacitive mode (i.e. the time between the MOSFET turn-on and tank current zero crossing becomes zero or negative). The system immediately shuts down both sections if the fault is triggered.

The fault can be latched or not latched depending on the “LLC ACP behavior”.

*Note: In case the hard ACP detection is disabled, the system doesn't shut down if ACP is sensed during deadtime, but it waits for the correct ZCD sign in order to turn on the next gate-drive*

### 3.4.12 Soft ACP feature

Size: 1 bit

Enables / disables the soft ACP management.

Available values are:

- . Enabled
- . Disabled

Soft ACP is the protection that is triggered when the system is approaching the capacitive mode (i.e. the time between the MOSFET turn-on and tank current zero crossing becomes smaller than the value programmed with the parameter “Soft ACP entering threshold”).

The feature tries to recover the capacitive mode, reducing the LLC time shift value of a quantity defined by the “Soft ACP TS decrement”, every time the protection is triggered, for a maximum number of occurrences of “Maximum soft ACP occurrences”.

Every time the system triggers the soft ACP feature, the STNRG012 moves to the soft-start state, to smoothly stabilize the regulation. It shuts down for the soft ACP fault if the minimum time shift or the maximum number of soft ACP occurrences are reached. The fault can be latched or not latched depending on the “LLC ACP behavior”.

The system shuts down for the soft ACP fault if the minimum time shift or the maximum number of soft ACP occurrences are reached. The fault can be latched or not latched depending on the “LLC ACP behavior”.

### 3.4.13 Soft ACP entering threshold

Size: 3 bits

Sets the time threshold for entering the soft ACP management.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
· 100 ns	· 200 ns
· 167 ns	· 333 ns
· 133 ns	· 267 ns
· 233 ns	· 467 ns
· 300 ns	· 600 ns
· 367 ns	· 733 ns
· 433 ns	· 867 ns
· 567 ns	· 1133 ns

#### Use

If the time between the MOSFET turn-on and LLC ZCD signal becomes lower than the threshold defined by this parameter (i.e. the system is approaching the capacitive mode), the IC enters the soft ACP management.

The available values depend on the LLC switching frequency range selected with the “LLC low frequency range” parameter.

### 3.4.14 Soft ACP TS decrement

Size: 3 bits

Sets the immediate time shift decrease during the soft ACP management.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
· 66.7 ns	· 133 ns
· 100 ns	· 200 ns
· 133 ns	· 267 ns
· 200 ns	· 400 ns
· 267 ns	· 533 ns
· 400 ns	· 800 ns
· 533 ns	· 1067 ns
· 800 ns	· 1600 ns

#### Use

During the Soft ACP management, the time shift value is decreased by the amount defined by this parameter. This delta is applied immediately, every time the system triggers the soft ACP. The higher the value, the faster the shift towards higher switching frequencies.

The system shuts down for the soft ACP fault if the minimum time shift is reached. The fault can be latched or not latched depending on the “LLC ACP behavior”.

The time shift decrement depends on the “LLC low frequency range” parameter.

### 3.4.15 Maximum soft ACP occurrences

Size: 1 bit

Sets the maximum number of consecutive soft ACP occurrences before the shutdown.

Available values are:

. 33

. 66

#### Use

This parameter defines the maximum consecutive number of times the soft ACP is managed.

Every time the system triggers the soft ACP feature, the STNRG012 moves to the soft-start state, to recover smoothly the regulation. The counter of the soft ACP managed is not cleared if the system cannot move to the normal running state.

The system shuts down for the soft ACP fault if the maximum number of soft ACP occurrences is reached. The fault can be latched or not latched depending on the “LLC ACP behavior” parameter.

## 3.5 Burst mode parameters

### 3.5.1 External burst mode

Size: 1 bit

Enables / disables the external burst mode feature.

Available values are:

. Disabled

. Enabled

#### Use

The external burst mode feature is used to drive the burst mode through an external signal. The feature enables / disables the external BM comparator active on the LLC\_AUX pin with a threshold of 0.9 V.

Two types of external burst mode can be defined:

- Pure external burst mode: only the external BM comparator manages the burst mode entering / exiting
- Hybrid external burst mode: if the external BM comparator is high, the system stays out of burst mode while if the external BM comparator is low, burst mode entering / exiting is managed by the LLC\_FB pin parameters.

The selection between the pure and hybrid is done with the “LLC\_FB burst entering thr” parameter.

In both external burst mode cases, the burst switching activity is managed by the LLC\_FB pin and the burst comparator.

### 3.5.2 BM enter for minimum TS

Size: 1 bit

Enables / disables the burst mode entering request if the minimum time shift is reached.

Available values are:

. Disabled

. Enabled

**Use**

This feature can be useful in case the resonant tank is not able to regulate the output at light/no loads even at the minimum time shift value. If the time shift has reached its minimum value, the feature allows entering the burst mode if the condition is asserted for at least 480  $\mu\text{s}$ , in addition to the “Burst entering digital filtering”. This prevents output overshoot. For this reason, the feature does not wait for the “No-burst window width” time before entering burst mode.

**3.5.3 Burst entering digital filtering**

Size: 2 bits

Sets the digital filtering to enter burst mode.

Available values are:

- 270  $\mu\text{s}$
- 510  $\mu\text{s}$
- 750  $\mu\text{s}$
- 990  $\mu\text{s}$

To enter burst mode, the burst request (external or LLC\_FB pin driven) must be asserted for the time defined by this parameter.

This allows reject noise on LLC\_FB and LLC\_AUX pins.

**3.5.4 LLC\_FB burst entering thr**

Size: 6 bits

Sets the voltage threshold to enter burst mode.

Available values are:

Voltage on LLC_FB pin	“LLC low frequency range”	
	= disabled	= enabled
·268.6 mV	·350 ns	·700 ns
·278.3 mV	·383.3 ns	·766.7 ns
·288.1 mV	·416.7 ns	·833.3 ns
·297.9 mV	·450 ns	·900 ns
·307.6 mV	·483.3 ns	·966.7 ns
·317.4 mV	·516.7 ns	·1033 ns
·327.1 mV	·550 ns	·1100 ns
·336.9 mV	·583.3 ns	·1167 ns
·346.7 mV	·616.7 ns	·1233 ns
·356.4 mV	·650 ns	·1300 ns
·366.2 mV	·683.3 ns	·1367 ns
·376.0 mV	·716.7 ns	·1433 ns
·385.7 mV	·750 ns	·1500 ns
·395.5 mV	·783.3 ns	·1567 ns
·405.3 mV	·816.7 ns	·1633 ns
·415.0 mV	·850 ns	·1700 ns
·424.8 mV	·883.3 ns	·1767 ns

·434.6 mV	·916.7 ns	·1833 ns
·444.3 mV	·950 ns	·1900 ns
·454.1 mV	·983.3 ns	·1967 ns
·463.9 mV	·1017 ns	·2033 ns
·473.6 mV	·1050 ns	·2100 ns
·483.4 mV	·1083 ns	·2167 ns
·493.2 mV	·1117 ns	·2233 ns
·502.9 mV	·1150 ns	·2300 ns
·512.7 mV	·1183 ns	·2367 ns
·522.5 mV	·1217 ns	·2433 ns
·532.2 mV	·1250 ns	·2500 ns
·542.0 mV	·1283 ns	·2567 ns
·551.8 mV	·1317 ns	·2633 ns
·561.5 mV	·1350 ns	·2700 ns
·571.3 mV	·1383 ns	·2767 ns
·581.1 mV	·1417 ns	·2833 ns
·590.8 mV	·1450 ns	·2900 ns
·600.6 mV	·1483 ns	·2967 ns
·610.4 mV	·1517 ns	·3033 ns
·620.1 mV	·1550 ns	·3100 ns
·629.9 mV	·1583 ns	·3167 ns
·639.6 mV	·1617 ns	·3233 ns
·649.4 mV	·1650 ns	·3300 ns
·659.2 mV	·1683 ns	·3367 ns
·668.9 mV	·1717 ns	·3433 ns
·678.7 mV	·1750 ns	·3500 ns
·688.5 mV	·1783 ns	·3567 ns
·698.2 mV	·1817 ns	·3633 ns
·708.0 mV	·1850 ns	·3700 ns
·717.8 mV	·1883 ns	·3767 ns
·727.5 mV	·1917 ns	·3833 ns
·737.3 mV	·1950 ns	·3900 ns
·747.1 mV	·1983 ns	·3967 ns
·756.8 mV	·2017 ns	·4033 ns
·766.6 mV	·2050 ns	·4100 ns
·776.4 mV	·2083 ns	·4167 ns
·786.1 mV	·2117 ns	·4233 ns
·795.9 mV	·2150 ns	·4300 ns
·805.7 mV	·2183 ns	·4367 ns
·815.4 mV	·2217 ns	·4433 ns
·825.2 mV	·2250 ns	·4500 ns
·835.0 mV	·2283 ns	·4567 ns
·844.7 mV	·2317 ns	·4633 ns

·854.5 mV	·2350 ns	·4700 ns
·864.3 mV	·2383 ns	·4767 ns
·874.0 mV	·2417 ns	·4833 ns
·883.8 mV	·2450 ns	·4900 ns

**Use**

When the external burst mode is disabled, the parameter sets the voltage threshold at the LLC\_FB pin to enter burst mode. In order to correctly select this parameter, set it first to the minimum level, then adjust the board to work at the required load to enter burst mode. Measure the voltage at the LLC\_FB pin and select the closer “LLC\_FB burst entering thr” value, from the values on the left.

If the external burst mode is enabled and the minimum value (268.6 mV) is selected, the pure external burst mode is activated: only the LLC\_AUX Ext. The BM comparator manages burst mode entering / exiting.

If the external burst mode is enabled and the minimum value (268.6 mV) is NOT selected, the hybrid external burst mode is activated: when the LLC\_AUX Ext. BM comparator is high, the system stays out of burst mode; when the LLC\_AUX Ext. BM comparator is low, burst mode entering / exiting is managed by the voltage at the “LLC\_FB burst entering thr”, as the standard burst mode.

*Note:* In order to enter the burst mode driven by LLC\_FB pin voltage, the equivalent time shift (on the right of the voltage threshold and depending on “LLC low frequency range”) must be higher than the “Minimum time shift”, otherwise the system does not enter the burst mode for LLC\_FB.

**3.5.5 LLC\_FB burst wake-up thr**

Size: 2 bits

Sets the threshold for the burst wake-up comparator (connected to the LLC\_FB pin).

Available values are:

"Voltage on LLC_FB range"	"LLC low frequency range"	"LLC low frequency range"
	= disabled	= enabled
· 0.75 V	· 2 μs	· 4 μs
· 1 V	· 2.85 μs	· 5.7 μs
· 1.25 V	· 3.7 μs	· 7.4 μs

During burst mode, the STNRG012 restarts switching and performs one burst when the LLC\_FB pin goes over this threshold.

**Use**

The wake-up threshold on the left has to be set higher than the “LLC\_FB burst entering thr”.

After wake-up, the time shift follows the LLC\_FB if it is higher than the “Min TS in burst mode”. On the right of the voltage threshold, the equivalent time shift of that voltage is shown and it depends on the “LLC low frequency range” parameter.

The most suitable values are usually 0.75 V or 1 V.



### 3.5.6 LLC\_FB burst wake-up hyst

Size: 1 bit

Sets the hysteresis for the burst wake-up comparator (connected to LLC\_FB).

Available values are:

. 5 mV

. 10 mV

#### **Use**

The best choice is usually 5 mV.

### 3.5.7 Min TS in burst mode

Size: 5 bits

Sets the minimum time shift value during the burst mode.

Available values are:

“LLC low frequency range” = disabled	“LLC low frequency range” = enabled
·1 μs	·4.2 μs
·1.13 μs	·4.33 μs
·1.27 μs	·4.47 μs
·1.4 μs	·4.6 μs
·1.53 μs	·4.73 μs
·1.67 μs	·4.87 μs
·1.8 μs	·5 μs
·1.93 μs	·5.13 μs
·2.07 μs	·5.27 μs
·2.2 μs	·5.4 μs
·2.33 μs	·5.53 μs
·2.47 μs	·5.67 μs
·2.6 μs	·5.8 μs
·2.73 μs	·5.93 μs
·2.87 μs	·6.07 μs
·3 μs	·6.2 μs
·3.13 μs	·6.33 μs
·3.27 μs	·6.47 μs
·3.4 μs	·6.6 μs
·3.53 μs	·6.73 μs
·3.67 μs	·6.87 μs
·3.8 μs	·7 μs
·3.93 μs	·7.13 μs
·4.07 μs	·7.27 μs
·4.2 μs	·7.4 μs
·4.33 μs	·7.53 μs
·4.47 μs	·7.67 μs
·4.6 μs	·7.8 μs
·4.73 μs	·7.93 μs
·4.87 μs	·8.07 μs
·5 μs	·8.2 μs
·5.13 μs	·8.33 μs

Setting the time shift value (and therefore the switching frequency), it is possible to fix how much energy is transferred to the output by one burst sequence.

The parameter sets the time shift of the first low-side and high-side gate drives of the burst sequence. Please note that the shift value also works as a low limit: if the feedback should ask for an increased time shift, the system follows the feedback request. This is very useful during load transient, in order to have a prompt response in case of large load increases. Consider also the equivalent time shift of the “LLC\_FB burst wake-up thr”: if this is higher, the time shift increases after the first pulses.

The time shift value depends on the “LLC low frequency range” parameter.

**Use**

The suggestion is to use a value that provides good energy transfer, in order to have efficient operation.

For example, in systems designed to work at resonance, the time shift during the burst mode can be selected to work at resonance or a little below it.

**3.5.8 Min number of burst pulses**

Size: 4 bits

Sets the minimum number of switching cycles inside one burst sequence.

Available values are:

- . 2
- . 3
- . 4
- . 5
- . 6
- . 7
- . 8
- . 9
- . 10
- . 11
- . 12
- . 13
- . 14
- . 15
- . 16
- . 17

This parameter defines the minimum number of switching cycles composing a single burst. This condition is reached at light loads.

**Use**

The minimum number of switching cycles is usually selected in order to not have a long distance between two bursts at the no-load and therefore to avoid the saturation of the optocoupler output transistor.

**3.5.9 Max number of burst pulses (delta)**

Size: 4 bits

Sets the maximum number of switching cycles inside one burst sequence.

Available values are:

. 0  
. 1  
. 2  
. 3  
. 4  
. 5  
. 6  
. 7  
. 8  
. 9  
. 10  
. 11  
. 12  
. 13  
. 14  
. 15

This parameter defines the maximum number of switching cycles composing a single burst. This condition is reached at medium/high loads (in the burst mode).

Please note that this parameter is defined as a positive delta with respect to the “Min number of burst pulses” parameter, so the total maximum number of burst pulses is

$$\text{“Max number of burst pulses”} = \text{“Min number of burst pulses”} + \text{“Max number of burst pulses (delta)”} \quad (16)$$

#### Use

The maximum number of switching cycles is usually selected in order to stay within the maximum output voltage ripple allowed.

If the designer wants a fixed number of switching cycles, it could be done by setting the parameter to 0.

### 3.5.10 Min time between burst seq

Size: 2 bits

Sets the minimum time between two burst sequences to increase the number of switching cycles.

Available values are:

. 5.93 ms  
. 10.2 ms  
. 14.47 ms  
. 18.73 ms

During the burst mode, if the load is increased and the distance between two bursts reaches the value defined by this parameter, the system increases the number of switching cycles by one.

The upper limit for the switching cycles is defined by the “Max number of burst pulses (delta)” parameter.

### 3.5.11 Max time between burst seq (delta)

Size: 2 bits

Sets the maximum time between two burst sequences to decrease the number of switching cycles.

Available values are:

- . 2.83 ms
- . 4.97 ms
- . 7.1 ms
- . 9.23 ms

During the burst mode, if the load is decreased and the distance between two bursts reaches the value defined by this parameter, the system decreases the number of switching cycles by one. The lower limit for the switching cycles is defined by the “Min number of burst pulses” parameter.

Please note that this parameter is defined as a positive delta with respect to the “Min time between burst seq” parameter, so the total maximum time between burst sequences is

$$\text{"Max time between burst seq"} = \text{"Min time burst seq"} + \text{"Max time between burst seq (delta)"} \quad (17)$$

### 3.5.12 Minimum period to exit burst

Size: 4 bits

Sets the minimum time between two consecutive burst sequences to exit the burst mode.

Available values are:

- . 66.7 μs
- . 100 μs
- . 133 μs
- . 167 μs
- . 200 μs
- . 233 μs
- . 267 μs
- . 300 μs
- . 333 μs
- . 367 μs
- . 400 μs
- . 433 μs
- . 467 μs
- . 500 μs
- . 533 μs
- . 567 μs

When the system is in the burst mode and the load increases, the time between two burst sequences is reduced. If the time distance between two consecutive burst sequences reaches the time threshold set by this parameter, the system exits the burst mode.

Therefore, the lower the value for this parameter, the higher the load for exiting the burst mode.

Please note that this mechanism is not used with the pure external burst mode.

#### Use

To tune this parameter, initially set it to a very low value. Bring the system to the burst mode and then increase the load to the desired burst exit point. Measure the distance between two consecutive burst sequences and program that value in the parameter.

### 3.5.13 No-burst window width

Size: 1 bit

Sets the minimum time that avoids burst re-entering.

Available values are:

- . 90  $\mu$ s
- . 7.5 ms

If the system exits the burst mode, burst mode re-entering is forbidden for a minimum time defined by this parameter.

#### Use

The suggested value is 7.5 ms to avoid burst mode re-entering at low load in case the feedback voltage undershoots at the burst mode exit.

Please note that the no-burst window does not apply for the “BM enter for minimum TS”.

## 3.6 Comparators setting

### 3.6.1 Surge comp digital filtering

Size: 1 bit

Sets the digital filtering for the line surge comparator.

Available values are:

- . 100 ns
- . 500 ns

### 3.6.2 PFC CS comp digital filtering

Size: 2 bits

Sets the digital filtering for the PFC CS comparator for the ReCOT functionality (THD improver).

Available values are:

- . No filtering
- . 16.7 ns
- . 33.3 ns
- . 50 ns

### 3.6.3 PFC OC2 comp digital filtering

Size: 2 bits

Sets the digital filtering for the PFC OC2 comparator.

Available values are:

- . No filtering
- . 133.3 ns

. 266.7 ns  
. 400 ns

### 3.6.4 PFC OC1 comp digital filtering (delta)

Size: 1 bit

Sets the digital filtering for the PFC OC1 comparator.

Available values are:

. 33.3 ns  
. 166.7 ns

#### Use

The digital filter for the PFC OCP1 comparator is defined as a positive delta with respect to the “PFC OC2 comp digital filtering” parameter:

$$\text{"PFC OC1 comp digital filtering"} = \text{"PFC OC2 comp digital filtering"} + \text{"PFC OC1 comp digital filtering (delta)"} \quad (18)$$

The digital filter in the OC1 comparator has to be longer than the one in the OCP2 because otherwise OC1 detection and management could mask the OC2 events.

### 3.6.5 PFC ZCD comp digital filtering

Size: 1 bit

Sets the digital filtering for the PFC ZCD comparator.

Available values are:

. 33.3 ns  
. 66.7 ns

### 3.6.6 PFC ZCD comp falling thr

Size: 2 bits

Sets the falling threshold for the PFC ZCD comparator (TH\_F).

Available values are:

. 0 mV  
. 50 mV  
. 100 mV  
. 200 mV

### 3.6.7 PFC ZCD comp rising thr

Size: 2 bits

Sets the rising threshold for the PFC ZCD comparator (TH\_R).

Available values are:

- . 210 mV
- . 110 mV (N/A with TH\_F = 200 mV)
- . 310 mV
- . TH\_F + 10 mV

**Use**

The rising threshold of the PFC ZCD comparator must be higher than the falling one. For this reason, the selection TH\_F = 200 mV and TH\_R = 110 mV is not allowed.

The last selection sets the rising threshold 10 mV higher with respect to any selection of the falling threshold.

**3.6.8 PFC HW OVP comp digital filtering**

Size: 2 bits

Sets the digital filtering for the PFC HW OVP comparator.

Available values are:

- . 4.25  $\mu$ s
- . 2.12  $\mu$ s
- . 1.05  $\mu$ s
- . 516.7  $\mu$ s

**3.6.9 LLC OLP comp digital filtering**

Size: 2 bits

Sets the digital filtering for the LLC OC1 comparator, for the OLP functionality.

Available values are:

- . No filtering
- . 16.7 ns
- . 33.3 ns
- . 50 ns

**Use**

The value 16.7 ns can be used as the starting value.

In noisy applications, it may be necessary to increase the filtering.

**3.6.10 LLC OC2 comp digital filtering**

Size: 2 bits

Sets the digital filtering for the LLC OC2 comparator.

Available values are:

- . 133.3 ns
- . 166.7 ns
- . 200 ns
- . 233.3 ns



### 3.6.11 LLC ZCD comp digital filtering

Size: 3 bits

Sets the digital filtering for the LLC ZCD comparator.

Available values are:

- . 50 ns
- . 116.7 ns
- . 183.3 ns
- . 250 ns
- . 316.7 ns
- . 383.3 ns
- . 450 ns
- . 516.7 ns

#### Use

The filtering has to be chosen considering the trade-off between the noise rejection and maximum operating frequency.

### 3.6.12 LLC ZCD comp hysteresis

Size: 1 bit

Sets the LLC ZCD comparator hysteresis.

Available values are:

- . 5 mV
- . 10 mV

#### Use

The comparator's hysteresis has to be chosen considering the trade-off between the noise rejection and LLC\_CS signal at the minimum time shift.

It is suggested to use 10 mV as hysteresis.

### 3.6.13 LLC OVP comp digital filtering

Size: 2 bits

Sets the digital filtering for the LLC OVP comparator.

Available values are:

- . 4.25  $\mu$ s
- . 2.12  $\mu$ s
- . 1.05  $\mu$ s
- . 516.7 ns

## Revision history

**Table 1. Document revision history**

Date	Version	Changes
27-Aug-2021	1	Initial release.

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