
STSW-L99DZ200 GUI

Introduction

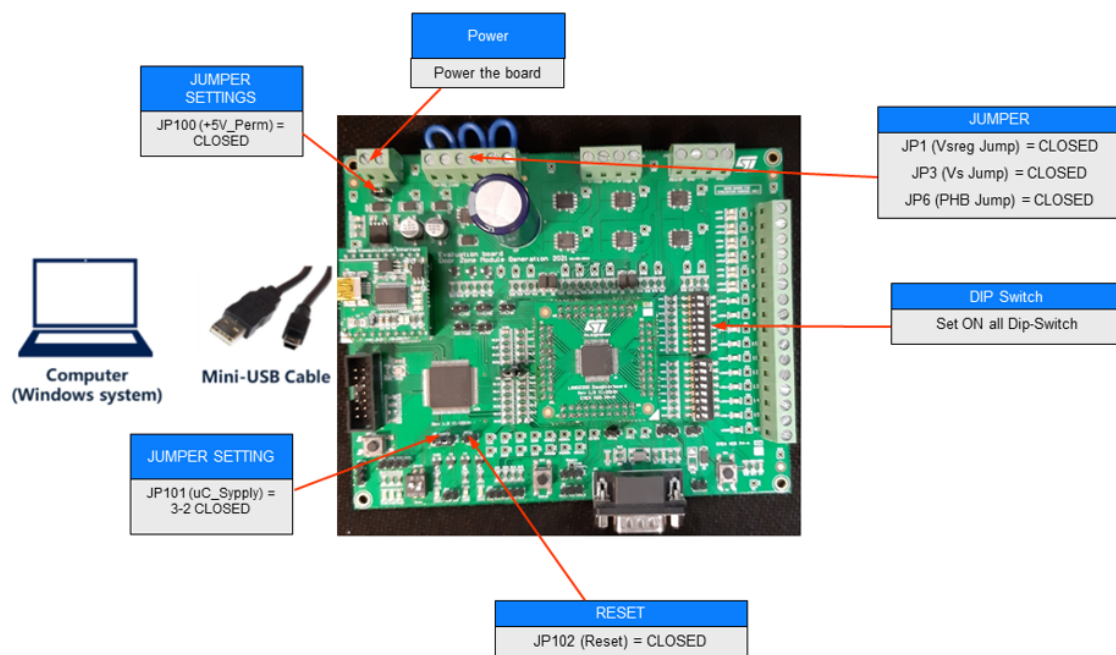
This document describes the STSW-L99DZ200 Graphical User Interface (GUI) dedicated to run the EVAL-L99DZ200.

The EVAL-L99DZ200 evaluation board is designed for automotive door zone application and it consists in a motherboard and a daughter board on which the L99DZ200G device is assembled. Both the boards provide electronic control modules with enhanced power management functionalities including a standby mode. These evaluation boards are designed to drive multiple DC motors. The STSW-L99DZ200 has been developed by using C++ and it works with a motherboard based on SPC582B60 microcontroller programmed with dedicated firmware that drives the L99DZ200G assembled in the daughter board.

1 How to connect the EVAL-L99DZ200

The following figure shows how to connect the EVAL-L99DZ200 and the main HW settings. Refer to the datasheet (see [Section 11 Reference documents](#)) for more information on the HW settings of the EVAL-L99DZ200.

Figure 1. Eval-L99DZ200 connection

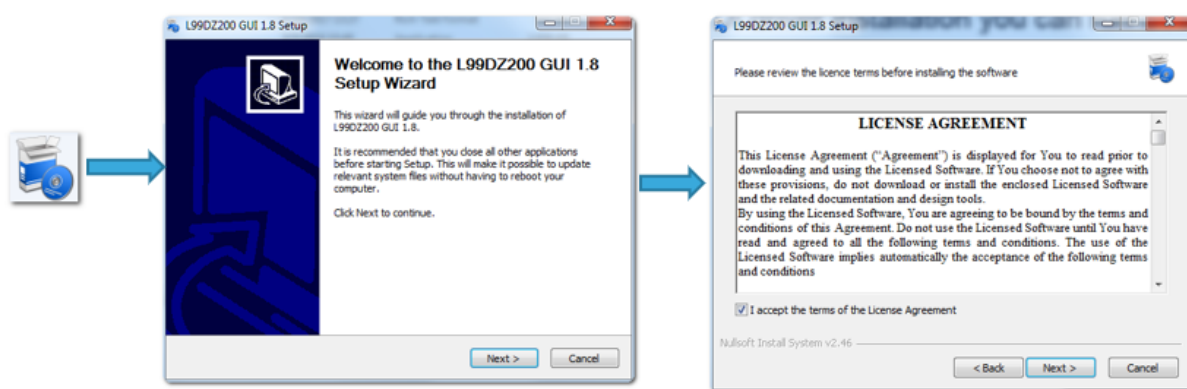


2

2.1

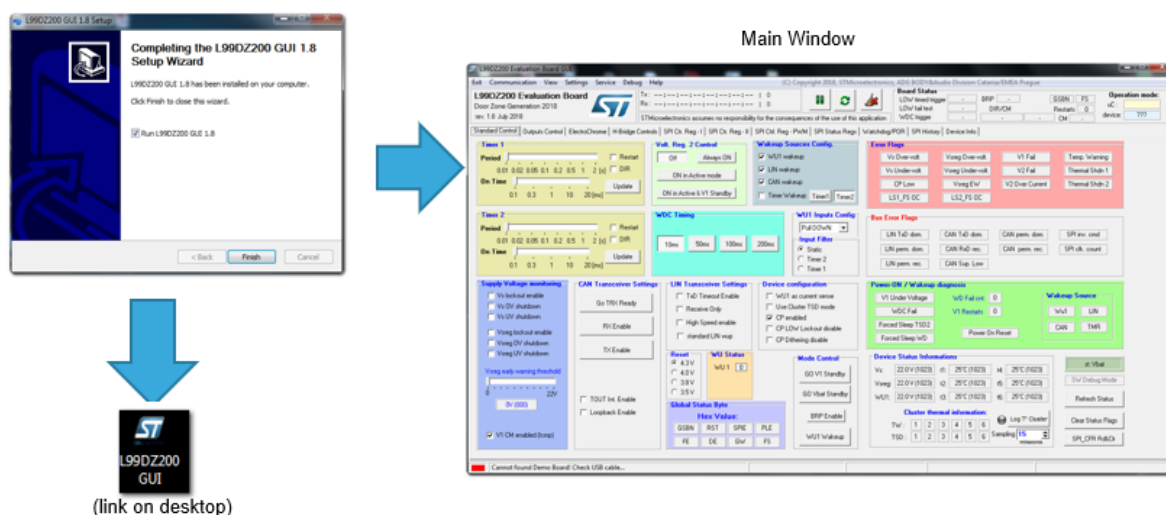
1. Install FDTI drive from supplier website
2. Complete the connection (see the [Figure 1. Eval-L99DZ200 connection](#)), then power-on
3. Run **Setup_GUI.exe**

Figure 2. Graphic User Interface setup (1/2)



When GUI installation is finished, GUI icon link is added on your desktop and a main window is showed:

Figure 3. Graphic User Interface setup (2/2)



3 Main window overview

When the EVAL-L99DZ200 is connected and the USB driver is installed, the message “**Board connected and ready**” will be displayed on the bottom left part of the main window.

Here below an overview of the main functions of the main window is reported.

Figure 4. Main window overview

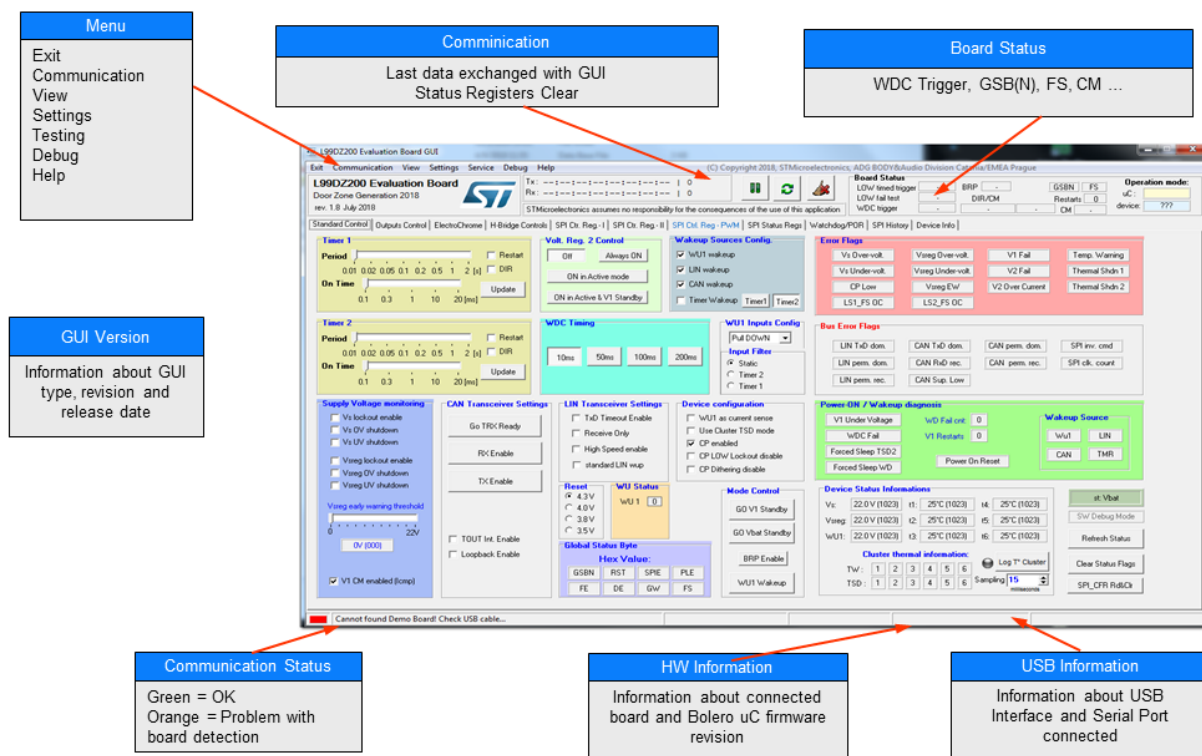
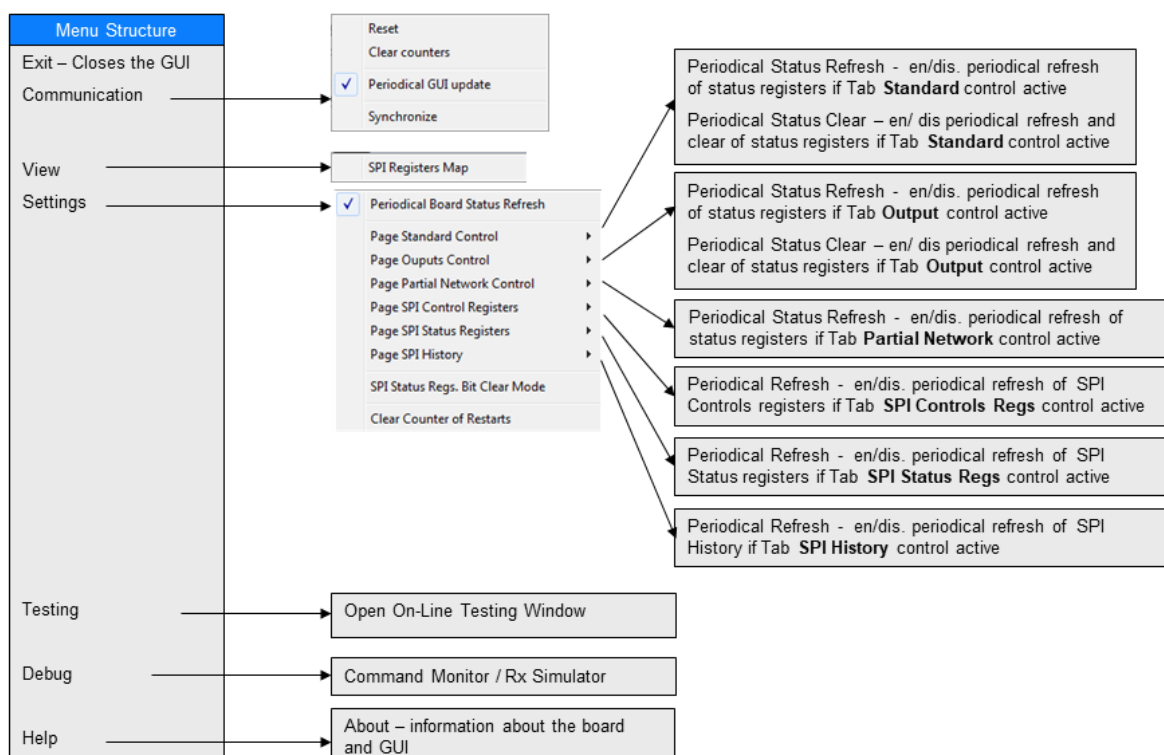


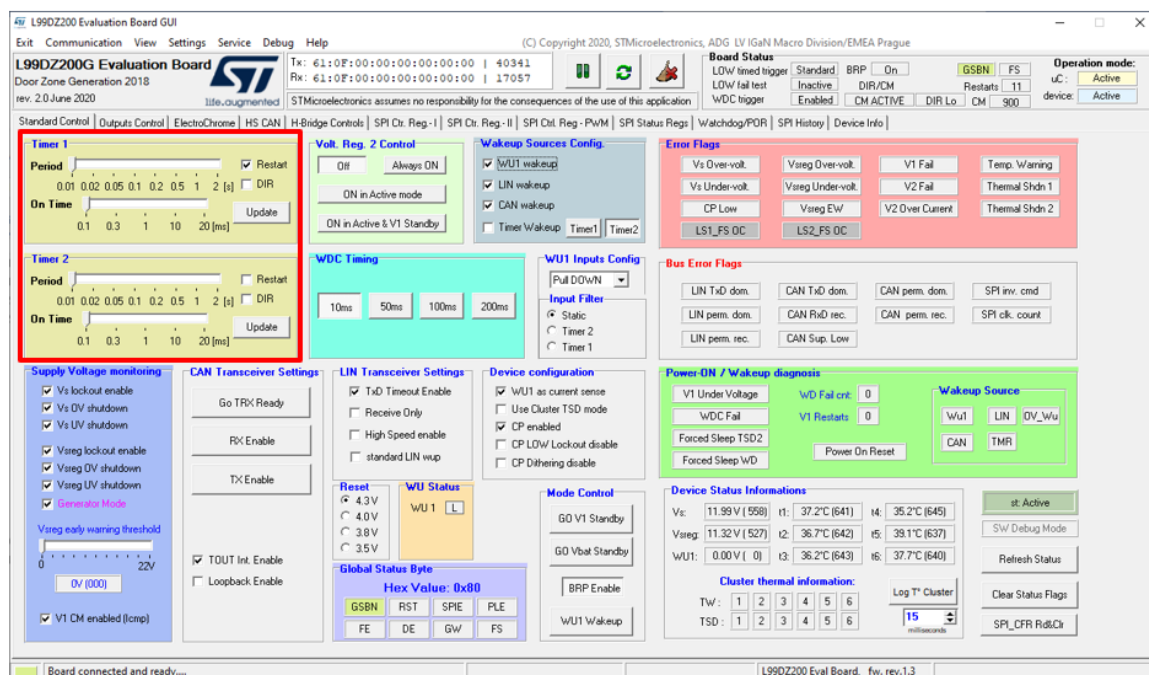
Figure 5. Main window menu items



4 Standard control panel

4.1 Timers section

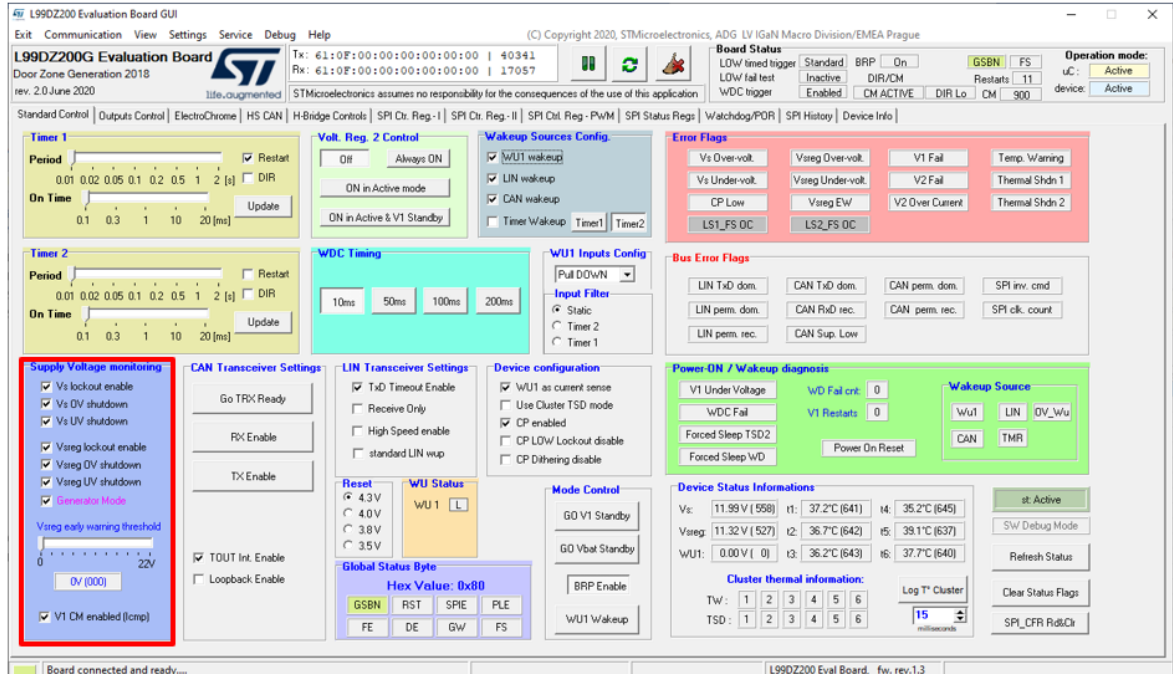
Figure 6. Standard control window – timers section



In Figure 6. Standard control window – timers section the section of the GUI related to the configuration of the two timers embedded in L99DZ200G is shown. For each of the two timers, the period (from 0.01 s to 2 s) and the on time (from 0.1 ms to 20 ms) is programmable. The restart flag allows to restart the timer with the defined settings when the SPI CSN goes from low to high (see Section 11 Reference documents). The DIR flag allows to control the timer from DIR input (see the datasheet Section 11 Reference documents). Once the configuration of the timers has been set, the update button allows the MCU to create and transfer to the L99DZ200G the corresponding SPI command.

4.2 Supply voltage monitoring section

Figure 7. Standard control window – supply voltage monitoring section



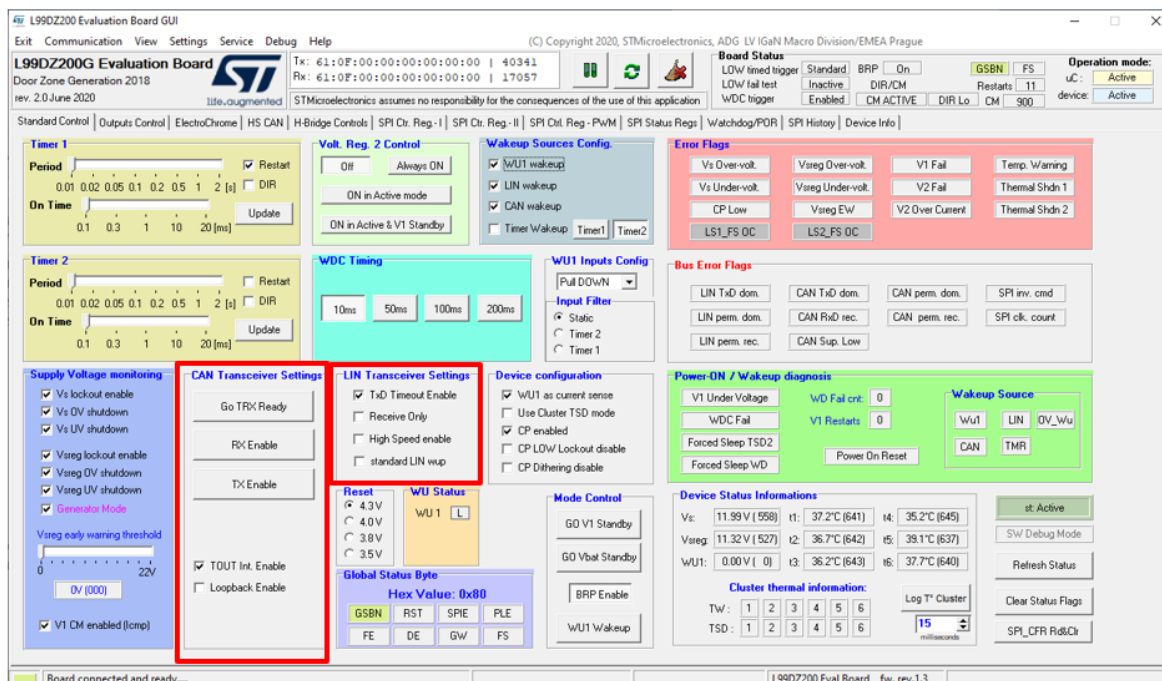
In Figure 7. Standard control window – supply voltage monitoring section the section of the GUI related to the configuration of the **supply voltage monitoring** is shown.

For both V_s and V_{sreg} there are some flags to enable the lockout and the OV/UV shutdown. A flag to configure the **generator mode** (see in the datasheet [Section 11 Reference documents](#)) is reported inside this section; the V_{sreg} early warning threshold can be here configured too.

One more flag is dedicated to the enabling of the V1 CM (lcmp); see [Figure 6. Standard control window – timers section](#) in its own datasheet (see [Section 11 Reference documents](#)).

4.3 CAN and LIN transceivers section

Figure 8. Standard control window – CAN and LIN transceiver sections



In the figure above the section of the GUI related to the setting of CAN and LIN transceivers is shown.

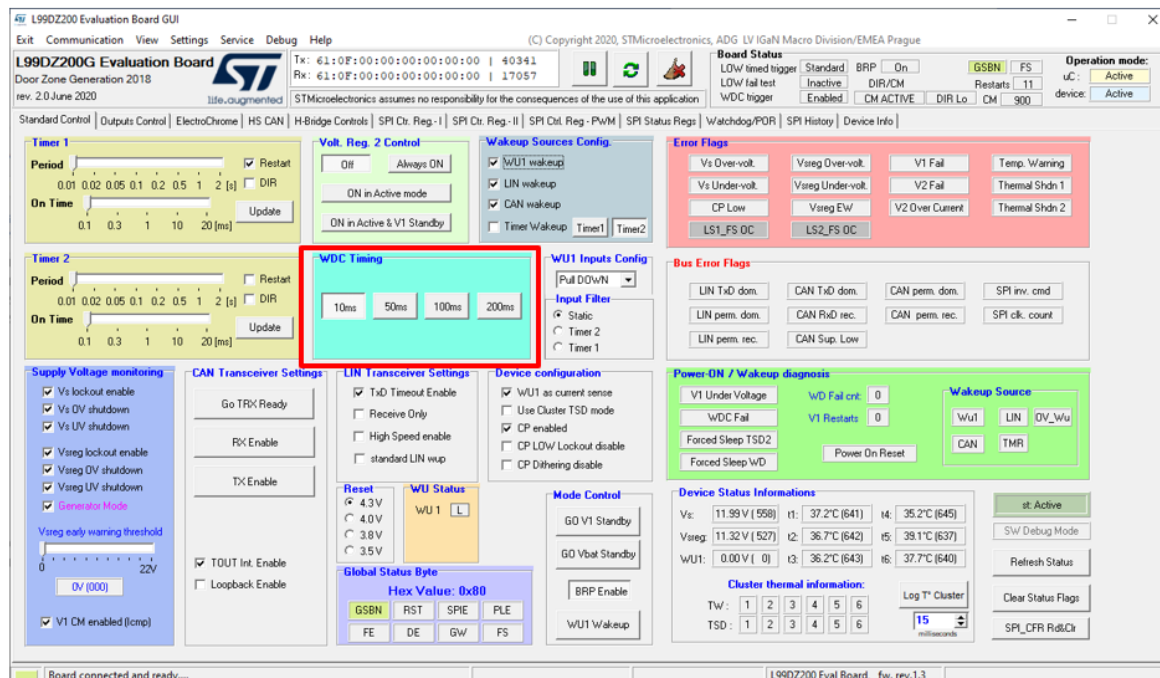
- **Go TRX Ready** button allows to set the CAN transceiver in TRX READY mode;
- **RX Enable** button allows to enable the CAN receiver;
- **TX Enable** button allows to enable the CAN transmitter;

TOUT Int. Enable flag allows to enable interrupt signal in case of CAN timeout (see CR1, bit 11)

Loopback Enable flag enables the loopback modality of L99DZ200G CAN transceiver (see CR2, bit 5).

4.4 Watchdog timing section

Figure 9. Standard control window – Watchdog timing sections

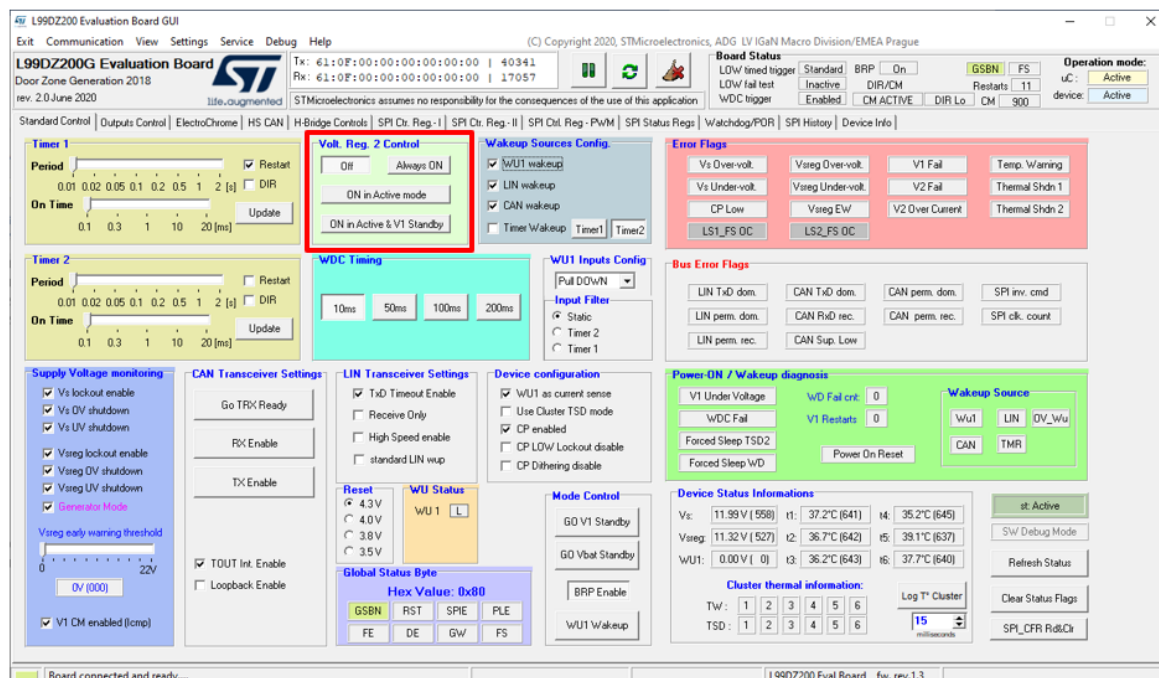


In the figure above the section of the GUI related to the setting of WatchDog timing is reported. One of the following values can be here set, as defined by the WD_TIME_0/1 bits (CR2, bit 0 and bit 1):

- 10 ms
- 50 ms
- 100 ms
- 200 ms

4.5 Voltage regulator control section

Figure 10. Standard control window – voltage regulator 2 control section



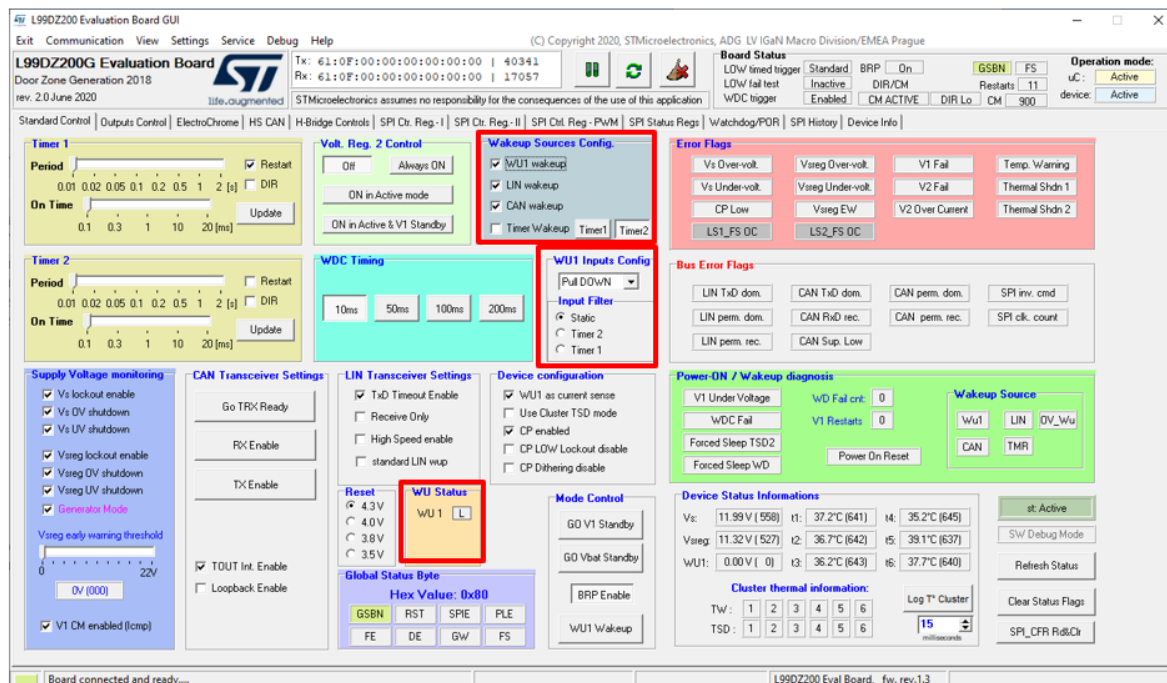
In the figure above the section of the GUI related to the control of the voltage regulator 2 is reported.

The **Off** button allows to switch OFF or switch ON the V2; in case the V2 is ON, one of the following cases can be used by setting the related button (see the datasheet [Section 11 Reference documents](#)):

- **Always ON**
- **ON in Active mode**
- **ON in Active & V1 Standby**

4.6 Wakeup section

Figure 11. Standard control window – wakeup section



In the figure above the sections of the GUI related to the setting of wake-up are reported.

One of the following values can be here set:

- **WU1 wakeup** flag allows to wake up the L99DZ200G from WU1 pin;
- **LIN wakeup** flag allows to wake up the L99DZ200G from LIN;
- **CAN wakeup** flag allows wake up the L99DZ200G from CAN;
- **Timer wakeup** flag allows wake up the L99DZ200G from **Timer 1** or **Timer 2**.

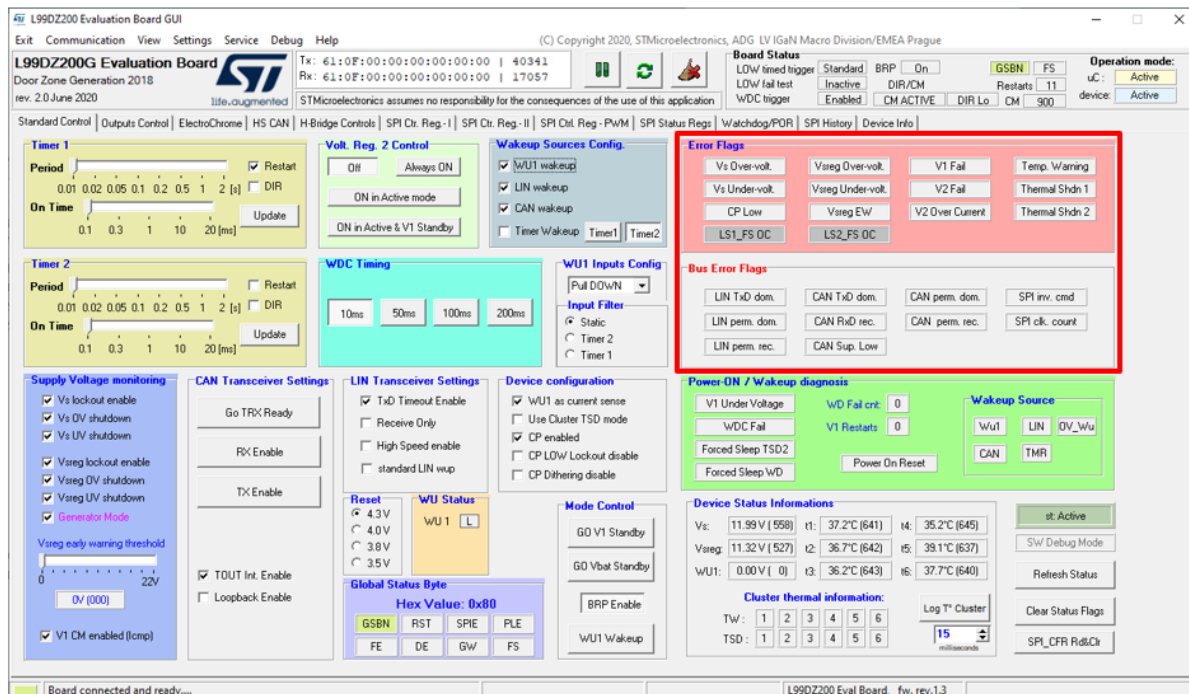
The **WU1 Inputs Config** can be set as **Pull DOWN** or pull up from the related window menu (as specified in CR 1, bit 20 - WU_PU).

The **Input Filter** can be set **Static** or from **Timer 1** or from **Timer 2**, as specified in bit 16, 17 of CR1.

The **WU Status** reports the value of the bit 22 of SR1 (WU_STATE).

4.7 Error flags section

Figure 12. Standard control window – error flags section



In the figure above the sections of the GUI related to the errors and bus errors flags are reported.

The following error flags are reported:

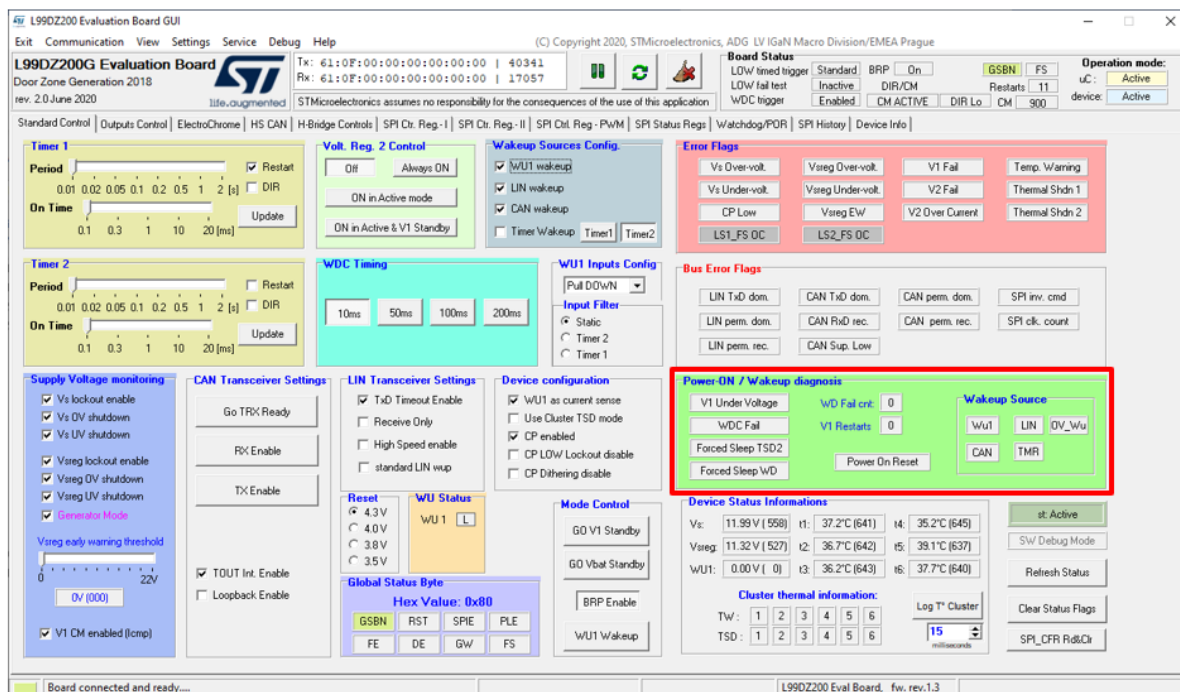
- Vs/Vsreg over voltage / under voltage
- V1/V2 fail
- Temperature warning
- Thermal shutdown 1 and thermal shutdown 2
- CP low
- Vsreg early warning
- V2 overcurrent
- LS1(LS2)_FS overcurrent

The following bus errors flags are reported:

- CAN Tx/D dominant
- CAN Rx/D recessive
- CAN permanent dominant
- CAN permanent recessive
- CAN supply low
- LIN Tx/D dominant
- LIN permanent dominant
- LIN permanent recessive
- SPI invalid command
- SPI clock count

4.8 Power-on / Diagnosis section

Figure 13. Standard control window – power-on / diagnosis section



In the figure above the section of the GUI related to the power-on / wakeup diagnosis is reported.

One of the following values can be here observed:

- **V1 Under Voltage**
- **WDC Fail**
- **Forced Sleep TSD2**
- **Forced Sleep WD**

The **WD Fail cnt** indicates number of subsequent watchdog failures (see SR1 from bit 8 to bit 11)

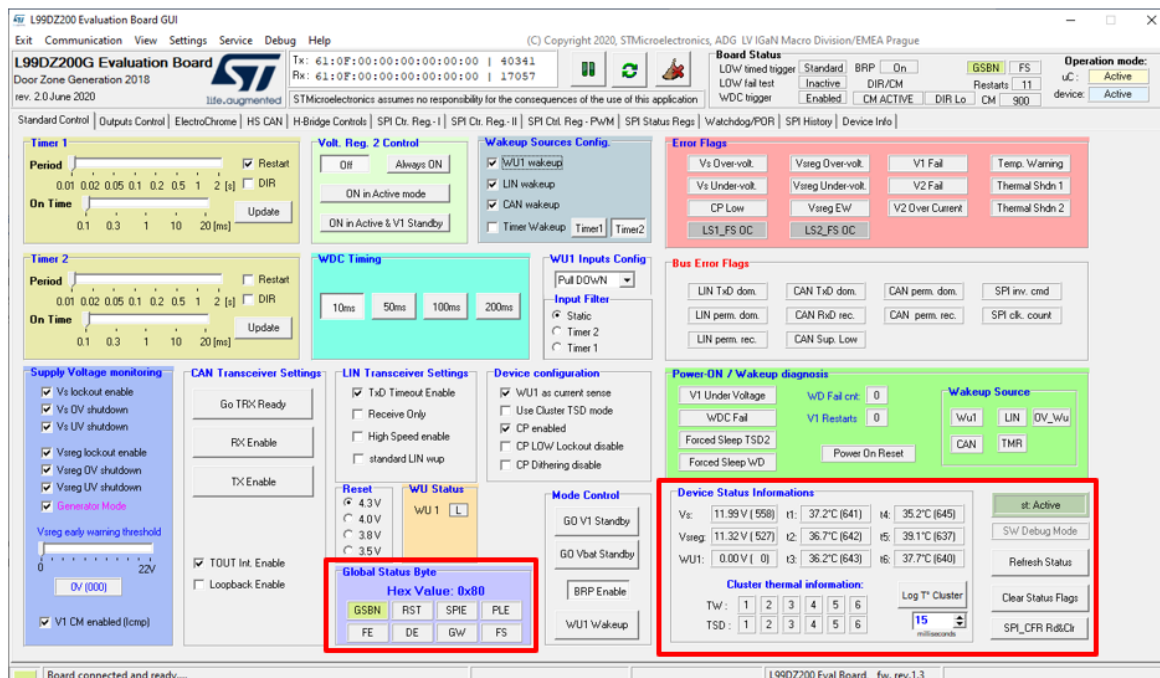
The **V1 Restarts** Indicates the number of TSD2 events which caused a restart of voltage regulator V1 (see SR1 from bit 12 to bit 14).

The **Power-on Reset** indicates when a Power-on reset occurs (see SR1, bit 0);

The **Wakeup Source** reports the source of the wake up (i.e. **Wu1**, **LIN**, **CAN** or **TMR**).

4.9 Device status and global status byte section

Figure 14. Standard control window – device status and global status byte section



In the figure above the sections of the GUI related to the device status information and global status byte are reported.

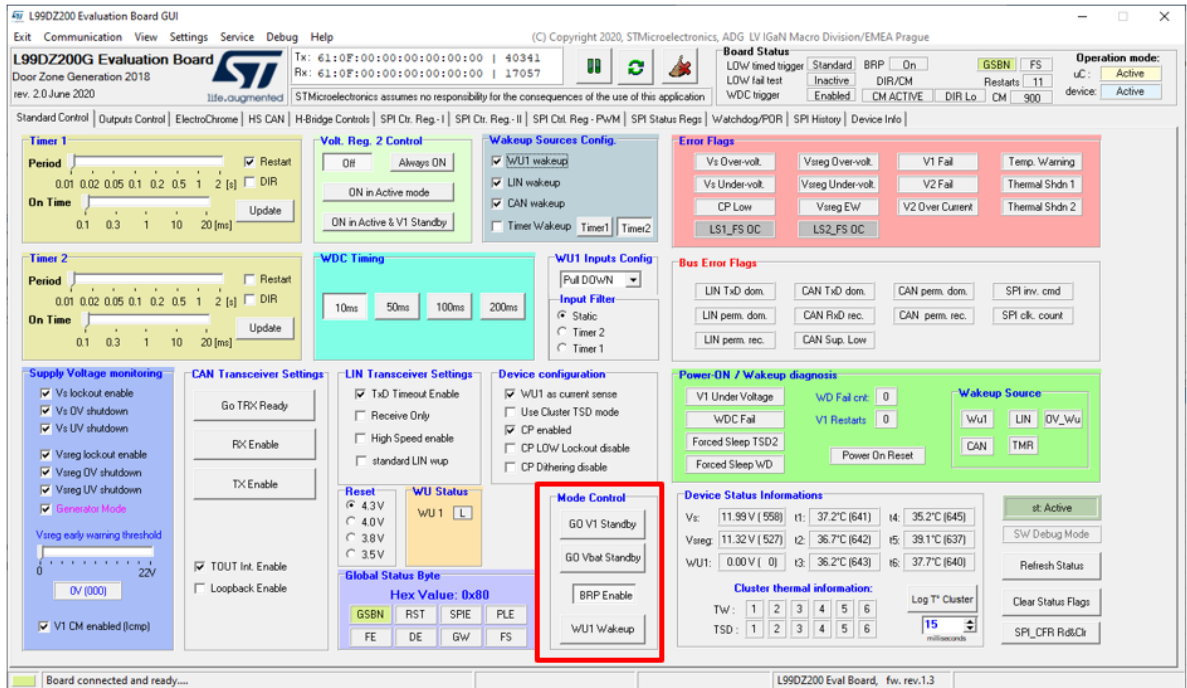
The runtime values for Vs, Vsreg, WU1 and thermal clusters 1-6 are reported.

The thermal cluster information visualize the status (TW or TSD) for each of the 6 thermal clusters; when a given thermal Cluster is in TW, the correspondent flag is orange; when it is in TSD, the correspondent flag becomes red.

V_{bat} value indicates if the L99DZ200G is in V_{bat} standby or V1 standby.

4.10 Mode control section

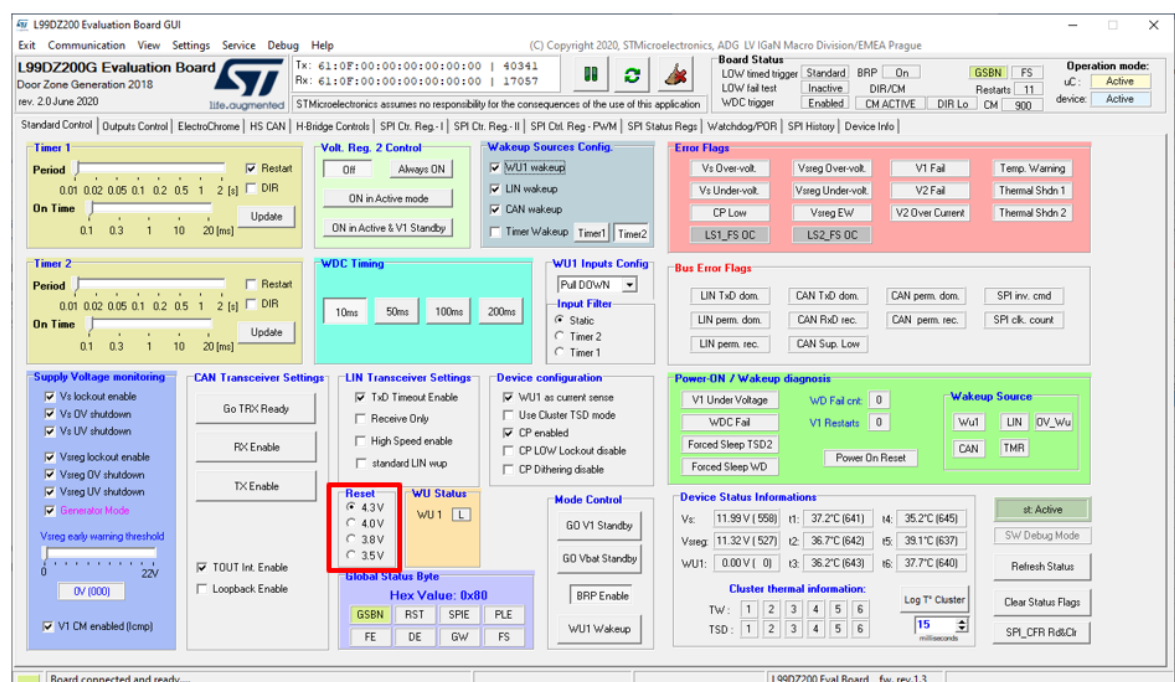
Figure 15. Standard control window – mode control section



In the figure above the section of the GUI related to the mode control of the L99DZ200G is reported.

4.11 Reset section

Figure 16. Standard control window – reset section



In the figure above the section of the GUI related to the reset of the L99DZ200G is reported.
In this section one of the 4 possible reset thresholds (4.3 V, 4.0 V, 3.8 V and 3.5 V) can be configured.

5 Outputs control panel

Figure 17. STSW-L99DZ200 outputs control panel

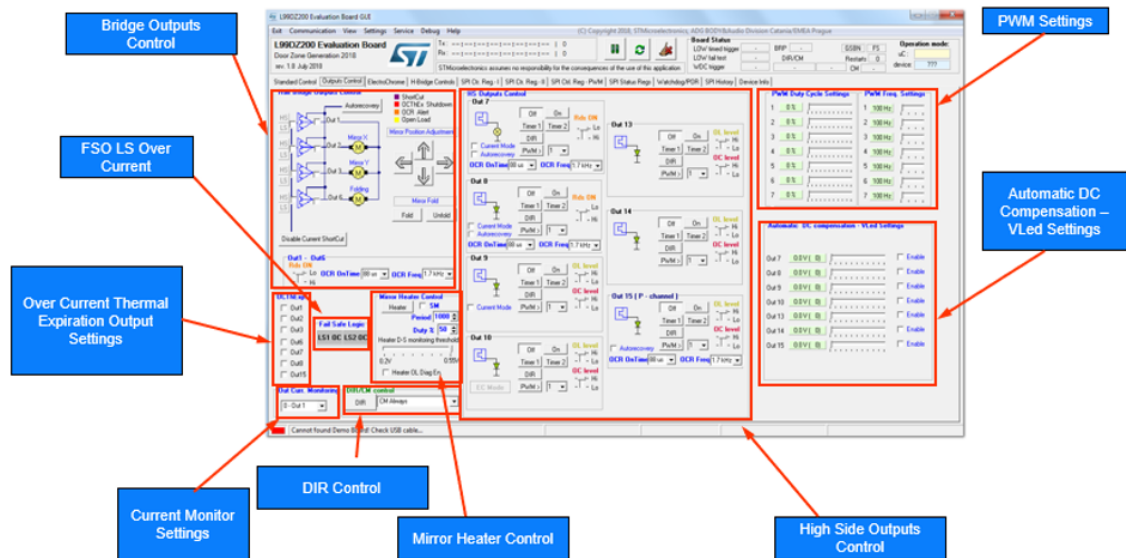


Figure 18. STSW-L99DZ200 outputs control - half-bridge outputs

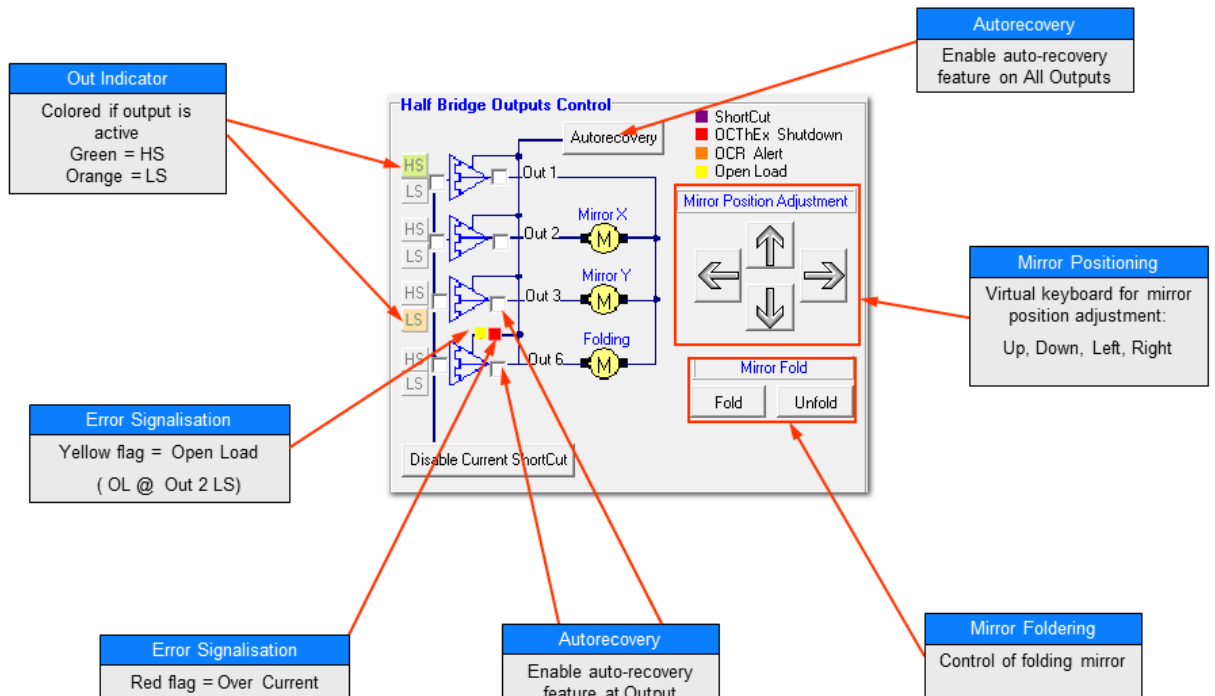


Figure 19. STSW-L99DZ200 outputs control – high sides

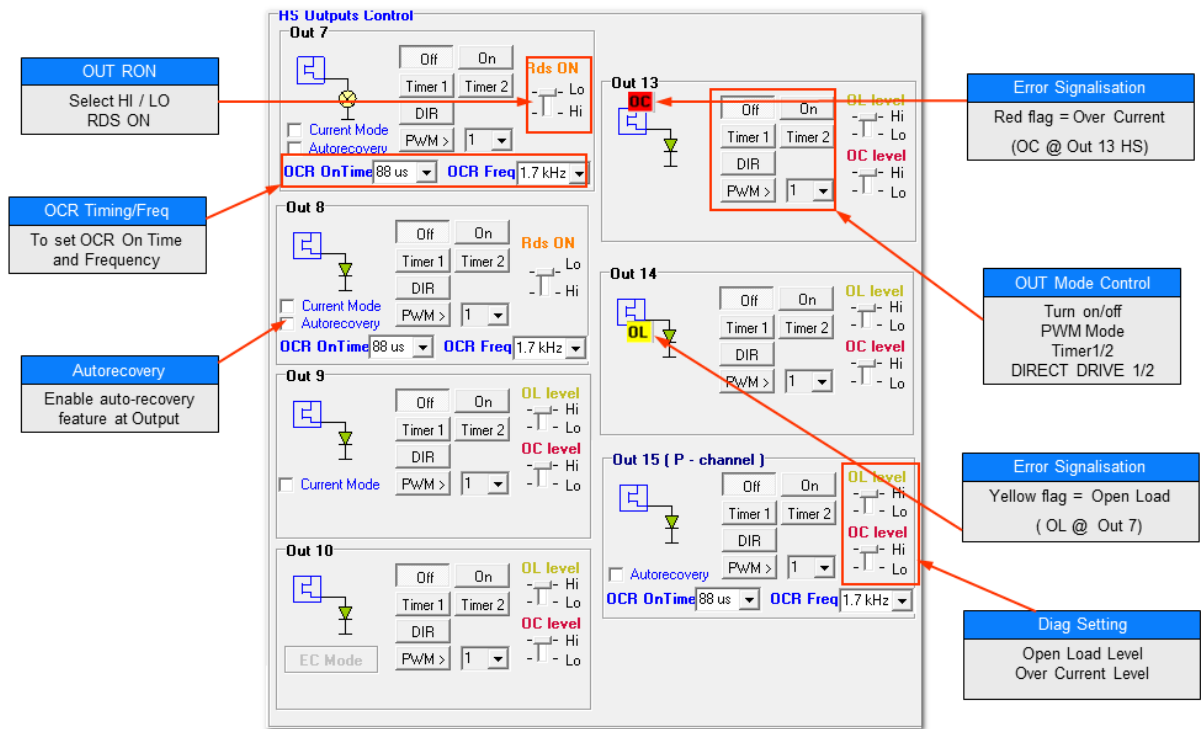
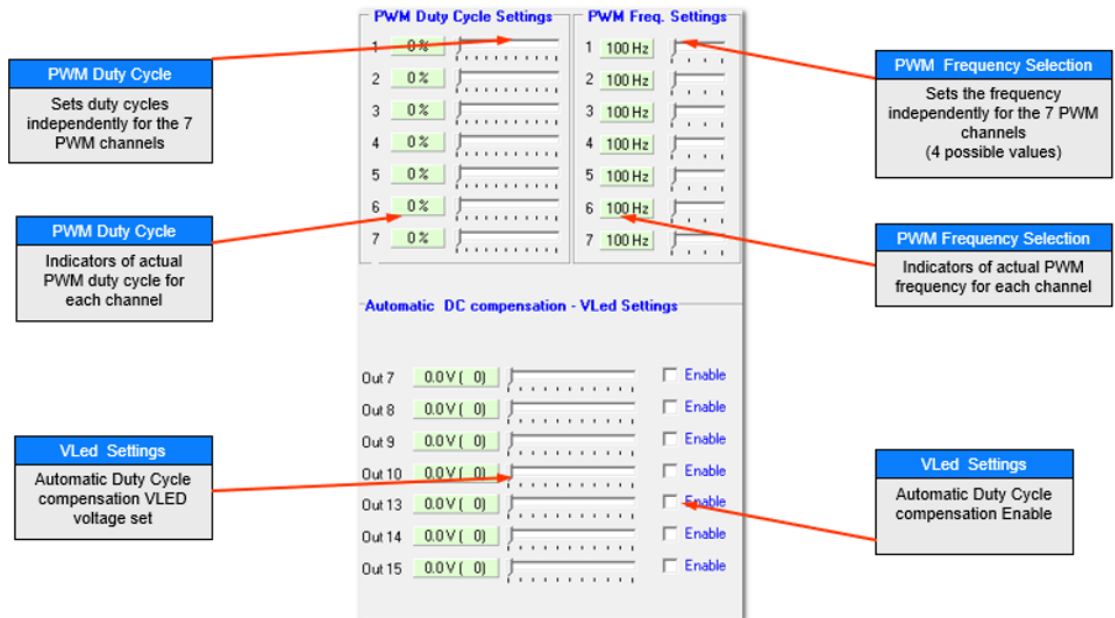
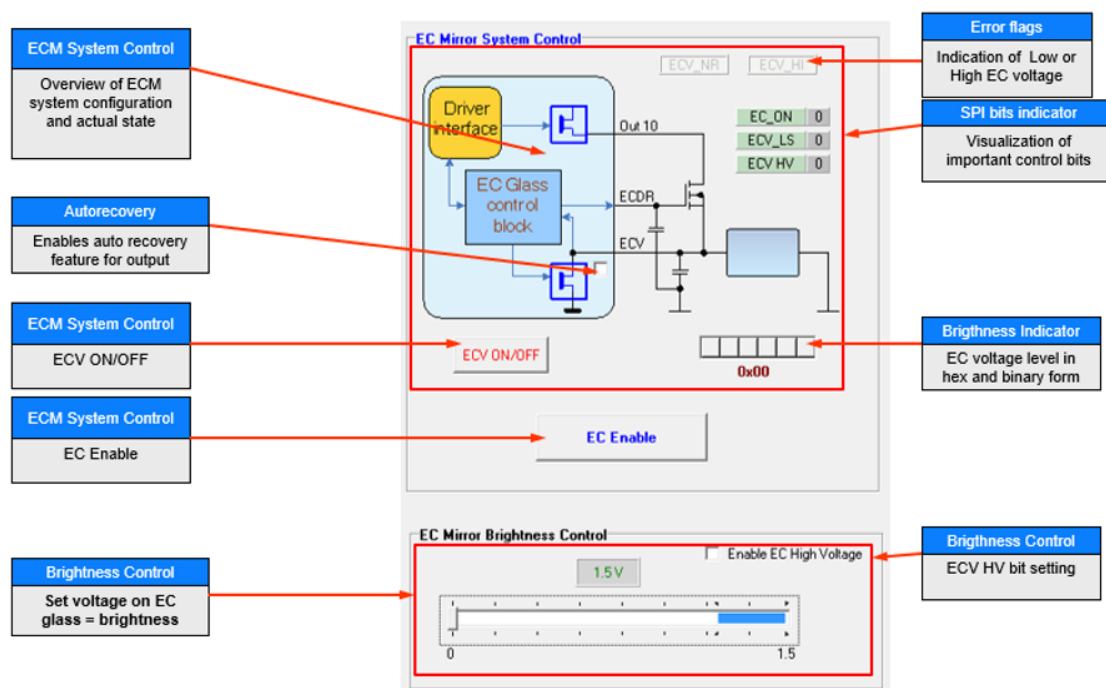


Figure 20. STSW-L99DZ200 outputs control – PWN configuration / automatic DC compensation



6 Electro chrome mirror panel

Figure 21. STSW-L99DZ200 –electro-chrome mirror panel



7 H-bridges control panel

Figure 22. STSW-L99DZ200 – power H-bridge A control

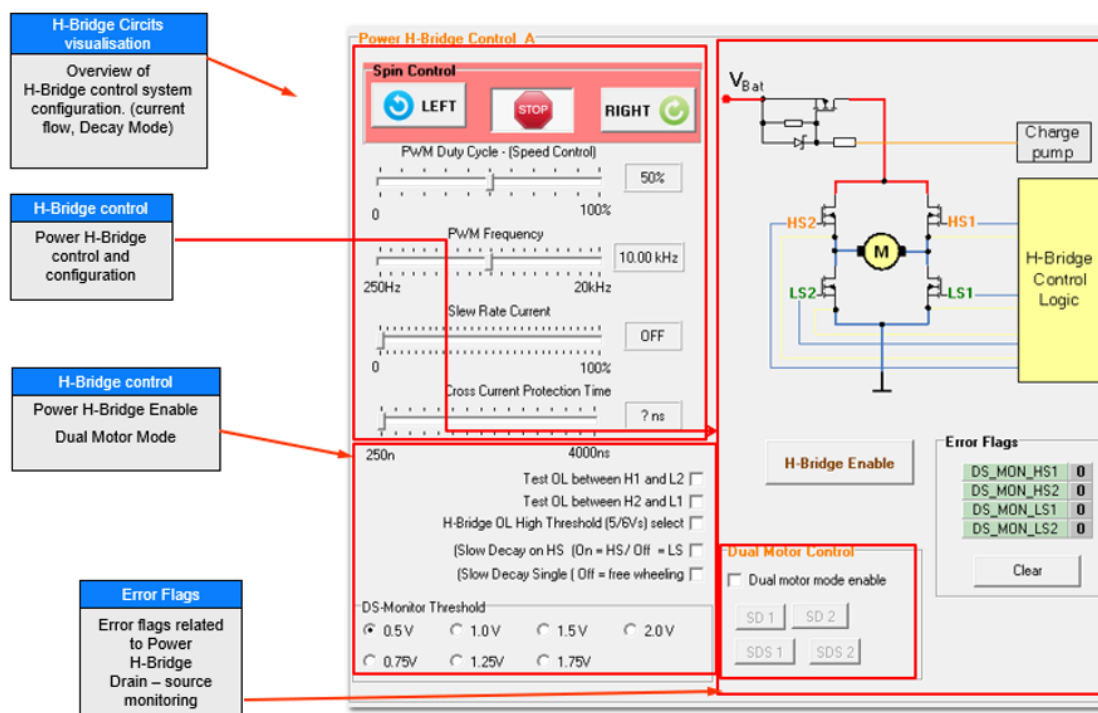
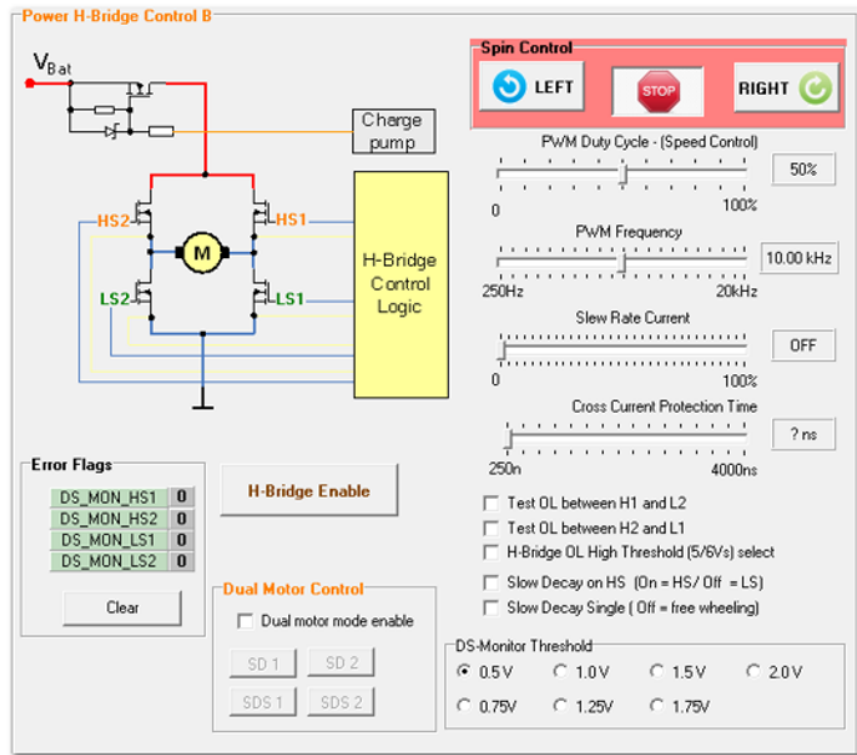
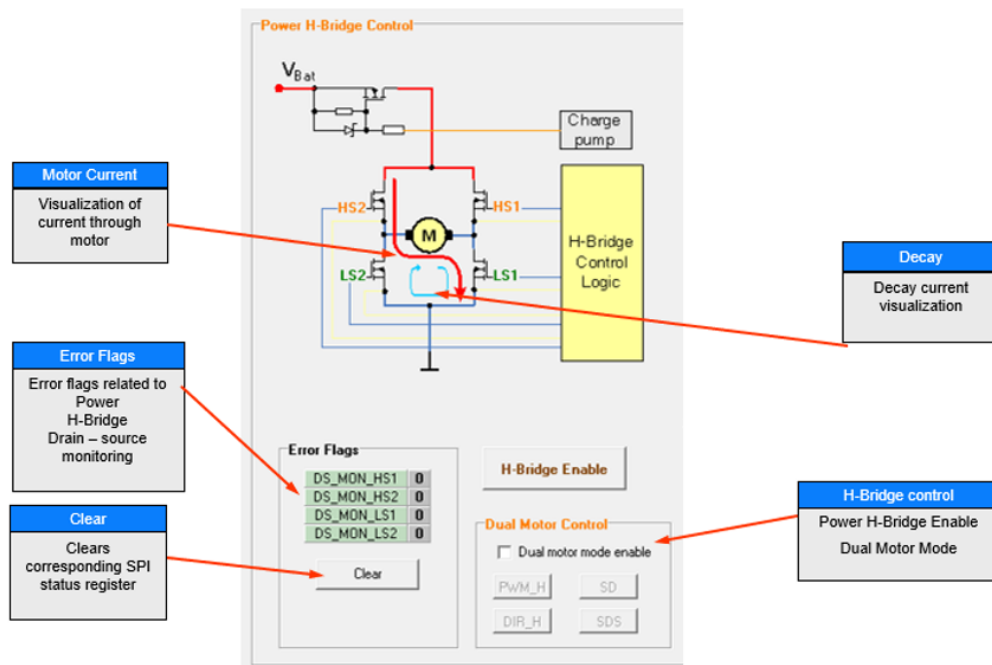


Figure 23. STSW-L99DZ200 – power H-bridge B control



H-Bridge B Controls
Similar Controls for Hbridge B are presents

Figure 24. STSW-L99DZ200 – power H-bridge A/B control



8 SPI control registers panel

Figure 25. STSW-L99DZ200 – SPI control register example

Red Color

Red color indicates values changed by user, which are not yet sent to L99DZ100P

Bold Font

Bold are marked all values what were changed from previous state (after receive from L99DZ100P)

Read/ Write Buttons

Sends / Reads the value of control register to/ from L99DZ80

Runtime Cfg.			Power On Cfg.			Half Bridge Ctrl.			HS Ou		
Control Reg. 1			Control Reg. 2			Control Reg. 3			Control Reg. 4		
Addr. 0x01			Addr. 0x02			Addr. 0x03			Addr. 0x04		Addr. 0x05
23	WU1 EN	0	23	T1 restart	0	23	VsregLock	1	23	Out7_3	0
22	WU1 PU	0	22	T1 DIR	0	22	VsLock	1	22	Out7_2	0
21	WU1 PU	0	21	T1 on2	0	21	Vsreg0VsD	1	21	Out7_1	0
20	WU1 PU	0	20	T1 on1	0	20	VsregUvSd	1	20	Out7_0	0
19	WU1 filter	0	19	T1 on0	0	19	Vs0VsD	1	19	Out8_3	0
18	WU1 filter	0	18	T1 per2	0	18	VsUvSd	1	18	Out8_2	0
17	WU1 filter	0	17	T1 per1	1	17		0	17	Out8_1	0
16	WU1 filter	0	16	T1 per0	0	16		0	16	Out8_0	0
15	Tmr Sel	0	15	T2 restart	0	15		0	15		0
14	Tmr WU	0	14	T2 DIR	0	14		0	14		0
13	LIN WU	1	13	T2 on2	0	13		0	13	Out3 HS	0
12	CAN WU	1	12	T2 on1	0	12		0	12	Out3 LS	0
11	C-TolrqEn	1	11	T2 on0	0	11		0	11	Out10_3	0
10	C-RxEn	0	10	T2 per2	0	10		0	10	Out10_2	0
9	C-TxEn	0	9	T2 per1	0	9	VsregEW_9	0	9	Out10_1	0
8	C-TxRdy	0	8	T2 per0	0	8	VsregEW_8	0	8	Out10_0	0
7	SWEN	0	7	LIN TxDis	0	7	VsregEW_7	0	7		0
6	HEN	0	6	LIN TxTO	1	6	VsregEW_6	0	6		0
5	V21	0	5	CAN loop	0	5	VsregEW_5	0	5	Out5 HS	0
4	V20	0	4	PNW EN	0	4	VsregEW_4	0	4	Out5 LS	0
3	Parity	0	3	V1 res	0	3	VsregEW_3	0	3	GH	0
2	Stby Sel	0	2	V1 res	0	2	VsregEW_2	0	2	OutHS_3	0
1	GO_Stby	0	1	WD time	0	1	VsregEW_1	0	1	OutHS_2	0
0	Trig	1	0	WD time	0	0	VsregEW_0	0	0	OutHS_1	0
										OutHS_0	0

0x403801
0x020040
0xc0000
0x000000
0x000000

RD WR

RD WR

RD WR

RD WR

RD WR

Control Registers

Control Registers Names and Addresses

Value change

Click to any of these fields to change Register value (available for all control registers)

CR Byte Value

Hexadecimal Value of the register

9 SPI status registers panel

Figure 26. STSW-L99DZ200 – SPI status register example

Status Registers

Status Registers Names and Addresses

Status Reg1				Status Reg2				Status Reg3				Status Reg4				Status Reg5				Status Reg6											
Addr. 0x31				Addr. 0x32				Addr. 0x33				Addr. 0x34				Addr. 0x35				Addr. 0x36											
23	-	0	23	LN perm dom	0	23	Out1H OC ThEx	0	23	Out1H OC ThEx	0	23	Out1H OC ThEx	0	23	Out1H OL	0	23	WdsL1	0	23	WdsL0	0	23	WdsL0	0					
22	WU1 state	0	22	LN Tx0 dom	0	22	Out1L OC ThEx	0	22	Out1L OC ThEx	0	22	Out1L OC ThEx	0	22	Out1L OL	0	22	WdsL1	0	22	WdsL0	0	22	WdsL0	0					
21	-	0	21	LN perm. rec	0	21	Out2H OC ThEx	0	21	Out2H OC ThEx	0	21	Out2H OC ThEx	0	21	Out2H OL	0	21	-	0	21	-	0	21	-	0					
20	Wake WU1	0	20	CAN Rx0 rec	0	20	Out2L OC ThEx	0	20	Out2L OC ThEx	0	20	Out2L OC ThEx	0	20	Out2L OL	0	20	-	0	20	-	0	20	-	0					
19	Wake CAN	0	19	CAN perm rec	0	19	Out3H OC ThEx	0	19	Out3H OC ThEx	0	19	Out3H OC ThEx	0	19	Out3H OL	0	19	-	0	19	-	0	19	-	0					
18	Wake LIN	0	18	CAN perm dom	0	18	Out3L OC ThEx	0	18	Out3L OC ThEx	0	18	Out3L OC ThEx	0	18	Out3L OL	0	18	-	0	18	-	0	18	-	0					
17	WK Timer	0	17	CAN Tx0 dom	0	17	Out6H OC ThEx	0	17	Out6H OC ThEx	0	17	Out6H OC ThEx	0	17	Out6H OL	0	17	ECV NR	0	17	ECV NR	0	17	ECV NR	0					
16	Debug Mode	0	16	CAN supp Low	0	16	Out6L OC ThEx	0	16	Out6L OC ThEx	0	16	Out6L OC ThEx	0	16	Out6L OL	0	16	ECV H	0	16	ECV H	0	16	ECV H	0					
15	V1 UV	0	15	DS mon HS2	0	15	Out7 OC ThEx	0	15	Out7 OC ThEx	0	15	Out7 OC ThEx	0	15	Out7 OL ST	0	15	-	0	15	-	0	15	-	0					
14	V1 rstst_2	0	14	DS mon HS1	0	14	Out8 OC ThEx	0	14	Out8 OC ThEx	0	14	Out8 OC ThEx	0	14	Out8 OL ST	0	14	-	0	14	-	0	14	-	0					
13	V1 rstst_1	0	13	DS mon LS2	0	13	Out9 OC ThEx	0	13	Out9 OC ThEx	0	13	Out9 OC ThEx	0	13	Out9 OL ST	0	13	TW 6	0	13	TW 6	0	13	TW 6	0					
12	V1 rstst_0	0	12	DS mon LS1	0	12	Out10 OC Stat	0	12	Out10 OC Stat	0	12	Out10 OC Stat	0	12	Out10 OL ST	0	12	TW 5	0	12	TW 5	0	12	TW 5	0					
11	WDFail_3	0	11	SPI inv. CMD	0	11	Out13 OC Stat	0	11	Out13 OC Stat	0	11	Out13 OC Stat	0	11	Out13 OL ST	0	11	TW 4	0	11	TW 4	0	11	TW 4	0					
10	WDFail_2	0	10	SPI clk cnt	0	10	Out14 OC Stat	0	10	Out14 OC Stat	0	10	Out14 OC Stat	0	10	Out14 OL ST	0	10	TW 3	0	10	TW 3	0	10	TW 3	0					
9	WDFail_1	0	9	CP low	0	9	Out15 OC ThEx	0	9	Out15 OC ThEx	0	9	Out15 OC ThEx	0	9	Out15 OL ST	0	9	TW 2	0	9	TW 2	0	9	TW 2	0					
8	WDFail_0	0	8	TW	0	8	-	0	8	-	0	8	-	0	8	GH OL	0	8	TW 1	0	8	TW 1	0	8	TW 1	0					
7	Dev State_1	0	7	V2 SC	0	7	DSMon_HS2_B	0	7	Out1_HS_Sht	0	7	ECV OL	0	7	-	0	7	-	0	7	-	0	7	-	0					
6	Dev State_0	0	6	V2 fail	0	6	DSMon_HS1_B	0	6	Out1_LS_Sht	0	6	-	0	6	-	0	6	-	0	6	-	0	6	-	0					
5	TDS2	0	5	V1 fail	0	5	DSMon_LS2_B	0	5	Out2_HS_Sht	0	5	-	0	5	-	0	5	TSD 6	0	5	TSD 6	0	5	TSD 6	0					
4	TDS1	0	4	Vreg EVW	0	4	DSMon_LS1_B	0	4	Out2_LS_Sht	0	4	-	0	4	-	0	4	TSD 5	0	4	TSD 5	0	4	TSD 5	0					
3	FSleep TSD2	0	3	Vreg OV	0	3	-	0	3	Out3_HS_Sht	0	3	-	0	3	-	0	3	TSD 4	0	3	TSD 4	0	3	TSD 4	0					
2	FSleep WD	0	2	Vreg UV	0	2	-	0	2	Out3_LS_Sht	0	2	-	0	2	-	0	2	TSD 3	0	2	TSD 3	0	2	TSD 3	0					
1	WD Fail	0	1	Vs OV	0	1	LSB_FSO_OC	0	1	Out6_HS_Sht	0	1	Ex_Mt_Hest	0	1	TSD 2	0	1	TSD 2	0	1	TSD 2	0	1	TSD 2	0					
0	RCR	0	0	Vs INV	0	0	LSA_FSO_OC	0	0	Out6_LS_Sht	0	0	Ex_FOC	0	0	TSD 1	0	0	TSD 1	0	0	TSD 1	0	0	TSD 1	0					
R				C				R				C				R				C				R				C			
0x000000				0x000000				0x000000				0x000000				0x000000				0x000000				0x000000				0x000000			

Status Registers

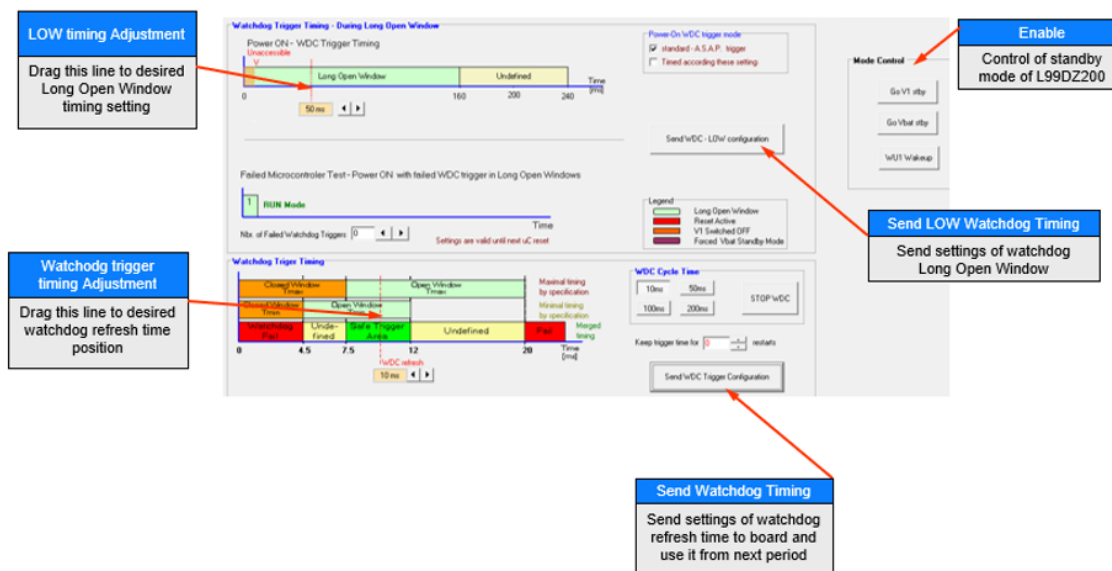
Actual Content of the register

Read / Clear Buttons

Reads or Reads and Clear values of L99DZ200 selected status register

10 Watchdog/POR settings panel

Figure 27. STSW-L99DZ200 – watchdog/POR settings



11 **Reference documents**

- L99DZ200G datasheet, DS13220.
- EVAL-L99DZ200 Data brief, DB4431.

Revision history

Table 1. Document revision history

Date	Version	Changes
16-Jun-2021	1	Initial release.

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