Getting started with the STEVAL-L6982NDR synchronous step-down switching regulator evaluation board based on the L6982NDR

Introduction

The STEVAL-L6982NDR evaluation board is based on the L6982NDR synchronous monolithic step-down regulator capable of delivering up to 2 A DC to the load.

Its wide input voltage range makes the device suitable for a broad range of applications.

The device implements peak current mode architecture in a SO 8L package with internal compensation to minimize design complexity and size.

The L6982 is available both in low consumption mode (LCM) and low noise mode (LNM) versions.

LCM maximizes efficiency at light-load with controlled output voltage ripple, which is ideal for battery-powered applications.

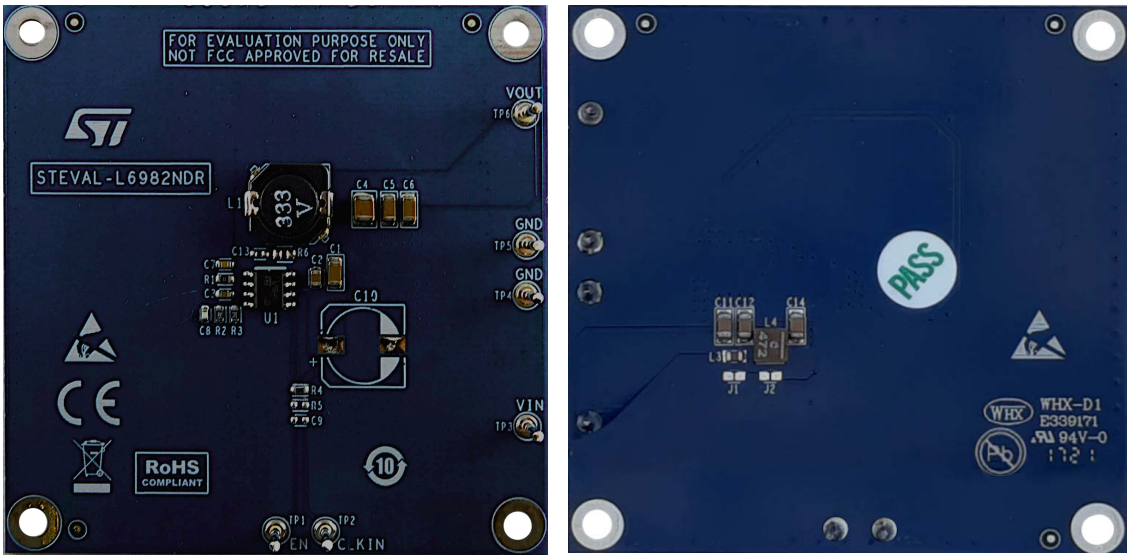
LNM makes the switching frequency constant and minimizes the output voltage ripple overload current range, meeting the specification for noise sensitive applications.

The EN pin provides enable/disable function. The typical shutdown current is 2 µA when disabled.

When the EN pin is pulled up, the device is enabled and the internal 1.3 ms soft start takes place.

Pulse-by-pulse current sensing on both power elements implements effective constant current protection and thermal shutdown prevents thermal run-away.

Figure 1. STEVAL-L6982NDR evaluation board (top and bottom views)



1 Getting started

1.1 Safety precautions

Caution: All operations involving transportation, installation, use and maintenance of the board must be performed by skilled technical personnel who is familiar with the installation, use and maintenance of power electronic systems.

A system architecture that supplies power to the evaluation board must be equipped with additional control and protective devices in accordance with the applicable safety requirements (i.e., compliance with technical equipment and accident prevention rules).

The electrical installation shall be completed in accordance with the appropriate requirements (e.g., cross-sectional areas of conductors, fusing, and GND connections).

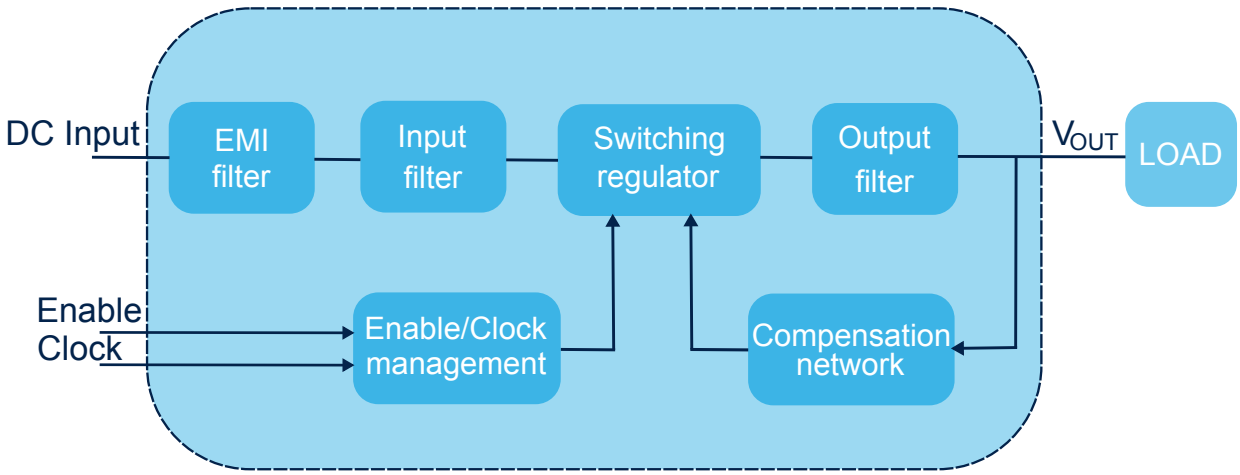
1.2 Overview

The STEVAL-L6982NDR features:

- 3.5 V to 38 V operating input voltage
- Programmable output voltage from 0.85 V to VIN
- 3.3 V and 5 V fixed output voltage versions
- 2 A DC output current
- Low operating quiescent current (LCM and fixed Vout part numbers)
- Internal compensation network
- Two different versions: LCM for high efficiency at light loads and LNM for noise sensitive applications
- 2 µA shutdown current
- Internal soft start
- Enable function
- Overvoltage protection
- Output voltage sequencing
- Thermal protection
- SO 8L package
- Synchronization to external clock for LNM devices

1.3 Block diagram

Figure 2. STEVAL-L6982NDR functional block diagram



1.4 Connectors and test points

- **V_{IN} - Tp3**: connect to the positive terminal of a supply voltage (from 6 V to 38 V with default 5 V V_{OUT}). Input voltage is filtered (see Section 1.5) to decrease the EMI. Supply voltage should be set with a current limitation compatible with the power board request. Typically, $I_{limit} > V_{OUT} \times I_{OUT}/V_{IN}$.
- **GND - Tp4, Tp5**: return of terminal of input and output capacitors.
- **V_{OUT} - Tp6**: connect to the positive terminal of the active load or to a power resistor between V_{OUT} and GND.

Important:
For all the above connections, short wires are recommended to avoid oscillation between the cable parasitic inductance and the input capacitor.

- **ENABLE**: the device starts the switching activity once the Enable pin rises over the wake-up threshold (1.2 V); thus, defining R4/R5 resistor ratio, it is possible to program the UVLO threshold. By default, the STEVAL-L6982NDR Enable pin is pulled up to V_{IN} with R4 = 10 K and R5 not mounted. Consequently, it is possible to disable the output voltage regulation driving the Enable test point to GND. Vice versa the system starts up once the Enable test point is left floating.

  For further details, see L6982 datasheet.
- **CLK_IN** : using L6982NDR (low noise mode), it is possible to synchronize with an external clock.

  For further details, see L6982 datasheet.

1.5 Input EMI filter

The STEVAL-L6982NDR is compliant with CISPR16-4-2.

An input filter helps to reduce EMI. The filter consists of a ferrite bead (L3), an inductor (L4) and three ceramic capacitors (C11, C12 and C14).

An electrolytic capacitor is used for bulk energy storage and input damping.

1.6 V_{OUT} settings

By default, the STEVAL-L6982NDR is with V_{OUT} = 5 V but the output voltage can be managed from 0.85 V to a higher voltage by selecting the right output partition resistors (R2 and R3):

$V_{OUT} = (R2 + R3)/R3 \times V_{FB}$

where V_{FB} is the fix to 0.85 V.

Once V_{OUT} has been changed, it is possible to increase the system performance in term of bandwidth.

We recommend eDesignSuite to select the compensation value (C8, R2 and R3), inductors and C_{OUT} value.

1.6.1 eDesignSuite

The eDesignSuite software tool developed by STMicroelectronics helps you configure ST products for power conversion applications.

You can use it to customize your board for a specific application. After entering the main specifications for your design, you can generate an automatic design or follow a sequential process to build a highly customized design.

2 How to use the board

The STEVAL-L6982NDR is configured with L6982 LNM with adjustable V_{OUT}. It is set to deliver a 5 V output voltage with F_{SW} = 400 KHz.

This board is best suited for applications where low output ripple is preferred to high efficiency at low current.

Step 1. Connect the voltage supply between V_{IN} and GND connectors.

Step 2. Connect the load (power resistor or active load) between V_{OUT} and GND connectors.

Note: For Step 1 and Step 2 short wires are recommended.

Step 3. Set the supply voltage V_{IN} from 6 V to 38 V.

Step 4. By default V_{OUT} is set to 5 V. Increase or decrease the output power resistor or active load to reach the suitable output current (max. 2 A).

Note: Using L6982CDR, from 0 A to 0.2 A the board works in PSK mode to guarantee high efficiency performance.

3 PCB layout

Figure 3. **STEVAL-L6982NDR evaluation board - PCB layout (top layer)**

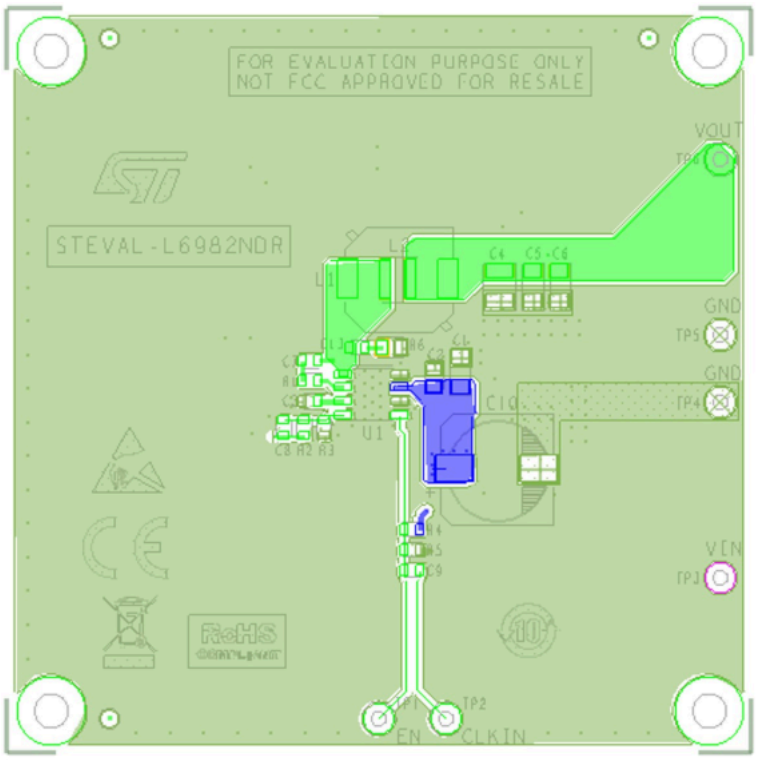
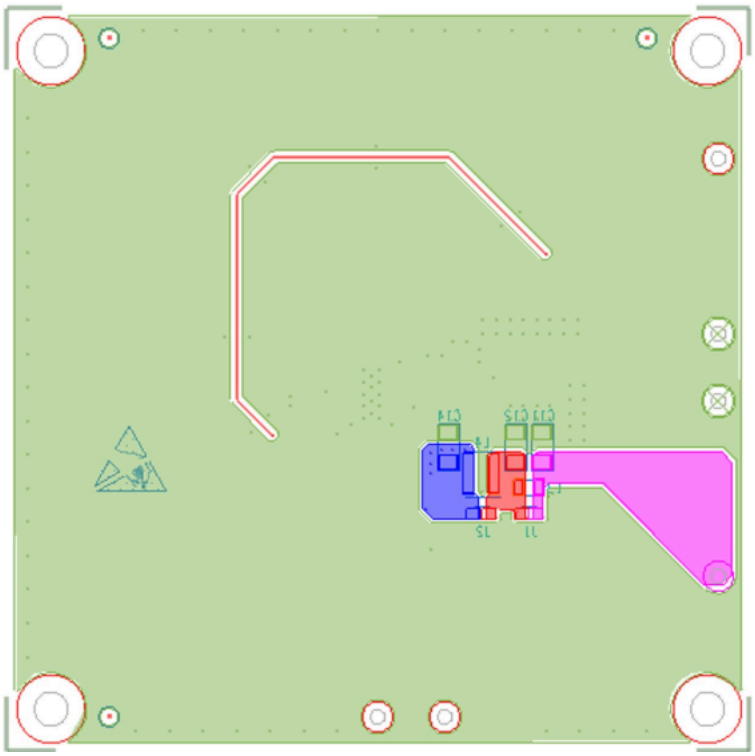
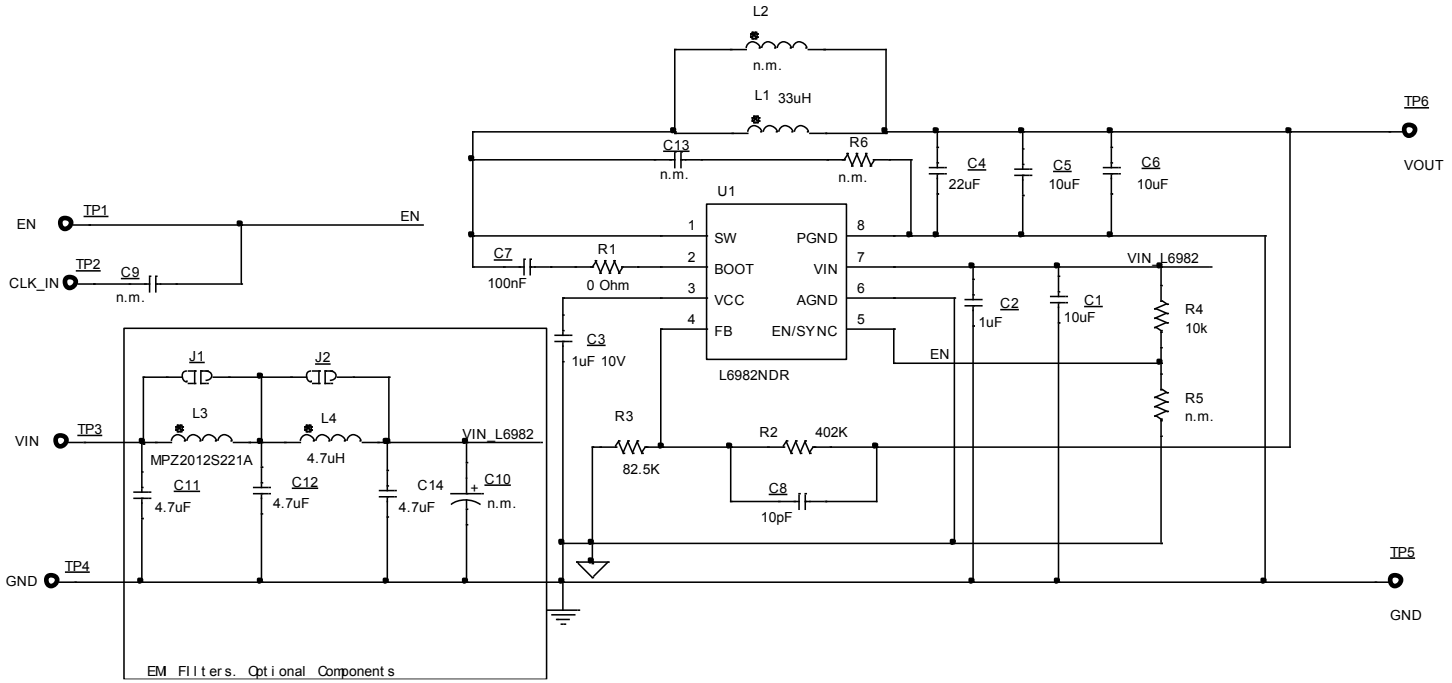


Figure 4. **STEVAL-L6982NDR evaluation board - PCB layout (bottom layer)**



4 Schematic diagrams

Figure 5. **STEVAL-L6982NDR circuit schematic**



5 Bill of materials

Table 1. **STEVAL-L6982NDR bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	C1	10µF, 1206(3216 Metric), 50V, +/-10%	Input capacitor	TDK	C3216X7R1H106K160AC
2	1	C2	1µF, 0805(2012 metric), 50V, +/-10%	Input capacitor	TDK	CGA4J3X7R1H105K125AB
3	1	C3	1µF, 0603 (1608 metric), 10V, +/-10%	Vcc capacitor	Any	
4	1	C4	22µF, 1210 (3225 metric), 25V, +/-10%	Vout capacitor	Murata	GRJ32EC71E226KE11
5	2	C5, C6	10µF, 1206(3216 Metric), 50V, +/-10%	Vout capacitors	TDK	C3216X7R1H106K160AC
6	1	C7	100nF, 0603 (1608 metric), 50V, +/-10%	Boot capacitor	Any	
7	1	C8	10pF, 0603 (1608 metric), 50V, +/-10%	Feed forward capacitor	Any	
8	1	C9	0603 (1608 metric)	CLKIN capacitor (not mounted)	Any	
9	1	C10	10x10mm	Pi filter capacitor (not mounted)	Any	
10	3	C11,C12,C14	4.7µF, 1206(3216 Metric), 50V, +/-10%	Pi filter capacitors	Murata	GRM31CR71H475KA12
11	1	C13	0603 (1608 metric)	Snubber capacitor not mounted)	Any	
12	1	L1	33µH, MSS 1038 family, +/-20%	Main Inductor	Coilcraft	MSS1038T-333ML
13	1	L2	XAL4040 family	Main Inductor (not mounted)	Any	
14	1	L3	220 Ω 100 MHz, 0805(2012 metric), +/-25%	Ferrite bead	TDK	MPZ2012S221AT000
15	1	L4	4.7µH, XAL4040 family, +/-20%	Pi filter Inductor	Coilcraft	XAL4030-472ME
16	1	R1	0 Ω, 0603 (1608 metric)	Boot resistor	Any	
17	1	R2	402KΩ, 0603 (1608 metric), +/-1%	FB partition HS resistor	Any	

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
18	1	R3	82.5KΩ, 0603 (1608 metric), +/-1%	FB partition LS resistor	Any	
19	1	R4	10KΩ, 0603 (1608 metric), +/-1%	EN partition HS resistor	Any	
20	1	R5	0603 (1608 metric)	EN partition LS resistor (not mounted)	Any	
21	1	R6	0805(2012 metric)	Snubber resitor (not mounted)	Any	
22	1	TP1	EN 1.3mm	Test point	Ettinger	13.14.239
23	1	TP2	CLKIN 1.3mm	Test point	Ettinger	13.14.240
24	1	TP3	VIN 1.3mm	Test point	Ettinger	13.14.241
25	1	TP4	GND 1.3mm	Test point	Ettinger	13.14.242
26	1	TP5	GND 1.3mm	Test point	Ettinger	13.14.243
27	1	TP6	VOUT 1.3mm	Test point	Ettinger	13.14.244
28	1	U1	SO8	DCDC converter	ST	L6982NDR

6 Board versions

Table 2. **STEVAL-L6982NDR versions**

Finished good	Schematic diagrams	Bill of materials
STEVAL$L6982NDRA (1)	STEVAL$L6982NDRA schematic diagrams	STEVAL$L6982NDRA bill of materials

1. *This code identifies the STEVAL-L6982NDR evaluation board first version.*

7 Regulatory compliance

Formal Notice Required by the U.S. Federal Communications Commission

FCC NOTICE:

This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

The evaluation kit has been designed to comply with part 15 of the FCC Technical Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

Standard applied: FCC CFR 47 Part 15 Subpart B. Test method applied: ANSI C63.4 (2014).

Formal Product Notice Required by Industry Canada Innovation, Science and Economic Development

Canada compliance:

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

This device has been tested with Innovation, Science and Economic Development RSS standards. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Standard applied: ICES-003 Issue 7 (2020), Class B. Test method applied: ANSI C63.4 (2014).

Cet appareil a été testé pour les normes RSS d'Innovation, Science et Développement économique. L'utilisation est soumise aux deux conditions suivantes: (1) cet appareil ne doit pas causer d'interférences nuisibles, et (2) cet appareil doit accepter de recevoir tous les types d’interférence, y comprises les interférences susceptibles d'entraîner un fonctionnement indésirable.

Norme appliquée: NMB-003, 7e édition (2020), Classe B. Méthode d'essai appliquée: ANSI C63.4 (2014).

Formal product notice required by EU

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2015/863/EU (RoHS).

Standards applied: EN 55032:2015 + A11:2020, EN 55035:2017, EN 61000-6-1 (2007), EN 61000-6-3 (2007) + A1 (2011), EN IEC 63000:2018

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
14-Sep-2021	1	Initial release.

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