Discovery kits with STM32U5x9NJ MCUs

Introduction

The STM32U5x9J-DKx Discovery kits (order codes STM32U5A9J-DK and STM32U5G9J-DK1) are complete demonstration and development platforms for the STM32U5x9NJH6Q microcontrollers, featuring an Arm® Cortex®-M33 core with Arm® TrustZone®.

Leveraging the innovative ultra-low-power oriented features, 3 Mbytes of embedded SRAM for STM32U5G9NJH6Q or 2.5 Mbytes for STM32U5A9NJH6Q, 4 Mbytes of embedded flash memory, and rich graphics features, the STM32U5x9J-DKx Discovery kits enable users to easily prototype applications with state-of-the-art energy efficiency, as well as provide stunning and optimized graphics rendering with the support of specific graphic features associated with each microcontroller.

The full range of hardware features available on the board helps users to enhance their application development by an evaluation of all the peripherals such as a 2.47-inch RGB 480 × 480 pixels TFT round LCD module with MIPI DSI® interface and capacitive touch panel, USB Type-C® HS, Octo-SPI flash memory device, Hexadeca-SPI PSRAM memory device, eMMC flash memory device, Time-of-Flight and gesture detection sensor, temperature sensor, 20-pin audio MEMS connector (for STM32U5G9J-DK1), and two 2.54 mm pitch double-row flexible expansion connectors for easy prototyping with daughterboards for specific applications (USART, LPUART, two SPIs, SAI, three I^2C, SDMMC, ADCs, timers, and GPIOs).

The STM32U5x9J-DKx Discovery kits integrate an STLINK-V3E embedded in-circuit debugger and programmer for the STM32 microcontroller with a USB Virtual COM port bridge and comes with the STM32CubeU5 MCU Package, which provides an STM32 comprehensive software HAL library as well as various software examples.

Figure 1. STM32U5G9J-DK1 top view

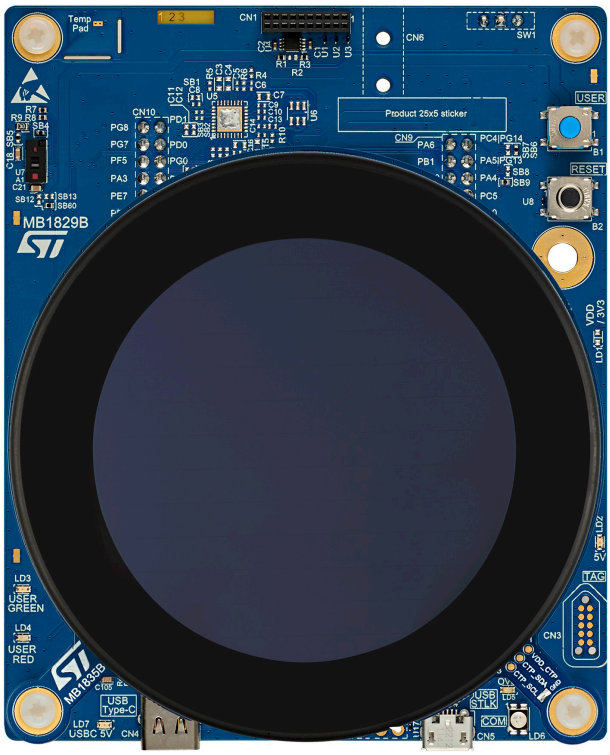
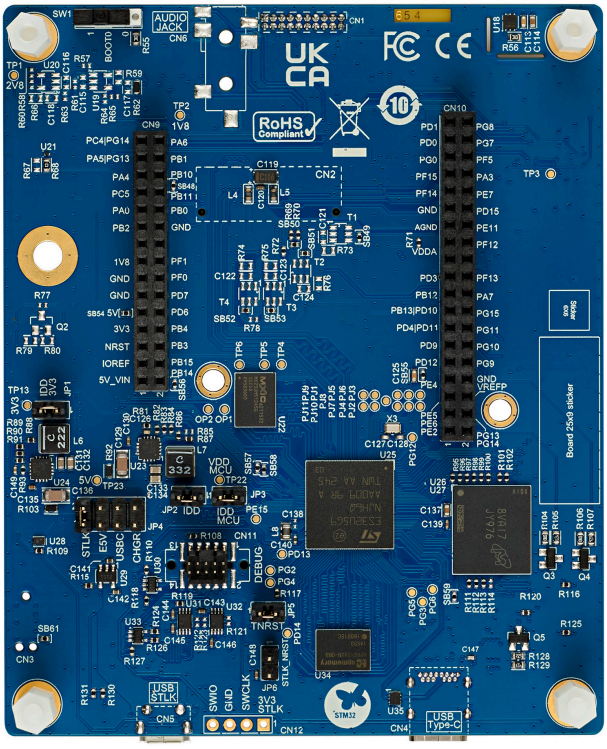


Figure 2. STM32U5G9J-DK1 bottom view



Pictures are not contractual.

1 Features

- Ultra-low-power STM32U5x9NJH6Q microcontroller based on the Arm® Cortex®-M33 core with Arm® TrustZone®, featuring 4 Mbytes of flash memory, 3 Mbytes of SRAM for STM32U5G9NJH6Q or 2.5 Mbytes for STM32U5A9NJH6Q, and SMPS in a TFBGA216 package
- 2.47" RGB 480 × 480 pixels TFT round LCD module with 16.7M color depth, with MIPI DSI® 2-data lane interface and capacitive touch panel
- USB Type-C® with USB 2.0 HS interface, sink only
- Low-power system designed for VDD at 1.8 V only
- MEMS sensors from STMicroelectronics
  - Time-of-Flight and gesture-detection sensor
  - Temperature sensor
- 512-Mbit Octo-SPI NOR flash memory
- 512-Mbit Hexadeca-SPI PSRAM
- 4-Gbyte eMMC flash memory
- Two user LEDs
- User and reset push-buttons
- Board connectors:
  - USB ST-LINK Micro-B
  - USB Type-C®
  - Two double-row 2.54 mm pitch expansion connectors for additional peripherals prototyping
  - Audio MEMS daughterboard expansion (for STM32U5G9J-DK1)
  - MIPI10
  - Tag-Connect™ 10-pin footprint
- Flexible power-supply options: ST-LINK USB V_{BUS}, USB connector, or external sources
- On-board STLINK-V3E debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeU5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

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2 Ordering information

To order the STM32U5x9J-DKx Discovery kits, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. List of available products

Order code	Board reference	Target STM32	Differentiating feature
STM32U5A9J-DK	• MB1829(1) • MB1835(2)	STM32U5A9NJH6Q	-
STM32U5G9J-DK1		STM32U5G9NJH6Q	• Audio MEMS daughterboard expansion

1. *Main board*
2. *LCD daughterboard*

2.1 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

STM32XXYYZ-DKT	Description	Example: STM32U5G9J-DK1
XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32U5 series
YY	MCU product line in the series	STM32U5F9/5G9 product line
Z	STM32 flash memory size: • J for 4 Mbytes	4 Mbytes
DK	Discovery kit	Discovery kit
T	Sequential number	First Discovery kit version

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to USB Type-C® cable
- USB Type-A or USB Type-C® to Micro-B cable

Note: *macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.*
Linux® is a registered trademark of Linus Torvalds.
Windows is a trademark of the Microsoft group of companies.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Laser consideration

The Time-of-Flight and gesture-detection sensor contains a laser emitter and the corresponding drive circuitry. The laser output is designed to remain within Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2014 (third edition). The laser output remains within Class 1 limits as long as the STMicroelectronics recommended device settings are used and the operating conditions specified in the datasheets are respected. The laser output power must not be increased by any means and no optics are used to focus the laser beam. Figure 3 shows the warning label for Class 1 laser products.

Figure 3. Class 1 laser product label

5 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

6 Quick start

Before installing and using the product, accept the Evaluation Product License Agreement from the *www.st.com/epla* webpage.

Follow the sequence below to configure the STM32U5x9J-DKx Discovery kit and launch the demonstration application (refer to Figure 5 and Figure 6 for component location):

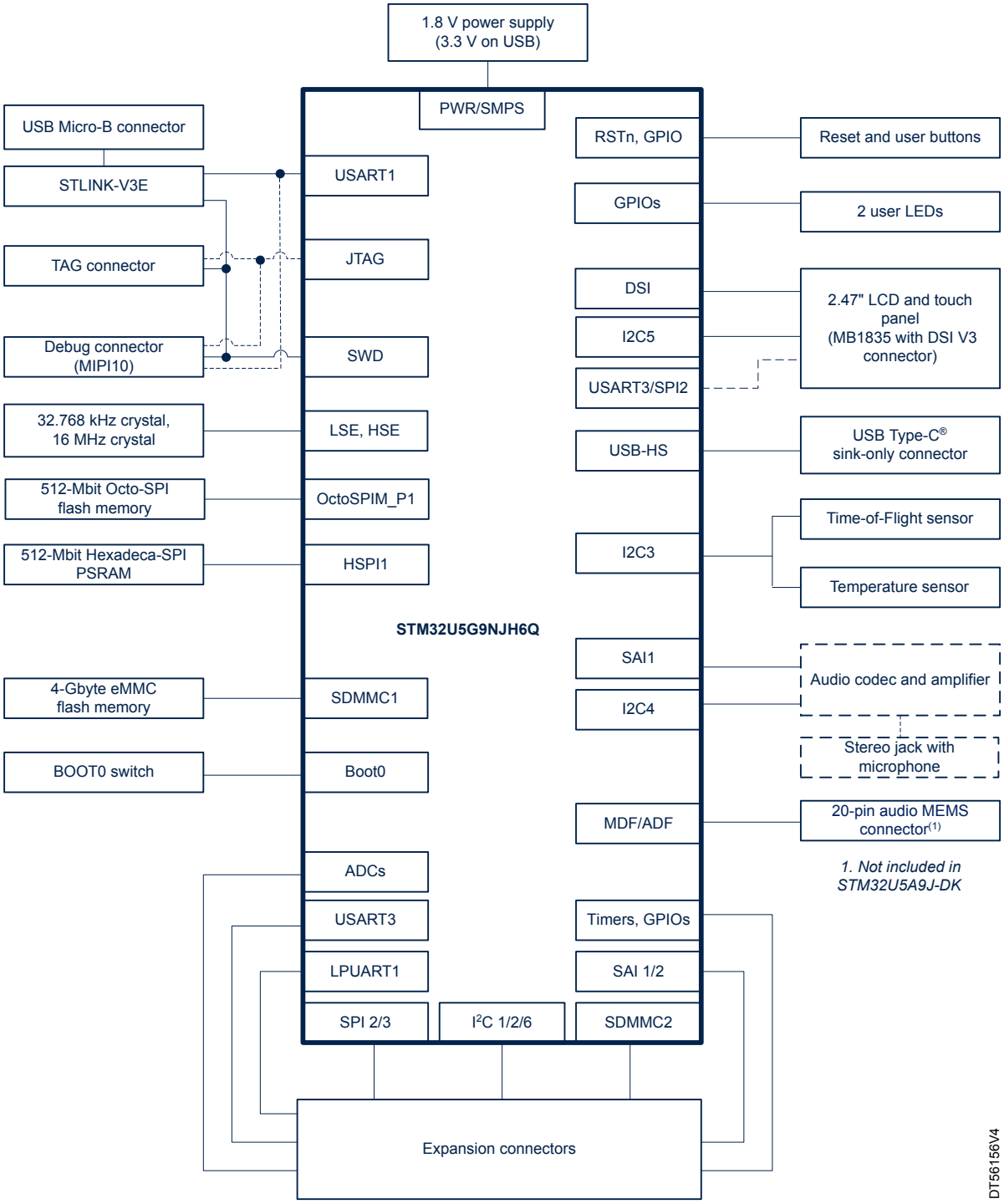
1. For the correct identification of all the device interfaces from the host PC and before connecting the kit, install the STLINK-V3 USB driver as described in the technical note *Overview of ST-LINK derivatives* (TN1235).
2. Check that jumpers JP1, JP2, JP3, and JP5 are ON, that JP4 is set on STLK, and SW1 white side switch is set to 0.
3. Connect the STM32U5x9J-DKx Discovery kit to a PC with a USB cable (USB Type-A or USB Type-C® to Micro-B) through the STLINK-V3E USB connector (CN5) to power the kit.
4. The 5V green LED (LD2) and the COM LED (LD6) light up.
5. The LCD module displays a menu with icons, indicating the demonstration application software startup.
6. The demonstration application software and its user manual, as well as other software examples for exploring STM32U5x9J-DKx features are available on the STM32CubeU5 webpage.
7. Proceed to the STLINK-V3 firmware upgrade and configuration as described in TN1235.
8. Develop your application using the available examples.

7 Hardware layout and configuration

7.1 Hardware block diagram

The STM32U5x9J-DKx Discovery kits are designed with the STM32U5x9NJH6Q microcontrollers, in a TFBGA216 package. The hardware block diagram in Figure 4 illustrates the connection between the microcontroller and the peripherals. Figure 5 and Figure 6 help to locate these features on the STM32U5G9J-DK1 Discovery main board.

Figure 4. STM32U5G9J-DK1 hardware block diagram



7.2 Main board layout

Figure 5. Main board layout (top view)

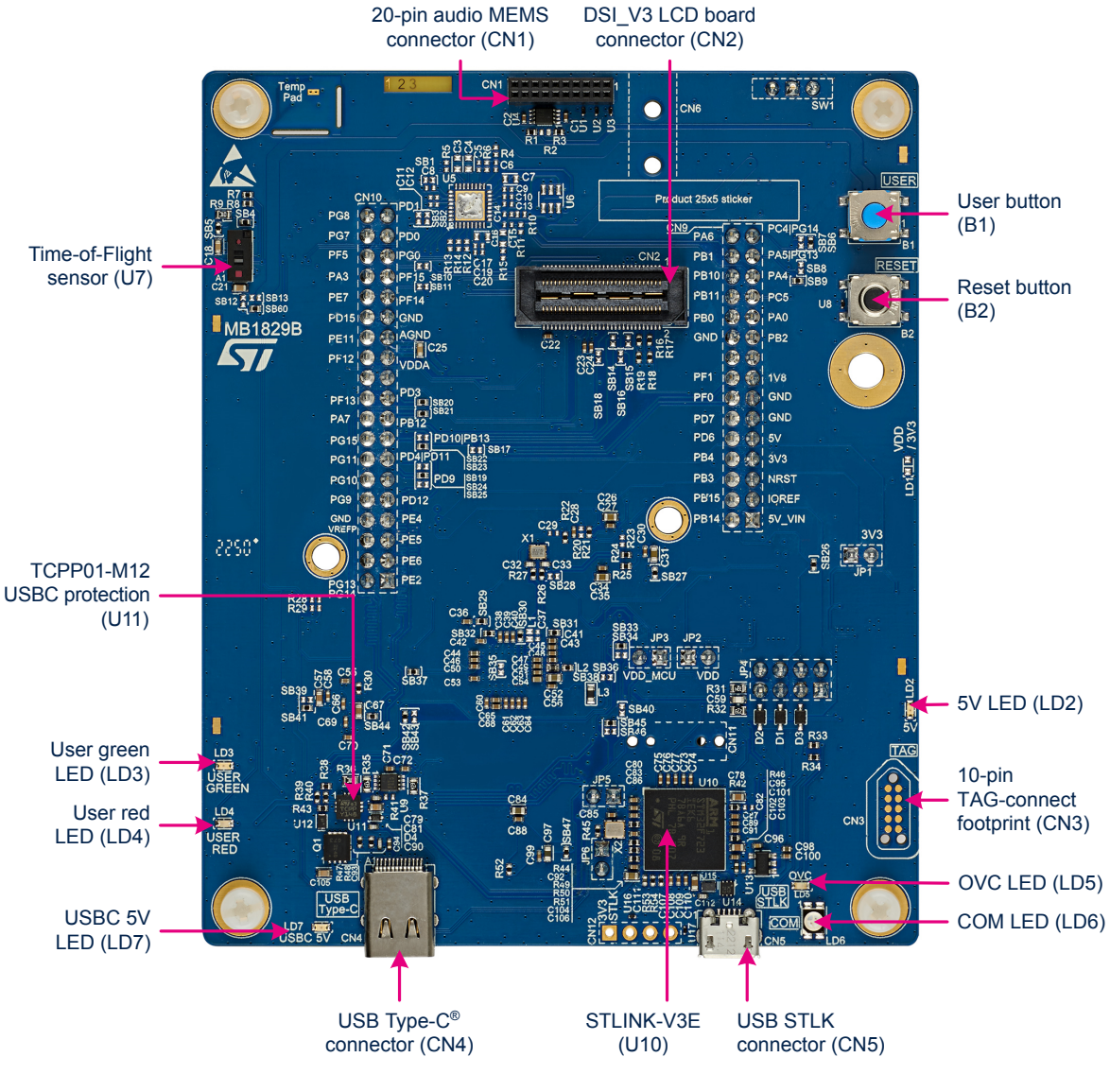


Figure 6. Main board layout (bottom view)

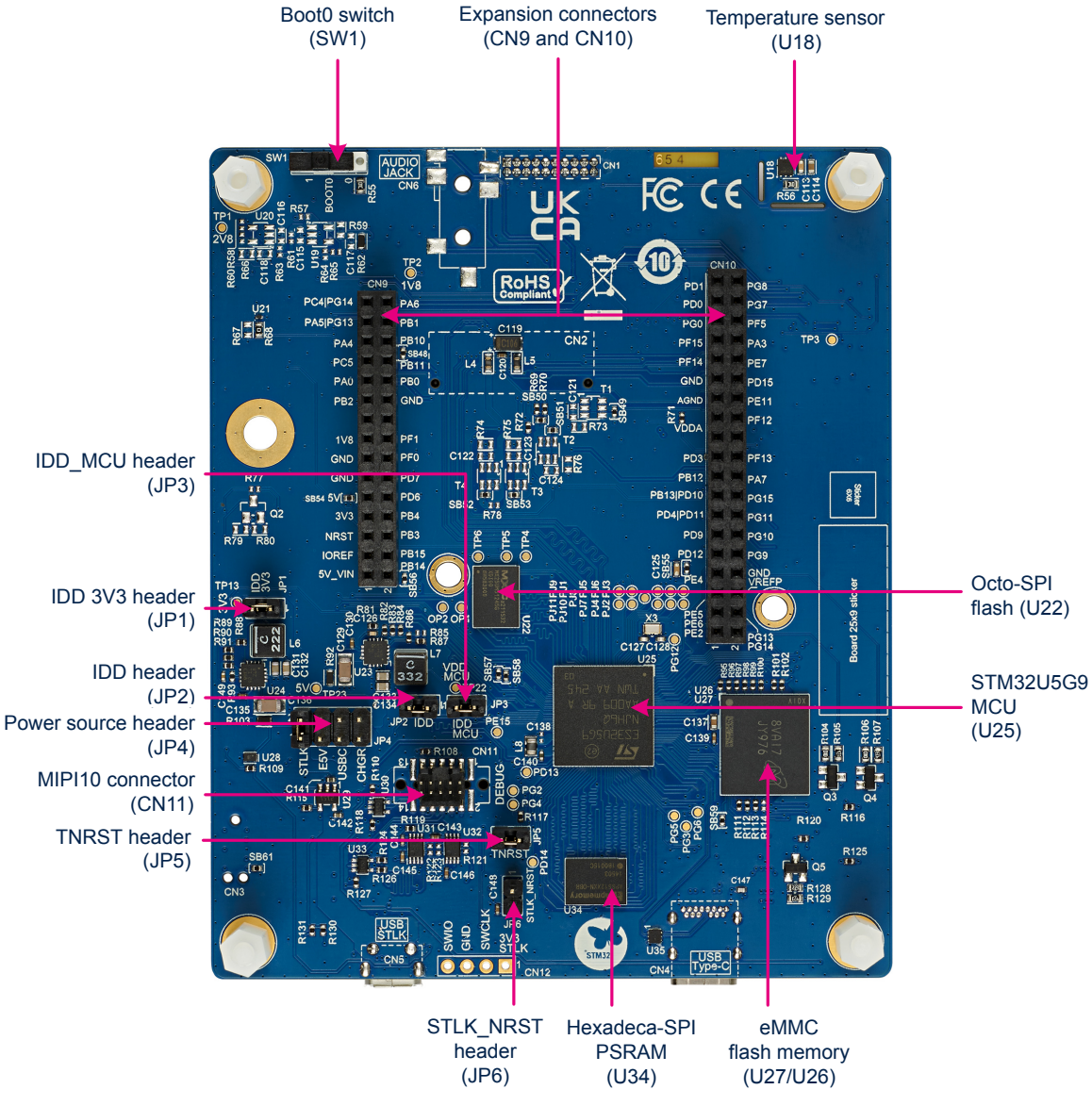


Figure 7. **LCD daughterboard layout (top view)**

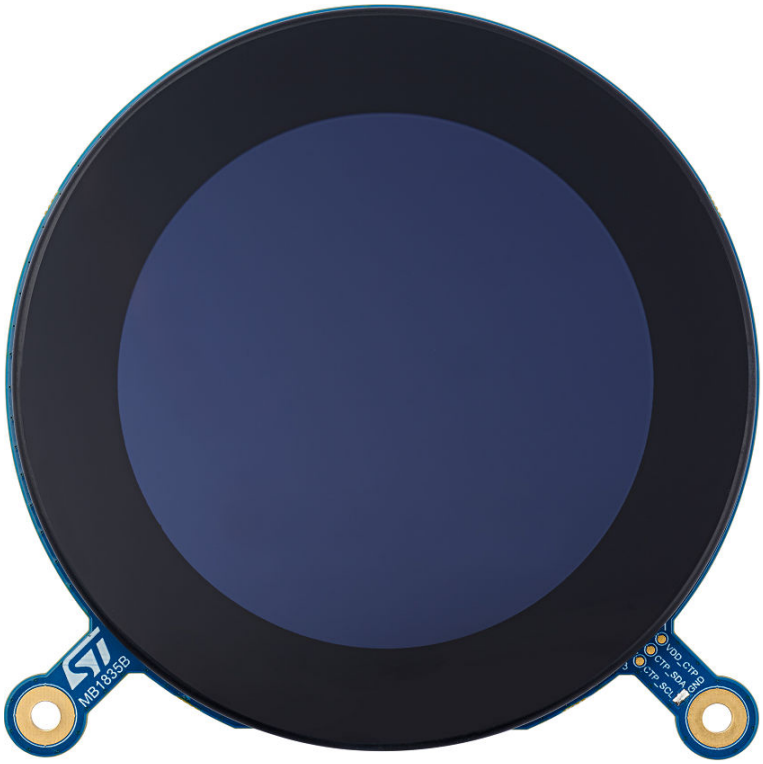
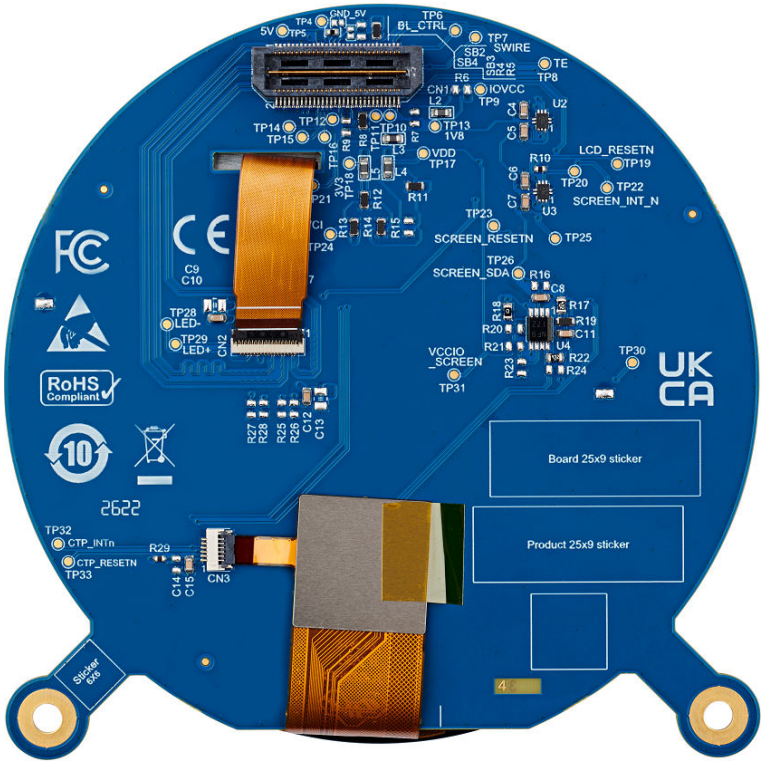


Figure 8. **LCD daughterboard layout (bottom view)**



7.3 Mechanical drawings

All measurements are in millimeters.

Figure 9. Main board top

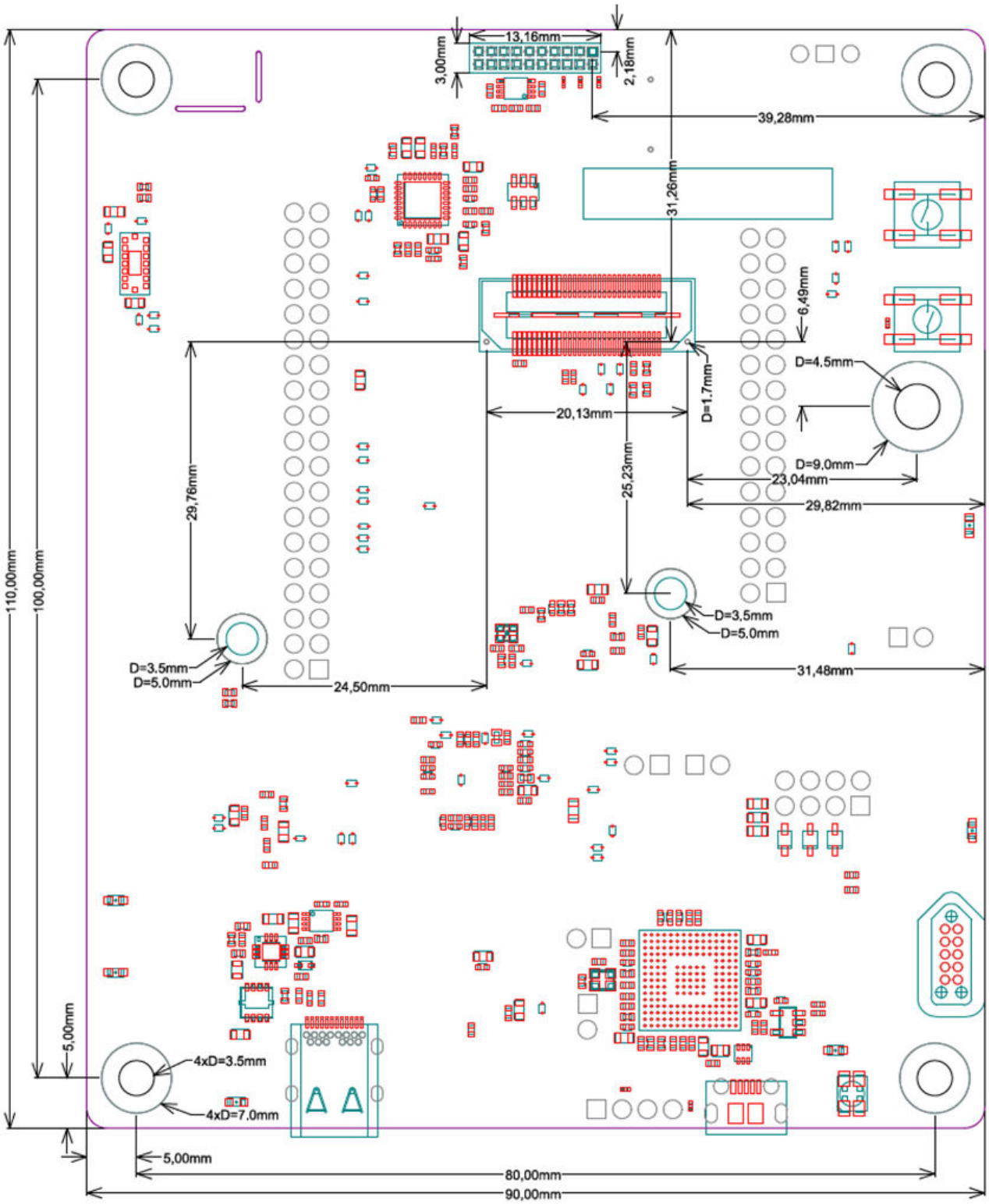


Figure 10. **Main board bottom**

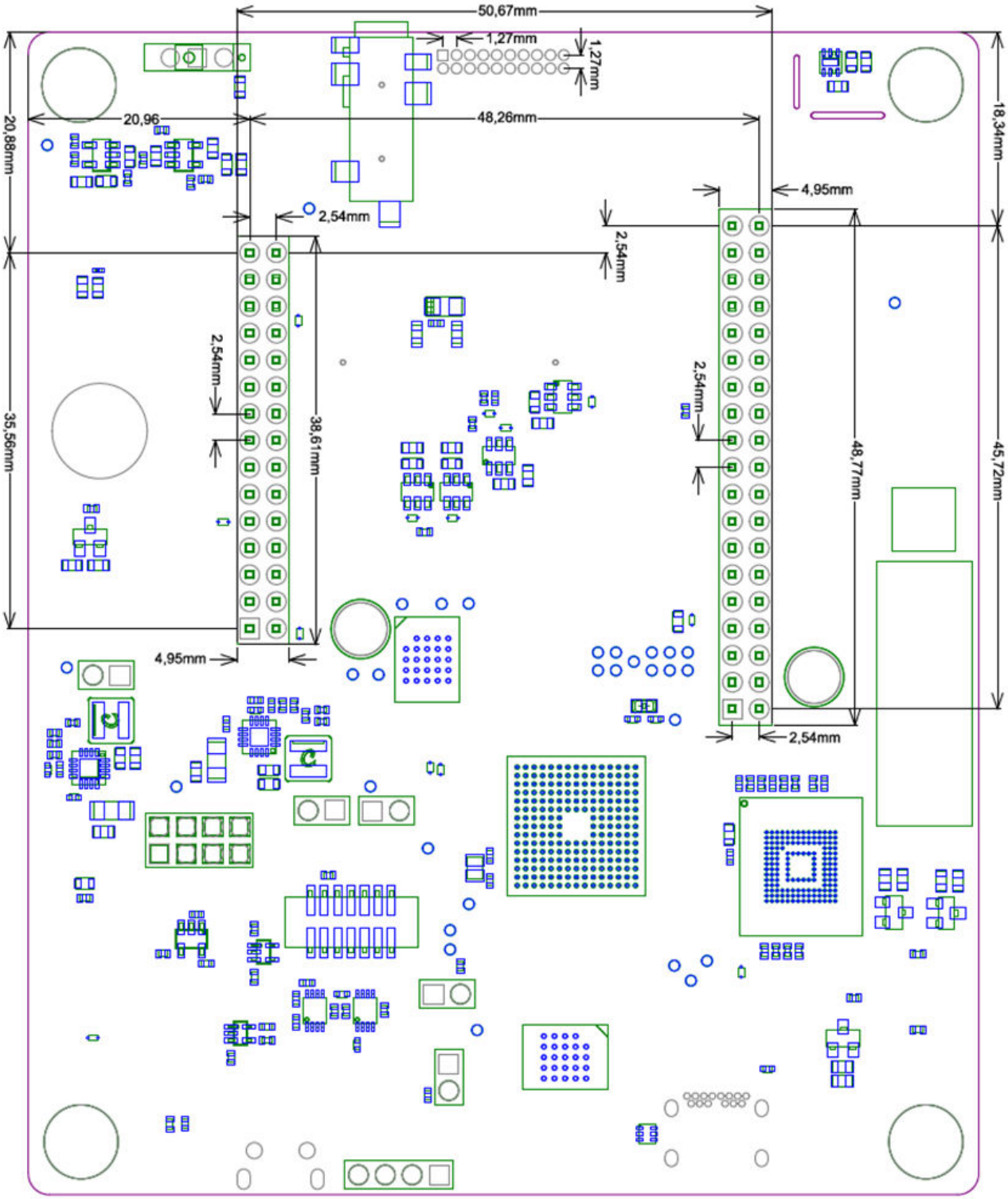


Figure 11. **LCD daughterboard top**

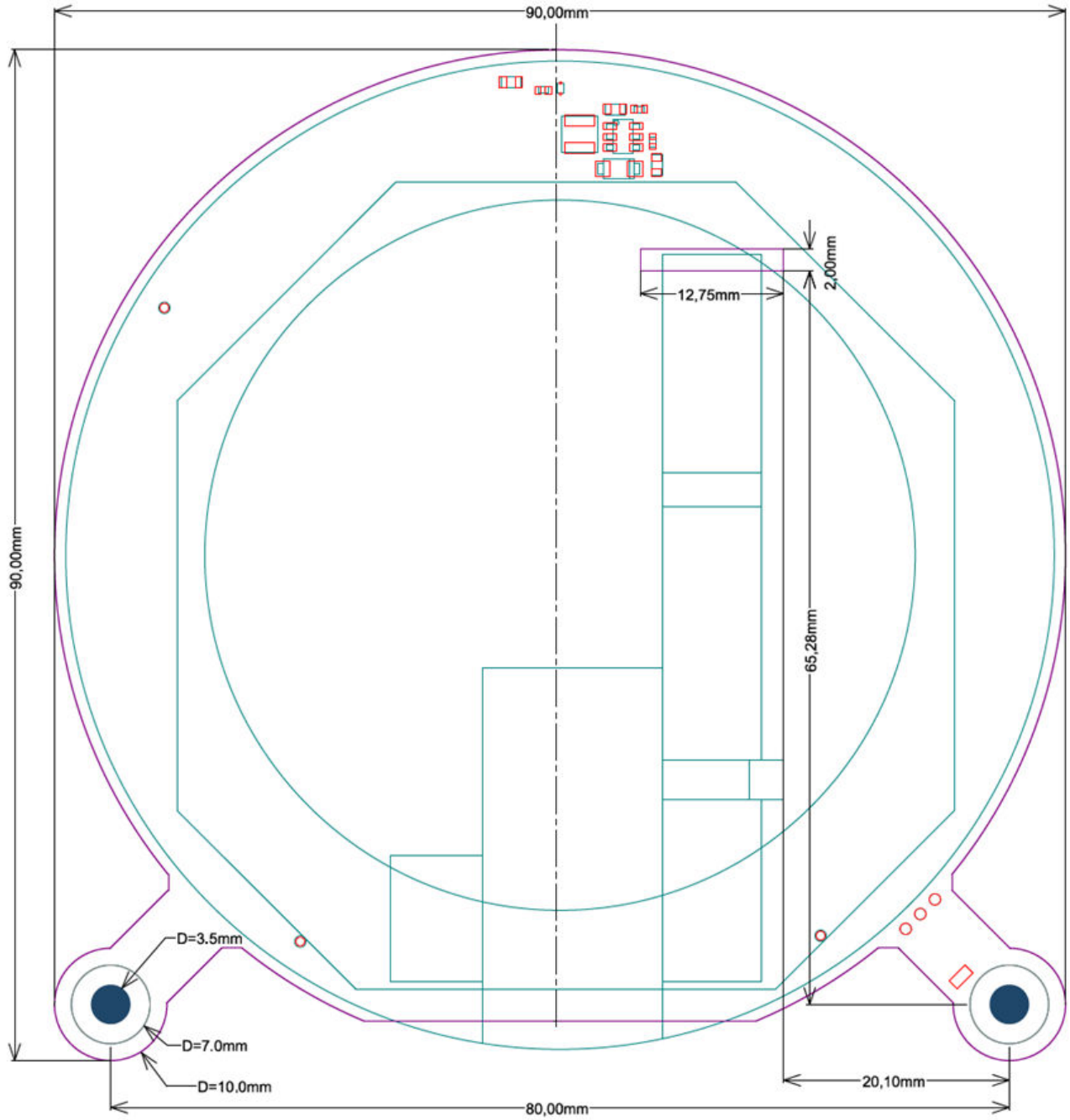
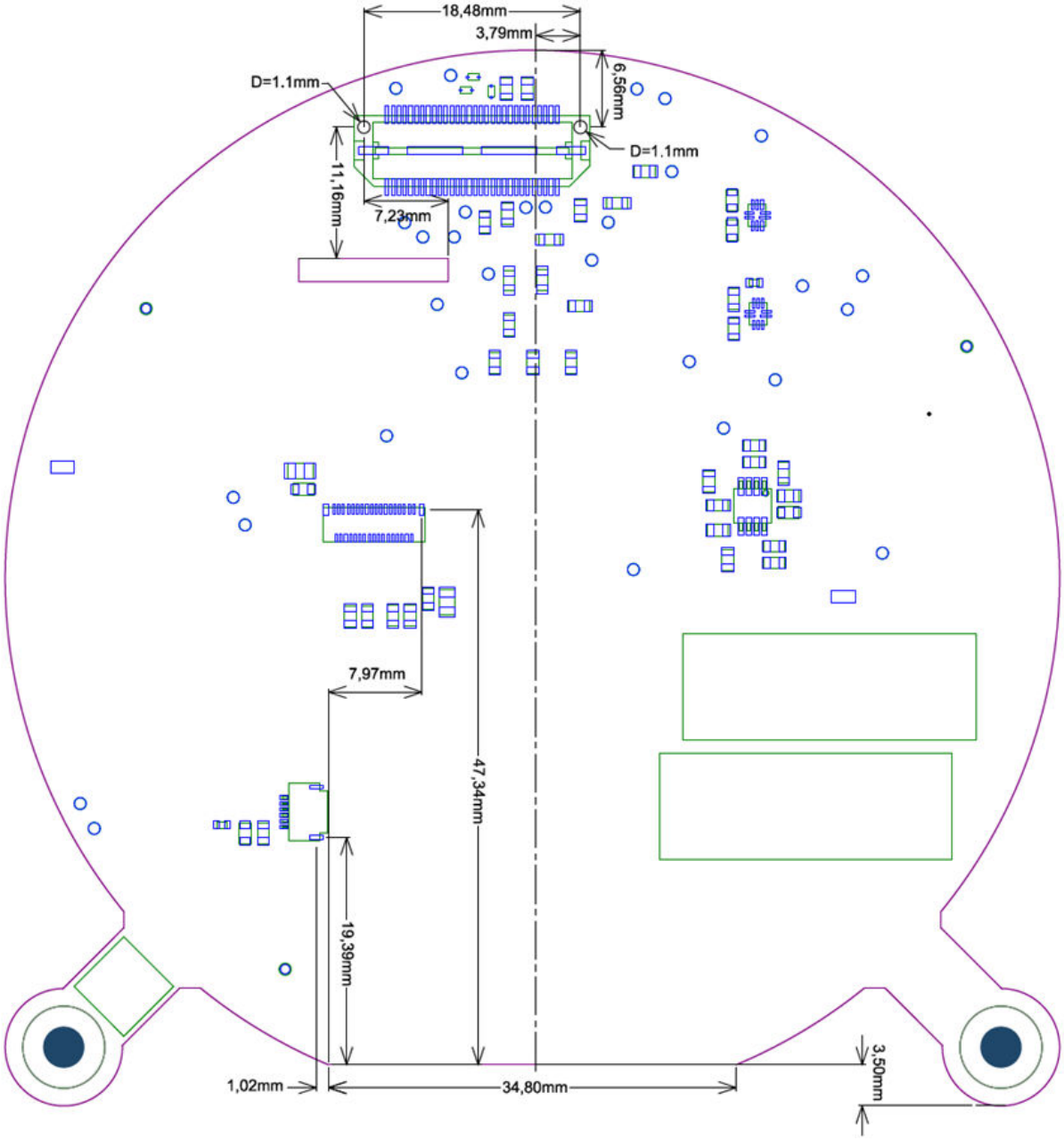


Figure 12. **LCD daughterboard bottom**



7.4 Embedded STLINK-V3E

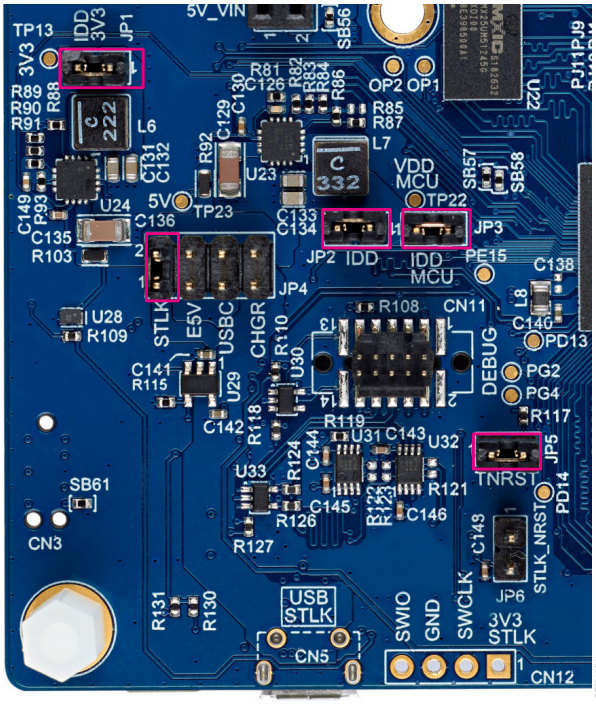
The chapter below gives some information about the implementation of the STLINK-V3E on this board.

Attention: *Before using STLINK-V3E, check your default configuration is the same as explained below. Then, ensure your complete system is well configured and up-to-date versus the STLINK-V3E function. For detailed information about the STLINK-V3E features such as drivers, firmware upgrade, USB interface selection, and LED management, refer to the technical note Overview of ST-LINK derivatives (TN1235).*

Ensure that the following default configuration is set on the main board (refer to Figure 13):

- The JP1, JP2, and JP3 jumpers must be ON to power STM32U5x9NJ and peripherals.
- The JP4 jumper must be ON (STLK power source selected) and the relevant power input connected as described in Section 7.5.2.1: STLK (for compatibility with USB Host port legacy).
- The JP5 jumper must be ON to connect the output reset from STLINK-V3E to the TNRST reset input of STM32U5x9NJH6Q.
- The JP6 jumper must be OFF to set STLINK-V3E in Active mode. The debug connector (CN11) and the TAG connector (CN3) are not used by default.

Figure 13. Default configuration to use STLINK-V3E



Note: STLINK-V3E can also be functional with other JP4 settings. Refer to Section 7.5.2: Power source selection for detailed configurations.

7.4.1 Description

There are two different ways to program and debug the onboard STM32 MCU:

- Using the embedded STLINK-V3E, adapted to MCU 1.8V signaling (embedded level shifters)
- Using an external debug tool compatible with 1.8 V signaling, to be connected to the MIPI10 connector (CN11) or the Tag-Connect™ footprint (CN3). Refer to Section 7.4.6.

Features supported in STLINK-V3E:

- 5 V/500 mA self-power supply by the USB Micro-B connector (CN5), with JP4 on STLK
- USB 2.0 high-speed-compatible interface
- Serial Wire Debug (SWD) and Serial Wire Viewer as option (SWV, on SWO output)
- Virtual COM port (VCP) on USB through USART1 interface
- COM status LED (LD6) and OVC overcurrent detection LED (LD5)
- Device firmware upgrade support (DFU)

Note: For a summary of all debug/program/trace or other interface capabilities, refer to Section 7.4.5.

Note: Always ensure your STLINK-V3E is up-to-date referring to the technical note Overview of ST-LINK derivatives (TN1235).

7.4.2 STLINK-V3E active mode

The STM32U5x9J-DKx products can be powered from the ST-LINK USB connector (CN5), but the host PC might provide only 100 mA to the ST-LINK circuit until the end of the USB enumeration. The 3V3_STLK LDO (U13) supplies 3.3 V to STLINK-V3E with up to 5.5 V recommended input voltage respecting these 100 mA consumption during enumeration. Then, STLINK-V3E requires a 500 mA current from the host PC.

If the host PC can provide the required power, the enumeration finishes, and then, the 5V_STLK power switch (U29) is turned ON, after which the STM32U5x9J-DKx products can drive a 500 mA current. At this step, the PC can rely on the overcurrent protection of this power switch. In case of overcurrent detection, the FAULT pin is asserted and the OVC overcurrent detection red LED (LD5) turns ON.

If the host PC is not able to provide the requested current, the enumeration fails. Therefore, the power switch remains OFF and the 5 V power reference of the board is OFF. The 5V green LED (LD2) is turned OFF.

The green LED (LD2) is turned ON when the STM32U5x9J-DKx product is correctly powered by 5V. The COM LED (LD6) indicates the STLINK-V3E communication status with the host (refer to the technical note Overview of ST-LINK derivatives (TN1235).

Note: In case the board is powered by a USB wall charger on CN5 with JP4 on STLK, there is no USB enumeration, but the power switch is activated and the board is powered up, with an 800 mA current protection.

7.4.3 STLINK-V3E deactivation (Reset mode)

It is simple to deactivate the STLINK-V3E function by moving the JP5 jumper on the JP6 header, to connect STLK_ NRST to GND (refer to Figure 14 and Table 4). Programming, debugging, and monitoring through ST-LINK are impossible in this Reset state, where all STLINK-V3E PIOs are in high impedance.

Attention: *The Reset mode is useful to connect an external probe to MIPI10/STDC14 debug (CN11) or TAG (CN3) connector for the embedded STM32U5x9NJ debug (refer to Section 7.4.5).*
In this Reset mode, when JP6 is ON, 5V selection JP4 STLK is not functional, but any other 5V selection on JP4 might be used to power the board from other sources without overcurrent onboard protection.

Figure 14. STLK_NRST default configuration (JP6)

Table 4. STLK_NRST configuration (JP6)

Reference	Jumper[1]	Function	Comment
JP6[2]	**OFF**	STLINK-V3E active	STLINK-V3E detects a USB ST-LINK plug on CN5.
	ON	STLINK-V3E Reset state	Set STLINK-V3E in Reset mode (all I/Os in high impedance). There is no power from JP4 STLK.

1. *The default setting is in bold.*
2. *In case JP6 is ON, JP5 must be OFF.*

7.4.4 STLINK-V3E TNRST disconnection

It is possible to isolate physically the STLINK-V3E output reset (T_NRST signal function) from the main STM32U5x9NJ NRST function by disconnecting JP5 (refer to Figure 15 and Table 5).

Figure 15. TNRST default configuration (JP5)

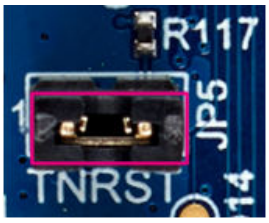


Table 5. TNRST configuration (JP5)

Reference	Jumper[1]	Function	Comment
JP5[2]	**ON**	T_NRST (PA6)	STLINK-V3E T_NRST output reset connected to NRST of STM32U5x9NJ.
	OFF		STLINK-V3E T_NRST output reset isolated from NRST of STM32U5x9NJ.

1. *The default setting is in bold.*
2. *In case JP5 is ON, JP6 must be OFF.*

7.4.5 SWD debug/program/trace and JTAG/USART

Attention: *Before using CN3 or CN11, also check the specific constraints detailed in Section 7.4.6: Using an external debug tool to program and debug the on-board STM32.*

The SWD debug/program/trace interface is accessible through the STLINK-V3E USB connector (CN5) by default, and the debug connector (CN11) or Tag-Connect™ 10-pin footprint (CN3) are other options.

By default, access to SWO trace and JTAG is not functional and needs hardware modification.

The USART1 bootloader is accessible through STLINK-V3E by default.

To debug/program/trace, first, choose any of the exclusive following connectors and consider Table 6 to summarize STM32U5x9J-DKx capabilities:

Table 6. Debug/program/trace and JTAG/USART interface overview

Connector	SWD debug/program	SWO trace(1)	JTAG(1)(2)(3)	USART1 bootloader
USB STLINK-V3E CN5	Yes	Yes, as an option	No	Yes
MIPI10 debug CN11 (STDC14 as an option)	Yes	Yes, as an option	Yes, as an option	No(4)
TAG footprint CN3	Yes	Yes, as an option	Yes, as an option	No

1. *SWO/JTDO (PB3) can be used by moving SB33 on SB34 (exclusive with SDMMC2.D2).*
2. *NJTRST(PB4) is not connected to connectors but is accessible on CN9 (exclusive with SDMMC2.D3).*
3. *JTDI is connected by default, and cannot be used when UCPD.CC1 is used.*
4. *The USART1 bootloader interface is only accessible on the CN11 footprint (pins 13 and 14): USART1_RX (PA10) and USART1_TX (PA9).*

Refer to Section 9.2 and Section 9.3 for CN11 and CN3 pin assignment details.

When using STLINK-V3E USB CN5 by default, refer to the software tool description for any specific constraints or capabilities.

Here are the interface signals between STM32U5x9NJ MCU and STLINK-V3E or the external probes:

Table 7. Default STM32U5x9NJ interface to STLINK-V3E and external debug tools

STM32U5x9NJ PIO	Configuration
PA14	SWCLK (T.SWCLK/T.JTCK)
PA13	SWDIO (T.SWDIO/T.JTMS)
PB3	SWO (T.SWO/T.JTDO)
PA15	JTDI (T.JTDI) -not available for STLINK-V3E
PB4	*NJTRST -not used*
NRST	NRST (NRST)
PA9	VCP_TX (T.VCP_TX)–*USART1_TX* -only for STLINK-V3E
PA10	VCP_RX (T.VCP_RX)–*USART1_RX* -only for STLINK-V3E
PH0	*MCO (T.MCO) -not used*

For details about relevant connector pin assignments, refer to Section 9.

7.4.6 Using an external debug tool to program and debug the on-board STM32

Warning: *Take care MIPI10 debug and TAG connectors are 1.8 V signaling interface by default. Use only adequate/compatible tools to connect.*

Warning: *Some TAG connector tools connect a 5 V external power on pin 5 of the CN3 footprint, which can create a short circuit. Pay attention to using the right tool combination of adapter/cable not to bring 5 V on pin 5, or simply remove the dedicated solder bridge from the PCB, or find a way to disconnect the 5 V signal from your tool.*

Warning: *The CN11 and CN3 connectors are exclusives, use only one at the same time to avoid conflict.*

Before using any external debug tool, read carefully its user manual, to check if specific constraints apply.

The following page details the list of things to consider and configure when using the CN11 or the CN3 connector.

1. Put the embedded STLINK-V3E in Reset mode: Move the TRNST jumper (JP5) on the STLK_NRST header (JP6), no data transfer is possible from USB ST-LINK. This allows the use of either CN11 or CN3 without the risk of signal conflict with STLINK-V3E on any interface.
2. Because STLINK-V3E is in Reset mode, you have also to remove the jumper (JP4) from the STLK position and put it in any other position according to your required configuration (refer to Section 7.5.2: Power source selection and Section 7.5.1: Power diagram).
3. If you use the SWD interface in 2-wire mode (without SWO), there is no need for further modifications.
4. If you use the SWD interface in 3-wire mode (with SWO), or the JTAG interface (with JTDO), disconnect SB33 and connect it to SB34.

Note: JTDI can be used by default as UCPD.CC1 is not used.

Note: CN11 and CN3 connectors provide access to the NRST pin of the STM32U5x9NJH6Q microcontroller, but do not offer access to the NJRST function. NJRST function is only accessible on PB4 on CN9 pin 8, and it is exclusive to SDMMC2_D3.

5. If you want to use the USART1 bootloader interface from CN11: Connect your tool to RX/TX on pin 13/14 of CN11 (it must be 1.8V compatible). (Or, if STDC14 is used as CN11, just connect the MIPI14 cable to your 1.8V compatible tool).
6. Power up the board: Connect your power source to the board.
7. Use any of the debug (CN11) or TAG (CN3) connectors for the STM32U5x9NJH6Q connection: Use a MIPI10 or MIPI14 cable to connect to the debug connector (CN11) or use a TAG connect cable to connect to the TAG footprint (CN3). Reminder: The board is 1.8 V by default, so only use adequate/compatible tools to connect.

7.5 Power supply

7.5.1 Power diagram

Warning: *This Discovery kit is a low-power system designed for VDD and VDD_MCU at 1.8 V only.*

Attention: *Do not remove JP3 when the board is powered up, or do not start the board with JP3 OFF, for this might have an impact on the long-term reliability of the MCU in specific temperature conditions. Use preferably JP4 OFF, Reset button, or power source removal to restart the board.*

Attention: *Do not remove the JP2 header when the board is powered up, for it might have an impact on the long-term reliability of the peripherals.*

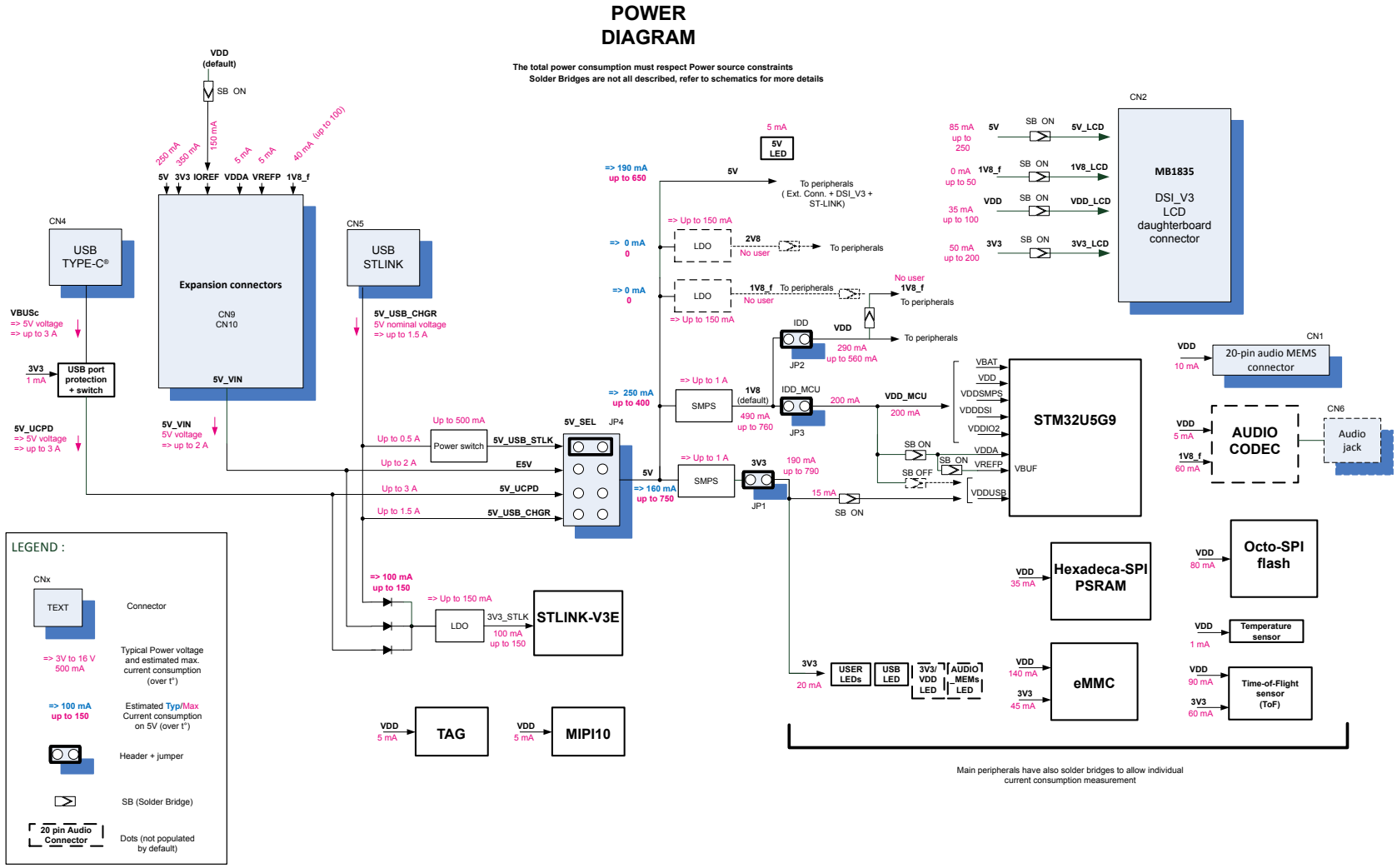
Attention: *This Discovery kit uses a power scheme that might be different from standard application notes. Refer to the relevant application notes for your design.*

Figure 16 describes the power architecture and the maximum voltage and current limits, under which functions can be safely used on the STM32U5x9J-DKx product. In any case, ensure the total power budget of the application always conforms to the selected 5 V power source mode, if not, malfunction can occur. For detailed configuration, refer to the relevant function description and technical application notes.

Note: When using expansion connectors, it might be necessary to use one of the three following power sources, depending on the application power budget:

- *5V_VIN, up to 2 A: Expansion connectors power the STM32U5x9J-DKx application*
- *5V_USB_CHGR, up to 1.5 A: Power the board from a 1.5 A compatible USB Host port or USB charger*
- *5V_UCPD, up to 3.0 A: Power the board from a 1.5 or 3.0 A compatible USB Host port or USB charger and check the 5 V power supply voltage tolerance fits with the application.*

Figure 16. Power diagram



7.5.2 Power source selection

The STM32U5x9J-DKx Discovery kits are designed to be powered by a 5V DC power supply. It is possible to configure the Discovery main board with JP4 header to use any of the four sources described in Table 8 for the 5V DC power supply.

Table 8. 5V selection configuration jumper (JP4)

Reference	Jumper (1)	Function	Comment
JP4	**STLK**	5 V is supplied by USB STLK (CN5).	• 5 V (+10%/-5%) • 800 mA typ. embedded overcurrent protection • Up to 500 mA capable
	CHGR	5 V is supplied by USB STLK (CN5).	• 5 V (+10%/-5%) • No embedded current protection • Up to 1.5 A current
	USBC	5 V is supplied by the USB Type-C® connector (CN4).	• 5 V (+10%/-5% at current < 500 mA) • 5 V (+/-10% at current < 1.5 A) • No embedded current protection • Up to 3 A (check USB Type-C® VBUS constraints in that case)
	E5V	5 V is supplied by 5V_VIN and GND pins on the expansion connector (CN9).	• 5 V (+/-5%), up to 2 A • No embedded current protection (can be included on the expansion add-on board)

1. *The default setting is in bold.*

In all the above four power source configurations, the LED 5V (LD2) must be lit when the Discovery main board is correctly powered by the 5V supply.

The recommended maximum voltage applied on 5 V in continuous mode must be 5.5 V in standard use cases.

7.5.2.1 *STLK (for compatibility with USB Host port legacy)*

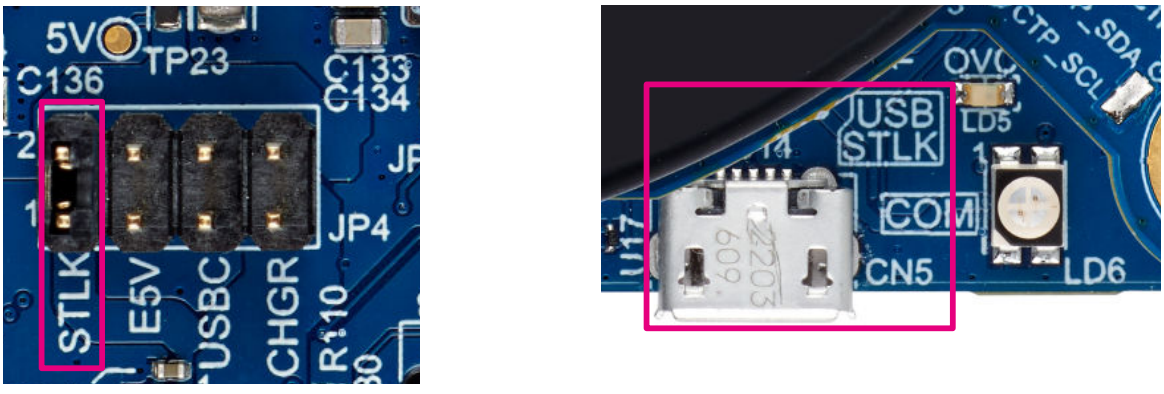
Figure 17 shows the selection of 5V from STLK on JP4, with a power source connected to USB ST-LINK (CN5). It is the default setting.

The USB ST-LINK CN5 connector can power the STM32U5x9J-DKx Discovery kits, but the host PC only provides 100 mA to the ST-LINK circuit until the end of USB enumeration. At the end of the USB enumeration, the STM32U5x9J-DKx Discovery kits require a 500 mA current from the host PC.

If the USB enumeration succeeds, a power switch supplies the board with up to 500 mA current. This power switch also features a current limitation to protect the PC in case of overcurrent on the board.

Note: In this mode, in case a wall charger powers the board, there is no USB enumeration but the overcurrent protection is still active on the powered board.

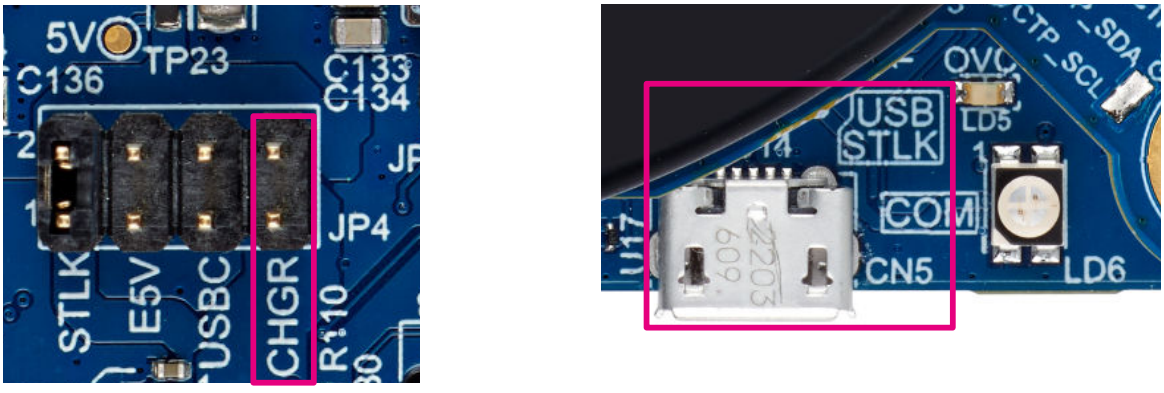
Figure 17. STLK (JP4) from USB STLK (CN5)



7.5.2.2 CHGR

Figure 18 shows 5 V DC power from CHGR on JP4, with a power source connected to USB ST-LINK (CN5) and without any current protection. Thus, if the Discovery kit is powered by a USB PC port, debug features are available, but with the risk of damaging the PC. If a simple USB wall charger powers the Discovery kit, the debug/monitor features through STLINK-V3E are not available. In that configuration, the board can draw up to 1.5 A maximum recommended current. Prefer using USB ports showing charging port marking in that case (⚡) or using a USB Type-C® port with a USB Micro-B cable adapter, they enable up to 1.5 A current capability including data communication. CHGR position can be used when using MIPI10 or Tag-Connect™ footprint.

Figure 18. CHGR (JP4) from USB STLK (CN5)



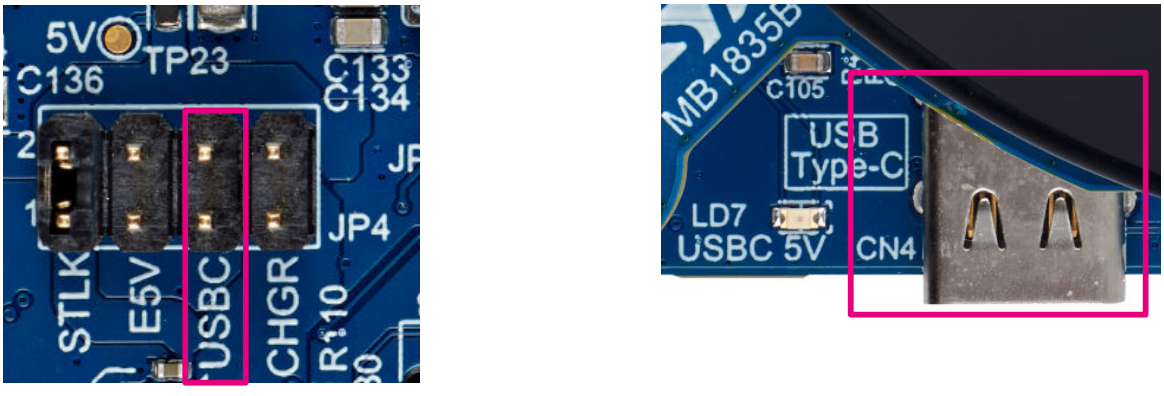
7.5.2.3 USBC

Figure 19 shows the selection of 5 V DC power from USBC on JP4, with a power source connected to the USB Type-C® connector (CN4). A USB Type-C® port protection device with a power switch protects the STM32U5x9J-DKx Discovery kits from overvoltage on V_{BUS}. USB Type-C® V_{BUS} nominal voltage must be in the 5 V +10%/-5% voltage range. The following constraints apply to USB Type-C® host types to use:

- Low-power USB hosts are not supported, and permanent damage might occur (100 mA is not enough to start).
- USB 2.0 or USB 3.x host ports might be used if they can provide 500 mA without data communication.

  Prefer using USB ports showing charging port marking in that case (⚡) or using a USB Type-C® port, they can provide a higher current.
- Any other USB Type-C® source type can supply and start up the STM32U5x9J-DKx Discovery kits.

Figure 19. USBC (JP4) from USB Type-C® (CN4)



7.5.2.4 *E5V*

Figure 20 shows the selection of 5 V DC power from E5V on JP4, with a power source connected to external 5V_VIN pin 1 (CN9) and GND pin 11 or 13 (CN9). Note that GND pins are also available on other pins of expansion connectors (CN9 and CN10). Refer to Section 9.7: Expansion connectors (CN9 and CN10) for details. In this case, a power supply unit or auxiliary equipment complying with standard EN 60950-1: 2006+A11/2009+A12/2011+A2/2013 or EN 62368-1 (2014+A11/2017) must power the STM32U5x9J-DKx Discovery kits and must be safety extra low voltage (SELV/ES1) with limited power capability (LPS/PS2).

Note: There is no input current protection on MB1829 in this configuration. The recommended maximum current to be drawn from this E5V pin is 1.5 A, but 2 A must also be functional in practice (current protection might be placed on the expansion board).

Figure 20. E5V (JP4) from 5V_IN/GND (CN9)

7.5.3 Microcontroller power

Warning: *The STM32U5x9J-DKx Discovery kits are low-power systems designed for VDD and VDD_MCU at 1.8 V only.*

Attention: *Do not remove the JP3 header when the board is powered up, or do not start the board with JP3 OFF, this might have an impact on the long-term reliability of the MCU in specific temperature conditions. Use preferably JP4 removal or the reset button or power source removal to restart the board.*

Attention: *Do not remove the JP2 header when the board is powered up, it might have an impact on the long-term reliability of the peripherals.*

Attention: *The STM32U5x9J-DKx Discovery kits use a power scheme that might be different from standard application notes. Refer to the relevant application notes for your design.*

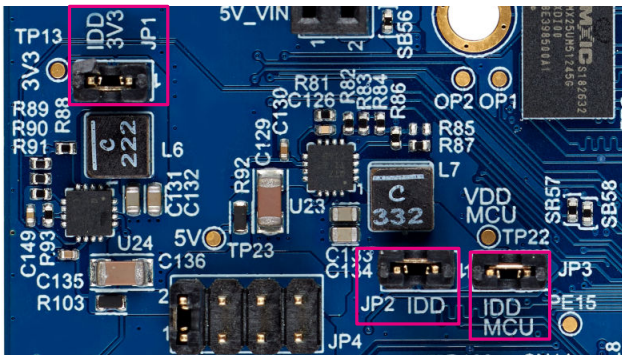
By default, the STM32U5x9NJH6Q microcontroller power supply pins are connected to the VDD_MCU power supply (1.8 V) and the 3V3 power supply (3.3 V). In case the user wants to test any other power supply configuration, a few solder bridges can be modified (refer to Section 10.2: Solder bridges).

Two SMPS devices supply the 1.8 V and the 3.3 V power supplies of the board (going to the microcontroller and peripherals). Both SMPS outputs can supply a current of 1 A. The three headers (JP1, JP2, and JP3) allow measuring the currents going respectively to:

- IDD 3V3 (JP1): Current from 3V3_SMPS to 3V3 power supply (VDDUSB of MCU and 3V3 of peripherals)
- IDD (JP2): Current from VDDMCU_SMPS to VDD peripheral power supply (VDD is going only to peripherals)
- IDD MCU (JP3): Current from VDDMCU_SMPS to VDD_MCU (only to the MCU)

A jumper is fitted on each header, but an ammeter can replace any jumper for easy IDD measurement. Refer to Figure 21 and Table 9.

Figure 21. Jumpers default configuration (JP1, JP2, and JP3)



DT56172V1

Some solder bridges or serial resistors are available on boards to measure the current of some microcontroller and peripheral supply rails (refer to schematics for detailed possibilities).

Table 9. IDD configuration (JP1, JP2, and JP3)

Reference	Jumper [1]	Function	Comment
JP1	**ON**	3V3 connected to SMPS output	SMPS powers 3V3. No current measurement.
	OFF	3V3 not connected to SMPS output	3V3 is not powered. Add an ammeter to power the MCU and peripherals and measure the current.
JP2	**ON**	VDD connected to SMPS output	SMPS powers VDD for peripherals. No current measurement.
	OFF	VDD not connected to SMPS output	VDD is not powered. Add an ammeter to power the peripherals and measure the current.
JP3	**ON**	VDD_MCU connected to SMPS output	SMPS powers VDD_MCU. No current measurement.
	OFF	VDD_MCU not connected to SMPS output	VDD_MCU is not powered. Add an ammeter to power the MCU and measure the current.

1. *The default setting is in bold.*

7.5.3.1 *VDD_MCU*

By default, the SMPS output to VDD_MCU is set to 1.8 V, to be compatible with the current design and peripherals.

VDDIO2 is a power rail dedicated to a few GPIOs (PG2 to PG15) and is independent of other GPIO power rails in the microcontroller. VDDIO2 is set at 1.8 V by default (connected to VDD_MCU).

VBAT is connected to VDD_MCU by default (for voltage measurement capability). Thus, VDD_MCU can be monitored through the internal ADC channel on ADC1/2/4 (VBAT/4).

7.5.3.2 *Internal SMPS*

An internal SMPS can supply power to a few IPs of the microcontroller. This internal SMPS is supplied by VDD_MCU and enables very low power consumption figures in some power modes of the STM32U5x9NJH6Q microcontroller.

7.5.3.3 *Analog power supplies*

VDDA is the external analog power supply for ADC converters, DAC converters, voltage reference buffers, operational amplifiers, and comparators. It is connected to VDD_MCU by default, through a ferrite bead.

VSSA/VREF- are connected to general ground VSS in one point of the design, thanks to a solder bridge. Other options are available.

VREF+ is the STM32U5x9NJH6Q input reference voltage for ADCs and DACs. It is connected to VDDA (default setting). Because VDDA is 1.8 V, VREFBUF cannot be used to power VREF+.

VDD_USB is fixed at 3.3 V (supplied by an SMPS as explained below) to enable USB Type-C® use.

7.5.4 Other peripheral power

The 1.8 V power rail supplies most of the board peripherals, through a dedicated jumper. The power rail is named VDD to differentiate with VDD_MCU, dedicated to the microcontroller.

Some components/peripherals need a 3.3 V supply: MCU, expansion connectors, MB1835 LCD daughterboard, ToF sensor, eMMC, and LEDs. A dedicated SMPS provides the 3.3 V power rail, to be compatible with the current design and peripherals.

STLINK-V3E is powered by the 3V3_STLK supply (LDO) from different 5 V sources. 5.5 V is the maximum recommended continuous input voltage, with at least 6.5 V peak AMR.

7.6 Clock sources

The STM32U5x9J-DKx Discovery kits rely on an HSE oscillator (16 MHz crystal) and an LSE oscillator (32.768 kHz crystal) as clock references.

Using the HSE (instead of HSI) is mandatory to manage the DSI interface for the LCD module and the USB high-speed interface.

Any other internal clock reference might be used, but the clock tree might be adapted, and some features might be unavailable.

HSE oscillator crystal might be replaced by an external clock reference thanks to a solder bridge (MCO clock source coming from STLINK-V3E, but the clock tree might be adapted, and some features might be unavailable).

The LSE might be replaced by internal LSI use, but the clock tree might be adapted, and some features might be unavailable.

7.7 Boot options

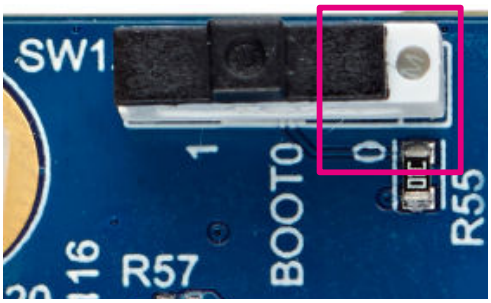
Attention: *The white side of the SW1 switch indicates the Boot0 value setting (default position white switch at the right indicates BOOT0 = 0), refer to Figure 22.*

By default, the boot procedure is managed through the PH3/BOOT0 pin of the MCU (center pin of the BOOT0 SW1 switch). The PH3/BOOT0 pin is connected either to a 10 kΩ pull-down (position 0) or to a 10 kΩ pull-up (position 1).

As the nSWBOOT0 option bit of STM32U5x9NJH6Q is set to 1, STM32U5x9J-DKx boot on internal flash memory, thanks to the SW1 switch default position (BOOT0 = 0).

SW1 is located on the bottom side of the board due to mechanical constraints. For specific purposes, the switch might be moved on top when CN1 is not used or replaced with a standard 3-pole header with a jumper.

Figure 22. BOOT0 default configuration, set on “0” (SW1)



DT56173V1

8 Board functions

This section explains all the functions, peripherals, and interfaces of the board. Refer to Features, Hardware layout and configuration, Figure 5, and Figure 6 STM32U5x9J-DKx top and bottom layout views.

8.1 2.47” round TFT DSI LCD daughterboard and DSI_V3 connector

Caution:
- To peel off the LCD protective liner, do it slowly and carefully.
- If fixed patterns are displayed for a long time, a remnant image is likely to occur.

Note: The microcontroller software system must invert DSI.CK_N and DSI.CK_P lines together to align with DSI_V3 add-on boards. The DSI clock differential signals (_N and _P) are inverted on CN2 for layout reasons (refer to the DSI_V3 connector standard pinning in Section 9.4: DSI_V3 display board connector (CN2)).

Note: The MB1835 display module board is designed to be compatible with a VDD setting of 1.8 V. Refer to the MB1835 schematics for more detailed constraints and options.

The LCD daughterboard is a 2.47” TFT round display, 480 × 480 resolution, 16.7 million color depth with a MIPI DSI® 2-lane interface and a capacitive multi-touch panel. The STM32U5x9J-DKx Discovery kits integrate two DSI_V3 compatible connectors (refer to Section 9.4: DSI_V3 display board connector (CN2) for details) to interface the main and LCD boards. The height between both boards is 8 mm.

8.1.1 Display management

The display uses a bidirectional two-data-lane DSI interface with one clock lane to interface with the MB1829 main board. The DSI interface is used to transfer display and command data to the display controller (including power-saving modes and synchronization to avoid the tearing effect).

The MB1829 main board provides four power supplies to the MB1835 LCD module board. These power supplies respect a power-up and power-down sequence following these timeframes:

- Power-up order (on 5V source activation): 5V_LCD -> 1V8_LCD -> VDD_LCD -> 3V3_LCD
- Power-down order (on 5V source removal): 5V_LCD -> 3V3_LCD -> 1V8_LCD -> VDD_LCD

Note: By default, 1V8_LCD is not used by MB1835. VDD_LCD is used instead of 1V8_LCD.

By default, the four power supplies are not switchable (power switches are replaced by 0 Ω solder bridges on the MB1829 main board).

The PIO list description of the DSI_V3 connector and the default PIO configuration is defined in Section 8.1.3: 2.47” display and DSI_V3 I/O interface. Many PIOs are not used by default. Refer to the I/O interface table.

Some PIOs are used by default to manage the LCD screen display (for dedicated touch-panel PIOs, refer to Section 8.1.2: Touch-panel management):

- DSI_RESETn (PD5, active Low), to control the hardware RESET (common control with the touch panel)
- DSI_BL_CTRL (PI6, active high), to control the backlight (PIO, PWM, or SWIRE modes are possible)

Refer to the “Reset timing” and “Power on/off sequence and timing” sections of the display controller datasheet or touch-panel datasheet for further DSI_RESETn management details.

DSI_TE PIO (PF11) is not used by default. It might be used with other LCD module boards to manage the tearing effect function and synchronize host frame writing with the display controller.

8.1.2 Touch-panel management

The capacitive touch panel is driven through the I2C5 microcontroller interface.

The DSI_RESETn PIO (PD5, active low) controls the touch-panel controller hardware reset, at the same time as the display reset, but each reset signal is adapted to the peripheral (thanks to level shifters on MB1835). Pay attention to respect hardware reset timings depending on the used LCD module board.

The DSI_TOUCH_INT PIO (PE8, active low) manages the touchscreen interrupt function, to synchronize touch-panel activation with the host. It might also wake up the MCU from standby/shutdown modes.

8.1.3 2.47” display and DSI_V3 I/O interface

Table 10. 2.47” display and DSI_V3 I/O interface

PIO	Configuration
PI6	BL_CTRL (DSI_BL_CTRL)
PD5	DSI_RESETn (DSI_RESETn)
PE8	TOUCH_INT (DSI_TOUCH_INT)
DSI_CKN	**CK_P (DSI.CK_P)–Polarity inversion on CN2 needs SW inversion on MCU.**
DSI_CKP	**CK_N (DSI.CK_N)–Polarity inversion on CN2 needs SW inversion on MCU.**
DSI_D0N	D0_N (DSI.D0_N)
DSI_D0P	D0_P (DSI.D0_P)
DSI_D1N	D1_N (DSI.D1_N)
DSI_D1P	D1_P (DSI.D1_P)
PH4	SDA (I2C5.SDA)
PH5	SCL (I2C5.SCL)
PI5	*DSI_PWR_ON (DSI_PWR_ON) –not used*
PD8	*DSI_SPI_CS (DSI_SPI_USART_CS) –not used*
PB13	*DSI_SPI_CK (DSI_SPI_CLK) –not used*
PD4	*DSI_SPI_MOSI (DSI_SPI_MOSI) –not used*
PD11	*DSI_SPI_DCX (DSI_SPI_D/CX) –not used*
PB10	*USART3_TX (DSI_USART_TX) –not used*
PD10	*USART3_CK (DSI_USART_CK) –not used*
PI7	*SWIRE (DSI_SWIRE) –not used*
PF11	*TE (DSI_TE) –not used*

8.1.4 Other DSI_V3 compatible peripherals

The MB1829 main board allows supporting the following peripherals (non-exhaustive list): MB1835B-01, MB1232A-01. Some peripherals require hardware adaptation (DSI_PWR_ON is not active by default):

- MB1829B-01 with MB1835B-01 (2.47” round LCD) uses the default hardware configuration.
- MB1829B-01 with MB1232A-01 (HDMI board) needs hardware changes.

Updates with MB1232A-01 HDMI board:

- Remove R72 from the MB1829 (PIO is 5V-tolerant. Ok to tie it to 3V3 on the MB1232A side).
- Check that SB53 is fitted on the MB1829 (or put a shunt on SB53, in case SB53 is formerly removed for development purposes).
- Remove SB50 from MB1829 (to use pull-ups values on the MB1232A side).
- Add 2.2 kΩ resistors on R8 and R9 of MB1232A.
- Add a 2.7 kΩ resistor on R5 of MB1232A.
- Use the free spacer/screw and pillar to attach MB1232A onto MB1829 for strong mechanical plugging.

Note: MB1232A-01 is part of B-LCDAD-HDMI1 product version 1.

8.2 USB Type-C® (High Speed, sink only)

The STM32U5x9J-DKx products support a USB HS 2.0 interface on the USB Type-C® receptacle connector (CN4). The STM32U5x9J-DKx products offer compatibility with USB Type-C® rev 1.3 and are configured by default to behave as self-powered USB devices (when JP4 is on STLK).

Caution: As required by the USB Type-C® specification, the STM32U5x9J-DKx products can interface on CN4 with USB2.0 and USB3.x legacy hosts supporting the USB high-speed data link but with these restrictions:

- JP4 must not be set on USBC (to respect the 100 mA maximum current before enumeration), or
- JP4 might be set on USBC, but the source must be 500 mA current capable (USB2.0 charging port for example)

Caution: The total drawn current on CN4 USB Type-C® V_{BUS} must not exceed 3 A in any application. When using CN4 to power the STM32U5x9J-DKx, check that the USB V_{BUS} voltage constraints are compatible with your 5 V-powered application on expansion connector CN9 (refer to the USB Type-C® current load line).

Warning: *The STM32U5x9J-DKx supports only a 5 V nominal voltage V_{BUS} on the USB Type-C® CN4 connector. Do not set V_{BUS} at higher or lower nominal voltages than 5 V. Using out-of-range nominal voltage V_{BUS} might result in board malfunction.*

The USB Type-C® connector (CN4) can be used to demonstrate different features of STM32U5x9J-DKx.

1. Power the Discovery main board with a 5 V V_{BUS} with a current of up to 3 A
2. High-speed data transfers with any USB Host

8.2.1 USB Type-C® sink only

Even if the Discovery kit is configured by default to behave as a self-powered USB device powered by USB ST-LINK connector CN5, the CN4 USB Type-C® connector can power the Discovery main board with a 5 V power coming from any USB Type-C® connected source (refer to Section 7.5.1: Power diagram) with the following constraints:

- A jumper must be set on the USBC position of the JP4 header (5 V source selection, to behave as a USB powered device).
- As per the USB Type-C® specification, V_{BUS} is in the range of 5 V +10%/-5% and the default sourcing current is 500 mA minimum while the UCPD.DBn control pin (PE9) is an input (default state).
- Sinking up to 1.5 A or up to 3 A from a USB Type-C® source requires:
  - To set the UCPD.DBn control pin (PE9) at a high level to be able to monitor CCx lines on UCPD.ADC1 (PG0)/UCPD.ADC2 (PF15) for host capability identification
  - To check whether V_{BUS} voltage constraints are compatible with any 5 V-powered application on the expansion connector (CN9). Refer to USB Type-C® current load lines and check that the 7 V maximum overvoltage V_{BUS} protection fits your needs.

A USB Type-C® port protection device, associated with a power switch, is used to protect STM32U5x9J-DKx from ESD and USB V_{BUS} overvoltage (6.5 V typical, up to 7 V). The USB Type-C® port protection device (U11) is called "USB Type-C® protection device" hereafter to simplify wording.

Five I/Os are used to manage the USB Type-C® connection: two configuration channels (CCx) connected on ADC inputs, a VBUS_SENSE on ADC input, a dead battery (UCPD.DBn), and a fault (UCPD.FLT) on GPIOs.

- Configuration Channel I/O (UCPD.ADCx): These signals are connected to the associated CCx line of the USB Type-C® connector through the USB Type-C® protection device. These lines are used for the configuration channel lines (CCx) to sense the cable orientation and identify power source capability. The Discovery kit supports only sink current mode with the default 5V power supply with up to 3 A current. To be compatible with the 1.8 V ADC voltage range, a resistor bridge is present between CCx lines and UCPD.ADCx inputs: It presents a total 5.1 kΩ pull-down on the USB connector and adapts the voltages from CCx lines to the maximum 1.8 V range of MCU inputs. According to the USB Type-C® specification, the following thresholds must be used in the context of MB1829 to identify the host source capability:

Table 11. UCPD.ADCx voltage range and threshold according to power source capability

Source advertisement	Minimum voltage on UCPD.ADCx	Maximum voltage on UCPD.ADCx	Threshold between modes
Default USB power (500 mA)	0.24 V	0.44 V	0.54 V
1.5 A @ 5 V	0.63 V	0.84 V	1 V
3 A @ 5 V	1.16 V	1.49 V	-

To measure UCPD.ADCx inputs, UCPD.DBn must be set high before. See below.

- Dead battery I/O (UCPD.DBn, PE9): This signal is connected to the associated DBn line of the USB Type-C® protection device. When UCPD.DBn is low, the USB Type-C® protection device manages internally the dead battery resistors on CCx lines that enable 5V, and at least 500 mA default mode. When going High, UCPD.DBn connects ADCx lines of the microcontroller to the connector and enables it to sink more current than 500 mA (in the limit of 3 A). Thus, if UCPD.DBn is not set to the high level, STM32U5x9J-DKx must not consume or activate used cases requiring more than 500 mA.
- V_{BUS} fault detection: UCPD.FLT (PE12, interrupt active low). This signal is provided by the USB Type-C® protection device. It is used as fault reporting to MCU after a bad V_{BUS} level detection. By design, the OVP V_{BUS} protection is set to 6.5 V nominal (7 V max) which is compatible with the absolute maximum ratings of the design. OVP V_{BUS} = 1.25 x (10 kΩ + 2.4 kΩ) / 2.4 kΩ.
- VBUS_SENSE ADC input (PG1) is used to detect attachment and detachment and to measure accurate V_{BUS} voltage at the JP4 header (5V_UCPD).

During startup, the DBn pin is tied to GND, and the USB Type-C® protection device manages directly the CC lines: It enables the host source to power the 5 V V_{BUS} by default. A green LED (LD2) is lit when 5V is present.

The USB Type-C® protection device controls a FET switch and protects the Discovery kits against V_{BUS} overvoltage. Moreover, in any case, to ensure the functional behavior of the kit, the maximum recommended voltage applied on USB V_{BUS} is 5.5 V in continuous mode.

Note: UCPD.ADC1 and UCPD.ADC2 functions are exclusive with respectively the ADC4_IN6 and ADC4_IN7 functions of the expansion connector (CN10). Solder bridges can handle it. Refer to Table 32. Solder bridge configuration.

8.2.2 USB 2.0 high-speed interface

STM32U5x9J-DKx supports a USB 2.0 high-speed interface on CN4 for compatibility with up to 480 Mbit/s. This allows limited time to transfer data into the embedded 4-Gbyte eMMC flash memory for example.

8.2.3 USB Type-C® function interface

Table 12. **USB Type-C® function interface**

PIO	Configuration
PE12	FLT (UCPD.FLT)
PE9	DBn (UCPD.DBn)
PG0	ADC1 (UCPD.ADC1) -optionally used
PF15	ADC2 (UCPD.ADC2) -optionally used
PA12	HS_P (USBC.HS_P)
PA11	HS_N (USBC.HS_N)
PG1	VBUS_SENSE (VBUS_SENSE)
PA15	*CC1 (UCPD.CC1) -not used*
PB15	*CC2 (UCPD.CC2) -not used*

8.3 Hexadeca-SPI PSRAM memory

The 512-Mbit PSRAM is managed through the Hexadeca-SPI interface.

Table 13. **Hexadeca-SPI PSRAM I/O interface**

PIO	Configuration
PH9	NCS (HEXASPI1.NCS)
PI3	CLK (HEXASPI1.CLK)
PI2	DQS0 (HEXASPI1.DQS0)
PH10	IO0 (HEXASPI1.IO0)
PH11	IO1 (HEXASPI1.IO1)
PH12	IO2 (HEXASPI1.IO2)
PH13	IO3 (HEXASPI1.IO3)
PH14	IO4 (HEXASPI1.IO4)
PH15	IO5 (HEXASPI1.IO5)
PI0	IO6 (HEXASPI1.IO6)
PI1	IO7 (HEXASPI1.IO7)
PI4	*NCLK -not used/not accessible*
PI8	DQS1 (HEXASPI1.DQS1)
PI9	IO8 (HEXASPI1.IO8)
PI10	IO9 (HEXASPI1.IO9)
PI11	IO10 (HEXASPI1.IO10)
PI12	IO11 (HEXASPI1.IO11)
PI13	IO12 (HEXASPI1.IO12)
PI14	IO13 (HEXASPI1.IO13)
PI15	IO14 (HEXASPI1.IO14)
PJ0	IO15 (HEXASPI1.IO15)

8.4 Octo-SPI flash memory

The 512-Mbit NOR flash memory is managed through the Octo-SPI interface.

The NRST reset pin from the microcontroller manages the Octo-SPI flash memory RESET function.

Table 14. Octo-SPI flash memory I/O interface

PIO	Configuration
PA2	NCS (OCTOSPIM_P1.NCS)
PA1	DQS (OCTOSPIM_P1.DQS)
PF10	CLK (OCTOSPIM_P1.CLK)
PF8	IO0 (OCTOSPIM_P1.IO0)
PF9	IO1 (OCTOSPIM_P1.IO1)
PF7	IO2 (OCTOSPIM_P1.IO2)
PF6	IO3 (OCTOSPIM_P1.IO3)
PC1	IO4 (OCTOSPIM_P1.IO4)
PC2	IO5 (OCTOSPIM_P1.IO5)
PC3	IO6 (OCTOSPIM_P1.IO6)
PC0	IO7 (OCTOSPIM_P1.IO7)
NRST	NRESET (NRESET)

8.5 eMMC flash memory

The 4-Gbyte eMMC flash memory is compatible with eMMC V5.0.

The eMMC_RSTn (PH6, active low) is the reset for eMMC.

The embedded footprint is also compatible with other eMMC references in the 153-ball package. Check the compatibility of the memory datasheet versus the MB1829 schematics.

Table 15. eMMC flash memory I/O interface

PIO	Configuration
PD2	CMD (SDMMC1.CMD)
PC12	CLK (SDMMC1.CK)
PC8	D0 (SDMMC1.D0)
PC9	D1 (SDMMC1.D1)
PC10	D2 (SDMMC1.D2)
PC11	D3 (SDMMC1.D3)
PB8	D4 (SDMMC1.D4)
PB9	D5 (SDMMC1.D5)
PC6	D6 (SDMMC1.D6)
PC7	D7 (SDMMC1.D7)
PH6	eMMC_RSTn (eMMC.RSTn)

8.6 Audio codec (not used)

Note: SAI audio codec (U5) and audio jack (CN6) functions are not populated by default.

The Discovery kit features an audio codec with an SAI interface and a 3.5 mm audio jack connector (for stereo output and analog microphone). For the audio jack description, refer to the connector section.

The audio codec is driven through the I2C4 interface. An SAI 5-wire interface transfers audio PCM data. A dedicated GPIO (Audio_RSTn, PH2, active low) is used to reset the audio codec.

Table 16. Audio codec I/O interface

PIO	Configuration
PB7	SDA (I2C4.SDA)
PB6	SCL (I2C4.SCL)
PE5	SCK_A (SAI1.SCK_A)
PE4	FS_A (SAI1.FS_A)
PE6	SD_A (SAI1.SD_A)
PE3	SD_B (SAI1.SD_B)
PE2	MCLK_A (SAI1.MCLK_A)
PH2	Audio_RSTn (RESETN)

8.7 20-pin audio MEMS connector

Note: The 20-pin audio MEMS connector function is a differentiating feature, refer to Section 2: Ordering information.

The Discovery kit features a 20-pin audio MEMS connector (CN1) to interface audio MEMS microphones on add-on boards. MDF and ADF interfaces are available through one clock and two data wires. PE10, PF4, and PF3 PIOs can manage up to four MEMS microphones. PE13 (Audio_MEMS_LED) is a control PIO to light a LED.

For details about CN1 pinning, refer to the Connectors section.

Table 17. 20-pin audio MEMS connector function I/O interface

PIO	Configuration
PE10	SDIN4 (MIC.SDIN4)
PF4	SDIN0 (MIC.SDIN0)
PF3	CCK0 (MIC.CCK0)
PE13	Audio_MEMs_LED (MEMS_LED)

8.8 Time-of-Flight sensor

Warning: *Refer to Section 4 for a detailed explanation.*

The Time-of-Flight (ToF) sensor is a laser-ranging sensor. It can be used for gesture control as well as for accurate distance measurements.

The device uses an analog power supply of 3.3 V, which starts after the 1.8 V digital supply. The ToF sensor (U7) is managed with an I^2C bus shared with a temperature sensor, an LPN control line, and an interrupt line. The I^2C can be accessed only if the LPN is high. The interrupt line is mapped on a WKUP PIO.

The Time-of-Flight sensor (U7) is subject to Class 1 laser product identification, refer to its datasheet for technical details, and refer to Figure 5 to identify its location on board.

Figure 23. Class 1 laser product label

Table 18. ToF sensor I/O interface

PIO	Configuration
PH8	SDA (I2C3.SDA)
PH7	SCL (I2C3.SCL)
PE14	TOF_LPN (ToF_LPN)
PB5	TOF_INTN (ToF_INTN)

8.9 Temperature sensor

The temperature sensor is managed with an I^2C shared with a ToF sensor, and an interrupt line. The interrupt line is mapped on a WKUP GPIO.

Table 19. Temperature sensor I/O interface

PIO	Configuration
PH8	SDA (I2C3.SDA)
PH7	SCL (I2C3.SCL)
PF2	TEMP_INTN (TEMP_INTN)

8.10 Expansion connectors

Warning: *The standard way to power the STM32U5x9J-DKx Discovery kits from expansion connectors is to use the 5V_VIN input power pin and GND pins from CN9.*

By default, pin 5V of CN9 is an output power to expansion connectors. Do not use it to power MB1829 to avoid conflict with the 5V source selection jumper (JP4). For development purposes, the 5V pin of CN9 might be used as 5V input to the MB1829, provided the jumper is removed from the JP4 header.

The two connectors (CN9 and CN10) provide access to many ports: 4-bit SDMMC, two SAI, three I^2C, a USART, an LPUART, two SPI, ADCs, timers, and GPIOs. They include four spare pins to connect any other PIOs from the design. They also provide access to power supplies from MB1829.

Some interfaces are not available by default, and others are exclusive to other onboard functions. Refer to Section 9.7: Expansion connectors (CN9 and CN10) for pin assignment details and limitations.

Note: ADC4_IN6 and ADC4_IN7 functions of the expansion connector (CN10) are not connected by default because they are exclusive to UCPD.ADC1 and UCPD.ADC2 functions of USBC. If two additional ADCs are necessary for user application, it is recommended to use ADC4_IN15 and ADC4_IN16 from PD11/PD12 providing SAI2 is not used on expansion connectors (solder bridges can handle it, refer to the solder bridge table).

Note: SDMMC2_D1 and SDMMC2_D2 functions of expansion connector CN9 are connected by default and are exclusive with respectively UCPD.CC1 and T.SWO (JTDO) functions (solder bridges can handle it, refer to the solder bridge table).

Note: The SAI1 function of the expansion connector (CN10) is shared with the audio codec function, which is not populated on-board (the audio codec can support a high impedance state on this bus).

Note: Some USART3 signals of expansion connectors might be connected to the DSI_V3 connector (solder bridges can handle it, refer to the solder bridge table).

Note: SPI2 signals of expansion connectors might be connected to the DSI_V3 connector (solder bridges can handle it, refer to the solder bridge table).

8.11 User button function

Warning: *Debounce filter, serial protection, and external pull-down are not present on the user button function.*

Note: The user button schematics have been optimized, so it is up to the user to manage the internal pull-down and debounce filtering by software. If the user wants to use PC13 as an output, it is recommended to disconnect the serial resistor (or change it to 220 Ω for example) to protect it from unwanted short circuits to VDD through the button.

The user button (B1) is a way to interact with software. This is a selection key, active high, which is mapped on a WKUP PIO (PC13).

A touch panel is also available on the display, and a ToF sensor is on the main board to interact with software.

8.12 Reset button and reset function

The B2 reset button can activate the NRST reset function for all connected onboard devices.

The hardware system reset is managed by the STM32U5x9NJH6Q microcontroller and is available on the NRST pin. NRST signal is tied to GND during reset while it has a permanent internal pull-up tied to VDD_MCU.

The NRST signal is connected to these peripherals: the Octo-SPI flash memory, expansion connector (CN9), debugging connector (CN11), TAG connector (CN3), and STLINK-V3E (through JP5). The STLINK-V3E can activate the NRST reset function if the JP5 jumper is ON and JP6 OFF (default settings).

8.13 Buttons and LEDs function

Table 20 summarizes the different buttons and LEDs of the STM32U5x9J-DKx Discovery kits and their function:

Table 20. Buttons and LEDs

Reference	Color	Function	Comment
B1	Blue	USER button (USER_Button)	PC13
B2	Black	RESET button (NRST)	Reset the board
LD1 (1)	Green	VDD/3V3 LED	Lit when VDD and 3V3 are present (VDD_MCU = VDD if JP2/JP3 populated)
LD2	Green	5V power LED	Lit when 5V is ON
LD3	Green	USER_GREEN LED	LED_GREEN, PE0
LD4	Red	USER_RED LED	LED_RED, PE1
LD5	Red	ST-LINK overcurrent LED (OVC)	Lit when STLK overcurrent detected
LD6	Red, green, or orange	ST-LINK COM LED	Lit according to ST-LINK status
LD7	Green	USBC power LED	Lit when USB Type-C® is connected and V_{BUS} is powered from CN4 source

1. *The LD1 function is not populated by default.*

9 Connectors

Nine connectors are implemented on the STM32U5x9J-DKx products:

- 20-pin audio MEMS connector (CN1)
- DSI V3 connector for display module board (CN2)
- TAG connector (CN3)
- USB Type-C® connector (CN4)
- USB Micro-B (CN5)
- *Audio jack connector (not used) (CN6)*
- Expansion connectors (CN9 and CN10)
- Debug connector (CN11)

9.1 USB Type-C® receptacle connector (CN4)

CN4 is a 24-pin double-row USB Type-C® hybrid right-angle receptacle compatible with USB Type-C® specifications and is shown in Figure 24. Refer also to Section 8.2: USB Type-C® (High Speed, sink only).

Figure 24. USB Type-C® receptacle connector (front view) (CN4)

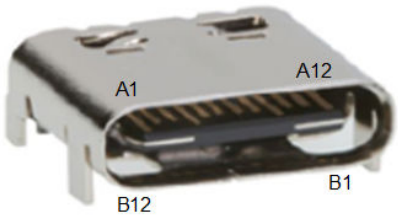


Figure 25. USB Type-C® connector pinout (CN4)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

The related top layer footprint pinout for the USB Type-C® connector is detailed in Figure 26 and Table 21.

Figure 26. USB Type-C® top layer footprint pinout (CN4)

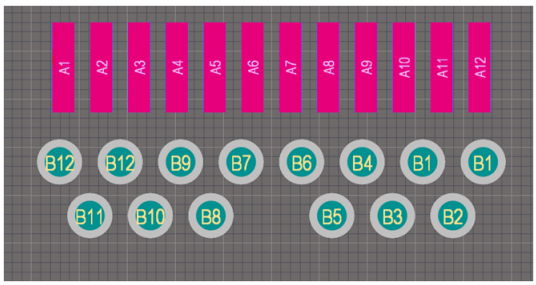


Table 21 describes the connections of the USB Type-C® connector (CN4).

Table 21. USB Type-C® receptacle connector (CN4)

Pin number	Description	Signal assignment	Pin number	Description	Signal assignment
B12	GND	GND	A1	GND	GND
B11	RX1_P	-	A2	TX1_P	-
B10	RX1_N	-	A3	TX1_N	-
B9	VBUS	VBUSc	A4	VBUS	VBUSc
B8	SBU2	-	A5	CC1(1)	UCPD_CC1_C
B7	DM2	USBC_CN_HS_N (PA11)	A6	DP1	USBC_CN_HS_P (PA12)
B6	DP2	USBC_CN_HS_P (PA12)	A7	DM1	USBC_CN_HS_N (PA11)
B5	CC2(1)	UCPD_CC2_C	A8	SBU1	-
B4	VBUS	VBUSc	A9	VBUS	VBUSc
B3	TX2_N	-	A10	RX2_N	-
B2	TX2_P	-	A11	RX2_P	-
B1	GND	GND	A12	GND	GND

1. *The CCx pins from CN4 are connected to the CCxc pins of TCPP01-M12. Depending on use cases, CCx signals might be used to connect to UCPD.ADCx signals of MCU (PG0 and PF15).*

9.2 Debug connector (CN11)

The Discovery kit embeds a MIPI10 debug connector on the bottom side of the main board (the 14-pin footprint also enables the support of an STDC14 connector as an option):

- MIPI10 10-pin connector on the 14-pin footprint (default configuration)
- STDC14 14-pin connector (option)

Attention: *Before using CN11, check specific constraints in Section 7.4.5: SWD debug/program/trace and JTAG/USART.*

9.2.1 MIPI10 debug connector (default configuration)

Figure 27. MIPI10 debug connector (CN11)

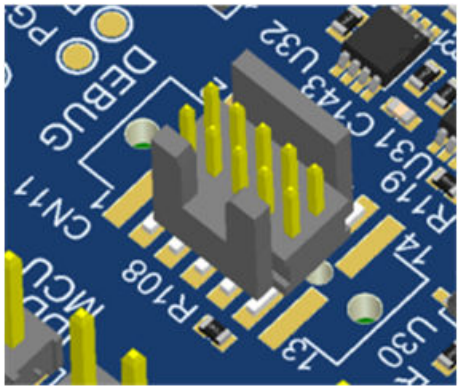


Table 22. **MIPI10 on STDC14 footprint**

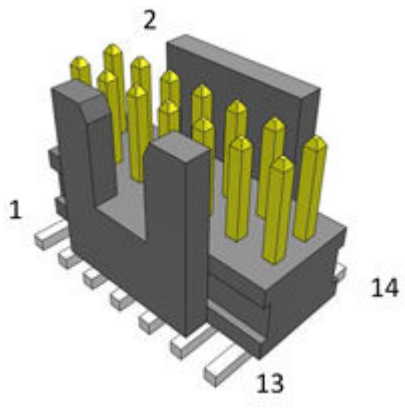
Pin number	Description	Signal assignment	Pin number	Description	Signal assignment
1	-	-	2	-	-
3	VDD power	VDD (1.8 V)	4	SWDIO/JTMS	T.SWDIO (PA13)
5	GND	GND	6	SWCLK/JTCK	T.SWCLK (PA14)
7	KEY	GND	8	SWO/JTDO	T.SWO (PB3)
9	-	-	10	JTDI	T.JTDI (PA15)
11	GNDDetect	100 Ω pull-down	12	RESET	NRST
13	-	-	14	-	-

Note: Pins 1, 2, 13, and 14 belong to the STDC14 footprint and are not accessible with a MIPI10 compatible probe.

9.2.2 STDC14 debug connector (option)

The STDC14 debug connector might be implemented, depending on supported tools, for easy interface with ST tools ecosystem.

Figure 28. **STDC14 debug connector (CN11)**



DT52375V1

If needed, a MIPI10 compatible probe can be plugged into the STDC14 connector (CN11) but you might have to bend or cut pins 1, 2, 13, and 14.

Table 23. **STDC14 connector pinout**

Pin number	Description	Signal assignment	Pin number	Description	Signal assignment
1	-	-	2	-	-
3	VDD power	VDD (1.8V)	4	SWDIO/JTMS	T.SWDIO (PA13)
5	GND	GND	6	SWCLK/JTCK	T.SWCLK (PA14)
7	KEY	GND	8	SWO/JTDO	T.SWO (PB3)
9	-	-	10	JTDI	T.JTDI (PA15)
11	GNDDetect	100 Ω pull-down	12	RESET	NRST
13	RX	USART1_RX (PA10)	14	TX	USART1_TX (PA9)

Note: USART1_RX and USART1_TX are signals from STM32U5x9NJ.

9.3 TAG connector (CN3)

A Tag-Connect™ 10-pin footprint is implemented on the top side of STM32U5x9J-DKx (on the border of the PCB). A 10-pin compatible cable can be used to connect to the STM32U5x9J-DKx Discovery kits.

Attention: *Before using CN3, check specific constraints in Section 7.4.5: SWD debug/program/trace and JTAG/USART.*

Figure 29. TAG connector (CN3)

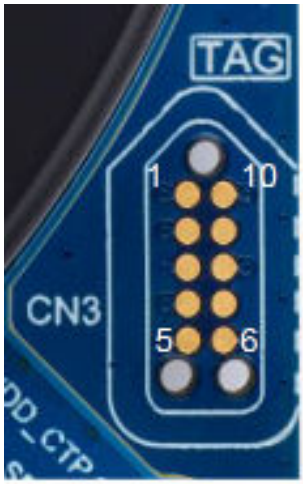


Figure 30. 10-pin compatible cable example

Table 24. TAG connector pinout

Pin number	Description	Signal assignment	Pin number	Description	Signal assignment
1	VDD	VDD (1.8V)	10	NRST	T_NRST (PG10)
2	SWDIO/JTMS	T.SWDIO (PA13)	9	-	-
3	GND	GND	8	JTDI	T.JTDI (PA15)
4	SWCLK/JTCK	T.SWCLK (PA14)	7	-	-
5	GND	-	6	SWO/JTDO	T.SWO (PB3)

9.4 DSI_V3 display board connector (CN2)

The 64-pin DSI V3 connector (CN2) supports DSI_V3 display add-on boards.

Pin 61 to 64 (central pads for ground reference) are not accessible when an add-on board is plugged in.

The mating connectors used on the MB1829 main board and the MB1835 LCD daughterboard are set to ensure a total height of 8 mm between boards.

Figure 31. DSI_V3 display connector (CN2)

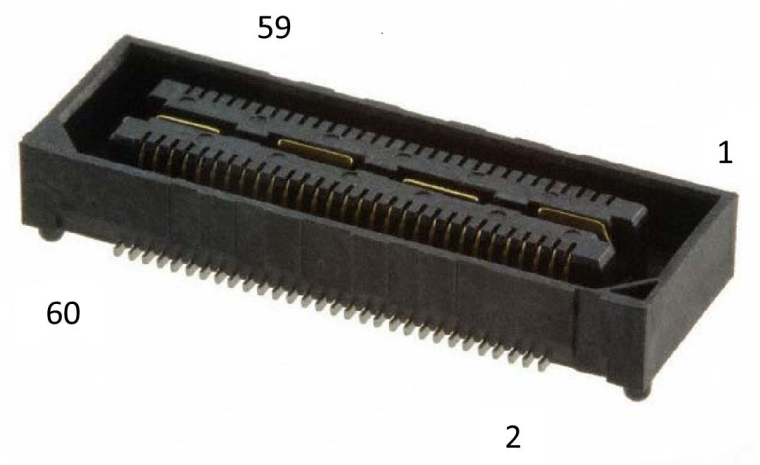


Table 25. DSI_V3 connector pin assignment (CN2)

Function	GPIO	Signal name	Pin number (CN2)		Signal name	GPIO	Function
General ground	-	GND	1	2	NC	-	-
Differential DSI clock(1)	-	DSI.CK_**N**	3	4	DSI_TOUCH_INT	PE8	Touch interrupt
	-	DSI.CK_**P**	5	6	GND	-	General ground
General ground	-	GND	7	8	DSI_D2_P	-	Not connected
Differential DSI data 0	-	DSI.D0_P	9	10	DSI_D2_N	-	Not connected
	-	DSI.D0_N	11	12	GND	-	General ground
General ground	-	GND	13	14	DSI_D3_P	-	Not connected
Differential DSI data 1	-	DSI.D1_P	15	16	DSI_D3_N	-	Not connected
	-	DSI.D1_N	17	18	GND		General ground
General ground	-	GND	19	20	NC	-	-
Power output	-	5V_LCD	21	22	DSI_SPI_CS	PD8	SPI chip select
Power output	-	5V_LCD	23	24	DSI_SPI_CLK	PB13/ PD10	SPI/USART clock
-	-	NC	25	26	DSI_SPI_MOSI	PD4/ PB10	SPI/USART data
-	-	BLGND	27	28	DSI_SPI_DCX	PD11	SPI data/control
-	-	BLGND	29	30	NC	-	-
-	-	NC	31	32	RESERVED	-	-
-	-	NC	33	34	NC	-	-
-	-	NC	35	36	3V3_LCD	-	3.3 V voltage
-	-	NC	37	38	VDD_LCD	-	VDD voltage reference (1.8 V)

Function	GPIO	Signal name	Pin number (CN2)		Signal name	GPIO	Function
-	-	NC	39	40	I2C5.SDA	PH4	Touch panel I²C data
-	-	NC	41	42	NC	-	-
SWIRE	PI7	DSI_SWIRE	43	44	I2C5.SCL	PH5	Touch panel I²C clock
-	-	NC	45	46	NC	-	-
-	-	NC	47	48	NC	-	-
Tearing effect	PF11	DSI_TE	49	50	NC	-	-
-	-	NC	51	52	NC	-	-
DSI backlight control output	PI6	DSI_BL_CTRL	53	54	NC	-	-
-	-	NC	55	56	NC	-	-
DSI and touch panel reset output	PD5	DSI_RESETn	57	58	NC	-	-
-	-	NC	59	60	1V8_LCD	-	1.8-V voltage
General ground	-	GND	61	62	GND	-	General ground
General ground	-	GND	63	64	GND	-	General ground

1. *The microcontroller software system must invert the DSI.CK_N and DSI.CK_P lines together to be aligned with the DSI_V3 add-on boards. The DSI clock differential signals (_N and _P) are originally inverted on the main board for layout reasons (refer to DSI_V3 connector standard pinning).*

9.5 Audio jack (not used) (CN6)

Note: SAI audio codec and audio jack are not present by default.

The 3.5 mm stereo audio jack supports stereo line or headphone outputs and an analog microphone:

Figure 32. Audio jack connector (CN6)

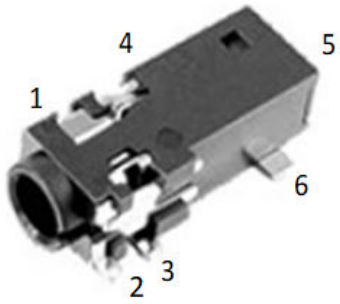


Table 26. Audio jack (CN6) pinout

Pin number	Description		Audio jack mating pinning
6	OUT_Left	SPK_L (33 Ω typical, 16 Ω minimum)	
4	OUT_Right	SPK_R (33 Ω typical, 16 Ω minimum)	
3	GND	GND	
2	MIC_IN	MIC (1.5 kΩ typical)	
1	NC	-	
5	NC	-	

9.6 STLINK-V3E USB Micro-B connector (CN5)

The USB connector (CN5) is used to interface with STLINK-V3E. It is compatible with USB 2.0 high-speed transfer data rate.

Figure 33. USB Micro-B connector (CN5)

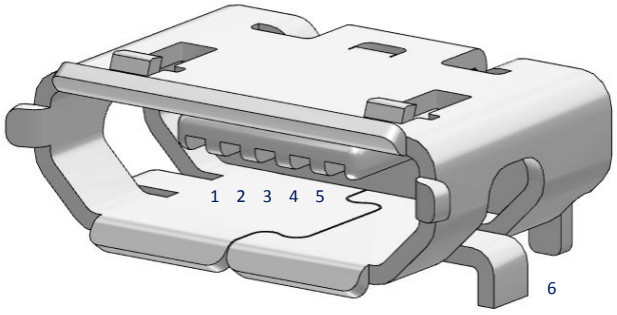


Table 27. USB Micro-B (CN5) pinout

Pin number	Description	Pin number	Description
1	VBUS	4	ID -not used
2	DM	5, 6	GND, Shield
3	DP	-	-

9.7 Expansion connectors (CN9 and CN10)

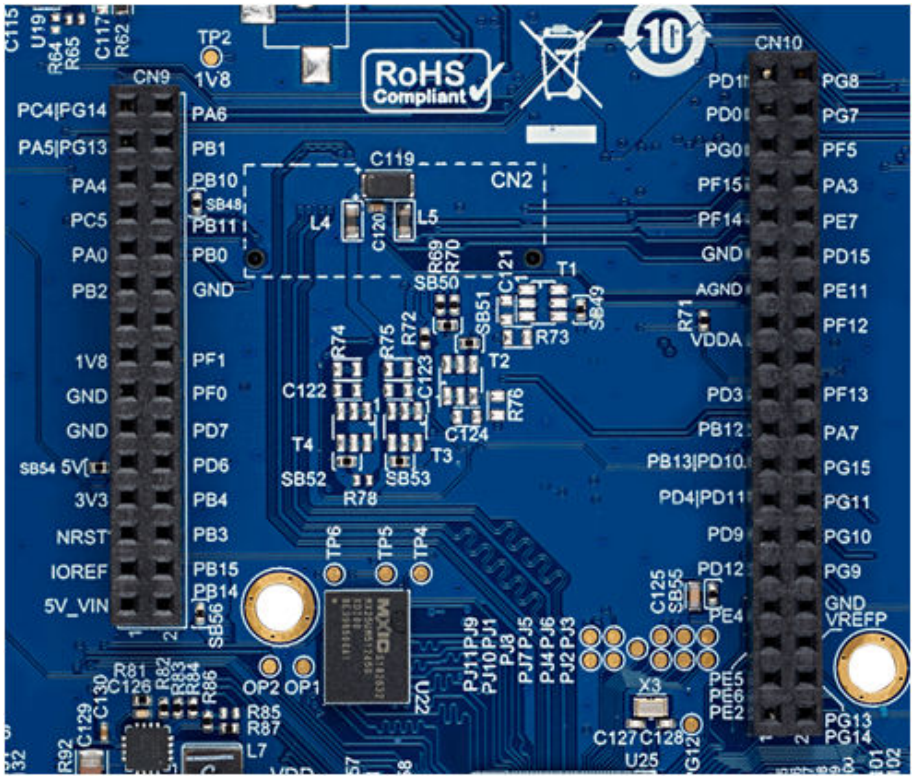
Attention: *Refer to Section 8.10: Expansion connectors for detailed electrical and functional constraints and refer to Section 7.3: Mechanical drawings for mechanical constraints.*

The two expansion connectors are described below:

- CN9 is a 30-pin double row, female, through-hole, 2.54 mm pitch connector of about 8.5 mm insulator height.
- CN10 is a 38-pin double row, female, through-hole, 2.54 mm pitch connector of about 8.5 mm insulator height.

9.7.1 Pin assignment and connectors

Figure 34. Female expansion connectors (CN9 and CN10)



The pinout of both connectors is summarized in Table 28 and Table 29.

The bold text describes the default configuration.

Table 28. Connector pinout (bottom view) (CN9)

Pin	Pin name: marking	Signal description	STM32 pin	MCU function	Pin	Pin name/ marking	Signal description	STM32 pin	MCU function
29	**PC4**/ PG14	**ADC12_IN13**/ I2C1_SCL	PC4	**ADC12**/I2C1	30	PA6	USART3_CTS	PA6	USART3
27	**PA5**/ PG13	**ADC124_IN10**/ I2C1_SDA	PA5	**ADC124**/I2C1	28	PB1	USART3_RTS	PB1	USART3
25	PA4	ADC124_IN9	PA4	ADC124	26	PB10	USART3_TX	PB10	USART3
23	PC5	ADC12_IN14	PC5	ADC12	24	PB11	USART3_RX	PB11	USART3
21	PA0	ADC12_IN5	PA0	ADC12	22	PB0	USART3_SCLK	PB0	USART3

Pin	Pin name: marking	Signal description	STM32 pin	MCU function	Pin	Pin name/ marking	Signal description	STM32 pin	MCU function
19	PB2	ADC12_IN17	PB2	ADC12	20	GND	GND	-	-
17	-	-	-	-	18	-	-	-	-
15	1V8	1V8	-	1V8 supply (opt)	16	PF1	I2C2_SCL	PF1	I2C2
13	GND	GND	-	GND	14	PF0	I2C2_SDA	PF0	I2C2
11	GND	GND	-	GND	12	PD7	SDMMC2_CMD	PD7	SDMMC2
9	5V	5V	-	5V supply(1)	10	PD6	SDMMC2_CK	PD6	SDMMC2
7	3V3	3V3	-	3V3 supply	8	PB4	SDMMC2_D3	PB4	SDMMC2
5	NRST	NRST	NRST	RESET	6	PB3	SDMMC2_D2	PB3	SDMMC2
3	IOREF	IOREF	-	VDD IO supply	4	PB15	SDMMC2_D1	PB15	SDMMC2
1	5V_VIN	5V_VIN	-	5V source(2)	2	PB14	SDMMC2_D0	PB14	SDMMC2

1. *5V output supply to the add-on board*
2. *5V input supply to the MB1829 board*

Note: Pins 17 and 18 are free of use.

Table 29. Connector pinout (bottom view) (CN10)

Pin	Pin name: marking	Signal description	STM32 pin	MCU function	Pin	Pin name/ marking	Signal description	STM32 pin	MCU function
37	PD1	I2C6_SCL	PD1	I2C6	38	PG8	LPUART1_RX	PG8	LPUART1
35	PD0	I2C6_SDA	PD0	I2C6	36	PG7	LPUART1_TX	PG7	LPUART1
33	PG0	**NC**/ADC4_IN7	**NC**/PG0	**NC**/ADC4	34	PF5	I/O	PF5	I/O
31	PF15	**NC**/ADC4_IN6	**NC**/PF15	**NC**/ADC4	32	PA3	TIM2_CH4	PA3	TIM2
29	PF14	ADC4_IN5	PF14	ADC4	30	PE7	I/O or SAI1_SD_B	PE7	I/O or SAI1
27	GND	GND	GND	GND	28	PD15	TIM4_CH4	PD15	TIM4
25	AGND	AGND	AGND	AGND	26	PE11	TIM1_CH2	PE11	TIM1
23	AVDD	VDDA	VDDA	VDDA	24	PF12	I/O	PF12	I/O
21	-	-	-	-	22	-	-	-	-
19	PD3	SPI2_MISO	PD3	SPI2	20	PF13	IO	PF13	I/O
17	PB12	SPI2_NSS	PB12	SPI2	18	PA7	TIM3_CH2	PA7	TIM3
15	**PB13**/ PD10	**SPI2_SCK**/ SAI2_SCK	**PB13**/ PD10	**SPI2**/SAI2	16	PG15	**SPI3_CS**/ LPTIM1_CH1	PG15	**SPI3**/ LPTIM1
13	**PD4**/ PD11	**SPI2_MOSI**/ SAI2_SD_A	**PD4**/ PD11	**SPI2**/SAI2	14	PG11	**SPI3_MOSI**/ TIM15_CH2	PG11	**SPI3**/ TIM15
11	PD9	SAI2_MCLK	PD9	SAI2	12	PG10	SPI3_MISO	PG10	SPI3
9	PD12	SAI2_FS	PD12	SAI2	10	PG9	SPI3_SCK	PG9	SPI3
7	PE4	SAI1_FS	PE4	SAI1	8	GND	GND	-	-
5	PE5	SAI1_SCK	PE5	SAI1	6	VREFP	VREFP	VREFP	VREF+
3	PE6	SAI1_SD_A	PE6	SAI1	4	PG13	I2C1_SDA	PG13	I2C1
1	PE2	SAI1_MCLK	PE2	SAI1	2	PG14	I2C1_SCL	PG14	I2C1

Note: Pins 21 and 22 are free of use.

9.8 20-pin audio MEMS connector (CN1)

Note: The 20-pin audio MEMS connector function is a differentiating feature, refer to Section 2: Ordering information.

The 20-pin audio MEMS connector allows connecting ADF or MDF audio MEMS add-on boards.

Figure 35. 20-pin audio MEMS connector (CN1)

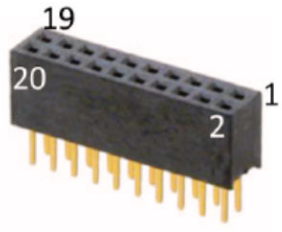


Table 30. 20-pin audio MEMS connector pinout (CN1)

Pin number	Description	Assignment	Pin number	Description	Assignment
1	GND	Ground	2	VDD	VDD (1.8 V)
3	-	-	4	CCK0	MIC.CCK0 (PF3)
5	SDIN4	MIC.SDIN4 (PE10)	6	SDIN0	MIC.SDIN0 (PF4)
7	-	-	8	-	-
9	-	-	10	-	-
11	-	-	12	MEMS_LED (3.3 V)	Audio_MEMs_LED (PE13)
13	-	-	14	-	-
15	-	-	16	-	-
17	-	-	18	-	-
19	VDD	VDD (1.8 V)	20	GND	Ground

10 Jumpers and solder bridges

10.1 Jumpers

The jumper functions and their default status are described in Table 31.

Table 31. Jumper configuration

Reference	Jumper[1]	Function	Comment
JP1	**ON**	3V3 connected to SMPS output	SMPS powers 3V3. No current measurement.
	OFF	3V3 not connected to SMPS output	3V3 is not powered. Add an ammeter to power the MCU and peripherals and measure the current.
JP2	**ON**	VDD connected to SMPS output	SMPS powers VDD for peripherals. No current measurement.
	OFF	VDD not connected to SMPS output	VDD is not powered. Add an ammeter to power the peripherals and measure the current.
JP3	**ON**	VDD_MCU connected to SMPS output	SMPS powers VDD_MCU. No current measurement.
	OFF	VDD_MCU not connected to SMPS output	VDD_MCU is not powered. Add an ammeter to power the MCU and measure the current.
JP4	**STLK**	5 V is supplied by USB STLK (CN5).	• 5 V (+10%/-5%), • 800 mA typical overcurrent protection • Up to 500 mA capable
	CHGR	5 V is supplied by USB STLK (CN5).	• 5 V (+10%/-5%) • No embedded current protection • Up to 1.5 A current
	USBC	5 V is supplied by the USB Type-C® connector (CN4).	• 5 V (+10%/-5% at current < 500 mA) • 5 V (+/-10% at current < 1.5 A) • No embedded current protection • Up to 3 A (check USB Type-C® VBUS constraints in that case)
	E5V	5 V is supplied by 5V_VIN and GND pins on the expansion connector (CN9).	• 5 V (+/-5%), up to 2 A • No embedded current protection (can be included on the expansion add-on board)
JP5[2]	**ON**	T_NRST (PA6)	STLINK-V3E T_NRST output reset connected to NRST of STM32U5x9NJ
	OFF		STLINK-V3E T_NRST output reset isolated from NRST of STM32U5x9NJ
JP6[2]	**OFF**	STLINK-V3E active	STLINK-V3E detects a USB ST-LINK plug on CN5.
	ON	STLINK-V3E Reset state	Set STLINK-V3E in Reset mode (all I/Os in high impedance). There is no power from JP4 STLK.

1. *The default setting is in bold.*
2. *JP5 and JP6 must not be ON together.*

10.2 Solder bridges

The solder bridge functions and their default status are described in Table 32.

Table 32. Solder bridge configuration

SB name	Status[1]	Function	Comment
SB1	ON	VL_AUDIO connection	Connect VL_AUDIO to VDD
	OFF		**Isolate VL_AUDIO from VDD**
SB2	ON	1V8_AUDIO connection	Connect 1V8_AUDIO to 1V8
	OFF		**Isolate 1V8_AUDIO from 1V8**
SB3	ON	1V8_AUDIO connection	Connect 1V8_AUDIO to VDD
	OFF		**Isolate 1V8_AUDIO from VDD**
SB4	**ON**	VDD_MEMs connection	**Connect VDD_MEMs to VDD**
	OFF		Isolate VDD_MEMs from VDD
SB5	**ON**	VDD_MEMs connection	**Connect VDD_MEMs to IOVDD (ToF sensor)**
	OFF		Isolate VDD_MEMs from IOVDD (ToF sensor)
SB6	**ON**	ADC12_IN13 connection on CN9	**ADC12_IN13 (PC4) is connected to CN9**
	OFF		ADC12_IN13 (PC4) is not connected to CN9
SB7	ON	I2C1.SCL connection on CN9	I2C1.SCL (PG14) is connected to CN9
	OFF		**I2C1.SCL (PG14) is not connected to CN9**
SB8	ON	I2C1.SDA connection on CN9	I2C1.SDA (PG13) is connected to CN9
	OFF		**I2C1.SDA (PG13) is not connected to CN9**
SB9	**ON**	ADC124_IN10 connection on CN9	**ADC124_IN10 (PA5) is connected to CN9**
	OFF		ADC124_IN10 (PA5) is not connected to CN9
SB10	ON	ADC4_IN7 connection on CN9	ADC4_IN7 (PG0) is connected to CN9
	OFF		**ADC4_IN7 (PG0) is not connected to CN9**
SB11	ON	ADC4_IN6 connection on CN9	ADC4_IN6 (PF15) is connected to CN9
	OFF		**ADC4_IN6 (PF15) is not connected to CN9**
SB12	ON	AVDD (ToF sensor) connection	Connect AVDD (ToF sensor) to VDD
	OFF		**Isolate AVDD (ToF sensor) from VDD**
SB13	ON	AVDD (ToF sensor) connection	Connect AVDD (ToF sensor) to 2V8
	OFF		**Isolate AVDD (ToF sensor) from 2V8**
SB14	ON	SPI_MOSI connection on CN2	Connect SPI_MOSI to PB10
	OFF		**Let SPI_MOSI floating**
SB15	ON	SPI_USART_CS connection on CN2	Connect SPI_USART_CS to PD8
	OFF		**Let SPI_USART_CS floating**
SB16	ON	SPI_CLK connection on CN2	Connect SPI_CLK to PD10
	OFF		**Let SPI_CLK floating**
SB17	ON	SPI_CLK connection on CN2	Connect SPI_CLK to PB13
	OFF		**Let SPI_CLK floating**
SB18	ON	SPI_D/CX connection on CN2	Connect SPI_D/CX to PD11
	OFF		**Let SPI_D/CX floating**

SB name	Status[1]	Function	Comment
SB19	ON	SPI_MOSI connection on CN2	Connect SPI_MOSI to PD4
	OFF		**Let SPI_MOSI floating**
SB20	**ON**	CN10 pin 19 connection	**Connect pin 19 to PD3 (SPI2_MISO)**
	OFF		Isolate pin 19 from PD3 (SPI2_MICO)
SB21	**ON**	CN10 pin 17 connection	**Connect pin 17 to PB12 (SPI2_NSS)**
	OFF		Isolate pin 17 from PB12 (SPI2_NSS)
SB22	ON	CN10 pin 15 connection	Connect pin 15 to PD10 (SAI2_SCK)
	OFF		**Isolate pin 15 from PD10 (SAI2_SCK)**
SB23	**ON**	CN10 pin 15 connection	**Connect pin 15 to PB13 (SPI2_SCK)**
	OFF		Isolate pin 15 from PB13 (SPI2_SCK)
SB24	**ON**	CN10 pin 13 connection	**Connect pin 13 to PD4 (SPI2_MOSI)**
	OFF		Isolate pin 13 from PD4 (SPI2_MOSI)
SB25	ON	CN10 pin 13 connection	Connect pin 13 to PD11 (SAI2_SD_A)
	OFF		**Isolate pin 13 from PD11 (SAI2_SD_A)**
SB26	**ON**	5V_VIN connection on CN9	**5V_VIN connected on CN9**
	OFF		5V_VIN not connected on CN9
SB27	**ON**	VDD_OCTOSPI connection	**Connect VDD_OCTOSPI to VDD**
	OFF		Isolate VDD_OCTOSPI from VDD
SB28	ON	STLK_MCO connection to the main MCU	STLK_MCO connected to OSC_IN of main MCU
	OFF		**STLK_MCO is not connected to the main MCU**
SB29	**ON**	VBAT connection	**VBAT is connected to VDD_MCU**
	OFF		VBAT not connected to VDD_MCU
SB30	**ON**	AGND to GND connection	**AGND connected to GND close to MCU**
	OFF		AGND disconnected from GND (connect L1 or C37)
SB31	**ON**	VREFP current measurement	**VREFP is connected to VDDA**
	OFF		VREFP is floating
SB32	**ON**	VDDDSI current measurement	**VDDDSI is connected to VDD_MCU**
	OFF		VDDDSI is floating
SB33	**ON**	SDMMC2_D2 connection to CN9	**Connect SDMMC2_D2 (PB3) to CN9**
	OFF		Isolate SDMMC2_D2 (PB3) from CN9
SB34	ON	PB3 connection to T.SWO	Connect PB3 to T.SWO
	OFF		**Isolate PB3 from T.SWO**
SB35	ON	VDDUSB connection	Connect VDDUSB to VDD_MCU
	OFF		**Isolate VDDUSB from VDD_MCU**
SB36	**ON**	VDDA connection	**VDDA is connected to VDD_MCU**
	OFF		VDDA not connected to VDD_MCU
SB37	**ON**	VDDUSB connection	**Connect VDDUSB to 3V3**
	OFF		Isolate VDDUSB from 3V3
SB38	ON	UCPD.ADC1 connection to PA15	UCPD.ADC1 connection to PA15 (needs SB43)
	OFF		**UCPD.ADC1 is not connected to PA15**
SB39	ON	VCC_eMMC connection	Connect VCC_eMMC to VDD

SB name	Status[1]	Function	Comment
SB39	**OFF**	VCC_eMMC connection	**Isolate VCC_eMMC from VDD**
SB40	ON	UCPD.ADC2 connection to PB15	UCPD.ADC2 connection to PB15 (needs SB46)
	OFF		**UCPD.ADC2 is not connected to PB15**
SB41	**ON**	VCC_eMMC connection	**Connect VCC_eMMC to 3V3**
	OFF		Isolate VCC_eMMC from 3V3
SB42	**ON**	PA15 connection to T.JTDI	**Connect PA15 to T.JTDI**
	OFF		Isolate PA15 from T.JTDI
SB43	ON	PA15 connection to UCPD.CC1	Connect PA15 to UCPD.CC1
	OFF		**Isolate PA15 from UCPD.CC1**
SB44	**ON**	VCCQ_eMMC connection	**Connect VCCQ_eMMC to VDD**
	OFF		Isolate VCCQ_eMMC from VDD
SB45	**ON**	SDMMC2_D1 connection to CN9	**Connect SDMMC2_D1 (PB15) to CN9**
	OFF		Isolate SDMMC2_D1 (PB15) from CN9
SB46	ON	PB15 connection to UCPD.CC2	Connect PB15 to UCPD.CC2
	OFF		**Isolate PB15 from UCPD.CC2**
SB47	**ON**	VDD_HEXASPI connection	**Connect VDD_HEXASPI to VDD**
	OFF		Isolate VDD_HEXASPI from VDD
SB48	**ON**	PB10 connection to CN9	**Connect USART3_TX (PB10) to CN9**
	OFF		Isolate USART3_TX (PB10) from CN9
SB49	**ON**	1V8_LCD connection	**Connect 1V8_LCD to 1V8**
	OFF		Isolate 1V8_LCD from 1V8
SB50	**ON**	I2C5 pull-ups connection	**Connect I2C5 pull-ups to VDD_LCD**
	OFF		Isolate I2C5 pull-ups from VDD_LCD
SB51	**ON**	VDD_LCD connection	**VDD_LCD is connected to 1V8.**
	OFF		Isolate VDD_LCD from VDD
SB52	**ON**	5V_LCD connection	**5V_LCD is connected to 5V.**
	OFF		Isolate 5V_LCD from 5V
SB53	**ON**	3V3_LCD connection	**3V3_LCD is connected to 3V3.**
	OFF		Isolate 3V3_LCD from 3V3
SB54	**ON**	5V connection on CN9	**5V connected on CN9**
	OFF		5V not connected on CN9
SB55	**ON**	VREFP connection to CN10	**Connect VREFP supply to CN10**
	OFF		VREFP is not connected to CN10.
SB56	**ON**	IOREF (VDD) connection to CN9	**Connect IOREF (VDD) to CN9**
	OFF		Isolate IOREF (VDD) from CN9
SB57	**ON**	UCPD.ADC2 (PF15) connection to USB-C	**UCPD.ADC2 (PF15) is connected to USB-C.**
	OFF		UCPD.ADC2 (PF15) is not connected to USB-C.
SB58	**ON**	UCPD.ADC1 (PG0) connection to USB-C	**UCPD.ADC1 (PG0) is connected to USB-C.**
	OFF		UCPD.ADC1 (PG0) is not connected to USB-C.
SB59	**ON**	Access to PA8 (MCO debug)	**PA8 access through SB59**
	OFF		PA8 access on SB59 footprint

SB name	Status[1]	Function	Comment
SB60	**ON**	3V3 connection to AVDD of ToF sensor	**3V3 is connected to AVDD_TOF_SENSOR.**
	OFF		3V3 is disconnected from AVDD_TOF_SENSOR.
SB61	**ON**	GND connection to TAG connector pin 5	**GND is connected to TAG pin 5.**
	OFF		GND is disconnected from TAG pin 5.

1. *The default setting is in bold.*

11 STM32U5x9NJH6Q MCU I/O assignment

Note: Free MCU GPIOs are easily accessible on test points identified by their GPIO name marking on board (PI4 not accessible, OP1/OP2 for OPAMP1/2 VINM pins).

Note: In this table, “Exp. conn.” stands for Expansion connectors.

Table 33. STM32U5x9NJH6Q MCU I/O assignment

STM32U5x9NJ pin name	Signal assignment	Main function (default)	Secondary function	Pin number of expansion connector or test point reference
PA0	ADC12_IN5	Exp. conn. ADC	-	Pin 21 of CN9
PA1	OCTOSPIM_P1.DQS	Octo-SPI	-	-
PA2	OCTOSPIM_P1.NCS	Octo-SPI	-	-
PA3	TIM2_CH4	Exp. conn. TIMER	-	Pin 32 of CN10
PA4	ADC124_IN9	Exp. conn. ADC	-	Pin 25 of CN9
PA5	ADC124_IN10	Exp. conn. ADC	-	Pin 27 of CN9
PA6	USART3 _CTS	Exp. conn. USART3	-	Pin 30 of CN9
PA7	TIM3_CH2	Exp. conn. TIMER	-	Pin 18 of CN10
PA8	-	-	MCO output	On SB59
PA9	T.VCP_TX (USART1_TX)	STLINK-V3E	VCP BOOT USART	-
PA10	T.VCP_RX (USART1_RX)	STLINK-V3E	VCP BOOT USART	-
PA11	USBC.HS_P	USB Type-C	-	-
PA12	USBC.HS_N	USB Type-C	-	-
PA13	T.SWDIO	STLINK-V3E/SWD debug	JTMS JTAG debug	-
PA14	T.SWCLK	STLINK-V3E/SWD debug	JTCK JTAG debug	-
PA15	T.JTDI	-	JTDI JTAG debug/ UCPD.CC1	-
PB0	USART3 _SCLK	Exp. conn. USART3	-	Pin 22 of CN9
PB1	USART3 _RTS	Exp. conn. USART3	-	Pin 28 of CN9
PB2	ADC12_IN17	Exp. conn. ADC	-	Pin 19 of CN9
PB3	SDMMC2_D2	Exp. conn. SDMMC2	T.SWO or JTDO JTAG debug	Pin 6 of CN9
PB4	SDMMC2_D3	Exp. conn. SDMMC2	JTNRST JTAG debug	Pin 8 of CN9
PB5	TOF_INTN	ToF sensor	-	-
PB6	I2C4.SCL	I^2C for audio codec	-	-
PB7	I2C4.SDA	I^2C for audio codec	-	-
PB8	SDMMC1.D4	eMMC	-	-
PB9	SDMMC1.D5	eMMC	-	-
PB10	USART3 _TX	Exp. conn. USART3	DSI_V3 connector	Pin 26 of CN9
PB11	USART3 _RX	Exp. conn. USART3	-	Pin 24 of CN9
PB12	SPI2 _NSS	Exp. conn. SPI2	-	Pin 17 of CN10
PB13	SPI2 _SCK	Exp. conn. SPI2	DSI_V3 connector	Pin 15 of CN10

STM32U5x9NJ pin name	Signal assignment	Main function (default)	Secondary function	Pin number of expansion connector or test point reference
PB14	SDMMC2_D0	Exp. conn. SDMMC2	-	Pin 2 of CN9
PB15	SDMMC2_D1	Exp. conn. SDMMC2	UCPD.CC2	Pin 4 of CN9
PC0	OCTOSPIM_P1.IO7	Octo-SPI	-	-
PC1	OCTOSPIM_P1.IO4	Octo-SPI	-	-
PC2	OCTOSPIM_P1.IO5	Octo-SPI	-	-
PC3	OCTOSPIM_P1.IO6	Octo-SPI	-	-
PC4	ADC12_IN13	Exp. conn. ADC	-	Pin 29 of CN9
PC5	ADC12_IN14	Exp. conn. ADC	-	Pin 23 of CN9
PC6	SDMMC1.D6	eMMC	-	-
PC7	SDMMC1.D7	eMMC	-	-
PC8	SDMMC1.D0	eMMC	-	-
PC9	SDMMC1.D1	eMMC	-	-
PC10	SDMMC1.D2	eMMC	-	-
PC11	SDMMC1.D3	eMMC	-	-
PC12	SDMMC1.CK	eMMC	-	-
PC13	USER_Button	Button	Wake-up	-
PC14-OSC32_IN	PC14-OSC32_IN	37.768 kHz LSE oscillator	-	-
PC15-OSC32_OUT	PC15-OSC32_OUT	37.768 kHz LSE oscillator	-	-
PD0	I2C6_SDA	Exp. conn. I2C6	-	Pin 35 of CN10
PD1	I2C6_SCL	Exp. conn. I2C6	-	Pin 37 of CN10
PD2	SDMMC1.CMD	eMMC	-	-
PD3	SPI2_MISO	Exp. conn. SPI2	-	Pin 19 of CN10
PD4	SPI2_MOSI	Exp. conn. SPI2	DSI_V3 connector	Pin 13 of CN10
PD5	DSI_RESETn	DSI_V3 connector	-	-
PD6	SDMMC2_CK	Exp. conn. SDMMC2	-	Pin 10 of CN9
PD7	SDMMC2_CMD	Exp. conn. SDMMC2	-	Pin 12 of CN9
PD8	DSI_SPI_USART_CS	-	DSI_V3 connector	
PD9	SAI2_MCLK	Exp. conn. option	-	Pin 11 of CN10
PD10	SAI2_SCK	Exp. conn. option	DSI_V3 connector USART3_CK	Pin 15 of CN10
PD11	SAI2_SD_A	Exp. conn. option	DSI_V3 connector DSI_SPI_D/CX	Pin 13 of CN10
PD12	SAI2_FS	Exp. conn. option	-	Pin 9 of CN10
PD13	PD13 (free)	-	-	TP25
PD14	PD14 (free)	-	-	TP31
PD15	TIM4_CH4	Exp. conn. TIMER	-	Pin 28 of CN10
PE0	LED_GREEN	USER LED	-	-
PE1	LED_RED	USER LED	-	-
PE2	SAI1.MCLK_A	SAI1 for audio codec and Exp. conn.	SAI1_MCLK	Pin 1 of CN10
PE3	SAI1.SD_B	SAI1 for audio codec	-	-

STM32U5x9NJ pin name	Signal assignment	Main function (default)	Secondary function	Pin number of expansion connector or test point reference
PE4	SAI1.FS_A	SAI1 for audio codec and Exp. conn.	SAI1_FS	Pin 7 of CN10
PE5	SAI1.SCK_A	SAI1 for audio codec and Exp. conn.	SAI1_SCK	Pin 5 of CN10
PE6	SAI1.SD_A	SAI1 for audio codec and Exp. conn.	SAI1_SD_A	Pin 3 of CN10
PE7	SAI1_SD_B	SAI1 for Exp. conn.	-	Pin 30 of CN10
PE8	DSI_TOUCH_INT	DSI_V3 connector	-	-
PE9	UCPD.DBn	USB Type-C	-	-
PE10	MIC.SDIN4	20-pin audio MEMs	-	-
PE11	TIM1_CH2	Exp. conn. TIMER	-	Pin 26 of CN10
PE12	UCPD.FLT	USB Type-C	-	-
PE13	AUDIO_MEMs_LED	20-pin audio MEMs	-	-
PE14	TOF_LPN	ToF sensor	-	-
PE15	PE15 (free)	-	-	TP24
PF0	I2C2_SDA	Exp. conn. I2C2	-	Pin 14 of CN9
PF1	I2C2_SCL	Exp. conn. I2C2	-	Pin 16 of CN9
PF2	TEMP_INTN	Temperature sensor	-	-
PF3	MIC.SDIN0	20-pin audio MEMs	-	-
PF4	MIC.CCK0	20-pin audio MEMs	-	-
PF5	PF5	Exp. conn. PIO	-	Pin 34 of CN10
PF6	OCTOSPIM_P1.IO3	Octo-SPI	-	-
PF7	OCTOSPIM_P1.IO2	Octo-SPI	-	-
PF8	OCTOSPIM_P1.IO0	Octo-SPI	-	-
PF9	OCTOSPIM_P1.IO1	Octo-SPI	-	-
PF10	OCTOSPIM_P1.CLK	Octo-SPI	-	-
PF11	DSI_TE	-	DSI_V3 connector	-
PF12	PF12	Exp. conn. PIO	-	Pin 24 of CN10
PF13	PF13	Exp. conn. PIO	-	Pin 20 of CN10
PF14	ADC4_IN5	Exp. conn. ADC	-	Pin 29 of CN10
PF15	UCPD.ADC2	USB Type-C	Exp. conn. ADC4_IN6	Pin 31 of CN10
PG0	UCPD.ADC1	USB Type-C	Exp. conn. ADC4_IN7	Pin 33 of CN10
PG1	VBUS_SENSE	USB Type-C	-	-
PG2	PG2 (free)	-	-	TP26
PG3	PG3 (free)	-	-	TP30
PG4	PG4 (free)	-	-	TP27
PG5	PG5 (free)	-	-	TP29
PG6	PG6 (free)	-	-	TP28
PG7	LPUART1_TX	Exp. conn. LPUART1	-	Pin 36 of CN10
PG8	LPUART1_RX	Exp. conn. LPUART1	-	Pin 38 of CN10

STM32U5x9NJ pin name	Signal assignment	Main function (default)	Secondary function	Pin number of expansion connector or test point reference
PG9	SPI3_SCK	Exp. conn. SPI3	-	Pin 10 of CN10
PG10	SPI3_MISO	Exp. conn. SPI3	-	Pin 12 of CN10
PG11	SPI3_MOSI_TIM15_CH12	Exp. conn. SPI3	TIMER	Pin 14 of CN10
PG12	PG12 (free)	-	-	TP21
PG13	I2C1.SDA	Exp. conn. I2C1	-	Pin 4 of CN10 Pin 27 of CN9 option
PG14	I2C1.SCL	Exp. conn. I2C1	-	Pin 2 of CN10 Pin 29 of CN9 option
PG15	SPI3_CS_LPTIM1_CH1	Exp. conn. SPI3	TIMER	Pin 16 of CN10
PH0–OSC_IN	PH0-OSC_IN	16 MHz HSE oscillator	-	-
PH1–OSC_OUT	PH1-OSC_OUT	16 MHz HSE oscillator	-	-
PH2	AUDIO_RSTn	Audio codec	-	-
PH3–BOOT0	PH3-BOOT0	BOOT0 switch	-	-
PH4	I2C5.SDA	I2C5 for DSI_V3 connector	-	-
PH5	I2C5.SCL	I2C5 for DSI_V3 connector	-	-
PH6	eMMC_RSTn	eMMC	-	-
PH7	I2C3.SCL	Temperature/ToF sensors	-	-
PH8	I2C3.SDA	Temperature/ToF sensors	-	-
PH9	HEXASPI1.NCS	Hexadeca-SPI	-	-
PH10	HEXASPI1.IO0	Hexadeca-SPI	-	-
PH11	HEXASPI1.IO1	Hexadeca-SPI	-	-
PH12	HEXASPI1.IO2	Hexadeca-SPI	-	-
PH13	HEXASPI1.IO3	Hexadeca-SPI	-	-
PH14	HEXASPI1.IO4	Hexadeca-SPI	-	-
PH15	HEXASPI1.IO5	Hexadeca-SPI	-	-
PI0	HEXASPI1.IO6	Hexadeca-SPI	-	-
PI1	HEXASPI1.IO7	Hexadeca-SPI	-	-
PI2	HEXASPI1.DQS0	Hexadeca-SPI	-	-
PI3	HEXASPI1.CLK	Hexadeca-SPI	-	-
PI4	PI4 (free)	-	-	Not accessible
PI5	DSI_PWR_ON	DSI_V3 connector	-	-
PI6	DSI_BL_CTRL	DSI_V3 connector	-	-
PI7	DSI_SWIRE	DSI_V3 connector	-	-
PI8	HEXASPI1.DQS1	Hexadeca-SPI	-	-
PI9	HEXASPI1.IO8	Hexadeca-SPI	-	-
PI10	HEXASPI1.IO9	Hexadeca-SPI	-	-
PI11	HEXASPI1.IO10	Hexadeca-SPI	-	-
PI12	HEXASPI1.IO11	Hexadeca-SPI	-	-
PI13	HEXASPI1.IO12	Hexadeca-SPI	-	-

STM32U5x9NJ pin name	Signal assignment	Main function (default)	Secondary function	Pin number of expansion connector or test point reference
PI14	HEXASPI1.IO13	Hexadeca-SPI	-	-
PI15	HEXASPI1.IO14	Hexadeca-SPI	-	-
PJ0	HEXASPI1.IO15	Hexadeca-SPI	-	-
PJ1	PJ1 (free)	-	-	TP8
PJ2	PJ2 (free)	-	-	TP18
PJ3	PJ3 (free)	-	-	TP11
PJ4	PJ4 (free)	-	-	TP17
PJ5	PJ5 (free)	-	-	TP9
PJ6	PJ6 (free)	-	-	TP10
PJ7	PJ7 (free)	-	-	TP16
PJ8	PJ8 (free)	-	-	TP12
PJ9	PJ9 (free)	-	-	TP7
PJ10	PJ10 (free)	-	-	TP15
PJ11	PJ11 (free)	-	-	TP14
NRST	NRST	MCU General reset/ Reset button	Reset to/from devices	Pin 5 of CN9
OPAMP1_VINM	OPAMP1_VINM	-	-	TP20
OPAMP2_VINM	OPAMP2_VINM	-	-	TP19
DSI_D0P	DSI.D0_P	DSI_V3 connector	-	-
DSI_D0N	DSI.D0_N	DSI_V3 connector	-	-
DSI_D1P	DSI.D1_P	DSI_V3 connector	-	-
DSI_D1N	DSI.D1_N	DSI_V3 connector	-	-
DSI_CKP	DSI.CK**_N (inverted)**	DSI_V3 connector	-	-
DSI_CKN	DSI.CK**_P (inverted)**	DSI_V3 connector	-	-
VDD	VDD_MCU	Power	-	-
VDDIO2	VDD_MCU	Power	-	-
VDDA	VDDA	Power	-	-
VSSA	AGND	AGND	-	-
VREFP	VREFP	Power	-	-
VREFM	AGND	AGND	-	-
VDDUSB	VDD_USB	Power	-	-
VDD11USB	V11	Power	-	-
VDDDSI	VDD_DSI	Power	-	-
VDD11DSI	V11	Power	-	-
VSSDSI	GND	DSI GND	-	-
VDDSMPS	VDD_SMPS	Power	-	-
VLXSMPS	VLX_SMPS	Power	-	-
VSSSMPS	GND_SMPS	SMPS GND	-	-
VSS	GND	GND	-	-
VBAT	VBAT	Power	-	-

12 STM32U5x9J-DKx product information

12.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

- First sticker: product order code and product identification, generally placed on the main board featuring the target device.
  Example:

  Product order code
  Product identification

- Second sticker: board reference with revision and serial number, available on each PCB.
  Example:

  MBxxxx-Variant-yzz
  syywwxxxxx

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: *"MBxxxx-Variant-yzz"*, where *"MBxxxx"* is the board reference, *"Variant"* (optional) identifies the mounting variant when several exist, *"y"* is the PCB revision, and *"zz"* is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as *"ES"* or *"E"* are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"ES" or *"E"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

12.2 STM32U5x9J-DKx product history

Table 34. Product history

Order code	Product identification	Product details	Product change description	Product limitations
STM32U5A9J-DK	DK32U5A9J$AT1	MCU: • STM32U5A9NJH6Q silicon revision "C"	Initial revision	The STM32U5A9NJH6Q silicon revision "C" does not support the SFI. It is embedded by default in STM32U5A9J-DK with the DK32U5A9J$AT1 product identification.
		MCU errata sheet: • *STM32U59xxx and STM32U5Axxx device errata* (ES0553)		
		Boards: • MB1829-U5A9NJQ-B01 (Main board) • MB1835-VDD1V8-B01 (LCD daughterboard)		
	DK32U5A9J$AT2	MCU: • STM32U5A9NJH6Q silicon revision "X"	New revision embedding STM32U5A9NJH6Q silicon revision "X"	No limitation
		MCU errata sheet: • *STM32U59xxx and STM32U5Axxx device errata* (ES0553)		
		Boards: • MB1829-U5A9NJQ-B01 (Main board) • MB1835-VDD1V8-B01 (LCD daughterboard)		
STM32U5G9J-DK1	DK32U5G9J1$AT1	MCU: • STM32U5G9NJH6Q silicon revision "Z"	Initial revision	No limitation
		MCU errata sheet: • *STM32U5Fxxx and STM32U5Gxxx device errata* (ES0595)		
		Boards: • MB1829-U5G9NJQ-B02 (Main board) • MB1835-VDD1V8-B01 (LCD daughterboard)		

12.3 Board revision history

Table 35. **Board revision history**

Board reference	Board variant and revision	Board change description	Board limitations
MB1829 (Main board)	U5A9NJQ-B01	Initial revision with STM32U5A9NJH6Q microcontroller	-
	U5G9NJQ-B02	Initial revision with STM32U5G9NJH6Q microcontroller	-
MB1835 (LCD daughterboard)	VDD1V8-B01	Initial revision	The C2 and C3 silkscreen are inverted by the PCB manufacturer (error present in original MB1835B Gerber files corrected by PCB manufacturer).

13 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

13.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

To satisfy FCC RF exposure requirements, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at a closer distance than this is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Responsible party (in the USA)

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13.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (B) / NMB-3 (B).

Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES-3 (B) / NMB-3 (B).

Revision history

Table 36. **Document revision history**

Date	Revision	Changes
14-Feb-2023	1	Initial release.
13-Mar-2023	2	Cleaned official version with updated *Figure 4* to *Figure 10* and new *Figure 25*.
12-Jun-2023	3	New *Figure 7*, *Figure 8*, and DK32U5A9J$AT2 product identification in *Table 35*.
12-Jan-2024	4	Integrated the *STM32U5G9J-DK1* Discovery kit in product references throughout the document. Added *Demonstration software*. Updated: • *Introduction*, *Ordering information*, *Codification*, *Connectors*, *20-pin audio MEMS connector (CN1)*, *STM32U5x9J-DKx product history*, and *Board revision history* sections • *Figure 4*, *Figure 5*, *Figure 6*, and *Figure 17*
04-Apr-2024	5	Alignment on Discovery kit document corporate standards. Section 7.4: Embedded STLINK-V3E updated and merged with other debug/programming function descriptions.

Contents

List of tables

List of figures