Teseo-LIV4F and Teseo-LIV4FM hardware documentation

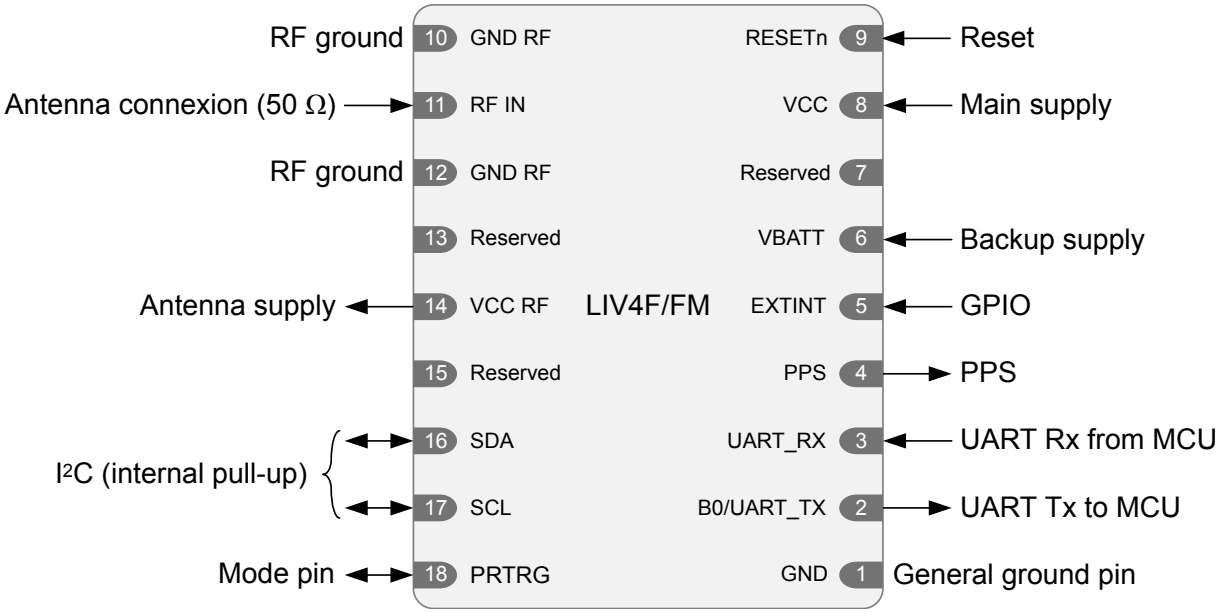
Introduction

The Teseo-LIV4F and Teseo-LIV4FM modules are an easy-to-use Global Navigation Satellite System (GNSS) standalone low power module, embedding Teseo IV single die GNSS receiver IC working simultaneously on multiple constellations (GPS/Galileo/Glonass/BeiDou/QZSS) able to provide positioning (Teseo-LIV4F) or raw measurement data (Teseo-LIV4FM).

1 Pin out

In the following figure, the pin out of the module:

Figure 1. Pin out



2 Power

Teseo-LIV4F/FM is supplied by two power pins:

- **VCC (pin 8)**
  VCC is the main supply: its range can be from 1.8 V to 3.3 V.
  At startup or during low power application, current can change suddenly. It is important to use power device able to provide this current variation. Use LDO above 200 mA current.
- **VBAT (pin 6)**
  VBAT is the supply for the low power domain backup: RAM and RTC. Its range can be from 1.8 V to 3.3 V.
  It can be either connected to VCC or it can be supplied by a dedicated supply always ON. VBAT supply can be kept ON during low power mode to allow fast recovery of GNSS fix.
  If no backup supply is available, leave VBAT pin floating.

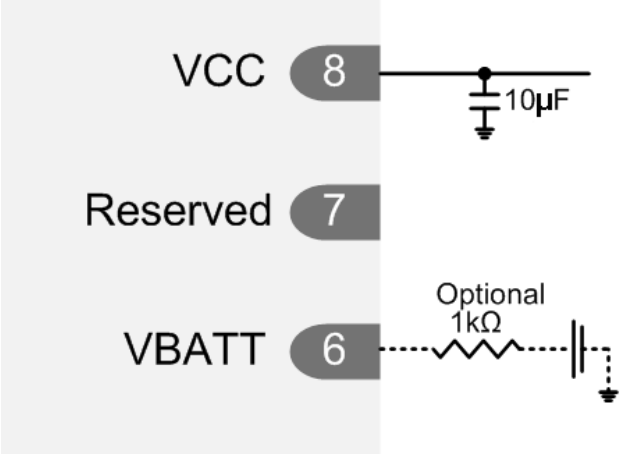
2.1 VCC_RF (pin 14)

VCC_RF is an output supply for external active antenna. The current is limited below 35 mA.

2.2 Power supply design reference

For first PCB, it is recommended to plan to have some filtering components on Teseo-LIV4F/FM power supplies as follows:

Figure 2. Power supply filtering

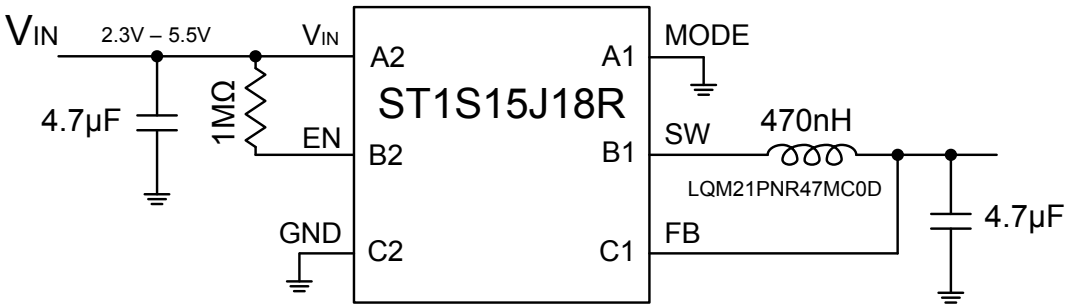


Note: Decoupling capacitor must be placed close to module pin.

2.3 Current consumption optimization

To optimize battery current consumption, it is possible to use a SMPS at 1.8 V to supply VCC.
Here is an application example with ST1S15J18R with an efficiency around 85%.

Figure 3. Example of SMPS to improve current consumption



3 Reserved (pin 7, pin 13 and pin 15)

In Teseo-LIV4F/FM, the pin 7, pin 13 and pin 15 are reserved. Let the pin floating.

4 Interfaces

4.1 I²C (pin 16, pin 17)

I²C is in slave only.

Internal 4.7 kΩ pull-up resistor on VCC is present. It is important to avoid having other pull-up for current leakage in low power mode.

4.2 UART (pin 2, pin 3)

UART is Universal Asynchronous Receiver/Transmitter that supports much of the functionality of the industry-standard 16C650 UART.

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels.
- The internal register map address space, and the bit function of each register differ.
- The deltas of the modem status signals are not available.
- 1.5 stop bit is not supported.
- Independent receive clock feature is not supported.

5 I/O pins

5.1 PPS (pin 4)

PPS is the time pulse every one second. It can be configured with different condition of pulses.

For firsts PCB, it is recommended to plan to have some filtering components on Teseo-LIV4F/FM PPS (pin 4).

5.2 EXTINT (pin 5)

It is a GPIO which, by default, is a trigger pin to external interrupt.

Leave it floating if not used.

5.3 RESETn (pin 9)

It can force a Teseo-LIV4F/FM under reset.

Reset signal is active low.

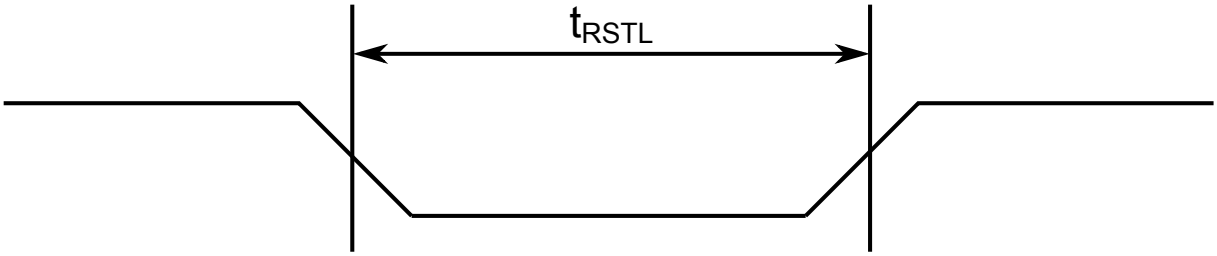
Host processor must have full control of this pin to guarantee the Teseo-LIV4F/FM's firmware upgrade support. Do not use pull-up or pull-down when connecting to MCU.

5.3.1 Reset minimum timing

Table 1. Reset minimum timing

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max	Unit
Reset input time	t_{RSTL}	RESETn	There is power supply and the oscillator is stable	100	-	-	mS

Figure 4. Reset (RESETn pin) minimum timing



5.4 RF_IN (pin 10)

It is the RF input.

DC (equals to VCC voltage) is present Teseo-LIV4F/FM version.

5.5 PRTRG (pin 18)

Keep PRTRG pin floating during system power-up or the external reset (RESETn from low to high), and the module will enter User Normal Mode.

It's a programming pin used to program the module in production line.

Leave PRTRG pin floating.

6 Standby mode

Standby mode is the mode where only low power backup domain is running and VCC is OFF. It means VBAT must be always maintained. It allows to have very low current consumption and fast GNSS reacquisition at the end of the standby time due to RTC.

Teseo-LIV4F/FM offers 1 way of standby: HW standby.

As IO buffers are not supplied during standby mode, it is important to keep all IO without external voltage to avoid any current leakage.

7 Front ends management

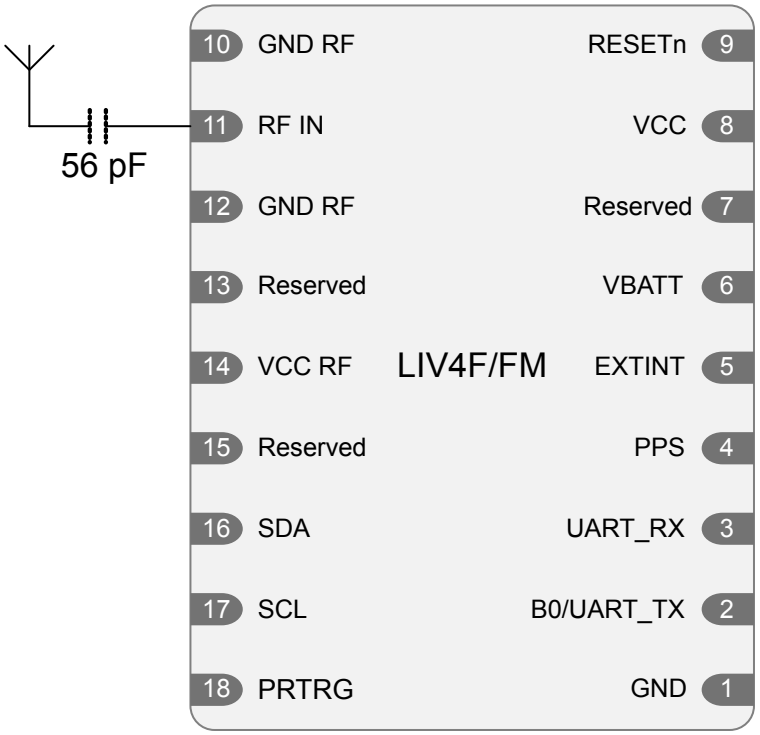
RF input impedance is 50 Ω.

7.1 Passive antenna

A passive antenna can be directly connected to Teseo-LIV4F/FM. Take care that the antenna must be close to the module. In addition, it could be possible that a matching component must be necessary to match the antenna.

As RF_IN provides supply for antenna, a DC cut capacitor could be necessary in case antenna presents a DC GND short cut.

Figure 5. Passive antenna



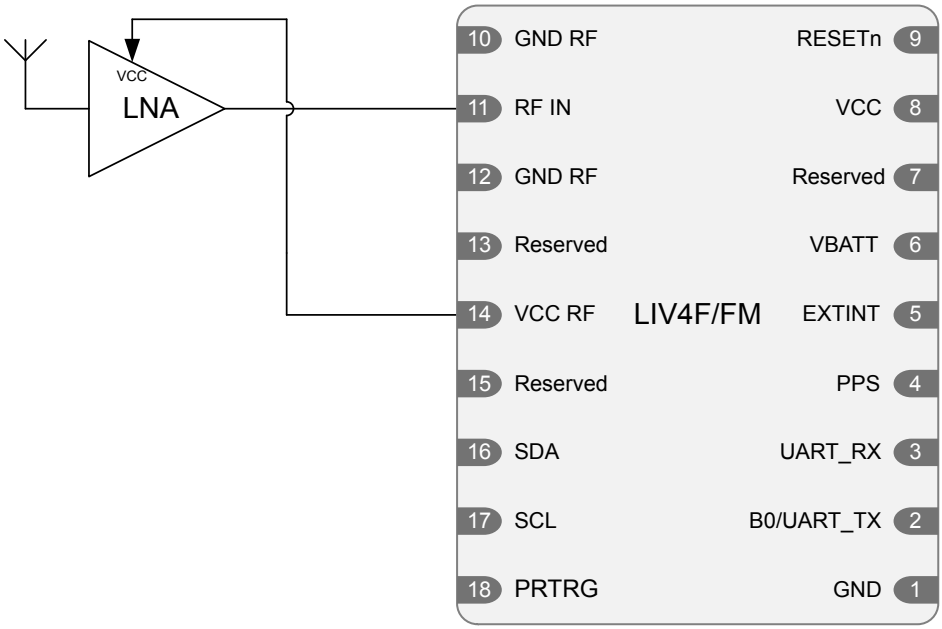
7.2 External LNA

External LNA means a passive antenna used with an LNA on the same PCB as Teseo-LIV4F/FM module.

There are built-in LNA and SAW in the GNSS module. It is recommended to use an LNA with gain less than 36 dB and noise figure less than 1.5 dB.

Here is a bloc diagram describing the connection:

Figure 6. External LNA control

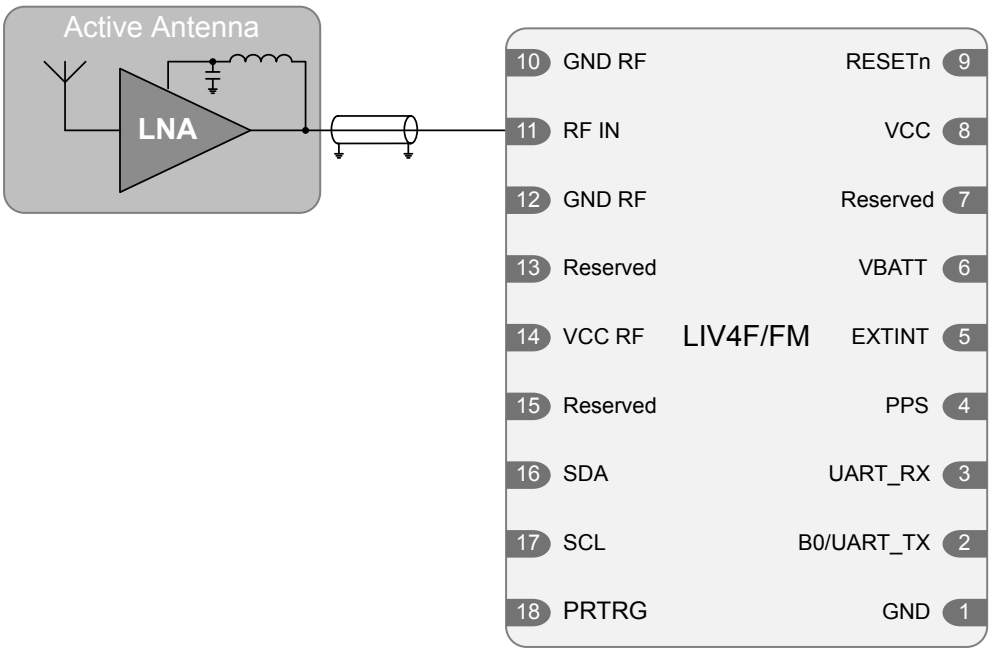


7.3 Active antenna

There are built-in LNA and SAW in the GNSS module. It is recommended to use an active antenna with gain less than 36 dB and noise figure less than 1.5 dB.

The active antenna can be supplied directly via RF_IN supply.

Figure 7. External antenna control



8 Layout recommendations

It is important to have a whole ground plane below Teseo-LIV4F/FM module. Avoid any signals below Teseo-LIV4F/FM.

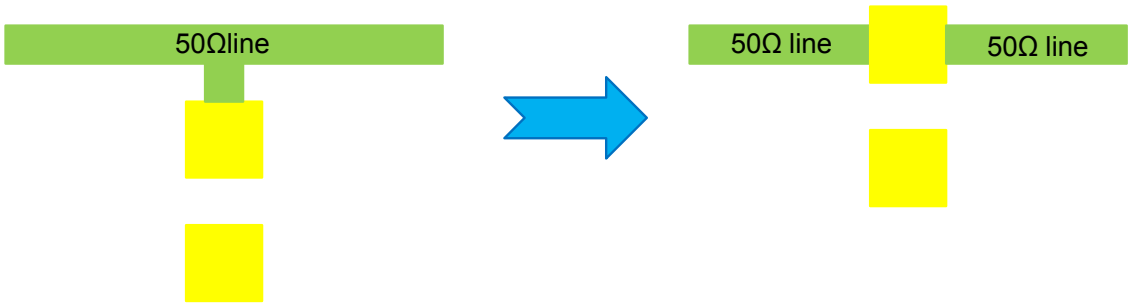
Do not place the module close to any EMI source, like antenna, RF routing, DC/DC or power conductor, clock signal or other high-frequency switching signal, etc.

For RF passive components, ST recommends using the 0402 (1 x 0.5 mm) components. Please choose the RF ground layer to be able to get 50 Ω RF line width as close as possible to components pads.

On 50 Ω RF line it is important to avoid all possible stubs:

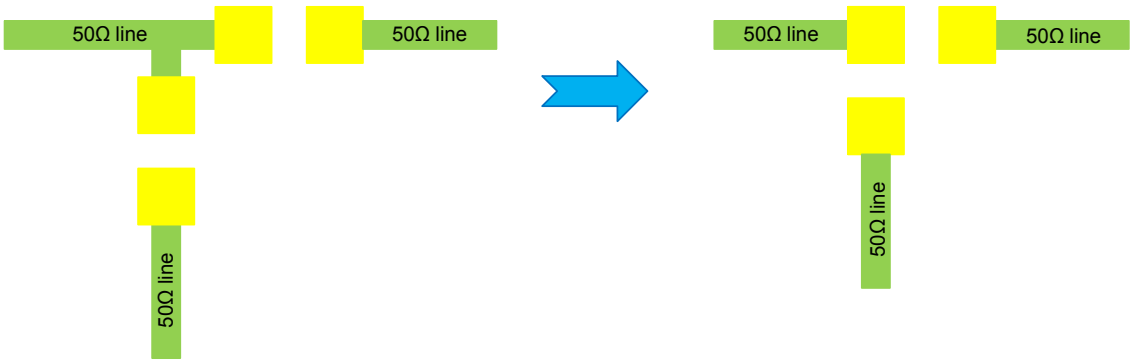
- For parallel components place one pad on the RF line.

Figure 8. Parallel component pads position



- If a bypass is needed, superimpose the two pads in one.

Figure 9. Bypass components pads position



Revision history

Table 2. **Document revision history**

Date	Version	Changes
22-Mar-2022	1	Initial release.
22-Nov-2022	2	Add *Section 5.3.1 Reset minimum timing*.
29-Nov-2023	3	Updated Section Introduction.

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