UM3064

User manual

ST-ONE parameter description

Introduction

This user manual provides information about the parameters for the ST-ONE device and the setup procedures for the most important ones.

The ST-ONE is the world's first digital controller embedding Arm® Cortex® M0+ core, an offline programmable controller with synchronous rectification, and USB PD PHY in a single package. Such a system is specifically designed to control ZVS non-complementary active clamp flyback converters to create high power density chargers and adapters with a USB Power Delivery interface.

The device includes a configuration memory that allows the user to configure the ST-ONE tailoring it for the required application.

This user manual goes through all the parameters in detail and explains how to set them in a real application. For any further information about the ST-ONE product, please refer to the ST-ONE datasheet (see www.st.com).

1 Prerequisites

In order to easily program the ST-ONE during the development of a new application, a graphical user interface (GUI) has been developed. The GUI works strictly with a communication interface board and allows real-time monitoring of the device, calculates the key hardware elements of the application and programming of the ST-ONE. For more information about the GUI and the interface board, please refer to the DB4310 - USB to I^2C/UART interface board for STNRG digital power controller products (STNRG01x and ST-ONE).

The default firmware loaded by factory does not provide the debug option, so it is possible to modify the parameter but not execute the live fine-tune of the application. In order to do this, please refer to st.com to download the debug firmware and related user guide.

2 Digital parameters configuration

This section describes the procedures to set up the most important IC parameters according to the board specifications and components.

By setting the parameters, the user can define the type of communication protocol (for example, USB PD) and the relative options, the thresholds and behavior of IC protections such as the overtemperature, and the switching control loop parameters.

By default, CC1 and CC2 act as serial communication for programming firmware and parameters. CC1 must be connected to Rx, and CC2 must be connected to Tx.

It is possible to program parameters using CC lines especially for production lines, which is the fastest option.

The parameters are divided into 4 different groups:

- Application set-up parameters
- Application code parameters
- USB PD related parameters
- Power parameters

ATTENTION: if you set USB PD protocol you cannot use CC lines for debug purposes or for changing parameters, so you must relocate the serial line on GPIOs the first time of programming.

2.1 Application setup parameters

On this area the user defines if USART interface is active and on which pin. Moreover, on this area it is possible to enable the application code write to protect.

Note: If the application code is protected but UART is active, it is possible to erase the entire area and reload a different setup or application entering in boot mode.

In the next section all the digital parameters of this portion of area are described.

2.1.1 BCMode

Select the boot code activity and, depending on the selection, enable the application code running or not.

Available values are:

- 0x01 = BMC1 = Jump to application if present (no debug)
- 0x02 = BMC2 = No jump to application area. BMC2 is also called “Programming Mode”
- 0x03 = BMC3 = Equal to BMC1 but add the possibility to use the external command (available only with debug firmware)

By default, the BCMode parameter is set to BCM02 so the IC is not allowed to start up. For starting the system up please put this parameter in BMC01, otherwise put this parameter in BMC03 to live fine tune the parameters (debug code download needed).

2.1.2 USART_enable

This field selects which USART interface is selected.

Available values are:

- bit0 = UART enable [Disabled (0) / (1) Enabled]
- bit1 = UART Rx disabling [Enabled (0) / (1) Disabled]
- bit4 = UART mapping [GPIO0-GPIO1 (0) / (1) CC1-CC2]
- bit7 = UART recovery mode disabling [Enabled (0) / (1) Disabled]

Note: If bit0=0, that is, UART disabled, the other bits are not taken into account.

Note: If UART Rx is disabled (bit1=1) the device could send messages while reception of UART (command) messages is disabled. It could be enabled for security reasons in case UART cannot be disabled.

2.1.3 Internal PULL-UP on GPIOX

Internal PULL-UP on GPIO0 and GPIO1 pads configuration.

Available values are:

- bit0 = internal PULL-UP on GPIO0 pad enable [Disabled (1) / (0) Enabled]
- bit1 = internal PULL-UP on GPIO1 pad enable [Disabled (1) / (0) Enabled]

2.1.4 ACP_protection

Application Code Protection area defines which page (2 Kbytes size) is hardware protected, that is, write/erase page commands are rejected:

- If 0, no pages are protected.
- When n > 0, protection is applied on pages from 0 to (n-1) and page 31, where n=1÷31. For example:
  - If 1, protection is applied on page 0 and page 31 (that is, data @0x00010000÷@0x000107FF and data @0x0001F8000÷@0x0001FFFF).
  - If 2, protection is applied on pages from 0 to 1 and page 31.
- If 31 the entire Main Flash is protected (that is, code @0x00010000@0x0001FFFF).

Note: Performing the Main Flash area Mass Erase, the protection is removed, and write/erase page commands are executed.

Note: Please consider in case the device is in boot mode the protections are disabled. To completely protect the device, please follow these steps:
- *Set the ACP_protection value to 31*
- *Once you program the device:*
  - *Remove the UART*
  - *Do not allow the boot entering*
    - *(recovery mode bit set to disable)*

2.1.5 APPL_SETUP

This field defines if, and which, protocol is used to communicate with the SINK.

Available values are:
- 0x00 = No stacks enabled – fixed 5 V 1.5A
- 0x04 = USB PD stack enabled
- 0x0F = Fixed output, voltage from Vout default and Iout default – no stack enabled
- 0x1F = Fixed output CC, same as 0x0F with Constant Current enabled

2.1.6 PWD_SETUP

This field defines if the power module (FW to control the power application) starts or not.

Available values are:
- 0x00 = Power module disable, never starts
- 0x01 = Power module starts immediately after power-on
- 0x02 = Power module starts only when requested by SVC command (function enabled only with debug firmware)

2.1.7 Vout default

Sets the V_{out} voltage when APPL_SETUP is set to “Fixed” (0x0F) or “Fixed CC” (0x1F). This field is expressed as 1 mV / LSB; accepted values are from 5000 (as for 5 V) to 21000 (as for 21 V). In USB PD mode, must be set to 5000.

2.1.8 Iout default

Sets the I_{out} current limit when APPL_SETUP is set to “Fixed” (0x0F) or “Fixed CC” (0x1F). This field is expressed as 1 mA / LSB; accepted values are from 1000 (1 A) to 5200 (as 5.2 A). In USB PD mode must be set to 3000.

2.1.9 APP_Ext

Defines if, and which, GPIO pin is used for the external thermistor.

Available values are:
- 0 = External thermistor not used
- 1 = Used GPIO0
- 2 = Used GPIO1

The external thermistor trigger point value is specified on ACP_WTP_EXT and ACP_OTP_EXT field specified below.

2.1.10 APP_MV_Add2_Init

Selects the SRGD clamp functionality match with the external circuit. Bit field definition:
- Bit 0 – synchronous rectifier enable (=1) or disable (=0)
- Bit [2-1]
  - If 00 = Charge Pump clamp voltage at 11 V
  - If 01 = Charge Pump clamp voltage at 9 V
  - If 10 = Charge Pump clamp voltage at 7 V
  - If 11 = Charge Pump clamp voltage at 5 V

- Bit [3] – unused – reserved
- Bit [4-5] – select ZCD filter
  - If 00 = No filter enabled
  - If 01 = 50 ns
  - If 10 = 100 ns
  - If 11 = 150 ns
- Bit [6] – unused – reserved
- Bit [7] – charge pump functionality enable (=1) or disable (=0)

2.2 Application code parameters

This area defines the power limit during a WTP or OTP event and related temperature limits.

2.2.1 ACP_PWWTP_1

Defines the maximum output power (10 mW/step) when internal temperature is over WTP point as per ACP_WTP_INT (example: 0x1388 → 50 W).

2.2.2 ACP_CLWTP_1

Defines the maximum output current (1 mA/step) when internal temperature is over WTP point as per ACP_WTP_INT (example: 0x6A4 → 1700 mA).

2.2.3 ACP_PWWTP_2

Defines the maximum output power (10 mW/step) when external temperature is over WTP point as per ACP_WTP_EXT (0x1388 → 50 W).

2.2.4 ACP_CLWTP_2

Defines the maximum output power (1 mA/step) when external temperature is over WTP point as per ACP_WTP_EXT (0x6A4 → 1700 mA).

2.2.5 ACP_WTP_INT

Defines the internal warning temperature trigger point, the higher this value (degree), the output is limited to ACP_PWWTP_1 power and ACP_CLWTP_1 current (0x46 → 70 °C).

2.2.6 ACP_OTP_INT

Defines the internal overtemperature trigger point, the higher this value (degree), the output power is switched off if remaining for one minute over (0x64 → 100 °C).

2.2.7 ACP_WTP_EXT

Defines the external warning temperature trigger point, the higher or lower (depending on the slope) this value (1 mV/step), the output is limited to ACP_PWWTP_2 power and ACP_CLWTP_2 current.

2.2.8 ACP_OTP_EXT

Defines the external overtemperature trigger point, the higher or lower (depending on the slope) this value (1mV/step), the output power is switched off.

2.2.9 ACP_TOP_HYST

Defines the external temperature hysteresis (1 mV/step) and bit-field slope.

- [0-14] define the hysteresis
- [15] define the external temperature 0 °C level (the slope).
  - Bit = 0 0 °C is low point, bit = 1 0 °C is high level

2.3 USB PD PDOs and APDOs

This area defines the USB PD parameters as the PDO and APDO data; the maximum power provided by ST-ONE applications and other values related to this communication protocol.

2.3.1 5 V-PDO

This field defines the first PDO used on the USB PD protocol. The suggested default PDO is 5 V@3 A and is equal to 0x0801912C hex value. NOTE: This filed is mandatory as 5 V.

2.3.2 UCPDOx (1 to 6)

This field defines the PDO or APDO used on the USB PD protocol. This structure is a one-to-one map of the structures described in USB PD 3.1 protocol specifications. For more details please see the official USB PD specifications.

This field can be used for either PDO or APDO.

In the case of PDO, the available values are:

- Dual-role power: set to disabled, enable not supported
- USB suspend supported: set to disable, enable not supported
- Unconstrained power: set to disable, enable not supported
- USB communication capable: set to disable, enable not supported
- Dual role data: set to disable, enable not supported
- Unchuncked communication capable: disable, enable not supported
- Peak current: 100%, other values not supported
- Voltage: target voltage to regulate at this PDO, minimum value 5 V maximum value 21 V
- Max current: maximum current allowed for this PDO, minimum value 1 A maximum value 5 A

In the case of APDO, the available values are:

- PPS power limit: set to disable, enable not supported
- Max. voltage: maximum voltage allowed by this APDO, minimum value 5 V maximum value 21 V
- Min. voltage: minimum voltage allowed by this APDO, minimum value 3.3 V maximum value 20 V
- Max current: threshold current for entering in constant current mode, minimum value 1 A maximum value 5 A

2.3.3 PPS_HIGH

This field is the Programmable Power Supply - high limit or PDP used for some USB PD messages (100 mW/step).

2.3.4 VOLT_REG

This field is the Voltage Regulation field on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.5 HOLDUP_TIME

This field is the Holdup time field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.6 COMPLIANCE

This field is the Compliance parameter field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.7 TOUCH_CURRENT

This field is the Touch current field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.8 PEAK_CURR1

This field is the Peak current 1 field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.9 PEAK_CURR2

This field is the Peak current 2 field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.10 PEAK_CURR3

This field is the Peak current 3 field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.11 TOUCH_TEMPERATURE

This field is the Touch temperature field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.12 SOURCE_INPUTS

This field is the Source Input field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a deeper explanation.

2.3.13 USBPD_XID

This field is the XID value provided by the USB-IF assigned to the product. Please refer to USB PD 3.1 standard for a deeper explanation.

2.4 Power parameters legend

Note: *These parameters must be taken from the datasheet as table values in this section could be outdated. They are taken only the typical value for simplicity (for more details look at the ST-ONE datasheet). For more details on how to practically tune power parameters, follow 'How to design an application guide'.*

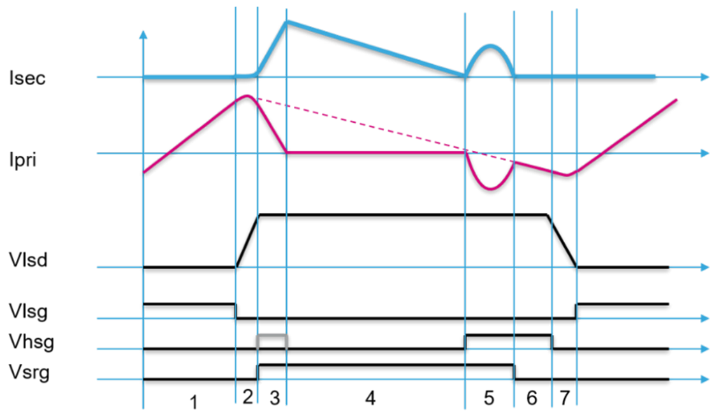
Table 1. Constant details

Name	Value	Meaning
G_{TV}	0.66 V/µs	Time to voltage conversion ratio, used for ipk computing
F_{clk}	133 MHz	High clock system frequency
$f_{clkslow}$	66 kHz	Low clock system frequency
$V_{IPEAKCLAMP}$	0.525 V	

Table 2. Variable details

Name	Meaning
R_{pri}	Current sense resistor at primary side
R_{sec}	Current sense resistor at secondary side
T_{OFF}	Secondary side conduction phase (see Figure 1, phase 4)
T_{ON}	Primary side conduction phase (see Figure 1, phase 1)
V_{ThOVP}	OVP overvoltage protection threshold, compared to V_{out}
V_{ThUVP}	UVP undervoltage protection threshold, compared to V_{out}
V_{drv}	SR driving voltage
V_{out}	Actual output voltage
V_{tgt}	Target voltage regulating, value after compensation, in typical cases equal to V_{tgtset}
T_{HS1}	Clamp conduction phase (see Figure 1, phase 3)
T_{HS2}	Clamp bump phase (see Figure 1, phase 5+6)
I_{Pk}	Peak current on primary side
V_{tgtset}	Target voltage, set by user or protocol, for example 5 V 9 V

Figure 1. Typical switching waveforms



2.5 Power parameters

The following parameters are used to set up and tune the power conversion control, including loop compensation, switching cycle timings, light load modes thresholds, etc.

Each parameter is given the conversion factor CF; the conversion is already implemented in the GUI. CF is useful for understanding the resolution of the parameter.

However, it is possible to compute the raw value of a parameter by computing:

$$Parameter[RAW] = Parameter[measure\ unit] \cdot CF$$

Where not specified CF is equal to 1.

2.5.1 Rsns_Iout

Sets the conversion factor between the secondary output current and internal IC representation. The value should be chosen according to the secondary side sense resistor. Make sure to also consider parasitic resistance, that is, PCB and soldering. See DAHU for choosing the right sense resistor.

$$CF[m\Omega] = 0.047$$

2.5.2 Vout_th_ChgPmp

Sets the turn-off threshold of the charge pump for generating V_{drv}.

V_{drv} must be enough for powering on SRGD MOSFET.

If V_{out} is greater than $V_{out\_th\_ChgPmp}$ – 0.3 charge pump is disabled. In this case:

$$V_{drv} = V_{out} - 2 \cdot V_{fdiode}$$

If V_{out} is less than $V_{out\_th\_ChgPmp}$ + 0.3 charge pump is enabled. In this case:

$$V_{drv} = 2 \cdot \left(V_{out} - V_{fdiode}\right)$$

Where V_{fdiode} is the forward voltage of the two diodes connected to the PUMP pin. Set a value of 2.5 V for always disabling it. Default value is 8.19 V suitable for most MOSFETs. For logic level MOSFET, this value can be decreased, that is, 5 V.

$$CF[V] = 0.000375$$

2.5.3 Ton_SR_ext

This parameter sets the maximum SR on duration after the IZCD comparator is triggered (see Figure 1, phase 5). The parameter are set as a half resonance period of the leakage inductance with the clamp capacitor.

$$CF[ns] = 7.52$$

2.5.4 Ton_HS2_max

This parameter sets the maximum HS on duration. It is particularly useful to limit the duration at very low output and high input voltage would lead to very long HS on pulses increasing the primary side conduction losses with limited gain in terms of switching losses.

A rule of thumb is to set this parameter in order to obtain soft switching up to 9 V output at 230 V_{AC} input voltage.

$$CF[ns] = 7.52$$

2.5.5 Ton_HS2_min

This parameter sets the minimum HS on duration.

The parameter is expressed as the number of clock cycles.

$$CF[ns] = 7.52$$

2.5.6 Ton_HS2_gain

This is the main parameter to set the HS on duration in order to obtain soft switching in almost all conditions.

The second HON duration is determined by the controller as:

$$T_{HS2} = \text{Ton\_HS2\_gain} \cdot \frac{T_{OFF}[s]}{T_{ON}[s]}$$

Ton is the LS on-time including LS-HS deadtime (see Figure 1, phases 1 and 2), Toff is the LS off-time (see Figure 1, phases 3 to 6). The HS-LS deadtime is excluded from the operation since it is of negligible impact.

Attention: *This value is saturated between $T_{on\_HS2\_min}$ and $T_{on\_HS2\_max}$.*

2.5.7 Ton_HS1_adjust

This parameter sets the first HON duration.

The first HON duration is defined as:

$$T_{HS1}[s] = \text{Ton\_HS1\_adjust} + \frac{1}{2}\begin{cases} T_{HS2}[s], & T_{HS2}[s] < Ton\_SR\_ext \\ Ton\_SR\_ext, & T_{HS2}[s] \geq Ton\_SR\_ext \end{cases}$$

The first HS on-time is determined as half of the duration of the SR pulse after the IZCD is triggered plus or minus a value determined by this parameter.

The setting of this parameter may be done by observing the current in the HS FET or the voltage on the transformer primary side. A long HS on pulse would cause a reversal of the primary side current during phase 3 of the switching (see Figure 1, phase 3), leading to a spike in the transformer voltage when the HS FET turns off.

$$CF[ns] = 7.52$$

2.5.8 Tdly_HS2-on_LS-off

Sets the deadtime between HS on and LS on.

The time is set long enough to obtain soft switching without keeping the LS body diode on for a long time (see Figure 1, phase 2).

$$CF[ns] = 7.52$$

2.5.9 Tvalley_V-SKIP

This parameter is set as the oscillation period of the LS drain voltage during valley skipping mode.

The parameter is expressed as the number of clock cycles.

$$CF[ns] = 7.52$$

2.5.10 Tdly_HS2-on_V-SKIP

Delay from the ZVS comparator rising and the valley of the signal, expressed in SMED cycles.

$$CF[ns] = 7.52$$

2.5.11 Tadv_I2-ZCD

This parameter sets the delay on ZCD0, between phase 4 and 5 (see Figure 1).

If no ZCD advance circuitry is set, this parameter must be set to 0.

$$CF[ns] = 7.52$$

2.5.12 Tsw_off_max

Maximum duration of phase secondary side conduction (see Figure 1, phase 3 + 4 + 5).

$$CF[ns] = 7.52$$

2.5.13 Tsw_ph21_V-SKIP_hyst

Hysteresis for changing skipping mode.

2.5.14 Vout_slope_ctrl

Rising time during soft-start and voltage transitions, falling time is 4 time slower.

Attention: *This parameter is a target and could not be respected at low load.*

$$CF[\mu s] = 0.0483$$

2.5.15 T_Autorestart_OCP

Time to re-attach the load switch after an Overcurrent Protection event.

$$CF[ms] = 1$$

2.5.16 T_Autorestart_BO

Time to re-attach the load switch after a Brownout event.

$$CF[ms] = 1$$

2.5.17 Itrip_max

This parameter sets the maximum value for the value computed by Internal PID limiting the maximum value for primary current peak during LON.

The maximum peak current is:

$$I_{PkMax}[A] = \frac{1}{R_{sense\_pri}[Ohm]} \cdot \frac{G_{TV}[V/s]}{2048 \cdot F_{CK}[Hz]} \mathrm{IpeakMax[RAW]} \approx \frac{2.44[\mu V]}{R_{sense\_pri}[Ohm]} \mathrm{IpeakMax[RAW]}$$

$$CF[\%\ of\ maximum\ Ipk] = 0.00043$$

2.5.18 PID_P_CV

Proportional gain factor during constant voltage mode.

2.5.19 PID_I_CV

Integral gain factor during constant voltage mode.

2.5.20 PID_I_CC

Integral gain factor during constant current mode.

2.5.21 Jitter_m_index

This parameter manages jitter for spread spectrum functionality.

Value is expressed as % of the I_{peak}.

$$CF[\%\ of\ Ipk] = 1.56\ each\ step$$

2.5.22 Iout_OCP_th

Threshold for triggering hard Overcurrent Protection expressed in mA.

$$CF[mA] = 0.001$$

2.5.23 Vout_OV/UV_th

Proportional factor for computing OVP and UVP threshold according to the formula:

$$V_{ThOVP}[V] = V_{tgt}[V] + Vout\_OV/UV\_th \cdot V_{tgt}[V] + Vout\_OV/UV\_msk[V]$$
$$V_{ThUVP}[V] = V_{tgt}[V] - Vout\_OV/UV\_th \cdot V_{tgt}[V] - \mathrm{Vout\_OV/UV\_msk}[V]$$

$$CF[\%\ of\ Vout] = 0.386$$

2.5.24 Vout_OV/UV_msk

Absolute value for computing OVP and UVP threshold according to the formula:

$$V_{ThOVP}[V] = V_{tgt}[V] + Vout\_OV/UV\_th \cdot V_{tgt}[V] + Vout\_OV/UV\_msk[V]$$
$$V_{ThUVP}[V] = V_{tgt}[V] - Vout\_OV/UV\_th \cdot V_{tgt}[V] - \mathrm{Vout\_OV/UV\_msk}[V]$$

Where V_{tgt} is the target voltage set by user or protocol and V_{out_OV/UV_th} is the previous parameter.

$$CF[mV] = 2.92$$

2.5.25 Itrip_clmp_V-SKIP

Minimum primary side peak current during valley skipping mode.

When the peak current reaches this value, the valley skipping controller starts to control the switching frequency instead of the peak current to regulate the output.

The value is expressed as % of maximum I_{peak} allowed.

$$CF[\% \; of \; Ipk] = 0.99$$

2.5.26 PFC OFF current threshold

Peak current threshold for which the PFC is turned off, GP1 pin set to 1. UART is disabled if this parameter is different from 0.

Set this parameter to 0 if PFC function is not used.

$$CF[\% \; of \; Ipk] = 0.99$$

2.5.27 PFC OFF current hysteresis

Peak current threshold hysteresis for which the PFC is turned on/off.

Set this parameter to 0 if PFC function not used.

$$CF[\% \; of \; Ipk] = 0.99$$

2.5.28 V_force_PFC_ON

Voltage threshold, above it the PFC.

Set this parameter to maximum value (0xFFFF) if PFC function not used.

$$CF[V] = 0.000375$$

2.5.29 PFC_Burst_ON_ticks

Number of sets of burst for which the PFC is kept on.

Set to 0 for always on (it needed also I_PFC_off_th, V_PFC_alwayson_th conditions are met).

2.5.30 PFC_Burst_ticks

Total sets of burst for which the on-off PFC cycle is restarted. Off-time can be computed as PFC_Burst_ticks - PFC_Burst_ON_ticks. PFC_Burst_ticks must be greater than PFC_Burst_ON_ticks.

Set to 0 if not used.

2.5.31 Trep_min_BRST

Time threshold for exiting burst. If time between two bursts is less than this threshold, the system exits burst.

Note: There is a filter on this time so it's not immediate.

$$CF[ms] = 0.015$$

2.5.32 Trep_min_BRST_PPS

Same as Trep_min_BRST but valid when there is USB PD enabled and an APDO is requested.

2.5.33 Trep_max_BRST

Time threshold for entering and exiting deep burst. If time between two bursts is more than this threshold, the system enters in deep burst mode, otherwise the system exits deep burst (it enters in normal burst mode).

Note: There is a filter on this time so it's not immediate.

$$CF[ms] = 0.015$$

2.5.34 Itrip_th_BRST

Minimum primary side peak current for entering burst mode. When the peak current reaches this value, the controller enters in burst mode.

The value is expressed as % of maximum I_{peak} allowed.

$$CF[\% \; of \; Ipk] = 0.99$$

2.5.35 Itrip_th_BRST_PPS

Same as Itrip_th_BRST but valid when there is USB PD enabled and an APDO is requested or in FixpowerCC.

2.5.36 PID_I_pre_BRST

When exiting burst, the value of integrator and by consequence I_{pk} is initialized according to the formula:

$$I_{pk} = PID\_I\_pre\_BRST * V_{out} * I_{out}$$

2.5.37 Burst_settings

2.5.37.1 Hysteresis

Hysteresis set point of the comparator for burst mode, valid only at 5 V,9 V,12 V,15 V and 20 V.

2.5.37.2 Threshold

Threshold for starting a new burst.

$$CF[\%\ of\ V_{out}] = 1$$

2.5.38 Itrip_clmp_BRST

Primary side peak current used during burst mode.

The value is expressed as % of maximum I_{pk} allowed.

$$CF[\%\ of\ Ipk] = 0.99$$

2.5.39 N-Tsw_gain_BRST

Gain factor used to calculate the number of pulses to be generated during each burst, depending on the output voltage.

The number of pulses is equal to:

$$n_{pulses} = \max\left[\text{N\_Tsw\_min\_BRST} + \left(\text{N\_Tsw\_gain\_BRST} \cdot \frac{V_{Tgt}[V] - 2.9V}{12V}\right), N\_Tsw\_max\_BRST\right]$$

2.5.40 N-Tsw_min_BRST

Minimum number of pulses in each burst.

2.5.41 N-Tsw_max_BRST

Maximum number of pulses in each burst.

2.5.42 Tdly_HS-off_LS-on_D-BRST

Additional deadtime during deep burst.

$$CF[ns] = 7.52$$

2.5.43 Toff_BLEEDER

Off-time during active bleeding operation.

$$CF[ns] = 7.52$$

2.5.44 Ton_BLEEDER

The gain for computing active bleeding on-time, according to formula:

$$T_{ONBLEED}[ns] = \text{Ton\_BLEEDER\_Gain} \cdot \frac{Vcc}{20V}$$

$$CF[ns] = 7.52$$

2.5.45 Tmsk_V2-ZCD

Mask time from LS turn-on to ZCD12 detection for first HS and SR turn-on. Can be used to anticipate.

$$CF[ns] = 7.52$$

2.5.46 V_CDC_max

Maximum voltage allowed for Cable Drop Compensation.

If the cable drop compensation (see R_Cable) overcomes the maximum V_0 allowed by application, it is possible to fix a maximum V_{tgt}. Above it, the Cable drop compensation is disabled.

$$CF[V] = 1$$

2.5.47 R_Cable

Resistance of the cable expressed in mΩ. Value used for computing the cable drop compensation. It changes the V_{tgt} according to the formula:

$$V_{tgt} = V_{tgtset} + I\_out \cdot \mathrm{R\_Cable}$$

In USB PD applications it is recommended to leave to 0 unless the cable is embedded.

$$CF[m\Omega] = 1$$

2.5.48 truncatehon

During skipping it truncates the second HON pulse, if this parameter is different from 0, otherwise it uses the value of Ton_SR_ext.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
14-Sep-2022	1	Initial release.

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