Evaluation board for L9679E airbag and battery cut-off IC

Introduction

The L9679E-EVB evaluation board allows the user to evaluate the L9679E device. The board provides the main input and output capabilities needed to properly drive the IC.

1 Hardware description

The L9679E-EVB evaluation board has been developed to allow to the user total access to the pins to simplify the probing of each signal.

Its main features are:

- L9679E placed into a socket allowing an easy change of the samples.
- Possibility to solder L9679E directly on the PCB.
- Total accessibility to all pins through test points
- L9679E board equipped with the IC external components and jumpers to fix the L9679E setup configuration.
- Motherboard equipped with microcontroller to drive in the most flexible way the L9679E signals.

Figure 1. L9679E-EVB evaluation board with socket

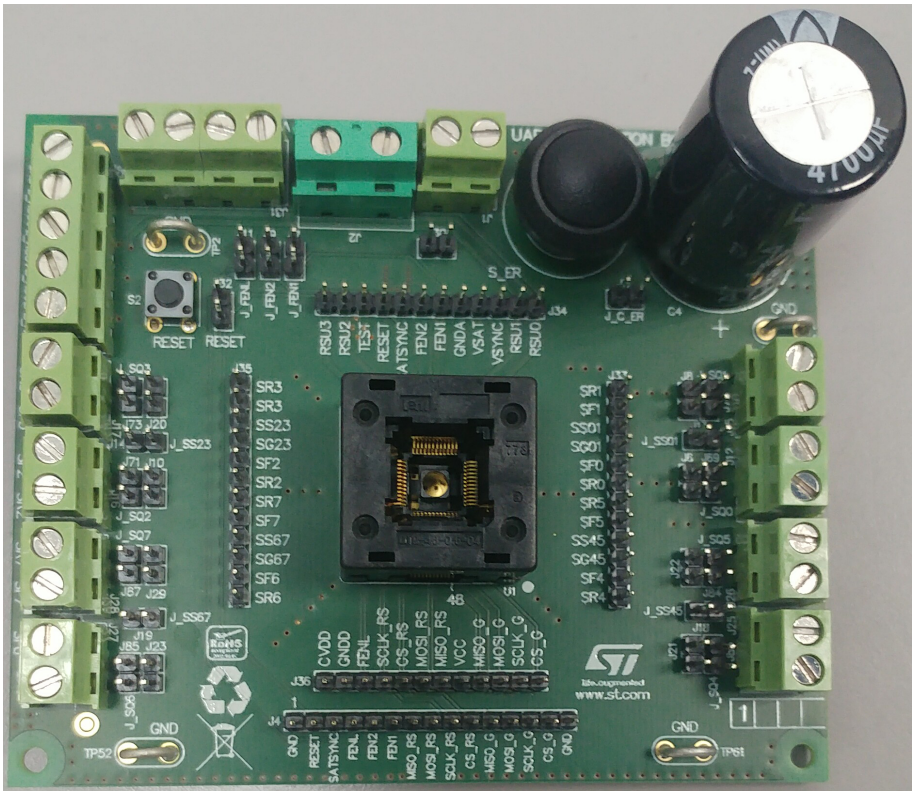
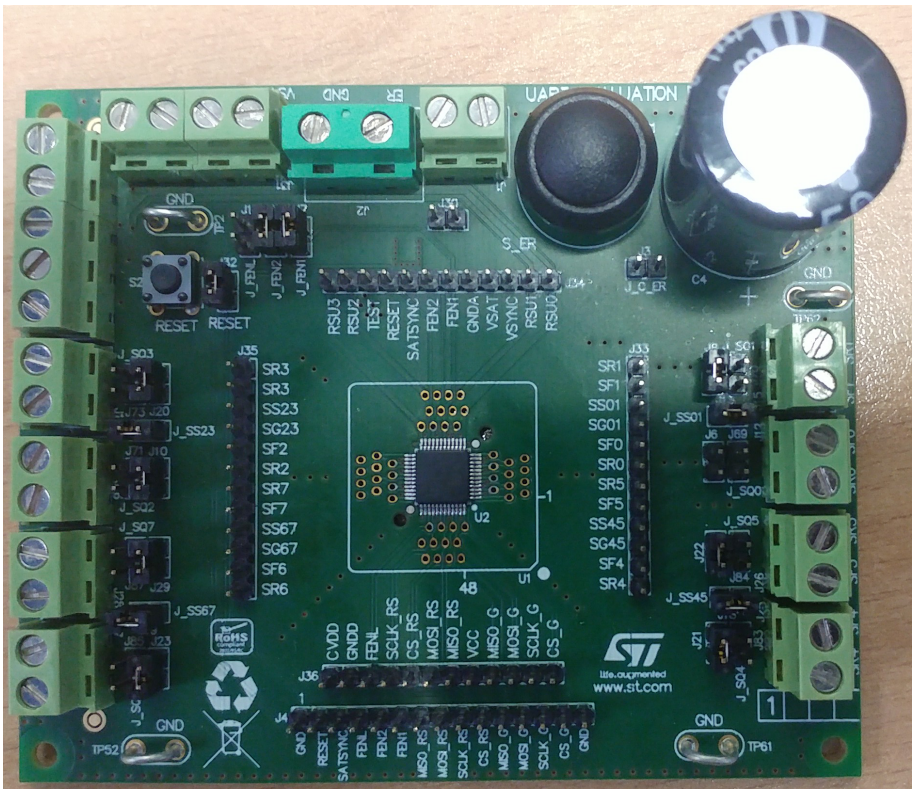


Figure 2. **L9679E-EVB evaluation board with soldered sample**



2 Board schematics

Figure 3. Board schematic - #1

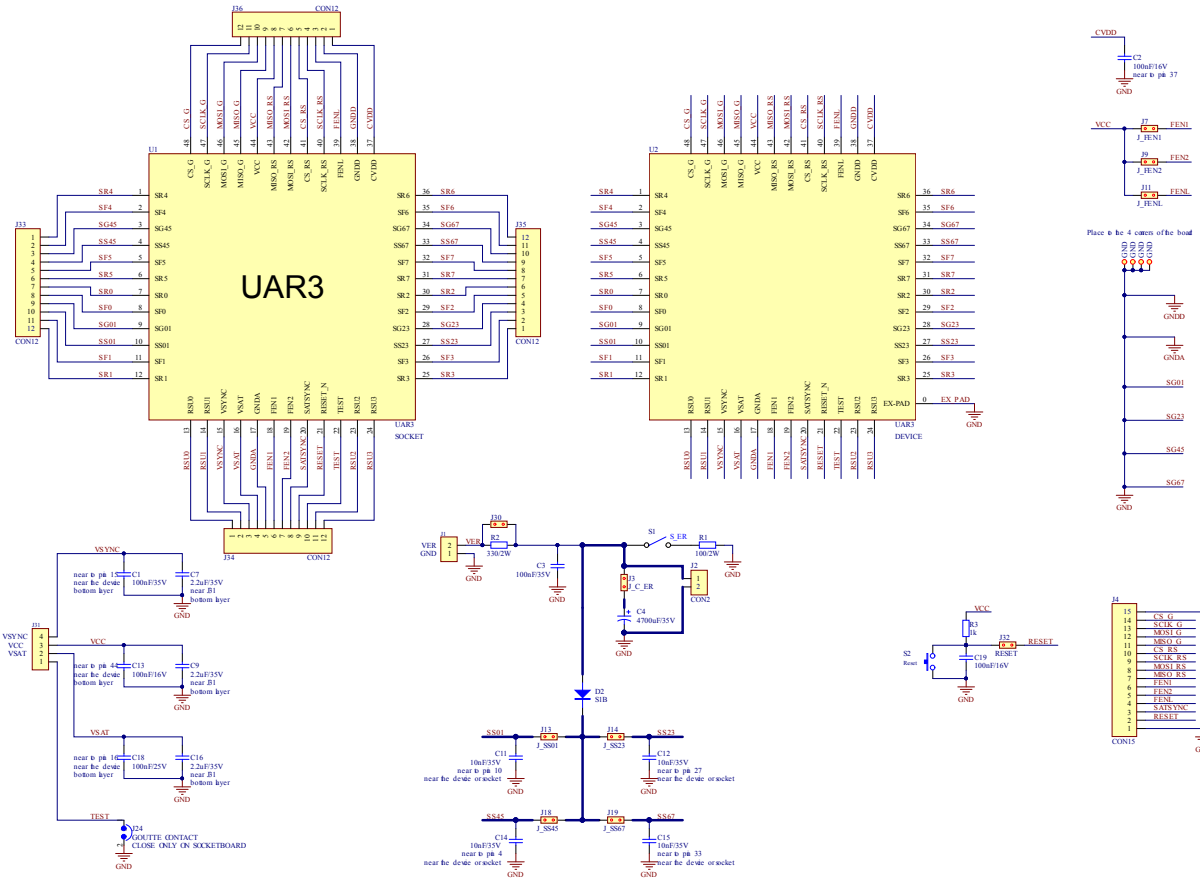
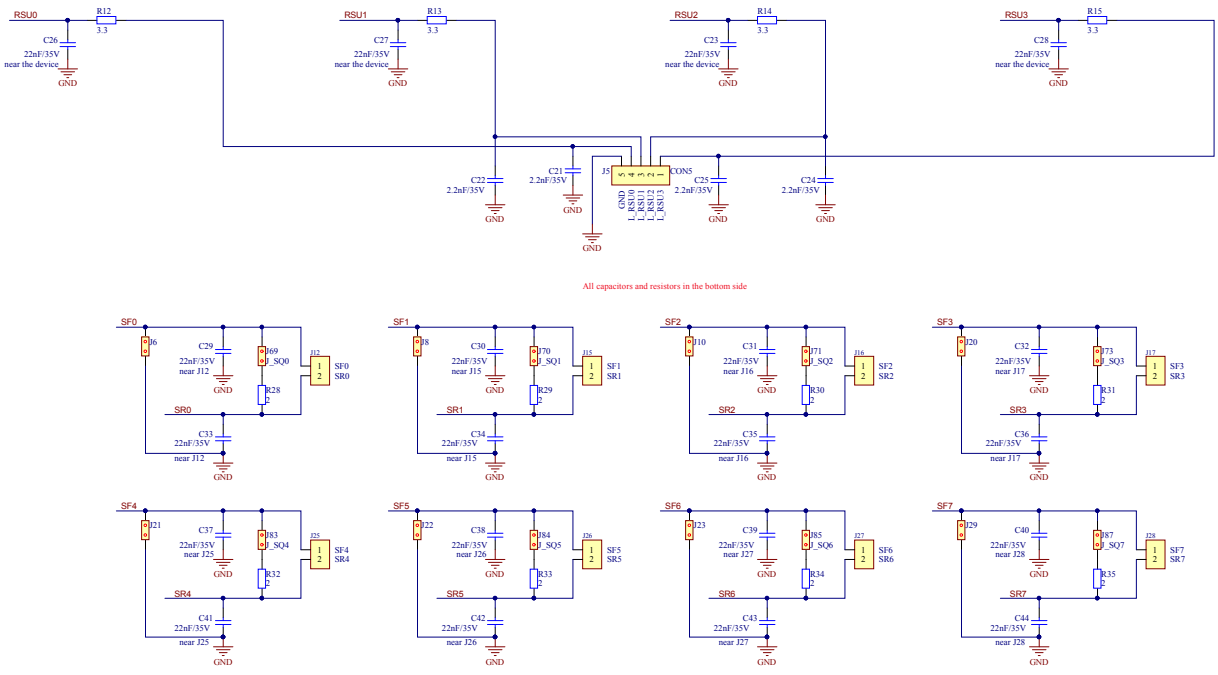
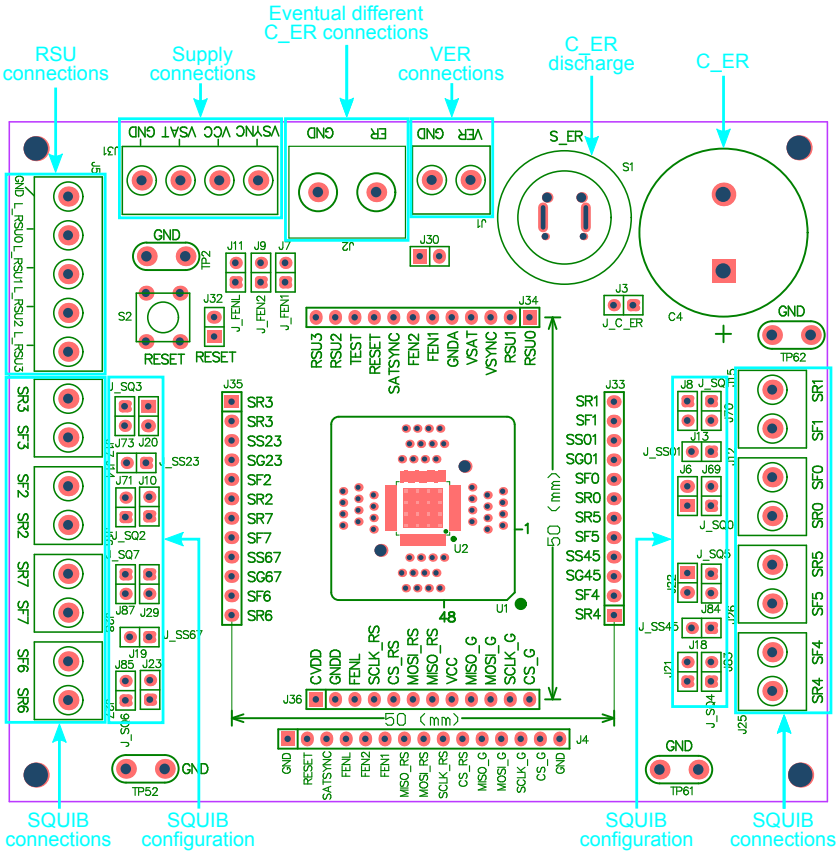


Figure 4. Board schematic - #2



3 Board layout

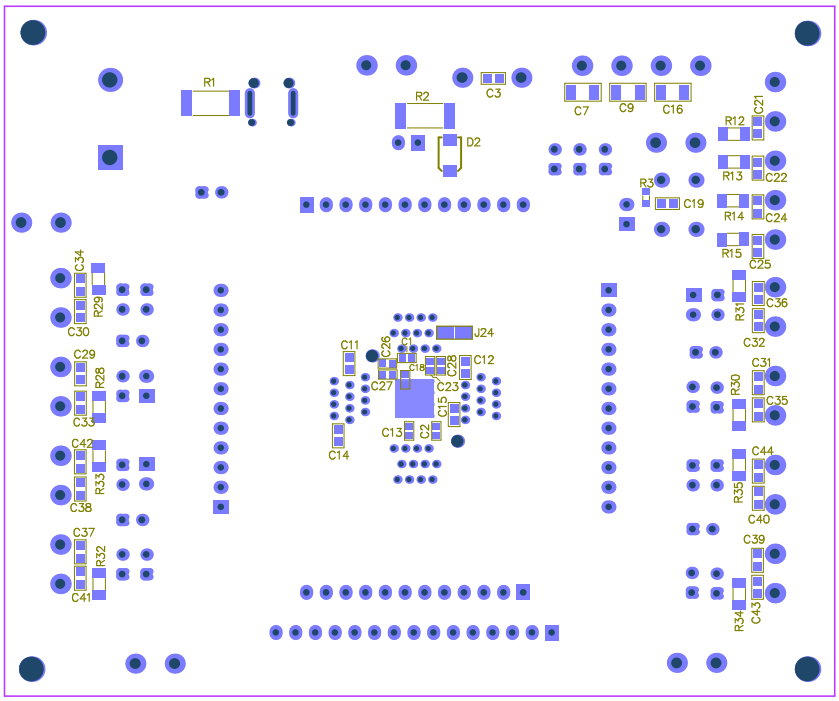
Figure 5. Assembly Top



In the Figure 5 are identified the following connectors:

- Terminal connectors for power supplies (J31)
- Terminal connectors for Squibs connection (J12, J15, J16, J17, J25, J26, J27, J28)
- Terminal connector for RSUs connection (J5)
- Terminal connector for digital signals (J4)
- Terminal connector for VER (J1)
- Terminal connector to eventually add/change C_ER (J2)

Figure 6. **Assembly Bottom**



4 Jumpers and connectors description

In Table 1, the name of each jumper on the board is listed while their default setting (closed or open) is reported in green; the name of the connectors and test points present on the board is also remarked.

Table 1. Jumpers and connectors description

#	Name	J = Jumper C = Connector	Function	Jumper closed/signal connection	Jumper open/ signal NOT connected	Test point
J1	VER	C	Connection to the external VER power supply	VER line externally supplied, connected to VER of L9678, L9679 or L9680(1)	-	Terminals of J30 are the test points for VER supply (J1 side) or C_ER (C_ER side)
J2	CON2	C	Connection of other external C_ER	Other external C_ER connected	No other external C_ER connected(1)	Terminal 1 of J2
J3	J_C_ER	J	To insert the on board C_ER (C4)	On board C_ER (C4) inserted(1)	On board C_ER (C4) NOT inserted	J3 itself
J4	CON15	C	Connections of the digital signals (from microcontroller)	Each signal is connected to the correspondent line coming from microcontroller(1)	Digital signals not driven	Each terminal of J4
J5	CON5	C	Connections of RSU sensors	Each RSUx interface is connected to the correspondent sensor(1)	RSUx interface NOT connected to the correspondent sensor	Each terminal of J5
J6		J	Allow deployment with SF0 shorted to GND	SF0 shorted to GND	SF0 NOT shorted to GND	The same of SF0 pin
J7	J_FEN1	J	FEN1 driven through microcontroller or stuck at VCC	FEN1 fixed at VCC Do not connect J4-6 if J7 is closed	FEN1 driven through microcontroller (J4-6 connected)(1)	The same of FEN1 pin
J8		J	Allow deployment with SF1 shorted to GND	SF1 shorted to GND	SF1 NOT shorted to GND	The same of SF1 pin
J9	J_FEN2	J	FEN2 driven through microcontroller or stuck at VCC	FEN2 fixed at VCC Do not connect J4-5 if J9 is closed	FEN2 driven through microcontroller (J4-5 connected)(1)	The same of FEN2 pin
J10		J	Allow deployment with SF2 shorted to GND	SF2 shorted to GND	SF2 NOT shorted to GND	The same of SF2 pin
J11	J_FENL	J	FENL driven through microcontroller or stuck at VCC	FENL fixed at VCC do not connect J4-4 if J11 is closed	FENL driven through microcontroller (J4-4 connected)(1)	The same of FENL pin
J12		C	Connection of Squib0	SF0 and SR0 connected to squib 0(1)	SF0 and SR0 NOT connected to squib 0	The same of SF0 and SR0 pins
J13	J_SS01	J	Connection of SS01 to C_ER	SS01 connected to C_ER(1)	SS01 NOT connected to C_ER	The same of SS01pin
J14	J_SS23	J	Connection of SS23 to C_ER	SS23 connected to C_ER(1)	SS23 NOT connected to C_ER	The same of SS23pin

#	Name	J = Jumper C = Connector	Function	Jumper closed/signal connection	Jumper open/ signal NOT connected	Test point
J15		C	Connection of Squib1	SF1 and SR1 connected to squib 1(1)	SF1 and SR1 NOT connected to squib 1	The same of SF1 and SR1 pins
J16		C	Connection of Squib2	SF2 and SR2 connected to squib 2(1)	SF2 and SR2 NOT connected to squib 2	The same of SF2 and SR2 pins
J17		C	Connection of Squib3	SF3 and SR3 connected to squib 3(1)	SF3 and SR3 NOT connected to squib 3	The same of SF3 and SR3 pins
J18	J_SS45	J	Connection of SS45 to C_ER	SS45 connected to C_ER(1)	SS45 NOT connected to C_ER	The same of SS45pin
J19	J_SS67	J	Connection of SS67 to C_ER	SS67 connected to C_ER(1)	SS67 NOT connected to C_ER	The same of SS67pin
J20		J	Allow deployment with SF3 shorted to GND	SF3 shorted to GND	SF3 NOT shorted to GND	The same of SF3 pin
J21		J	Allow deployment with SF4 shorted to GND	SF4 shorted to GND	SF4 NOT shorted to GND	The same of SF4 pin
J22		J	Allow deployment with SF5 shorted to GND	SF5 shorted to GND	SF5 NOT shorted to GND	The same of SF5 pin
J23		J	Allow deployment with SF6 shorted to GND	SF6 shorted to GND	SF6 NOT shorted to GND	The same of SF6 pin
J24		J	Allow to close TEST pin to GND	TEST pin shorted to GND(1)	TEST pin left open	-
J25		C	Connection of Squib4	SF4 and SR4 connected to squib 4(1)	SF4 and SR4 NOT connected to squib 4	The same of SF4 and SR4 pins
J26		C	Connection of Squib5	SF5 and SR5 connected to squib 5(1)	SF5 and SR5 NOT connected to squib 5	The same of SF5 and SR5 pins
J27		C	Connection of Squib6	SF6 and SR6 connected to squib 6(1)	SF6 and SR6 NOT connected to squib 6	The same of SF6 and SR6 pins
J28		C	Connection of Squib7	SF7 and SR7 connected to squib 7(1)	SF7 and SR7 NOT connected to squib 7	The same of SF7 and SR7 pins
J29		J	Allow deployment with SF7 shorted to GND	SF7 shorted to GND	SF7 NOT shorted to GND	The same of SF7 pin
J30		J	Allow to reduce the C4 charge current	C4 charge current NOT limited through R2	C4 charge current limited through R2(1)	Each terminal of j30
J31		C	Connection to the external VSYNC, VCC and VSAT power supply	VSYNC, VCC and VSAT lines externally supplied, connected to VSYNC, VCC and VSAT of the L9678, L9679 or L9680(1)	-	Terminals J34_3, J33_8 and J34_4 are the test pionts for VSYNC, VCC and VSAT power supplies
J32		J	Allow to keep RESET signal at VCC or toggle it through S2 button	RESET permanently at VCC/toggle (at GND) through S2	RESET driven by microcontroller through J4_2	J32 terminal on device side or J34_9

#	Name	J = Jumper C = Connector	Function	Jumper closed/signal connection	Jumper open/ signal NOT connected	Test point
J33	CON12	C	Each terminal J33_1:J33_12 corresponds to the device pins from 1 to 12	-	-	Each terminal J33_1:J33_12 corresponds to the device pins from 1 to 12
J34	CON12	C	Each terminal J34_1:J34_12 corresponds to the device pins from 13 to 24	-	-	Each terminal J34_1:J34_12 corresponds to the device pins from 13 to 24
J35	CON12	C	Each terminal J35_1:J35_12 corresponds to the device pins from 25 to 36	-	-	Each terminal J35_1:J35_12 corresponds to the device pins from 25 to 36
J36	CON12	C	Each terminal J36_1:J36_12 corresponds to the device pins from 37 to 48	-	-	Each terminal J36_1:J36_12 corresponds to the device pins from 37 to 48

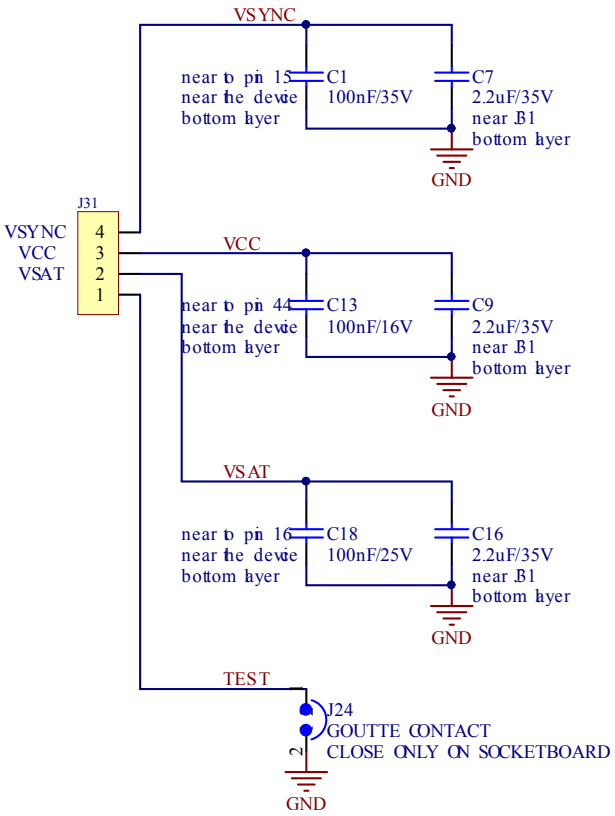
1. *Default condition.*

5 Supply connections

Power supply connection is reported in Figure 7.

VSAT, that is the main power supply, can be connected to SATBUCK of L9779 or L9680 device; VSYNC can be connected to SYNCBOOST of L9779 or L9680 device; VCC can be connected to VCCBUCK of L9779 or L9680 device.

Figure 7. Power supply connections

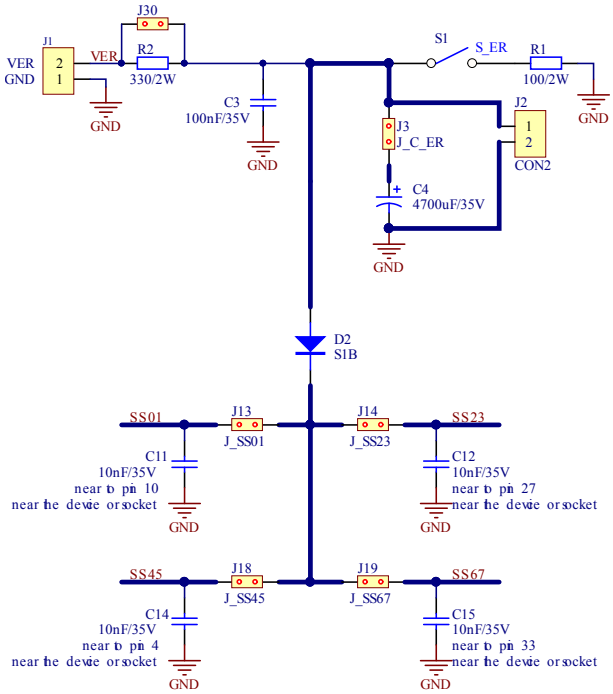


Squib power supply connection, VER, is reported in Figure 8.

VER can be connected to VER of L9779 or L9680 device; in order to be able to sustain deployments, the tank capacitor can be connected closing J3 - J_C_ER on the board, or an external capacitor can be connected through J2.

In order to reduce the charge current of the tank capacitor, resistor R2 can be inserted (J30 open). S1 switch allows to discharge the tank capacitor through R1.

Figure 8. **Squib power supply connections**

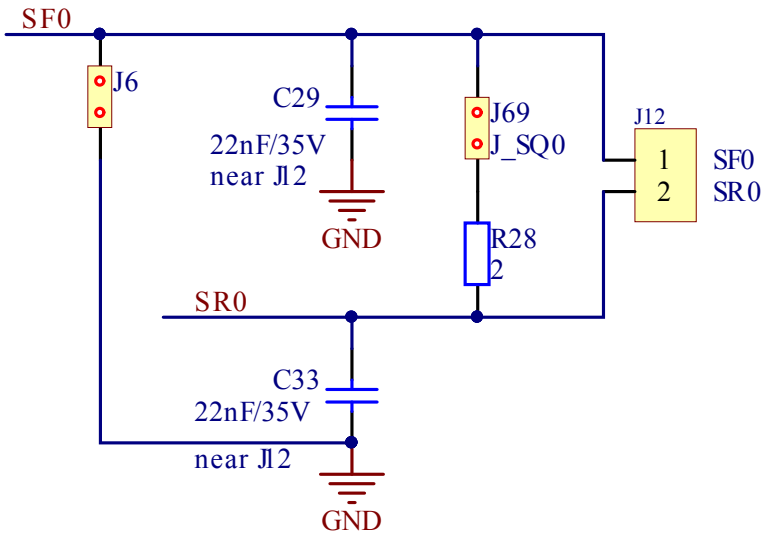


6 Squib connections

Referring to Figure 9, external squibs have to be connected through J12 (squib0) and the other squib connector available on the board; J69 has to be left open (the same for the correspondent jumpers of the others channels).

In order to test the deployment having the high side shorted to GND, J6 (squib0) or the correspondent for the others squibs has to be closed.

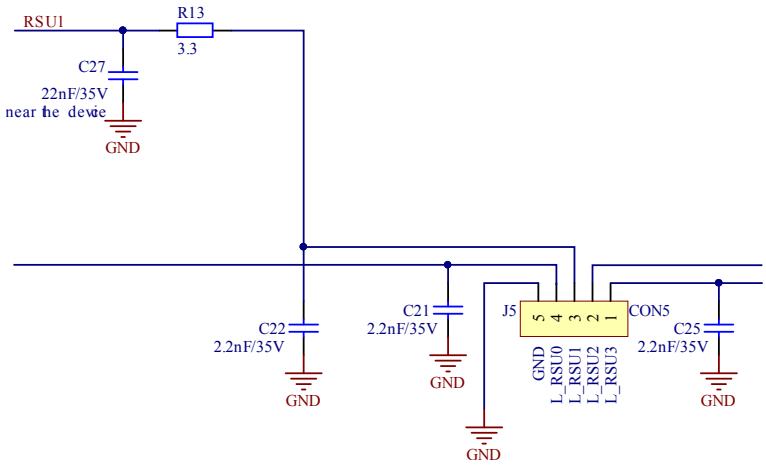
Figure 9. Squib connection



7 RSUx connections

Referring to Figure 10, RSUx can be connected through J5 where only RSU1 is shown:

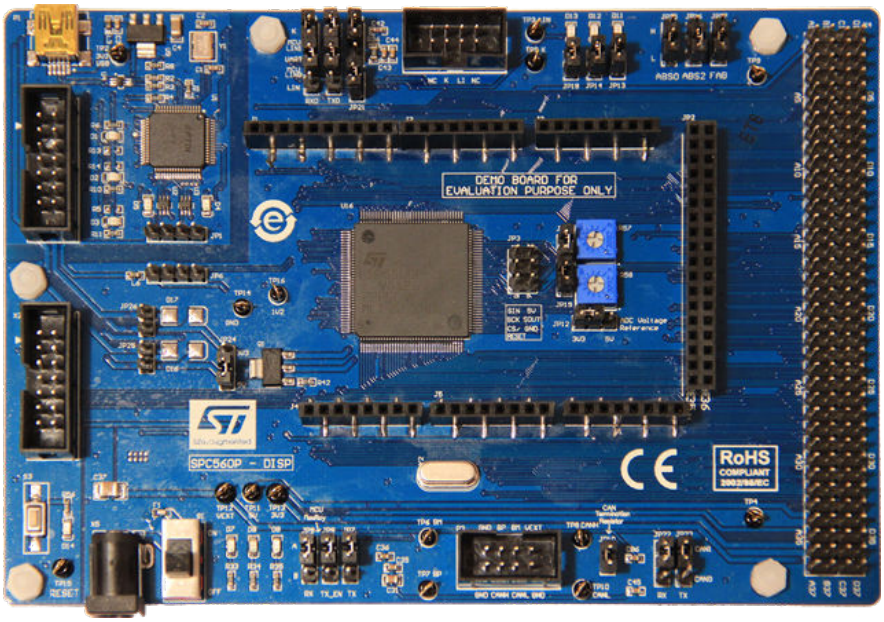
Figure 10. RSUx connection



8 Signals exchanged with microcontroller

L9679E board is supposed to work with SPC56P-Discovery board shown in Figure 11, available at st website.

Figure 11. SPC56-Discovery board



Signals exchanged with microcontroller are available on J4 (see Figure 12).

Each signals has to be connected to the correspondent pin of the 4x36 connector available on the microcontroller board following **Error! Reference source not found.**: GUI interface drives 4 GPIOs, FENL, FENH, UC_DIAGEN and UC_DEPEN; these GPIOs can be connected to J4 in order to drive FEN1, FEN2, FENL.

Table 2. SPC56-Discovery, 4x36 connector

SPC56 board pin	Signal	L9679E J4 pin
Pin # A1 - A36		
A1	-	-
A2	-	-
A3	-	-
A4	-	-
A5	-	-
A6	-	-
A7	-	-
A8	-	-
A9	MCUFAULT	-
A10		-
A11	FENL	4
A12	RESET	2
A13	-	-
A14	-	-

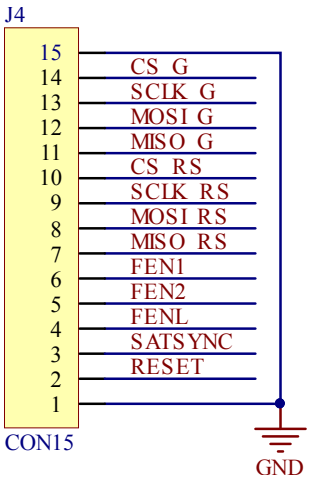
SPC56 board pin	Signal	L9679E J4 pin
A15	CS_G	14
A16	MOSI_G	12
A17	-	-
A18	-	-
A19	-	-
A20	-	-
A21	-	-
A22	-	-
A23	-	-
A24	-	-
A25	-	-
A26	-	-
A27	-	-
A28	-	-
A29	-	-
A30	-	-
A31	-	-
A32	-	-
A33	-	-
A34	-	-
A35	-	-
A36	-	-
Pin #B1 - B36		
B1	-	-
B2	-	-
B3	-	-
B4	-	-
B5	-	-
B6	-	-
B7	-	-
B8	-	-
B9	-	-
B10	ACL	-
B11	FENH	-
B12	-	-
B13	-	-
B14	-	-
B15	SCLK_G	13
B16	MISO_G	11
B17	UC_DIAGEN	
B18	-	-

SPC56 board pin	Signal	L9679E J4 pin
B19	-	-
B20	-	-
B21	-	-
B22	-	-
B23	SATSYNC	3
B24	-	-
B25	-	-
B26	-	-
B27	-	-
B28	-	-
B29	-	-
B30	-	-
B31	-	-
B32	-	-
B33	-	-
B34	-	-
B35	-	-
B36	-	-
Pin # C1 - C36		
C1	-	-
C2	-	-
C3	-	-
C4	-	-
C5	-	-
C6	-	-
C7	-	-
C8	-	-
C9	-	-
C10	-	-
C11	-	-
C12	-	-
C13	-	-
C14	-	-
C15	-	-
C16	UC_DEPEN	
C17	FEN2	5
C18	-	-
C19	-	-
C20	-	-
C21	-	-
C22	-	-

SPC56 board pin	Signal	L9679E J4 pin
C23	-	-
C24	-	-
C25	-	-
C26	MOSI_RS	8
C27	-	-
C28	-	-
C29	-	-
C30	-	-
C31	-	-
C32	-	-
C33	-	-
C34	-	-
C35	-	-
C36	-	-
Pin # D1 - D36		
D1	-	-
D2	-	-
D3	-	-
D4	-	-
D5	-	-
D6	-	-
D7	-	-
D8	-	-
D9	FEN1	6
D10	-	-
D11	-	-
D12	-	-
D13	-	-
D14	-	-
D15	-	-
D16	-	-
D17	-	-
D18	-	-
D19	-	-
D20	-	-
D21	CS_RS	10
D22	-	-
D23	-	-
D24	-	-
D25	SCLK_RS	9
D26	MISO_RS	7

SPC56 board pin	Signal	L9679E J4 pin
D27	-	-
D28	-	-
D29	-	-
D30	-	-
D31	-	-
D32	-	-
D33	-	-
D34	-	-
D35	-	-
D36	-	-

Figure 12. J4 connector for L9679E signals



Revision history

Table 3. **Document revision history**

Date	Version	Changes
03-Mar-2023	1	Initial release.

Contents

List of tables

List of figures