Evaluation board for STGAP4S advanced galvanically isolated gate driver

Introduction

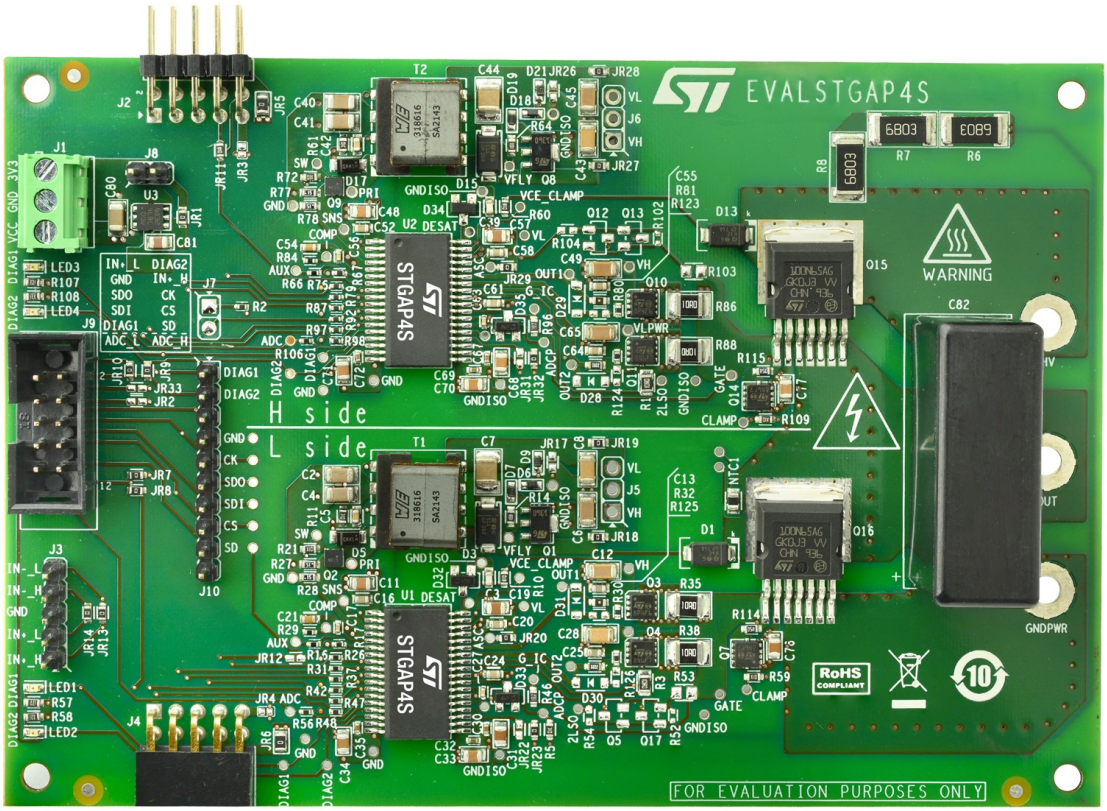
The STGAP4S is a galvanically isolated single gate driver for IGBTs and SiC MOSFETs with advanced protection, configuration, and diagnostic features. The architecture of the STGAP4S isolates the channel gate driving from the control and from the low voltage interface circuitry through true galvanic isolation. The unique output architecture is designed to allow the use of an external MOSFET push-pull stage giving flexibility in terms of current capability dimensioning and easing the use of several power switches in parallel. The 2 pre-driver outputs are characterized by current capability and output voltage swing optimized for that topology and allow the use of a negative gate driving supply.

The EVALSTGAP4S board allows to evaluate all the STGAP4S features. The board is equipped with two STGAP4S drivers connected in an SPI daisy chain and with each high voltage side fed by its own flyback power supply, whose controller is integrated in the driver itself. Each STGAP4S drives the gate of an SiC MOSFET in H2PAK-7 package having 650 V voltage rating and connected in half-bridge.

Multiple EVALSTGAP4S boards can be connected together allowing the implementation of an SPI daisy chain with more than two devices and also the evaluation of more complex topologies, as a full bridge inverter.

The use in combination with the STEVAL-PCC009V2 communication board allows the easy configuration of all the driver's protection and control features, through the SPI interface, as well as access to the driver's status registers, offering an advanced diagnostic. The board can be used also in standalone mode without a communication board using the default device configuration at power-on.

Figure 1. **EVALSTGAP4S evaluation board**



1 Safety and operating instructions

1.1 General terms

During assembly, testing, and operation, the evaluation board poses several inherent hazards, including bare wires, moving or rotating parts and hot surfaces.

Danger: *There is danger of serious personal injury, property damage or death due to electrical shock and burn hazards if the kit or components are improperly used or installed incorrectly.*

The kit is not electrically isolated from the high-voltage supply DC input. No insulation is ensured between the accessible parts and the high voltage. All measuring equipment must use adequately insulated probes, clamps, and connecting wires. Never touch the evaluation board while it is energized as it can cause an electrical shock hazard.

When a tool is used to interface the board to a PC and the board is supplied (HV BUS) at a voltage outside the ELV range, a proper insulation method such as a USB isolator must be used to operate the board.

All operations involving transportation, installation and use, and maintenance must be performed by skilled technical personnel able to understand and implement national accident prevention regulations. For the purposes of these basic safety instructions, “skilled technical personnel” are suitably qualified people who are familiar with the installation, use, and maintenance of power electronic systems.

1.2 Intended use of evaluation board

The board is designed for evaluation purposes only and must not be used for electrical installations or machinery. Technical data and information concerning the power supply conditions are detailed in the documentation and should be strictly observed.

1.3 Installing the evaluation board

- The installation and cooling of the evaluation board must be in accordance with the specifications and target application.
- The board must be protected against excessive strain. In particular, components should not be bent or isolating distances altered during transportation or handling.
- No contact must be made with other electronic components and contacts.
- The board contains electrostatically-sensitive components that are prone to damage if used incorrectly. Do not mechanically damage or destroy the electrical components (potential health risks).

1.4 Operating the evaluation board

To properly operate the board, follow these safety rules.

1. Work area safety:
   - The work area must be clean and tidy.
   - Do not work alone when boards are energized.
   - Protect against inadvertent access to the area where the board is energized using suitable barriers and signs.
   - A system architecture that supplies power to the evaluation board must be equipped with additional control and protective devices in accordance with the applicable safety requirements (that is, compliance with technical equipment and accident prevention rules).
   - Use non-conductive and stable work surface.
   - Use adequately insulated clamps and wires to attach measurement probes and instruments.
2. Electrical safety:
   - Remove power supply from the board and electrical loads before performing any electrical measurement.
   - Proceed with the arrangement of measurement setup, wiring, or configuration paying attention to high voltage sections.
   - Once the setup is complete, energize the board.
   - The kit is not electrically isolated from the AC/DC input. If a tool is used to interface the board with a PC and the board is supplied (HV BUS) at a voltage outside the ELV range, a proper insulation method such as a USB isolator must be used to operate the board.

Danger: *Do not touch the board when it is energized or immediately after it has been disconnected from the voltage supply as several parts and power terminals containing potentially energized capacitors need time to discharge. Do not touch the boards after disconnection from the voltage supply as several parts, included PCB, may still be very hot. The kit is not electrically isolated from the DC input.*

3. Personal safety
   - Always wear suitable personal protective equipment such as insulating gloves and safety glasses.
   - Take adequate precautions and install the board in such a way to prevent accidental touch. Use protective shields such as an insulating box with interlocks if necessary.

2 Getting started

2.1 EVALSTGAP4S with STEVAL-PCC009V2 and evaluation software

The EVALSTGAP4S board, in combination with the STEVAL-PCC009V2 interface board and the STSW-STGAP4 software toolset, allows to easily evaluate the STGAP4S functionalities. Indeed, the evaluation software allows to quickly configure the device parameters and to monitor the status flags as well as the diagnostic outputs. Moreover, the software also allows to save a configuration set and recall it when needed, for instance after the board power-on.

The PWM input signals must be provided to the dedicated connector using an external function generator.

2.1.1 Check list

- PC with Microsoft® Windows® 10 with a free USB port
- EVALSTGAP4S board
- STEVAL-PCC009V2 interface board (with installed the dedicated firmware STSW-STGAP4_FW.hex)
- STSW-STGAP4 GUI evaluation software
- 10-pin flat cable
- USB to Mini-USB cable
- Power supply for VCC supply voltage
- PWM function generator

For information about the installation of the STSW-STGAP4_FW.hex firmware in the STEVAL-PCC009V2 interface board and of the STSW-STGAP4 GUI evaluation software, see the STSW-STGAP4 toolset User Manual.

2.1.2 Single board setup example

- Connect the EVALSTGAP4S J9 connector to the STEVAL-PCC009V2 10-pin connector using the flat cable.
- Connect the EVALSTGAP4S VCC power supply, present on J1 connector, to a power supply keeping it off.
- Connect the STEVAL-PCC009V2 to the PC using the USB cable.
- Turn on the VCC power supply (8 V<VCC<24 V) of the EVALSTGAP4S. The DIAG1 and DIAG2 LEDs turn on.
- Connect the input signals IN+_H, IN+_L of EVALSTGAP4S J3 connector to the PWM function generator signals.
- Start the STSW-STGAP4 GUI evaluation software.

The board is ready to be used. See the STSW-STGAP4 toolset User Manual for details about the available operations. The minimum operations to enable the PWM outputs are:

- Execute the ResetStatus, the fault flags are cleared and the DIAG1 and DIAG2 LEDs switch off.
- Set the $\overline{SD}$ high, the input to output PWM is now enabled.

2.1.3 Multiple board setup example

- Refer to Section 5 for the hardware setup of the EVALSTGAP4S boards.
- Connect the MASTER EVALSTGAP4S J9 connector to the STEVAL-PCC009V2 10-pin connector using the flat cable.
- Connect the MASTER EVALSTGAP4S VCC power supply, present on J1 connector, to a power supply keeping it off.
- Connect the STEVAL-PCC009V2 to the PC using the USB cable.
- Turn on the VCC power supply (8 V<VCC<24 V) of the MASTER EVALSTGAP4S. The DIAG1 and DIAG2 LEDs turn-on.
- Connect the input signals IN+_H, IN+_L of each EVALSTGAP4S J3 connector to the PWM function generator signals.
- Start the STSW-STGAP4 GUI evaluation software.

The board is ready to be used. See the STSW-STGAP4 toolset User Manual for details about the available operations. The minimum operations to enable the PWM outputs are:

- Execute the ResetStatus, the fault flags are cleared and the DIAG1 and DIAG2 LEDs switch off.
- Set the $\overline{SD}$ high, the input to output PWM is now enabled.

2.2 EVALSTGAP4S in standalone mode

The board can also work without SPI programming using the STGAP4S default values at power-on.

2.2.1 Check list

- EVALSTGAP4S board
- Power supply for VCC supply voltage
- PWM function generator

2.2.2 Single board setup example

- Connect the EVALSTGAP4S VCC power supply, present on J1 connector, to a power supply and turn it on (8 V<VCC<24 V). The DIAG1 and DIAG2 LEDs turn on.
- Connect the input signals IN+_H, IN+_L of EVALSTGAP4S J3 connector to the PWM function generator signals.
- Set the $\overline{SD}$ pin low for at least 100 µs (J1 connector).
- Set the $\overline{SD}$ pin high value: the fault flags are cleared at the rise and the DIAG1 and DIAG2 LEDs switch off.
- The input to output PWM is now enabled.

2.2.3 Multiple board setup example

- Refer to Section 5 for the hardware setup of the EVALSTGAP4S boards.
- Connect the MASTER EVALSTGAP4S VCC power supply, present on J1 connector, to a power supply and turn it on (8V<VCC<24V). The DIAG1 and DIAG2 LEDs turn on.
- Connect the input signals to IN+_H, IN+_L of EVALSTGAP4S J3 connector to the PWM function generator signals.
- Connect the PWM input signals IN+_H, IN+_L of each EVALSTGAP4S J3 connector to the PWM function generator signals.
- Set the $\overline{SD}$ pin low for at least 100 µs (J1 connector).
- Set the $\overline{SD}$ pin high value: the fault flags are cleared at the rise and the DIAG1 and DIAG2 LEDs switch off.
- The input to output PWM is now enabled.

3 Hardware description and configuration

The EVALSTGAP4S is provided with a ready-to-use hardware configuration.

The power stage is composed by two SiC MOSFETs in half-bridge configuration with a small capacitor bulk connected to the HV BUS:

- SiC MOSFETs: SCTH100N65G2-7AG 650 V 20 mΩ - H7PAK
- Bulk capacitor: (2.2 uF//470 nF//470 nF) - 630 V (see Figure 16 for details)
- High-voltage rail up to 520 V: limited by MOSFETs and capacitor ratings
- Maximum working voltage across isolation: 1200 V

The EVALSTGAP4S is provided with a linear regulator supplied by the VCC voltage that generates the 3.3 V supply for the low-voltage side of both the STGAP4S present on the board. The VCC voltage is also used to supply the two isolated flyback power supplies (one for each driver) that are driven by the controller integrated in each STGAP4S and generates the positive and negative voltages for the driving side. Thus, only the VCC voltage is needed to fully supply the board (except for the HV BUS voltage):

- Only VCC voltage needed to supply the board
- On-board 3.3 V linear regulator for the LV side supply (common to both drivers)
- Isolated flyback for HV +18/-5 V driving supply (one for each driver)

The STGAP4S features an SPI interface that is used to set the device parameters, enable or disable the device functions, and access the advanced diagnostic. The EVALSTGAP4S is suitable to be used in combination with STEVAL-PCC009V2 (with the dedicated firmware STSW-STGAP4_FW.hex installed) and STSW-STGAP4 GUI software. However, it is also possible to operate the STGAP4S without using the SPI interface. In this case, the driver works with the default configuration values and protections.

Table 1. Connector description

Name	Type	Function
J1	Power supply	VCC supply voltage to the flyback and to the 3.3V on-board linear regulator. Optional 3V3IN supply for the logic control side.
J2	Board extension	Connection to an optional slave EVALSTGAP4S board
J3	Control signal	PWM logic inputs
J4	Board extension	Connection to an optional master EVALSTGAP4S board
J5	Power supply	Optional external VH and VL supplies for the HV side of the LOW-side driver
J6	Power supply	Optional external VH and VL supplies for the HV side of the HIGH-side driver
J9	Control signal	SPI and diagnostic interfacing. Suitable for STEVAL-PCC009V2 interface board.
J10	Control signal	Connector for SPI and diagnostic probing
HV	Power connection	Plated hole for connection to the positive pole of the high-voltage bus. Drain of the high-side power MOSFET.
OUT	Power connection	Plated hole for connection to a load. Source of the high-side power MOSFET and drain of the low-side power MOSFET.
GNDPWR	Power connection	Plated hole for connection to the negative pole of the high-voltage bus. Source of the low-side power MOSFET.

Figure 2. **Connectors location**

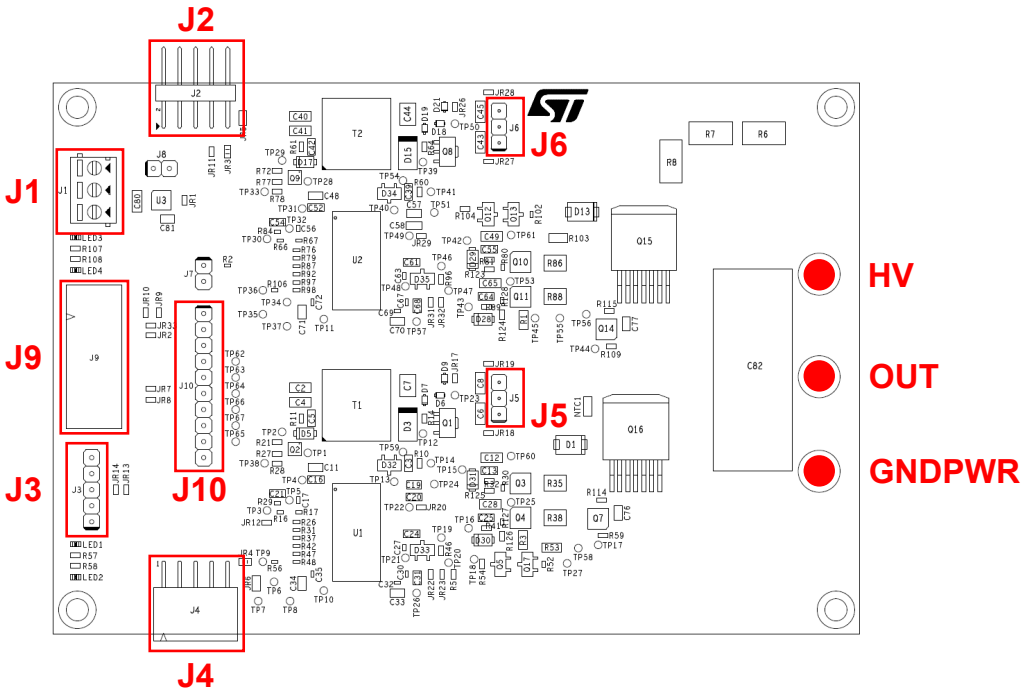


Table 2. **Jumper resistor description**

Name	Side	Driver	Function
JR1	LV	Both	3V3IN from on-board regulator
JR3, JR5	LV	Both	Slave board power supply
JR4, JR6	LV	Both	Master board power supply
JR7, JR8, JR9, JR10	LV	Both	Cumulative diagnostic (DIAG1, DIAG2)
JR11, JR12	LV	Both	Options for the SPI chain
JR13, JR14	LV	Both	PWM logic input configuration
JR17	HV	Low-side	VL to GNDSISO bypass
JR18, JR19	HV	Low-side	VH, VL on-board regulation disconnection
JR20	HV	Low-side	ASC to GNDSISO bypass
JR21	HV	Low-side	SENSE to GNDSISO bypass
JR22, JR23	HV	Low-side	DEFAULT pin setting
JR26	HV	High-side	VL to GNDSISO bypass
JR27, JR28	HV	High-side	VH, VL on-board regulation disconnection
JR29	HV	High-side	ASC to GNDSISO bypass
JR30	HV	High-side	SENSE to GNDSISO bypass
JR31, JR32	HV	High-side	DEFAULT pin setting

Figure 3. **Jumper location – TOP layer**

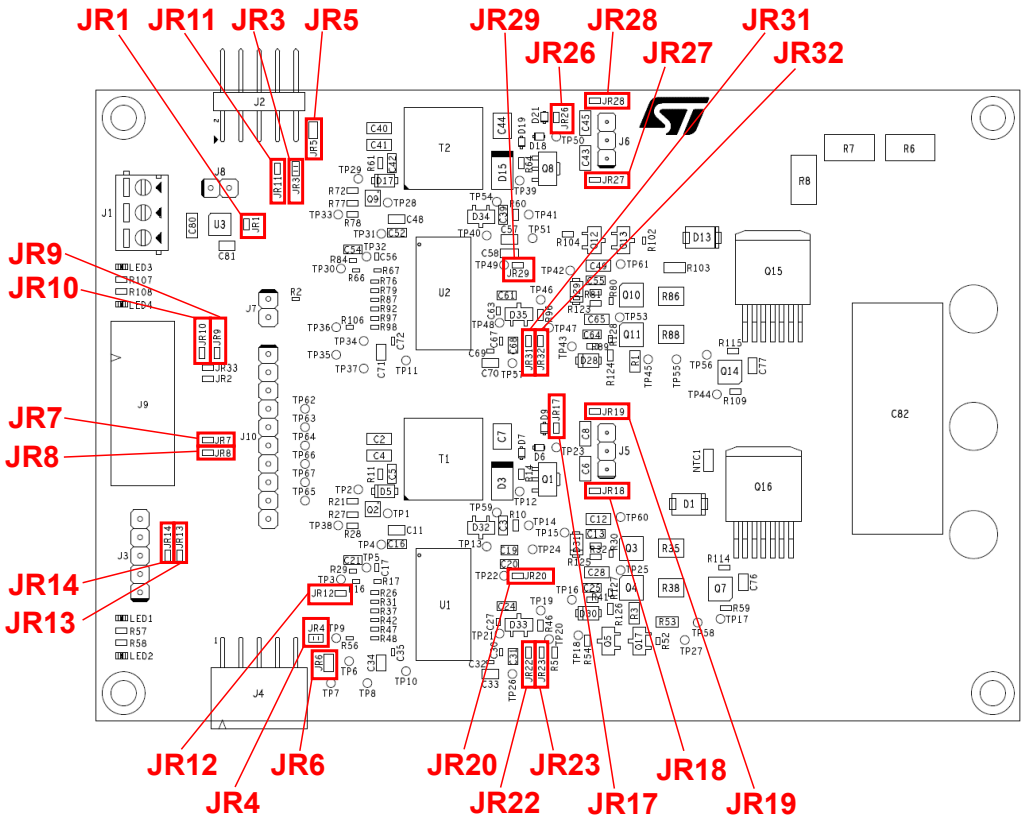


Figure 4. **Jumper location – BOT layer**

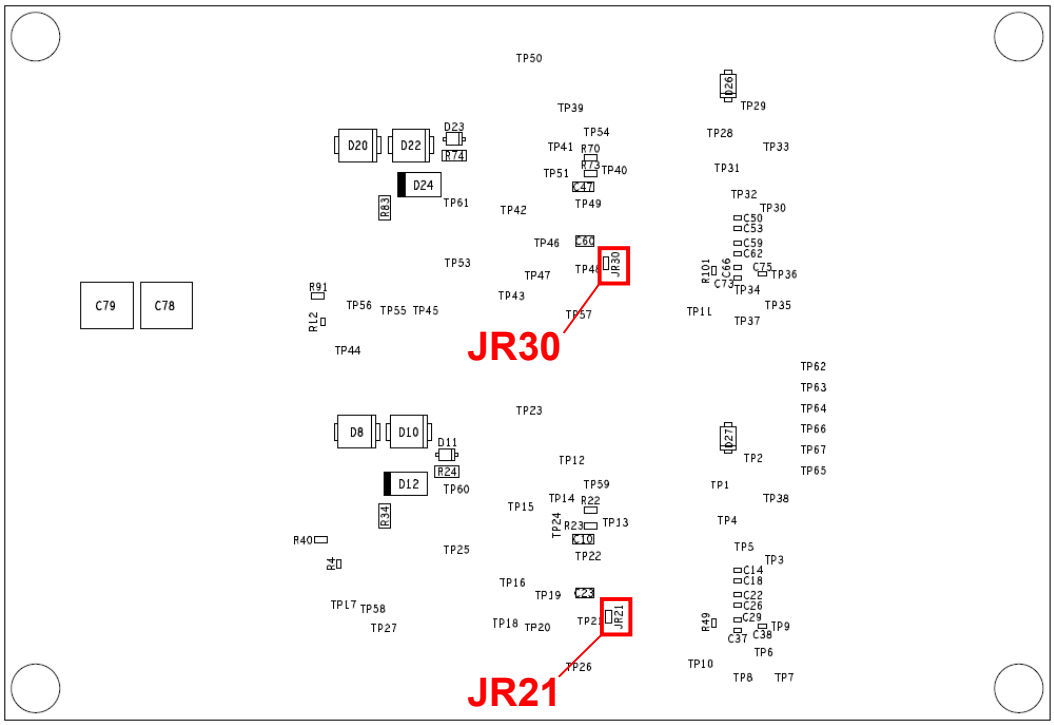


Table 3. Jumper configuration of 3V3IN power supply source

Operating voltage	Supply voltage source	Jumper configurations	Default configuration
3V3IN = 3.3V±5%	On-board regulator (from U3) (VCC must be present, see Table 4)	JR1 = CLOSE JR3 = OPEN JR4 = OPEN	X
	External power supply (from J1)	JR1 = OPEN JR3 = OPEN JR4 = OPEN	
	External power supply (from J1) and fed to board extension connectors (to J2 and J4) or Supplied from board extension connectors (from J2 or J4)	JR1 = OPEN JR3 = CLOSE JR4 = CLOSE	

Table 4. Jumper configuration of VCC power supply source

Operating voltage	Supply voltage source	Jumper configuration	Default configuration
8V < VCC < 24V	External power supply (from J1)	JR5 = OPEN JR6 = OPEN	X
	External power supply (from J1) and feed to board extension connectors (to J2 and J4) or Supply from board extension connectors (from J2 or J4)	JR5 = CLOSE JR6 = CLOSE	

Table 5. Jumper configuration of LOW-side VH, VL power supply source

Operating voltage	Supply voltage source	Jumper configuration	Default configuration
VH_L = +18V VL_L = -5V	On-board flyback with post regulator (VCC must be present, see Table 4)	JR17 = OPEN JR18 = CLOSE JR19 = CLOSE	X
VH_L = +18V VL_L = 0V	On-board flyback with post regulator (VCC must be present, see Table 4)	JR17 = CLOSE JR18 = CLOSE JR19 = CLOSE	
See STGAP4S Datasheet for recommended values on www.st.com	External power supply (from J5)	JR17 = DON'T CARE JR18 = OPEN JR19 = OPEN	

Table 6. Jumper configuration of HIGH-side VH, VL power supply source

Operating voltage	Supply voltage source	Jumper configuration	Default configuration
VH_H = +18V VL_H = -5V	On-board flyback with post regulator (VCC must be present, see Table 4)	JR26 = OPEN JR27 = CLOSE JR28 = CLOSE	X
VH_H = +18V	On-board flyback with post regulator	JR26 = CLOSE	

Operating voltage	Supply voltage source	Jumper configuration	Default configuration
VL_H = 0V	(VCC must be present, see Table 4)	JR27 = CLOSE JR28 = CLOSE	
See STGAP4S Datasheet for recommended values www.st.com	External power supply (from J6)	JR26 = DON'T CARE JR27 = CLOSE JR28 = CLOSE	

Table 7. Jumper configuration of PWM input signal (J3 connector)

PWM inputs	Function	Jumper configuration	Default configuration
IN+_H = IN-_L IN+_L = IN-_H	The LOW-side and HIGH-side drivers are interlocked. Configuration for cross conduction prevention.	JR13 = CLOSE JR14 = CLOSE	X
LS: IN+_L, IN-_L HS: IN+_H, IN-_H	The LOW-side and HIGH-side drivers are separate. No cross conduction prevention.	JR13 = OPEN JR14 = OPEN	

Table 8. Jumper configuration of diagnostic DIAG1 (J7, J2, J4 connectors)

Signal	Function	Jumper configuration	Default configuration
DIAG1 = DIAG1_L and DIAG1_H	The DIAG1 signal is the cumulative of the open drain outputs DIAG1_L and DIAG1_H. LED1 and LED3 are driven according to DIAG1	JR7 = CLOSE JR8 = CLOSE	X
DIAG1 = DIAG1_L	Only DIAG1_L is reported to the DIAG1 signal. LED1 is driven according to DIAG1=DIAG1_L LED3 is driven according to DIAG1_H	JR7 = OPEN JR8 = CLOSE	
DIAG1 = DIAG1_H	Only DIAG1_H is reported to the DIAG1 signal. LED1 is driven according to DIAG1_L LED3 is driven according to DIAG1=DIAG1_H	JR7 = CLOSE JR8 = OPEN	

Table 9. Jumper configuration of diagnostic DIAG2 (J7, J2, J4 connectors)

Signal	Function	Jumper configuration	Default configuration
DIAG2 = DIAG2_L and DIAG2_H	The DIAG2 signal is the cumulative of the open drain outputs DIAG2_L and DIAG2_H. LED2 and LED4 are driven according to DIAG2	JR9 = CLOSE JR10 = CLOSE	X
DIAG2 = DIAG2_L	Only DIAG2_L is reported to the DIAG2 signal. LED2 is driven according to DIAG2=DIAG2_L LED4 is driven according to DIAG2_H	JR9 = CLOSE JR10 = OPEN	
DIAG2 = DIAG2_H	Only DIAG2_H is reported to the DIAG2 signal. LED2 is driven according to DIAG2_L LED4 is driven according to DIAG2=DIAG2_H	JR9 = CLOSE JR10 = OPEN	

Table 10. Jumper configuration of SPI chain

Signal	Function	Jumper configuration	Default configuration
SDO = SDO_H	Configuration of SPI daisy chain loop with two devices (HS+LS) Suitable for: • single board configuration with two device daisy chain. See Section 4 • slave board closing the chain in multiple board configuration. See Section 5	JR11 = CLOSE JR12 = OPEN	X
SDO = SDO_L	Configuration of SPI daisy chain loop with only one device (LS). Suitable for single board configuration with only LS connected.	JR11 = OPEN JR12 = CLOSE	
Master board: SDO from J2 Slave board SDO from J2 to J4	Configuration to leave open the SPI daisy chain loop and to propagate SDO_H in multiple board configuration Suitable in multiple board configuration for: • the master board • the middle slave board(s) See Section 5	JR11 = OPEN JR12 = OPEN	

Table 11. Jumper configuration of LOW-side ASC bypass jumper

Signal	Function	Jumper configuration	Default configuration
ASC_L = GNDISO_L	ASC pin shorted to GNDISO	JR20 = CLOSE	X
ASC_L = OPEN	ASC pin open, TP22 can be used to drive the signal	JR20 = OPEN	

Table 12. Jumper configuration of HIGH-side ASC bypass jumper

Signal	Function	Jumper configuration	Default configuration
ASC_H = GNDISO_H	ASC pin shorted to GNDISO	JR29 = CLOSE	X
ASC_H = OPEN	ASC pin open, TP49 can be used to drive the signal	JR29 = OPEN	

Table 13. Jumper configuration of LOW-side SENSE bypass jumper

Signal	Function	Jumper configuration	Default configuration
SENSE_L = GNDISO_L	SENSE pin shorted to GNDISO	JR21 = CLOSE	X
SENSE_L = OPEN	SENSE pin open, TP21 can be used to drive the signal	JR21 = OPEN	

Table 14. Jumper configuration of HIGH-side SENSE bypass jumper

Signal	Function	Jumper configuration	Default configuration
SENSE_H = GNDISO_H	SENSE pin shorted to GNDISO	JR29 = CLOSE	X
SENSE_H = OPEN	SENSE pin open, TP48 can be used to drive the signal	JR29 = OPEN	

Table 15. Jumper configuration for LOW-side DEFAULT function (Operation flow chart)

Name	Function	Jumper configuration	Default configuration
DEFAULT_L	DEFAULT PIN set LOW	JR22 = CLOSE JR23 = OPEN	X

Name	Function	Jumper configuration	Default configuration
DEFAULT_L	DEFAULT PIN set HIGH	JR22 = OPEN JR23 = CLOSE	

Table 16. Jumper configuration for HIGH-side DEFAULT function

Name	Function	Jumper configuration	Default configuration
DEFAULT_H	DEFAULT PIN set LOW	JR31 = CLOSE JR32 = OPEN	X
	DEFAULT PIN set HIGH	JR31 = OPEN JR32 = CLOSE	

Table 17. Test points

Pin	Side	Driver	Connection
TP1	Low-voltage	Low-side	Flyback – MOSFET drain
TP2	Low-voltage	Low-side	Flyback – MOSFET gate
TP3	Low-voltage	Low-side	Flyback – AUX T1
TP4	Low-voltage	Low-side	Flyback – SNS_L
TP5	Low-voltage	Low-side	Flyback – COMP_L
TP6	Low-voltage	Low-side	GND
TP7	Low-voltage	Low-side	DIAG1_L
TP8	Low-voltage	Low-side	DIAG2_L
TP9	Low-voltage	Low-side	ADC_L
TP10	Low-voltage	Low-side	GND
TP11	Low-voltage	Low-side	GND
TP12	High-voltage	Low-side	Flyback – VFLY_L (secondary)
TP13	High-voltage	Low-side	DESAT_L
TP14	High-voltage	Low-side	VCE_CLAMP_L
TP15	High-voltage	Low-side	OUT1_L
TP16	High-voltage	Low-side	OUT2_L
TP17	High-voltage	Low-side	CLAMP_L
TP18	High-voltage	Low-side	2LSO_L
TP19	High-voltage	Low-side	GATE_IC_L (device pin)
TP20	High-voltage	Low-side	ADCP_L
TP21	High-voltage	Low-side	SENSE_L
TP22	High-voltage	Low-side	ASC_L
TP23	High-voltage	Low-side	GNDISO_L
TP24	High-voltage	Low-side	VL_L
TP25	High-voltage	Low-side	VLPWR_L
TP60	High-voltage	Low-side	VH_L
TP26	High-voltage	Low-side	GNDISO_L
TP27	High-voltage	Low-side	GNDISO_L
TP28	Low-voltage	High-side	Flyback – MOSFET drain

Pin	Side	Driver	Connection
TP29	Low-voltage	High-side	Flyback – MOSFET gate
TP30	Low-voltage	High-side	Flyback – AUX T2
TP31	Low-voltage	High-side	Flyback – SNS_H
TP32	Low-voltage	High-side	Flyback – COMP_H
TP33	Low-voltage	High-side	GND
TP34	Low-voltage	High-side	DIAG1_H
TP35	Low-voltage	High-side	DIAG2_H
TP36	Low-voltage	High-side	ADC_H
TP37	Low-voltage	High-side	GND
TP38	Low-voltage	High-side	GND
TP39	Low-voltage	High-side	Flyback – VFLY_H (secondary)
TP40	Low-voltage	High-side	DESAT_H
TP41	High-voltage	High-side	VCE_CLAMP_H
TP42	High-voltage	High-side	OUT1_H
TP43	High-voltage	High-side	OUT2_H
TP44	High-voltage	High-side	CLAMP_H
TP45	High-voltage	High-side	2LSO_H
TP46	High-voltage	High-side	GATE_IC_H (device pin)
TP47	High-voltage	High-side	ADCP_H
TP48	High-voltage	High-side	SENSE_H
TP49	High-voltage	High-side	ASC_H
TP50	High-voltage	High-side	GNDISO_H
TP51	High-voltage	High-side	VL_H
TP53	High-voltage	High-side	VLPWR_H
TP61	High-voltage	High-side	VH_H
TP54	High-voltage	High-side	GNDISO_H
TP55	High-voltage	High-side	GNDISO_H
TP56	High-voltage	High-side	GATE_H (SiC gate)
TP57	High-voltage	High-side	GNDISO_H
TP58	High-voltage	Low-side	GATE_L (SiC gate)
TP59	High-voltage	Low-side	GNDISO_L
TP62	Low-voltage	Both	GND
TP63	Low-voltage	Both	SPI: CK
TP64	Low-voltage	Both	SPI: SDO
TP65	Low-voltage	Both	SPI: SDO_L
TP66	Low-voltage	Both	SPI: SDI
TP67	Low-voltage	Both	SPI: CS

4 Single board

The EVALSTGAP4S is provided with a ready-to-use SiC MOSFET half-bridge. The board must be supplied feeding the VCC voltage to the J1 connector. The VCC voltage is used to supply the flyback section of each driver and the on-board linear regulator that generates the 3V3IN for both the drivers. The high-voltage side of each driver is fed by its own integrated flyback power supply followed by a post-regulator.

The board is set in order to supply the driver with the following voltages:

- 3V3IN = 3.3 V
- VH-GNDISO = 18 V
- VL-GNDISO = -5 V

The drivers can be used with the default configuration or programmed through SPI to set the internal configuration registers. The drivers are connected in daisy chain, where the low-side driver is the master and the high-side is the slave.

The logic lines $\overline{SD}$, DIAG1, and DIAG2 are shared by the two drivers. The IN+ and IN- pins of the drivers are connected in order to achieve the interlocking function for cross conduction prevention. The power switches can be turned on properly driving the two lines IN+_L, IN+_H available on the J3 connector.

Alternatively, the board can be set to independently control the PWM pins of each driver (see Table 7 for details about the configuration of the jumpers).

Figure 5. Single board configuration with hardware shoot-through protection

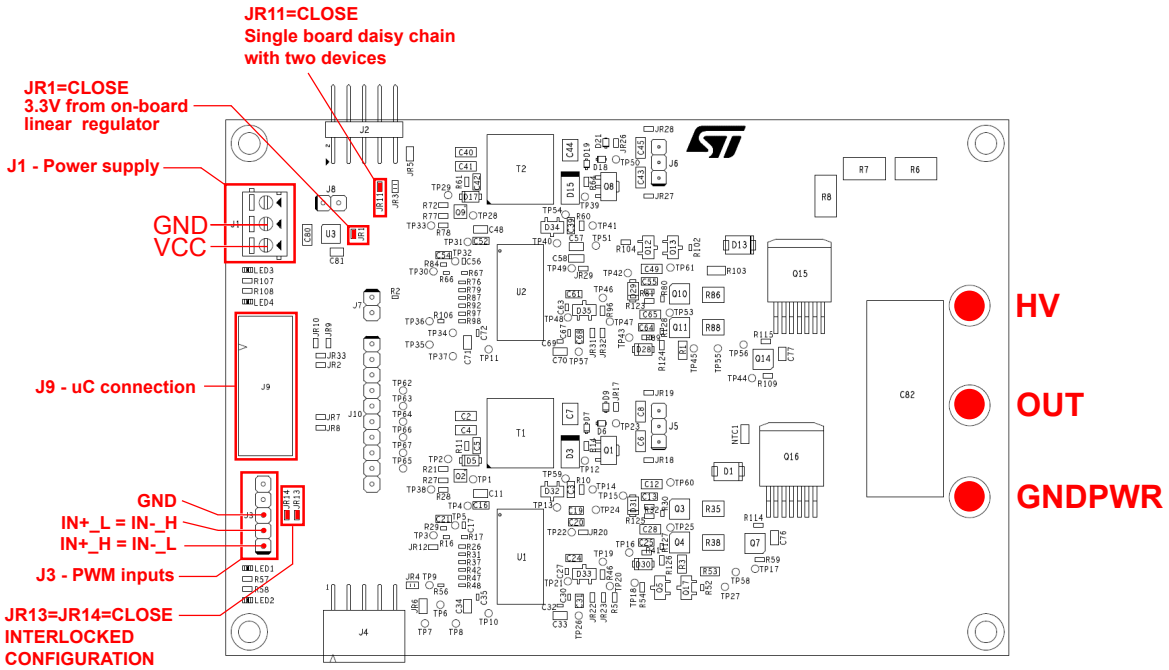


Figure 6. **Half-bridge configuration with hardware shoot-through protection**

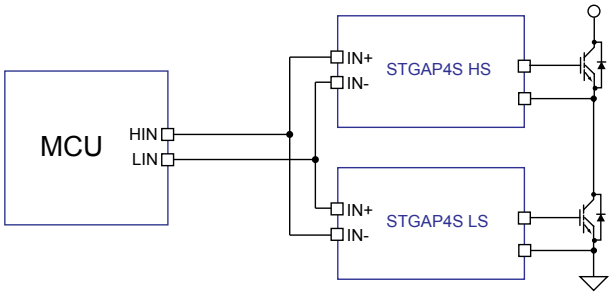
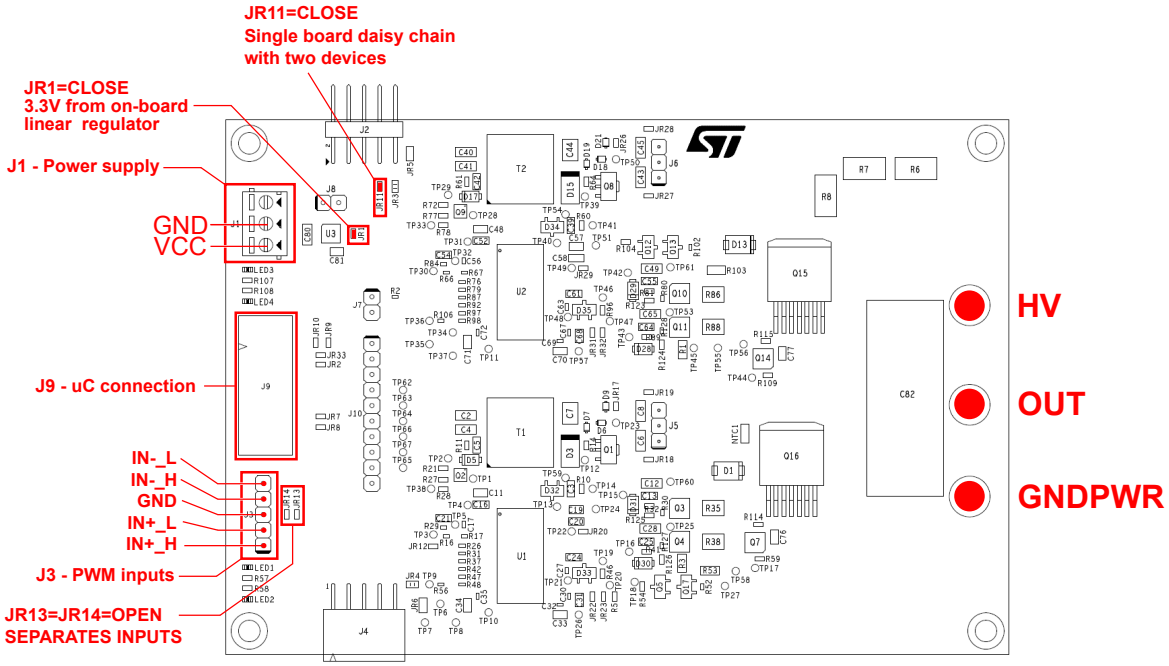


Figure 7. **Single board configuration with independent inputs**



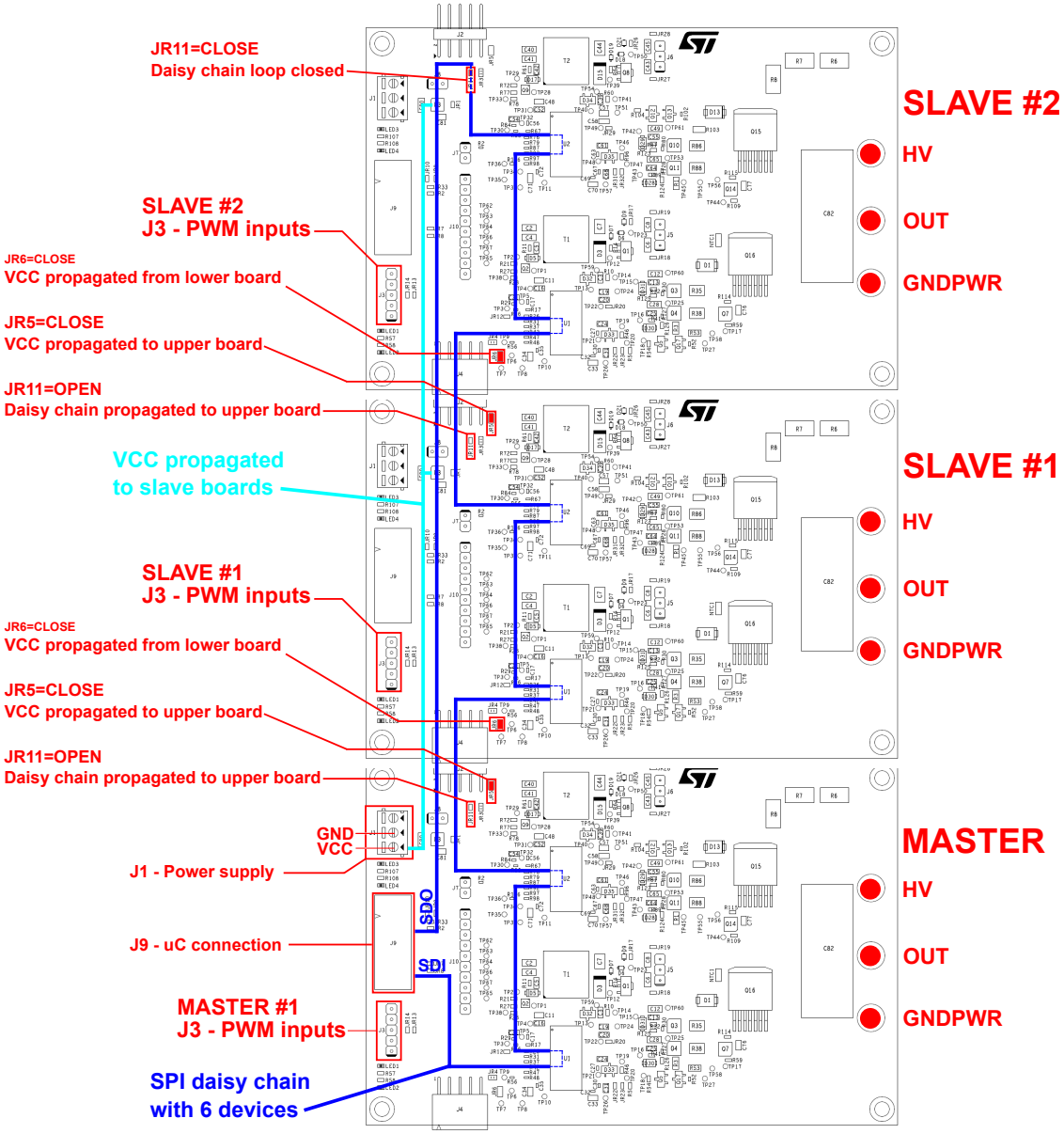
5 Multiple boards connection

To evaluate complex topologies, like a full inverter, it is possible to connect multiple EVALSTGAP4S boards through connectors J2 and J4. The drivers can be configured through the daisy chain connection of the SPI bus where the driver in the lowest board is the master and must be connected to the µC board using the J7 connector and all the other drivers in the chain are slaves. In Figure 8 the connection of three boards is shown, that allows to implement a full three-phase inverter.

The master board must be supplied with VCC, as done in the single board topology, and the supply is propagated to slave boards through the J2 connector. On each board, the VCC feeds the local flyback and the local on-board 3.3 V linear regulator. The upper slave board (#2 in Figure 8) is set with JR11=CLOSE to close the SPI loop, while on the other boards the setting must be with JR11=OPEN to propagate the SPI communication through the J2 connector.

The PWM input signals can be set either as “shoot-through protection” or “independent” as already reported for the single board configuration and according to Table 7.

Figure 8. Three boards connection



6 Power supply options

The EVALSTGAP4S board is provided with an on-board linear regulator to supply the 3V3IN of the LV side and a flyback circuit to supply the HV side.

The linear regulator is fed by the VCC and generates a 3.3 V that is used to supply both the STGAP4S devices mounted on the board, as shown in Figure 9. Alternatively, opening the jumper JR1, the 3V3IN can be provided by an external power supply, as shown in Figure 10.

Figure 9. On-board linear regulator (default setting)

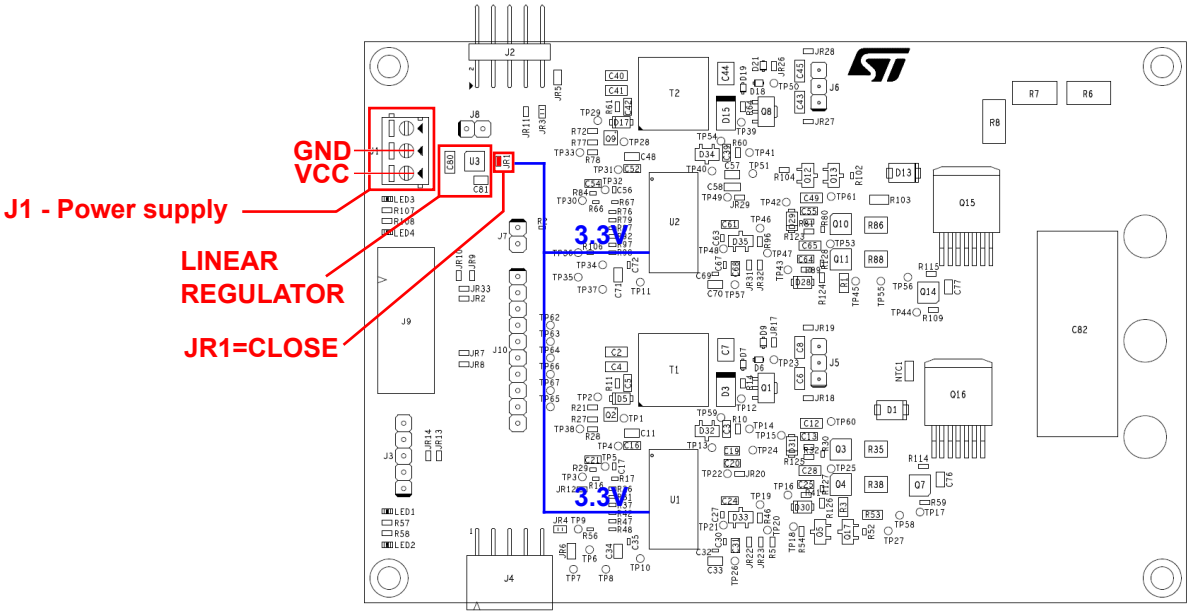
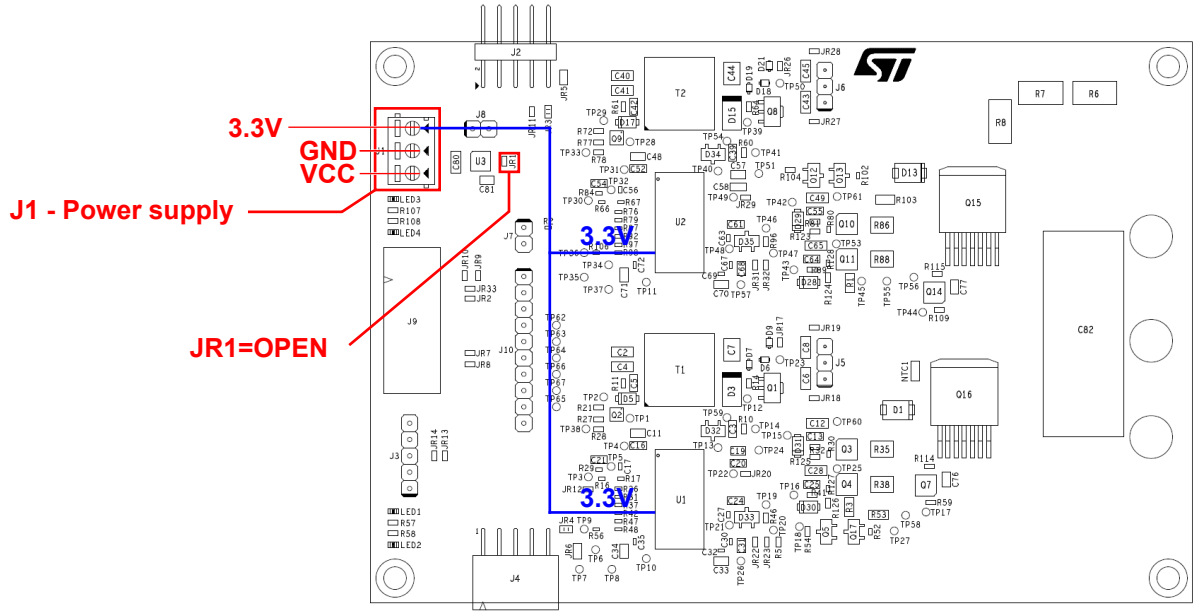


Figure 10. 3V3IN fed by external power supply



As as shown in Figure 11, the VCC voltage feeds also the flyback converter that generates an isolated secondary voltage used to supply a post-regulator that stabilizes the HV side supply voltages to the following values:

- VH-GNDISO = 18 V
- VL-GNDISO = -5 V

The flyback controller integrated in the STGAP4S works only if the 3V3IN voltage supply is present.

As shown in Figure 12, alternatively the VH and VL supplies can be fed by an external power supply using the J5 connector for the LOW-side driver and J6 for the HIGH-side driver. See Table 5 and Table 6 for details about the configuration of the jumpers.

Figure 11. Flyback power supply (default setting)

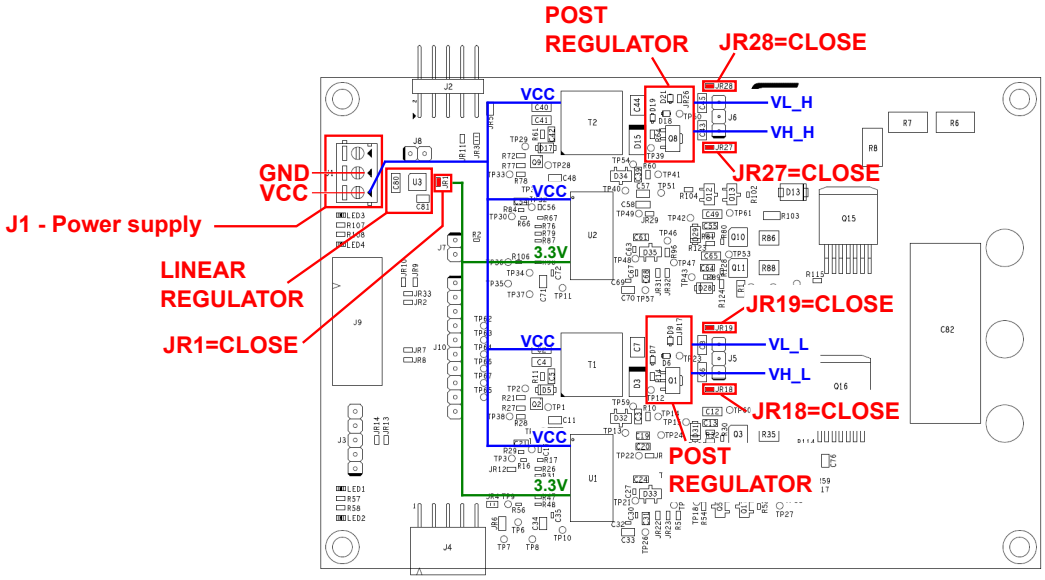
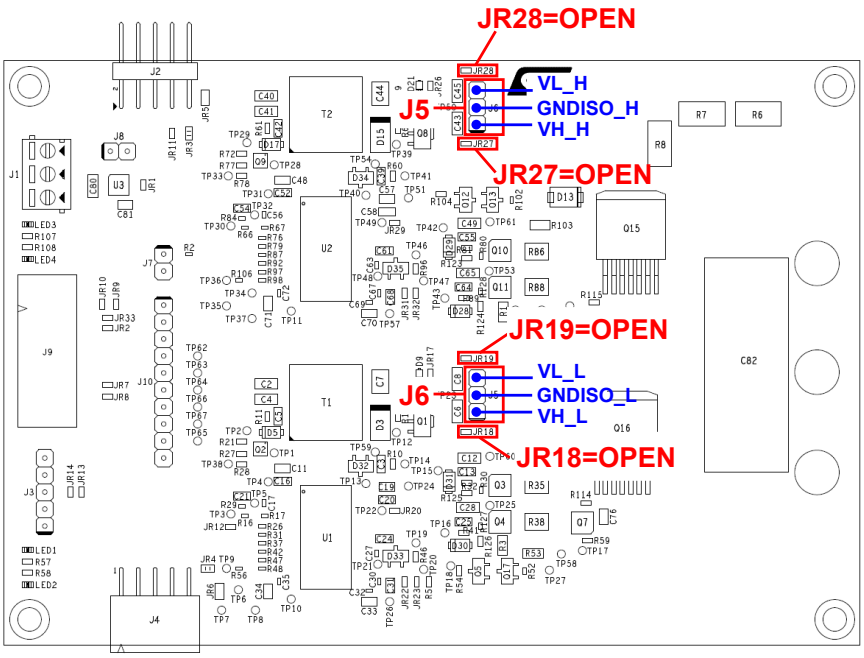


Figure 12. VH, VL fed by external power supply



7 EVALSTGAP4S schematic diagram

Figure 13. **EVALSTGAP4S schematic diagram - connectors**

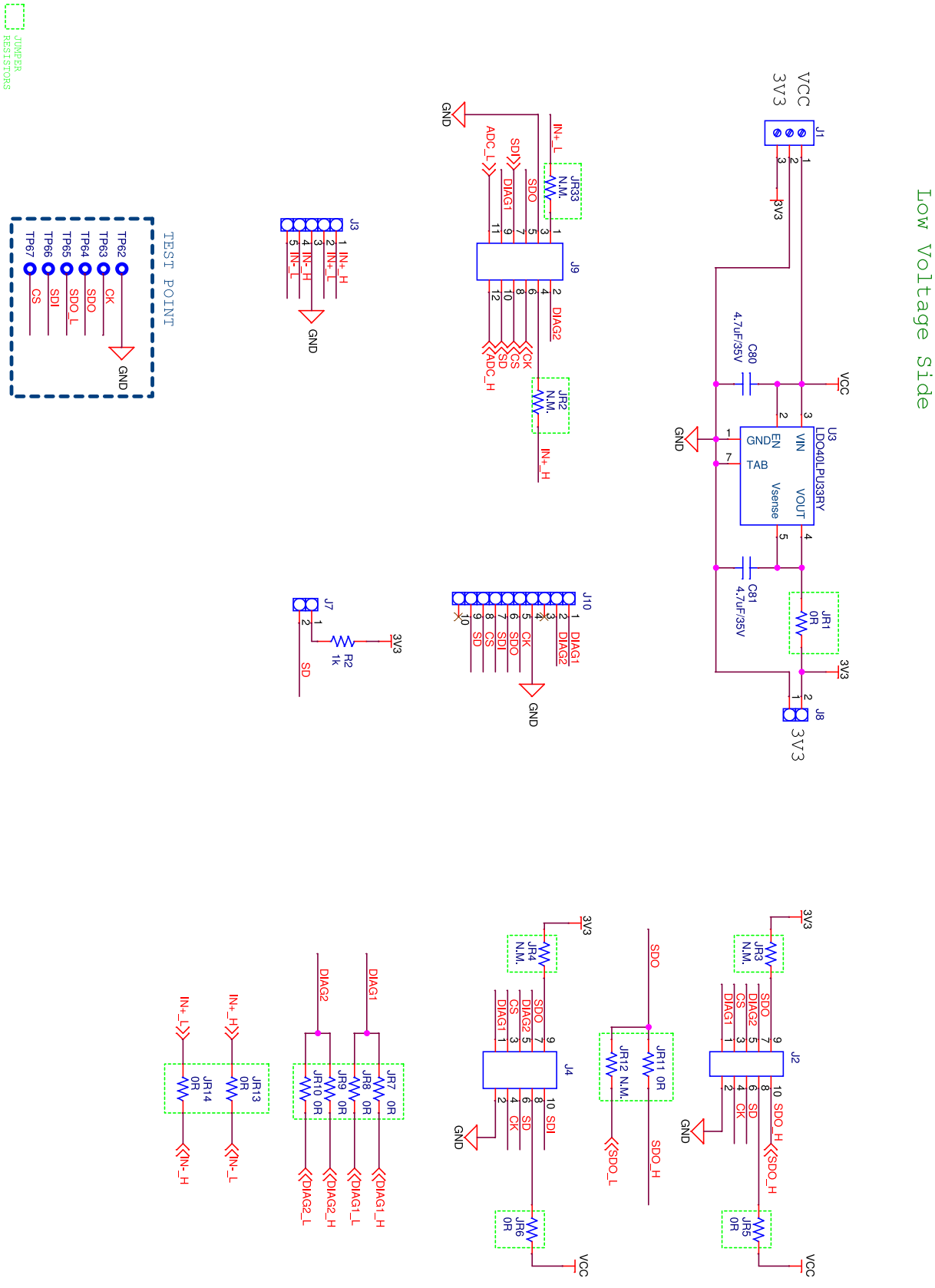


Figure 14. **EVALSTGAP4S schematic diagram - low-side**

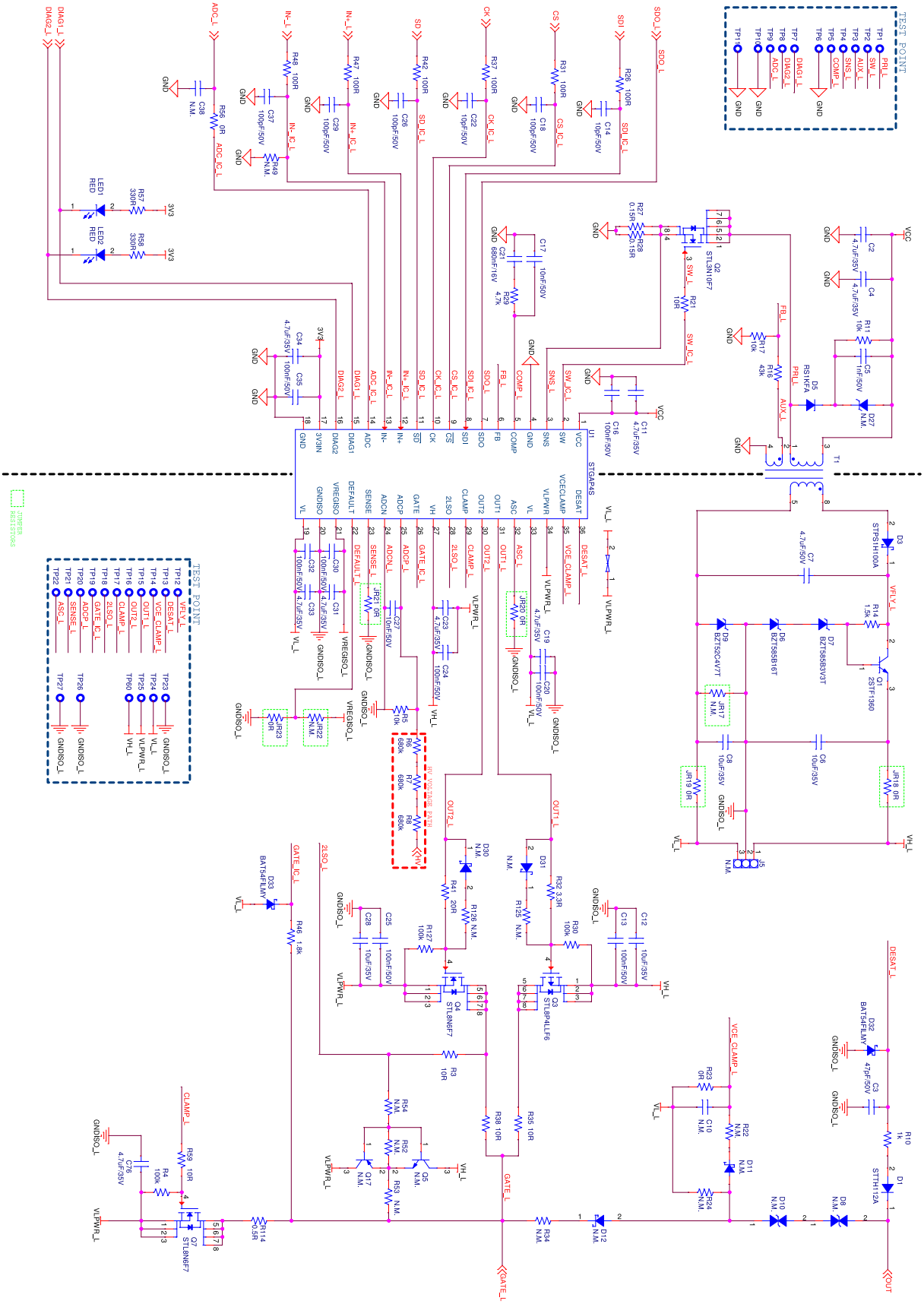


Figure 15. **EVALSTGAP4S schematic diagram - high-side**

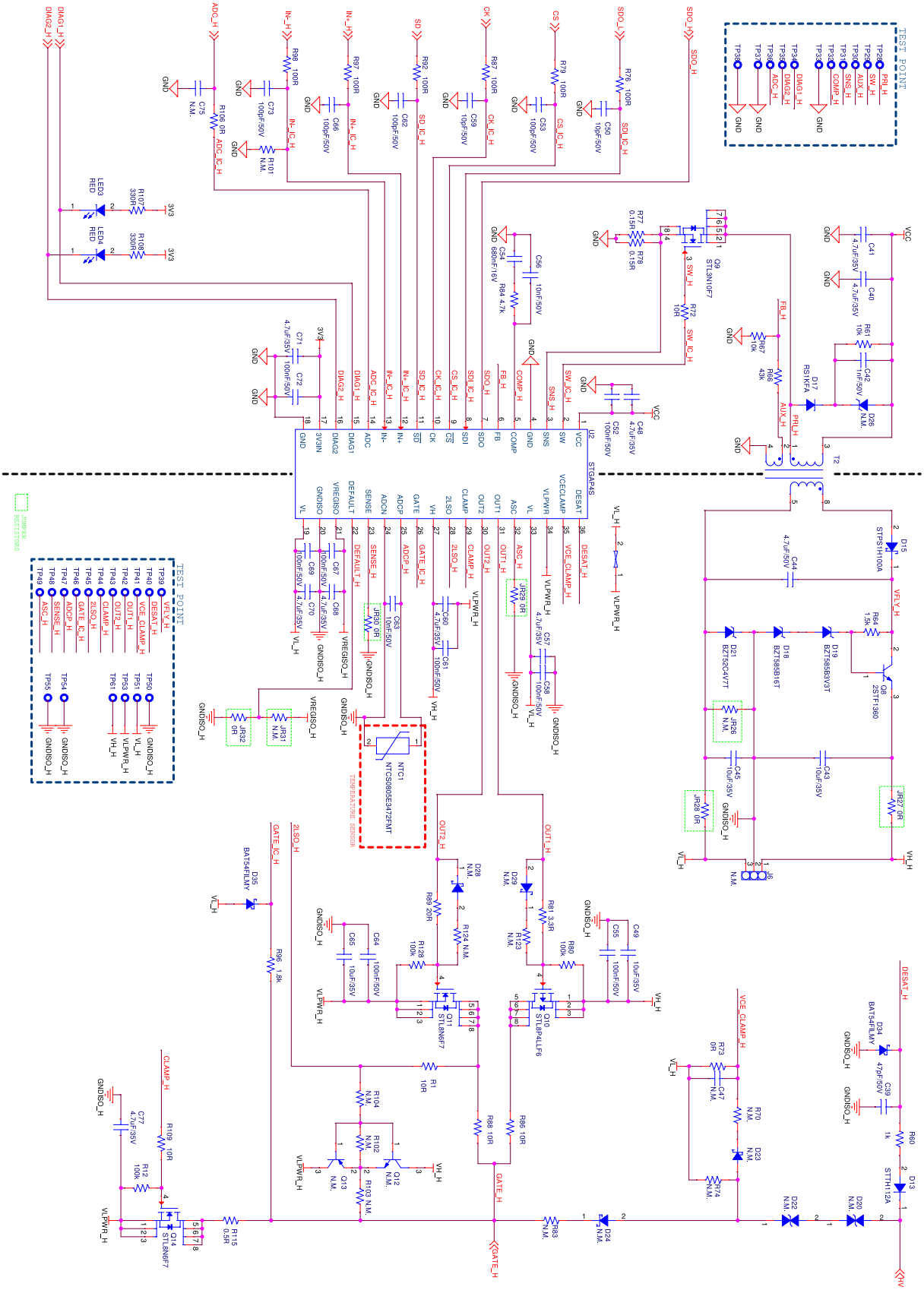
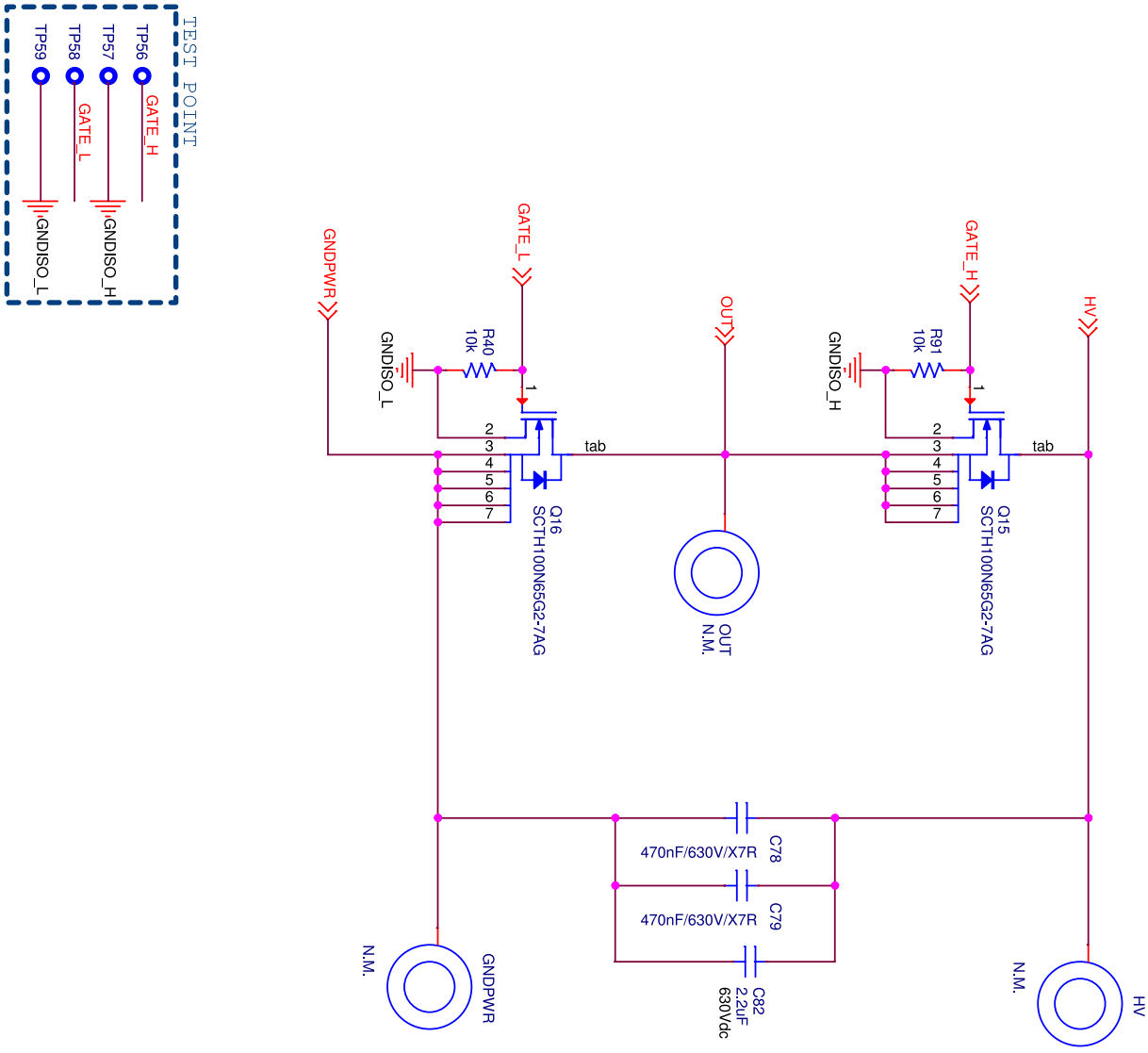


Figure 16. **EVALSTGAP4S schematic diagram - power stage**



Revision history

Table 18. **Document revision history**

Date	Version	Changes
24-May-2023	1	Initial release.
20-Nov-2023	2	Updated Figure 13, Figure 14, Figure 15, Figure 16.

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