
OTP programming for STi²Fuse devices

Introduction

OTP (one-time programmable) is a type of non-volatile memory that can be programmed only once and cannot be modified later. This means that once a '1' has been written into the OTP memory, it cannot be erased.

In an integrated circuit, data is usually processed by a series of functional blocks, each of which has one or more inputs and one or more outputs. With customer programmable bits technology through OTP, it is possible to program the OTP memory to customize some features.

This approach offers several advantages to the end customer: possibility to use the same device in different configurations, reduce the number of microcontroller I/Os dedicated to parallel commands, define an appropriate strategy for fail safe operation, or define some specific feature options. Furthermore, it reduces the number of functional blocks required to process data, simplifying the design of the integrated circuit, and reducing power consumption.

OTP programming mode can be entered with the device in fail safe or normal mode operating state. In case of normal mode state the watchdog must be toggled during OTP programming. The RAM registers maintain their contents during OTP mode and we suggest no write operations apart from OTP sequences messages.



1 Monolithic devices

Monolithic devices single die dual (VNF9D5F, VNF9D5SF) and quad (VNF9Q20F, VNF9Q20SF).

OTP (one-time programmable) bits are automatically read after transitioning from STANDBY mode to FAILSAFE mode.

Customer may program OTP bits to set:

- Direct input pins association (see direct input logic)
- MCUext functionality (see direct input logic)
- I²t parameters (see nominal time and nominal current)
- Parallel mode (see parallel mode)
- Ilim latch (see overload section)
- Lock

The following table shows the detailed structure of the 8-bit OTP rows programmable by the user for four channels:

Table 1. Programmable OTP by user for quad channel efuse

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1000	Unused	OTP_ILIM_LATCH (3:0)				Parallel	NOT_MCUe xt	Lock
1001	DIOTP0(1:0)		INOM0(2:0)			TNOM0(2:0)		
1010	DIOTP1(1:0)		INOM1(2:0)			TNOM1(2:0)		
1011	DIOTP2(1:0)		INOM2(2:0)			TNOM2(2:0)		
1100	DIOTP3(1:0)		INOM3(2:0)			TNOM3(2:0)		

1.1 OTP programming procedure description

OTP programming mode can be entered by using the following dedicated procedure.

The OTP programming procedure consists of the following five steps:

1. Enter the OTP programming mode.
2. Emulate configurations: to try different OTP settings.
This step is optional and the effect of the emulation is reversible and temporary. The effect can be observed in the involved modified features but it is not possible to double check in the affected control registers.
3. Perform the OTP write content (burn): to permanently program OTP default settings.
4. Perform the read back operation: to check the correct writing operation.
This step allows a “read-margin” mode to double check the performed programmed sequence. This reading option is specifically done in OTP mode and is more sensitive than standard reading mode. The effect of burn can also be done by standard reading of the content of affected control register after OTP exit followed by a software reset or a V_{bat} removal/supply cycle to allow a new loading after transitioning from STANDBY mode to FAILSAFE mode.
5. Exit from the OTP programming mode.

Description of each OTP programming step:
1. Enter the OTP programming mode:

- The battery voltage (V_{CC}) can be set to 13 V or in a value inside the operative range 4–28V. We suggest choosing a value in the range 15–21 V in order to maintain it during writing operations.
- Apply a voltage of 5 V on STDBY_NOT pin or (CSN low and $V_{DD} > V_{DD_TH}$) to wake up the device in case the OTP programming will be done in fail safe mode respecting tstdby_out_CSN and waiting the time needed for V_{reg} capacitor charge before start the SPI frame exchange.
The OTP programming can also be executed on the device in normal mode then wake up could be done through proper SPI sequence commands on CTRL register including UNLOCK = 1 followed by EN = 1 and GOSTBY = 0.
- Perform the following two dedicated SPI communications:

Table 2. SPI communication

1 st SPI frame		2 nd SPI frame	
Address	Content	Address	Content
39h	F5AEh	39h	0A51h

2. Emulate configurations to try different OTP settings:

- Send a WRITE command to address 3Dh:
 - Write (3Dh, 3000h)
- Send a write command to the address 3Eh:
 - Write (000 + Row_Address + + 8 bits to simulate + parity)
- Apply a 2 μ s pulse on the SDI pin to trigger the write operation in OTP. In case of SDI idle state is high, the procedure is working fine without toggling SDI.
What is needed to validate OTP operations is a detection of high state on SDI once CSN has been released to its idle state (high on these ST products) at the end of the communication, so:
 - In case of SDI idle state is low → it is mandatory to toggle SDI high for at least 2 μ s with CSN high.
 - In case of SDI idle state is high → it is not needed to toggle SDI.
For other SPI pins, we have SCK idle state low and SDO will be in HiZ when out of communication (when CSN high).

Note: If VREG pin voltage falls below the NPOR threshold, any emulated configuration is lost.

3. Perform the OTP write content (burn) to permanently program OTPs:

- Increase the battery voltage V_{CC} (depending on adopted initial value) to programming voltage that must be greater than or equal to 15 V (minimum value needed to perform the writing operation in a stable and reliable way). Burn operation was built to work at $V_{CC} = 20$ V, but this voltage value can be reduced down to 15 V as visible in the [Figure 2](#).
- Enable OTP write operation with the following dedicated SPI frame in the 3Dh register:
 - Write (3Dh, 4001h).
- Send a WRITE command to address 3Eh:
 - Write ('000' + Row_Address + 8 bits to burn + parity)
- Apply a 2 μ s pulse on the SDI pin to trigger the write operation in OTP and wait 500 μ s per trimmed bit (for example: in case of two bits put at '1', it is needed to wait 1 ms for the next operation. In case of "n" bits to burn the procedure requires to wait "n" times 500 μ s after SDI pulse to allow the internal logic to manage the successive trimming of the "n" bits put at "1".
 - Repeat the programming procedure for the minimum number of SDI pulses specified from the chosen V_{CC} programming voltage (see the [Figure 2](#)).

4. Perform read back from dedicated register to check the correct writing operation:

This operation checks the correct writing operation for all channels,

- Send a WRITE command to address 3Dh:
 - Write (3Dh, 3801h).
- Send a WRITE command to address 3Eh:
 - Write ('010' + Row_Address + '00000000' + parity).
- Apply a 2 μ s pulse on the SDI pin to trigger the margin read operation in OTP.
- Send a READ command to a specified read back register that for dual and quad monolithic devices is 31h where the read bits from 4 to 11 correspond to the content of selected OTP raw in this specific test mode. 31h address has a specific content when the device is in normal mode and in addition it reports the OTP content only when the device is in OTP mode.
For example if you want to check the Efuse parameters for channel 4, the row to be chosen is 1100 and the frames to be sent are:
 - 3D3801h;
 - Then 3E5801h (00111110 010+1100+00000000 + parity);
 - Then SDI pulse;
 - Then read register 31h (bit 4 to 11 representing the content of OTP raw 1100) sending the frame 710001h = 01110001. On SDO the bit from 4 to 11 will correspond to the bit from 0 to 7 of row 1100 while all other bits are "don't care".

5. Exit from OTP assignment mode:

- Perform the dedicated SPI communication at the specified address 39h:

Table 3. SPI frame

SPI frame	
Address	Content
39h	BAC0h

Note: Once OTP programming is finished, the customer may write a lock bit (burning the corresponding OTP) to disable any further future writings on not yet programmed OTP (already burnt OTP may not be recovered).

1.2 OTP customer programming mode

OTP customer programming detailed instructions (example for VNF9Q20F).

Table 4. OTP customer instruction for VNF9Q20F

Test name	OTP simulation	OTP read	OTP write
GND	ground	ground	Ground
VCC	13 V	13 V	Chosen programming voltage
VDD	5 V	5 V	5 V
VREG	1 μ F	1 μ F	1 μ F
STDBY_NOT	5 V	5 V	5 V
DI0	x	x	x
DI1	x	x	x
CSN	SPI communication	SPI communication	SPI communication
SCK	SPI communication	SPI communication	SPI communication
SDI	SPI communication for test mode or pulse from tester for OTP simulation trigger	SPI communication for test mode or pulse from tester for OTP margin read trigger	SPI communication for test mode or pulse from tester for OTP write trigger
PWM_CLK	x	x	x

Test name	OTP simulation	OTP read	OTP write
SDO	SPI communication	SPI communication	SPI communication
OUT0	x	x	x
OUT1	x	x	x
OUT2	x	x	x
OUT3	x	x	x
Code	0011000000000000 (WRITE 3DH, 3000h)	0011100000000001 (WRITE 3DH, 3801H)	0100000000000001 (WRITE 3DH, 4001H)
Data	000 + Row_Address + +8 bits to simulate + parity	010 + Row_Address + + 00000000 + parity	000 + Row_Address + + 8 bits to burn + parity
Details	Step 1: to enter customer programming mode Step 2: enter specific test mode (3Dh) Step 3: write in register 3Eh the OTP address Step 4: apply a pulse on SDI (2 μs min)	Step 1: to enter customer programming mode Step 2: enter specific test mode (3Dh) Step 3: write in register 3Eh the OTP address Step 4: apply a pulse on SDI (2 μs min) Step 5: to read the 8-bits OTP data in register 31h (bits from 11 to 4: these infos are visible on register 31h only when the device is in OTP mode)	Step 1: to enter customer programming mode Step 2: enter specific test mode (3Dh) Step 3: write in register 3Eh the OTP address Step 4: apply a pulse on SDI (2 μs min)

2 System in package devices (hybrid)

System in package devices hybrid VNF9D1M5Q, VNF9D3Q, VNF9D1M2Q.

OTP bit contents are automatically downloaded to some internal registers when a transition from STANDBY mode to FAILSAFE mode occurs (30 μ s after a power on reset event). Some fields of the RAM registers are initialized to the content of these shadow registers.

OTP management includes three possible operations:

- **OTP read:** allows reading the content of a row of the OTP macrocells in different modes (margin mode, blank check, standard), refreshing corresponding “otp_data” registers and storing the read data in a dedicated register, readable by SPI (this dedicated read register is Reg 27h for VNF9D1M5Q that reports OTP content infos only when the device is in OTP mode while in normal mode it maintains its specific content as per specification document).
- **OTP write (or burn):** allows burning the antifuses connecting them to a high voltage supply.
- **OTP simulation:** allows emulating the effect of a write operation without physically burning the OTP antifuses but just overwriting the “otp_data” register for VNF9D1M5Q.

The following table shows an example of the detailed structure of the 8-bit OTP rows programmable by the user for VNF9D1M5Q:

Table 5. Programmable OTP by user for VNF9D1M5Q

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1000	INOM1_6x_10x	INOM0_6x_10x	TNOM0(2:0)		INOM0(2:0)			
1001	CAPCM1	CAPCM0	TNOM1(2:0)		INOM1(2:0)			
1010	INOM1_6x_10x (2 nd trial)	INOM0_6x_10x (2 nd trial)	TNOM0(2:0) (2 nd trial)		INOM0(2:0) (2 nd trial)			
1011	Reserved	SEL01	TNOM1(2:0) (2 nd trial)		INOM1(2:0) (2 nd trial)			

Legend:

- **INOMy(2:0):** the default value of the nominal current for I2t associated to the channel y.
- **TNOMy(2:0):** the default value of the nominal time for I2t associated to the channel y.
- **INOMy_6x_10x:** the default value of the option setting the level of digital Ipeak (1: 6 times INOM, 0: 10 times INOM) associated to channel y.
- **SEL01:** allows selecting two possible sets of OTP data for the I2t configuration OTPs (0: selects the first set of OTPs: INOMy, TNOMy, INOMy_6x_10x; 1: selects the second set of OTPs: INOMy (2nd trial), TNOMy (2nd trial), INOMy_6x_10x (2nd trial)).
- **CAPCMy:** the default value of the option setting the automatic start of the CCM (capacitive charge mode) after POR (1: enabled, 0: disabled) associated to the channel y.

2.1 OTP programming procedure description

OTP programming mode can be entered by using the following dedicated procedure to ensure a very high safety level for the stored configurations and to prevent unwanted changing.

OTP programming procedure consists of the following five steps:

1. Enter the OTP programming mode.
2. Emulate configurations: to try different OTP settings.
This step is optional and the effect of the emulation is reversible and temporary. The effect can be observed in the involved modified features but it is not possible to double check in the affected control registers.
3. Perform the OTP write content (burn): to permanently program OTP default settings.
4. Perform the read back operation: to check the correct writing operation.
This step allows a “read-margin” mode to double check the performed programmed sequence. The effect of burn can also be done by standard reading of the content of the affected control register after OTP exit followed by a software reset or a V_{bat} removal/supply cycle to allow a new loading after transitioning from STANDBY mode to FAILSAFE mode.
5. Exit from the OTP programming mode.

Description of each OTP programming step:

1. Enter the OTP programming mode:

- The battery voltage (V_{CC}) can be set to 13 V or in a value inside the operative range 4–28V. We suggest choosing a value in the range 15–21 V in order to maintain it during writing operations.
- Perform the following two dedicated SPI communications:

Table 6. SPI communication

1 st SPI frame		2 nd SPI frame	
Address	Content	Address	Content
39h	F5AEh	39h	0A51h

2. Emulate configurations to try different OTP settings:

- Send a WRITE command to address 3Dh:
 - Write (3Dh, BB99h).
- Send a WRITE command to address 3Eh:
 - Write ('000' + Row_Address + 8 bits to simulate + parity).
- Apply a 2 μ s pulse on the SDI pin to trigger the write operation in OTP. In case of SDI idle state is high, the procedure is working fine without toggling SDI.
What is needed to validate OTP operations is a detection of high state on SDI once CSN has been released to its idle state (high on these ST products) at the end of the communication, so:
 - In case of SDI idle state is low → it is mandatory to toggle SDI high for at least 2 μ s with CSN high.
 - In case of SDI idle state is high → it is not needed to toggle SDI.

For other SPI pins, we have SCK idle state low and SDO will be in HiZ when out of communication (when CSN high).

Note: If VREG pin voltage falls below the NPOR threshold, any emulated configuration is lost.

3. Perform the OTP write content (burn) to permanently program OTP:

- Increase the battery voltage V_{CC} (depending on adopted initial value) to programming voltage that must be greater than or equal to 15 V (minimum value needed to perform the writing operation in a stable and reliable way). Burn operation was built to work at $V_{CC} = 20$ V, but this voltage value can be reduced down to 15 V as visible in the [Figure 2](#).
- Enable OTP write operation with the following dedicated SPI frame in the 3Dh register:
 - Write (3Dh, BB9Ch).
- Send a WRITE command to address 3Eh:
 - Write ('000' + Row_Address + 8 bits to burn + parity).
- Apply a 2 μ s pulse on the SDI pin to trigger the write operation in OTP and wait 500 μ s per trimmed bit (for example: in case of two bits put at '1', it is needed to wait 1 ms for the next operation). In case of "n" bits to burn the procedure requires to wait "n" times 500 μ s after SDI pulse to allow the internal logic to manage the successive trimming of the "n" bits put at "1".
 - Repeat the programming procedure for the minimum number of SDI pulses specified from the chosen V_{CC} programming voltage.

4. Perform read back from dedicated register to check the correct writing operation:

This operation checks the correct writing operation for all channels.

- Send a WRITE command to address 3Dh:
 - Write (3Dh, BB9Ah).
- Send a WRITE command to address 3Eh:
 - Write ('010' + Row_Address + 00000000 + parity).
- Apply a 2 μ s pulse on the SDI pin to trigger the write operation in OTP.
- Send a READ command to specified read back register at address 27h and read bits 4 to 11 for [VNF9D1M5Q](#).

5. Exit from OTP programming mode:

- Perform the dedicated SPI communication at the specified address 39h:

Table 7. SPI frame

SPI frame	
Address	Content
39h	BAC0h

Note: Once OTP programming is finished, the customer may write LOCK bit (burning the corresponding OTP) to disable any further future writings on not yet programmed OTP. (Already burnt OTP may not be recovered).

2.2 OTP customer programming mode

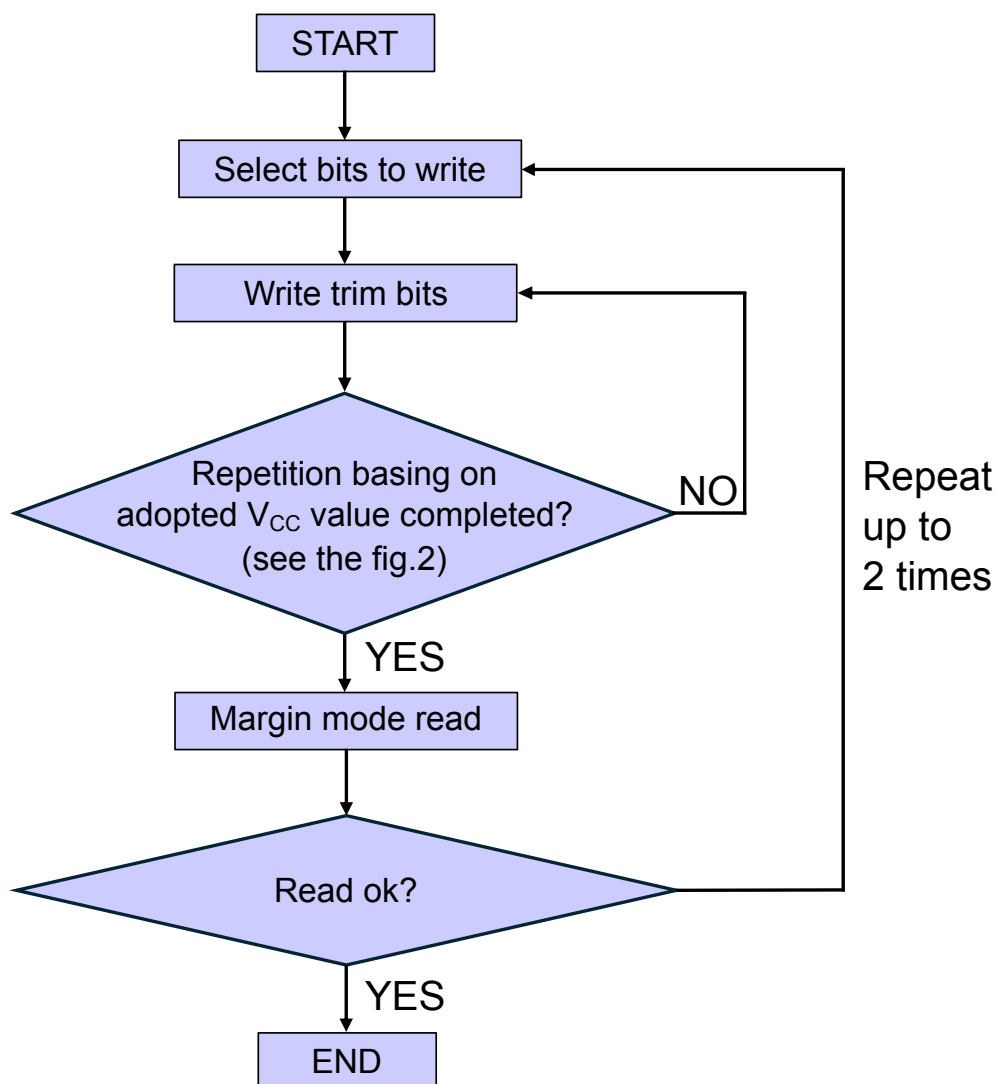
OTP customer programming detailed instructions (example for VNF9D1M5Q):

Table 8. OTP customer instruction for VNF9D1M5Q

Test name	OTP simulation	OTP read	OTP write
GND	Ground	Ground	Ground
VCC	13 V	13 V	Selected programming voltage
VDD	5 V	5 V	5 V
VREG	-	-	-
DI0	-	-	-
DI1	-	-	-
CSN	SPI communication for test mode	SPI communication for test mode	SPI communication for test mode
SCK	SPI communication for test mode	SPI communication for test mode	SPI communication for test mode
SDI	SPI communication for test mode or pulse from tester for OTP simulation trigger	SPI communication for test mode or pulse from tester for OTP margin read trigger	SPI communication for test mode or pulse from tester for OTP write trigger
SDO	-	-	-
OUT0	X	X	X
OUT1	X	X	X
Test code 3Dh	1011101110011001 (WRITE 3DH, BB99H)	1011101110011010 (WRITE 3DH, BB9AH)	1011101110011100 (WRITE 3DH, BB9CH)
Test data 3Eh	000 + Row_Address + 8 bits to simulate	010 + Row_Address + 00000000	000 + Row_Address + 8 bits to burn
Test details	Step 1: to enter customer programming mode Step 2: to enter OTP simulation test code (3Dh) Step 3: to write in register 3Eh the OTP row address + the 8 bits data to be emulated on the specified row Step 4: to apply a pulse on SDI (2 µs)	Step 1: to enter customer programming mode Step 2: to enter OTP read test code (3Dh) Step 3: to write in register 3Eh the OTP row address Step 4: to apply a pulse on SDI (2 µs) Step 5: to read the 8 bits of selected OTP raw data in register 27h (bits from 11 to 4. These infos are visible on register 27h only when the device is in OTP mode)	Step 1: to enter customer programming mode Step 2: to enter OTP write test code (3Dh) Step 3: to write in register 3Eh the OTP row address + the 8 bits data to be burned on the specified row Step 4: to apply a pulse on SDI (2 µs)

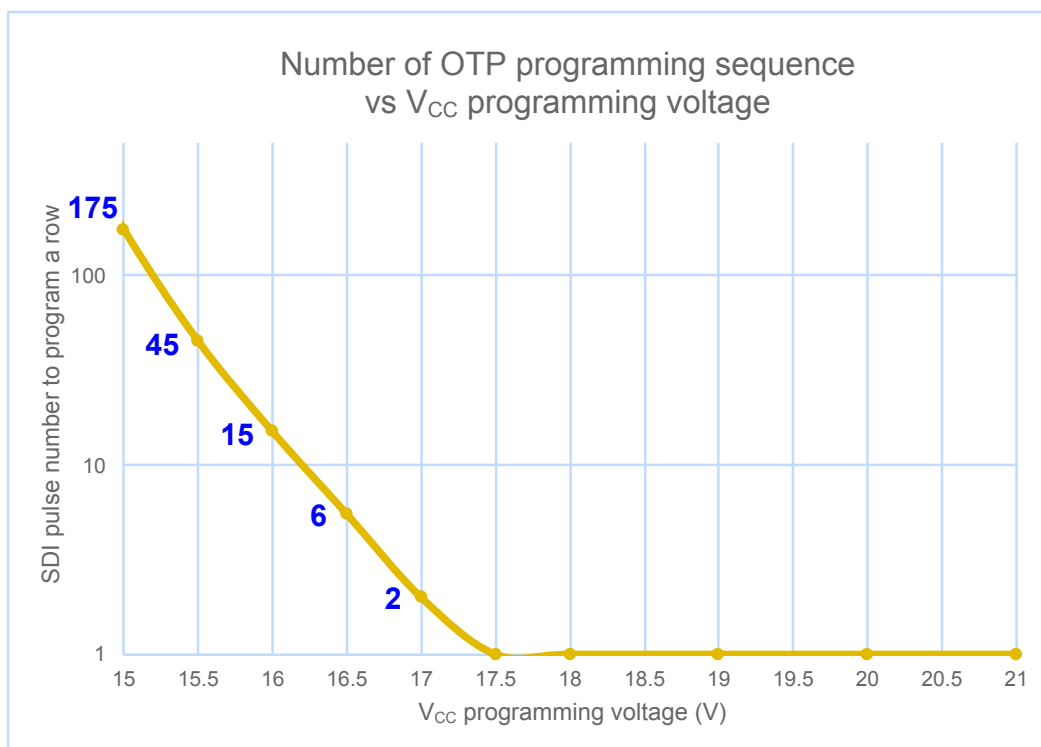
3 OTP write flow chart

Figure 1. Flow chart



For V_{bat} values greater than or equal to 17.5 V the burn is effective after one sequence execution. Permanent burn can be also produced by cumulative effect depending on the time in which the high voltage is applied. The reduction of V_{bat} value will involve longer time corresponding to number of repetitions of write sequence to burn the selected bit.

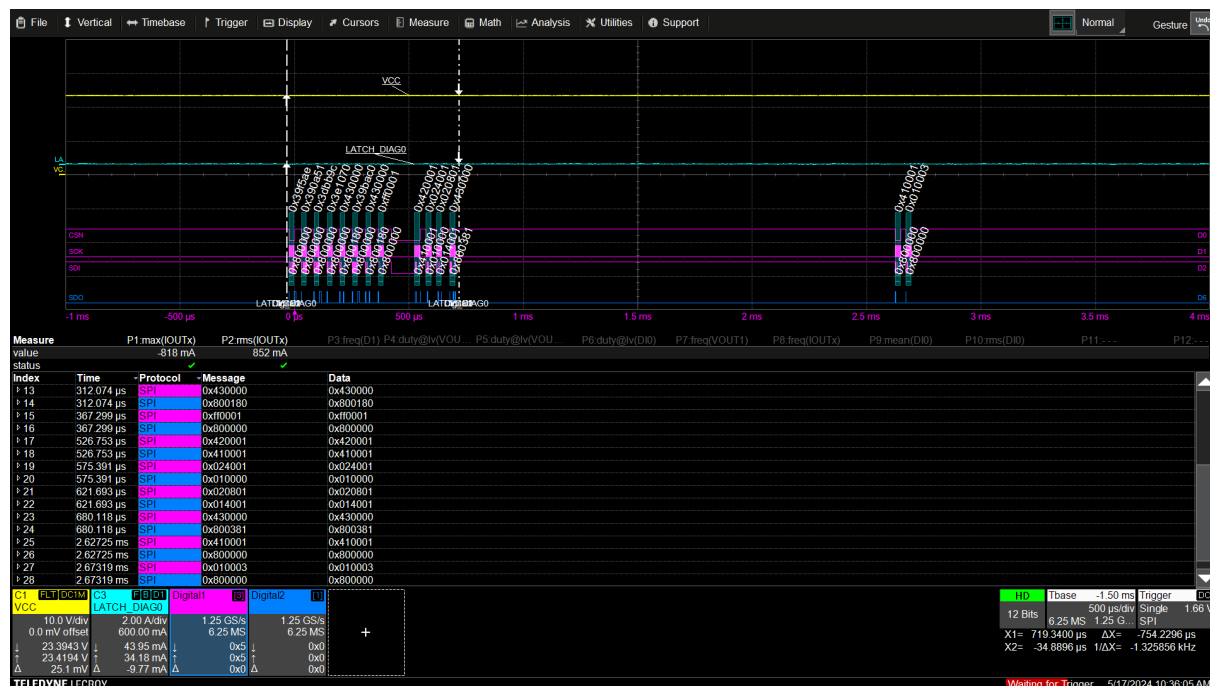
Figure 2. Number of programming sequence vs V_{CC} programming voltage



4 Real case example of OTP burn on VNF9D1M5Q

The Figure 3 reports the frames exchanged during the OTP burn on a VNF9D1M5Q in normal mode. The same result is achieved if the sequence is exchanged with device in fail safe.

Figure 3. Frames exchanged on VNF9D1M5Q to burn OTP related to bit 3 of address 1000_b (TNOM00)



In this case the operation is done with $V_{bat} = 23$ V. Our GUI uses SDI idle state high, SCK idle state low and SDO low when out of communication with CSN at high value.

Here below the detailed adopted sequence with related comment are listed.

Table 9. Frames exchanged on VNF9D1M5Q to burn OTP related to bit 3 of address 1000_b (TNOM00)

Message on SDI (frame number in the Figure 3)	Comment	Message on SDO (frame number in the Figure 3)	Comment
0x39F5AE (1)	1 st frame to enter in OTP mode	0x800000 (2)	Device in normal mode
0x390A51 (3)	2 nd frame to enter in OTP mode	0x800000 (4)	Device in normal mode
0x3DDB9C (5)	Frame to enable OTP write operation	0x800000 (6)	Device in normal mode
0x3E1070 (7)	Frame to write OTP bit3 related to TNOM0 at address 1000 (bit 5 and 4 were previously burn)	0x800000 (8)	Device in normal mode
0x430000 (9)	Frame to read address 03h corresponding to ITCFGCR0 to check the TNOMSR20 (bit9), TNOMSR10 (bit8) and TNOMSR00 (bit7)	0x800180 (10)	Device in normal mode with: TNOMSR20=1, TNOMSR10 = 1 and TNOMSR00 = 0
0x39BAC0 (11)	Frame to exit from OTP mode	0x800000 (12)	Device in normal mode

Message on SDI (frame number in the Figure 3)	Comment	Message on SDO (frame number in the Figure 3)	Comment
0x430000 (13)	New reading of CR 03h corresponding to ITCFGCR0 to check the TNOMSR20, TNOMSR10 and TNOMSR00	0x800180 (14)	Device in normal mode with: TNOMSR20 = 1, TNOMSR10 = 1 and TNOMSR00 = 0 The burn of TNOMSR00 bit is not visible
0xFF0001 (15)	Frame to give a software reset	0x800000 (16)	Device in normal mode
0x420001 (17)	Frame to read CR 02h corresponding to CTRL	0x410001 (18)	GSB points out RST and FS flags
0x024001 (19)	1 st frame on 02h to move from fail safe to normal mode with UNLOCK = 1	0x010000 (20)	Device in fail safe
0x020801 (21)	2 nd frame on 02h to move from fail safe to normal mode with GOSTBY = 0 and EN = 1	0x140001 (22)	Device in fail safe
0x430000 (23)	New reading of CR 03h corresponding to ITCFGCR0 to check the TNOMSR20 (bit9), TNOMSR10 (bit8) and TNOMSR00 (bit7)	0x800381 (24)	Device in normal mode with: TNOMSR20 = 1, TNOMSR10 = 1 and TNOMSR00 = 1 The burn of TNOMSR00 bit is visible
0x410001 (25)	Frame to read CR 01h corresponding to SOCR	0x800000 (26)	Device in normal mode
0x010003 (27)	Frame to write CR 01h to toggle WDTB bit	0x800000 (28)	Device in normal mode

Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Feb-2024	1	Initial release.
02-Sep-2024	2	Update including additional details on OTP sequence and real case example.
16-Mar-2026	3	Minor changes.
10-Jun-2026	4	Added web links of the st.com pages for the mentioned products .

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