UM3365

User manual

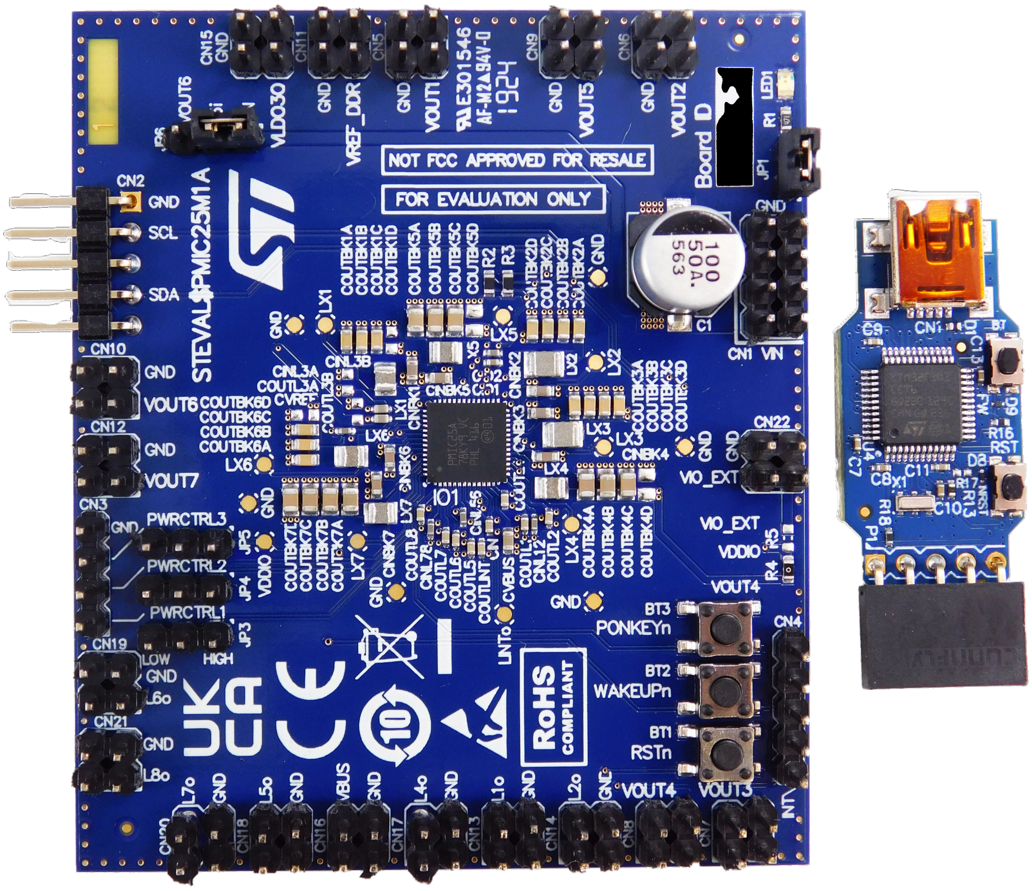
# User manual for STEVAL-PMIC25V1 based on STPMIC25A

## Introduction

This user manual provides detailed instructions for configuring and utilizing the STEVAL-PMIC25V1 kit. The kit includes the following components:

1. STEVAL-PMIC25M1 evaluation board: designed specifically for the STPMIC25A.
2. STEVAL-USBDNGV1 USB dongle: utilized for programming the STPMIC25 via the I$^2$C bus protocol, in conjunction with the STSW-PMIC25GUI software.

**Figure 1. STEVAL-PMIC25V1 kit**

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# 1 STPMIC25 overview

The STPMIC25 is a fully integrated power management IC designed for STM32MP25x lines MPU applications requiring low power and high efficiency.

The device integrates advanced low-power features controlled by a host processor via I²C and I/O interfaces.

The STPMIC25 regulators are designed to supply power to the application processor as well as to the external system peripherals such as: DDR, flash memories and other system devices.

Seven buck SMPS are optimized to provide an excellent transient response and an output voltage precision for a wide range of operating conditions. Very high efficiency in the full output load range is achieved thanks to low power (LPM) and high power (HPM) modes selection.

All the buck converters are provided with a smooth transition from LPM to HPM. Advanced PWM phase shift synchronization technique with integrated PLL (low noise and reduced EMI).

The main features of the STPMIC25 are:

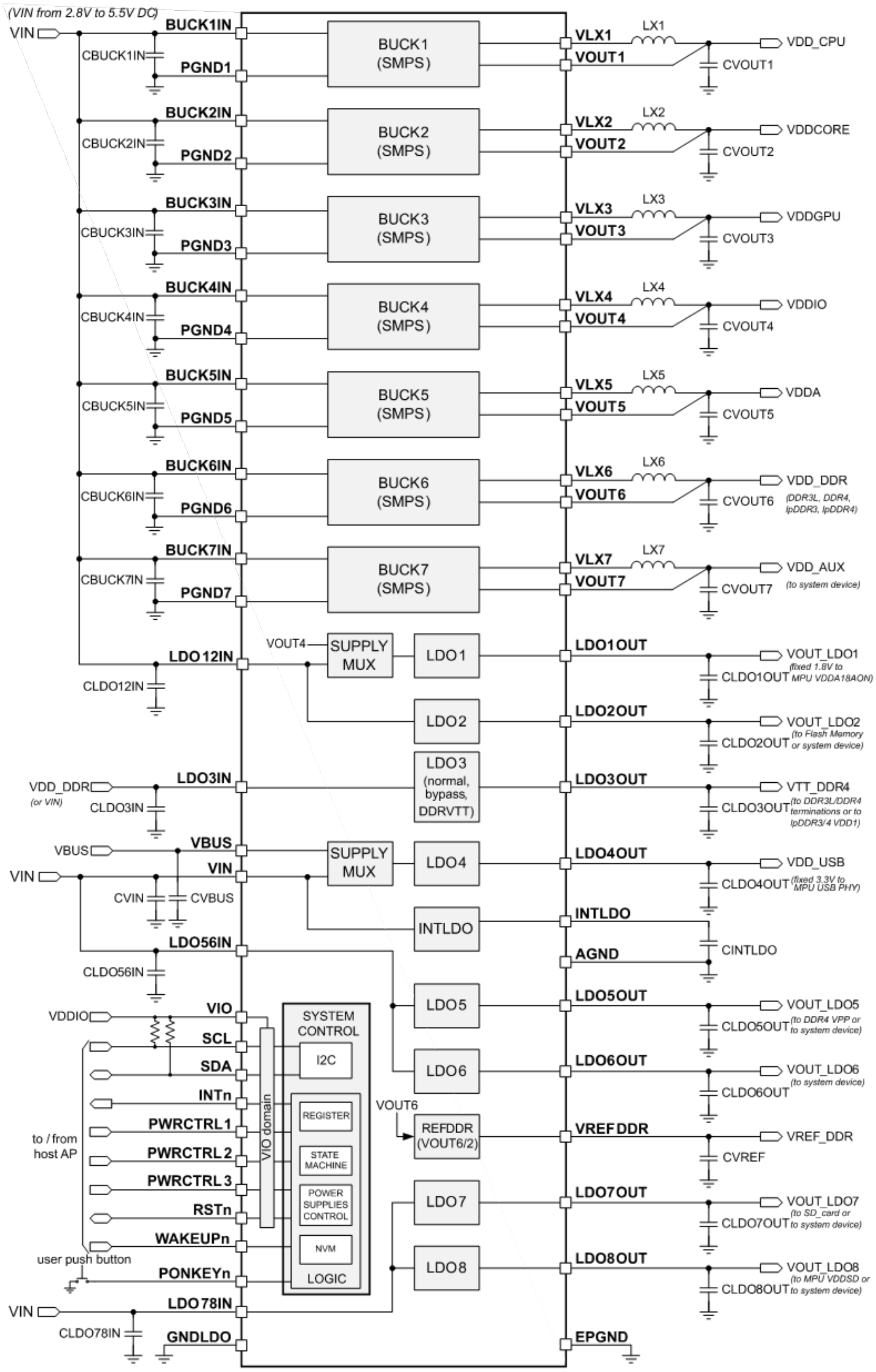
- Input voltage range is from 2.8 V to 5.5 V
- 7 Buck converters with adaptive constant on-time (COT) topology
- 2 MHz switching frequency
- Selectable forced PWM
- Spread spectrum function
- Phase shift synchronization
- 6 adjustable general-purpose LDOs
- 1 LDO configurable as:
  - Sink-source mode for DDR4 termination
  - Bypass mode for lpDDR
  - Adjustable output (normal mode) for general-purpose use
- 1 LDO for USB PHY supply with automatic power source detection
- 1 reference voltage LDO for DDR memory
- User programmable nonvolatile memory (NVM), enabling scalability to support a wide range of applications.
- Immediate output alternate settings toggle by dedicated power control pins
- Programmable output voltages turn ON/OFF sequences.
- I²C and digital I/O control interface
- Advanced customizable safety managements
- WFQFN 56 L package (6.5x6.5x0.9 mm)

Typical applications of the STPMIC25 are:

- Power management for embedded microprocessor units
- Wearable and IoT
- Portable devices
- Man-machine interfaces
- Smart home
- Power management unit companion chip of the STM32MP2 MPUs family

A typical application schematic of STPMIC25 is shown in the below figure:

**Figure 2. STPMIC25 typical application schematic**



The STPMIC25 features a large input voltage range from 2.8 V to 5.5 V to supply:

- 5 V DC wall-adaptor applications
- 1-cell 3.6 V Li-Ion / LiPo battery applications
- 5 V USB port (bus-powered) applications

The STPMIC25 provides all regulators needed to power supply a complete application:

- 8 LDOs + 1 reference voltage LDO for DDR memories
- 7 step-down (buck) converters

Table 1 shows a general description of each regulator and the typical application use (in STM32MP25x lines MPU application):

**Table 1. General description of STPMIC25 regulators**

| Regulator | Output voltage (V) | Programming step (mV) | Rated output current (mA) | Application use |
|---|---|---|---|---|
| LDO1 | 1.8 | - | 20 | VDDA18AON |
| LDO2, LDO5, LDO6, LDO7 | 0.9 V - 4.0<br>bypass mode | 100 | 400 / 200 / 100 / 50 | General purpose<br>(eMMC, DDR4 VPP, SD card, LCD camera…) |
| LDO8 | 0.9 - 4.0<br>bypass mode | 100 | 150 | General purpose<br>(Low voltage peripheral) |
| LDO3<br>normal mode | 0.9 V - 4.0 | 100 | 120 | General purpose / lpDDR VDD1 |
| LDO3<br>sink-source mode | VREFDDR | - | +/-120 (rms)<br>+/-230 (peak) | DDR3L/DDR4 terminations (VTT) |
| LDO3<br>bypass mode | 1.8 V | - | 80 | lpDDR VDD1 |
| LDO4 | 3.3 | - | 40 | VDD33USB<br>VDD33UCPD |
| VREFDDR | VOUT6 / 2 | - | +/-5 (rms)<br>+/-10 (peak) | DDR3L, DDR4, lpDDR3, VREF,<br>DDR_VREF |
| BUCK1, BUCK6 | 0.5 - 1.5 | 10 | 2000, 1500, 1000,<br>500 | Buck1 = VDDCPU Buck6 = VDDQ<br>(DDR3L, DDR4, lpDDR3, lpDDR4) |
| BUCK2, BUCK3 | 0.5 - 1.5 | 10 | 2000, 1500, 1000,<br>500 | Buck2 = VDDCORE<br>Buck3 = VDDGPU |
| BUCK4, BUCK5 | 1.5 - 4.2 | 100 | 500, 250 | Buck4 = VDD (VDDIO)<br>Buck5 = VDDA18x |
| BUCK7 | 1.5 - 4.2 | 100 | 2500, 2000, 1500,<br>1000 | General purpose |

*Note:*

- *VIN is the main STPMIC25 supply. All Buck converters and linear regulators have dedicated or shared power supply pins.*
- *A dedicated VIO supply is for all digital interface pins.*
- *Except for VBUS, no other supplies voltage must be applied before VIN or set higher than VIN.*

# 2 STPMIC25 NVM settings

The STPMIC25 has a non-volatile memory (NVM) that can be (re)programmed via $I^2C$ directly in target applications to facilitate mass production, enabling scalability to support a wide range of applications. The main settings of STPMIC25 are stored in the NVM memory:

- VIN voltage threshold
- Auto turn-on feature
- Default $I^2C$ slave device address
- Regulators default output voltages at startup
- Regulators Power-up sequence at startup (rank)
- Safety management (behavior in case of failure) → overcurrent protection, over temperature protection, VIN_low, watchdog and ponkey fault counters
- Possibility to lock the NVM content to prevent further re-programming by writing the LOCK_NVM bit
- Other features (see the STPMIC25 datasheet DS14278 for further details)

The STPMIC25A, STPMIC25B and STPMIC25D are the three standard NVM configuration to support the STM32MP25x lines MPU application versions, in particular:

- STPMIC25A version:
  - Typical use case: 5V continuous input voltage (wall adaptor) applications
  - VDDIO @ 3.3V (BUCK4 output)
  - Minimum set of regulators enabled by default
- STPMIC25B version:
  - Typical use case: Li-Ion/Li-PO single cell battery applications
  - VDDIO @ 1.8V (BUCK4 output)
  - Minimum set of regulators enabled by default
- STPMIC25D version:
  - Typical use case: 5V continuous input voltage (wall adaptor) applications
  - VDDIO @ 3.3V (BUCK4 output)
  - Minimum set of regulators enabled by default (same as STPMIC25A but with LDO7 and LDO8 enabled in bypass mode for SD-Card UHS-I boot)

The main settings of STPMIC25A, STPMIC25B and STPMIC25D versions are listed in the table below:

**Table 2. Main settings of STPMIC25A, STPMIC25B and STPMIC25D**

| IP | STPMIC25A | | | | STPMIC25B | | | | STPMIC25D | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Voltage | Mode | Pull-down | Rank | Voltage | Mode | Pull-down | Rank | Voltage | Mode | Pull-down | Rank |
| **LDO1 (VDDA18AON)** | 1.8V | Bypass OFF | YES | 1 | 1.8V | Bypass OFF | YES | 1 | 1.8V | Bypass OFF | YES | 1 |
| **LDO2 (VDD_FLASH)** | 3.3V | Bypass OFF | YES | 4 | 2.9V | Bypass OFF | YES | 4 | 3.3V | Bypass OFF | YES | 4 |
| **LDO3 (VTT/VDD1_DDR)** | OFF | OFF | YES | 0 | OFF | OFF | YES | 0 | OFF | OFF | YES | 0 |
| **LDO4 (VDD33USB)** | 3.3V | Bypass OFF | YES | 5 | 3.3V | Bypass OFF | YES | 5 | 3.3V | Bypass OFF | YES | 5 |
| **LDO5 (GP LDO)** | OFF | OFF | YES | 0 | OFF | OFF | OFF | 0 | OFF | OFF | YES | 0 |
| **LDO6 (GP LDO)** | OFF | OFF | YES | 0 | OFF | OFF | OFF | 0 | OFF | OFF | YES | 0 |
| **LDO7 (GP LDO)** | OFF | OFF | YES | 0 | OFF | OFF | OFF | 0 | LDO7OUT=LDO78IN | Bypass ON | YES | 4 |
| **LDO8 (GP LDO)** | OFF | OFF | YES | 0 | OFF | OFF | OFF | 0 | LDO8OUT=LDO78IN | Bypass ON | YES | 4 |

| IP | STPMIC25A | | | | STPMIC25B | | | | STPMIC25D | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Voltag e | Mode | Pull-down | Rank | Voltag e | Mode | Pull-down | Rank | Voltage | Mode | Pull-down | Rank |
| **REFDDR (VREF_DDR)** | OFF | OFF | YES | 0 | OFF | OFF | OFF | 0 | OFF | OFF | YES | 0 |
| **BUCK1 (VDDCPU)** | 0.8V | HP | SLOW | 3 | 0.8V | HP | SLOW | 3 | 0.8V | HP | SLOW | 3 |
| **BUCK2 (VDDCORE)** | 0.82V | HP | SLOW | 2 | 0.82V | HP | SLOW | 2 | 0.82V | HP | SLOW | 2 |
| **BUCK3 (VDDGPU)** | OFF | OFF | SLOW | 0 | OFF | OFF | SLOW | 0 | OFF | OFF | SLOW | 0 |
| **BUCK4 (VDDIO)** | 3.3V | HP | SLOW | 1 | 1.8V | HP | SLOW | 1 | 3.3V | HP | SLOW | 1 |
| **BUCK5 (VDDA)** | 1.8V | HP | SLOW | 3 | 1.8V | HP | SLOW | 3 | 1.8V | HP | SLOW | 3 |
| **BUCK6 (VDD_DDR)** | OFF | OFF | FAST | 0 | OFF | OFF | FAST | 0 | OFF | OFF | FAST | 0 |
| **BUCK7 (Peripherals)** | 3.3V | HP | SLOW | 4 | OFF | OFF | SLOW | 0 | 3.3V | HP | SLOW | 4 |

The startup sequence of STPMIC25 is divided into four steps (Rank0 to Rank5).

Each BUCK converter or LDO regulator can be programmed to be automatically turned ON in one of these ranks. Each rank phase is separated by a delay, which is by default 1.5ms. This rank delay can be programmed in NVM (Reg0x91[7:6]) at 1.5ms, 3ms, 4.5ms or 6ms (RANK_DLY[1:0]).

- Rank=0: rail not turned ON automatically, no output voltage appears after POWER-UP sequence
- Rank=1: rail automatically turned ON after 7 ms (which is the fixed delay from VIN>VINOK_rise to the start of IPs with rank1), following a Turn_ON condition
- Rank=2: rail automatically turned ON after further 1.5ms compared to Rank1 output rails
- Rank=3: rail automatically turned ON after further 1.5ms compared to Rank2 output rails
- Rank=4: rail automatically turned ON after further 1.5ms compared to Rank3 output rails
- Rank=5: rail automatically turned ON after further 1.5ms compared to Rank4 output rails

Whatever the STPMIC25 version:

- AUTO_TURN_ON option is set

Table 3 shows the miscellaneous settings at startup of STPMIC25A, STPMIC25B and STPMIC25D:

**Table 3. Miscellaneous settings of STPMIC25A, STPMIC25B and STPMIC25D at startup**

| Parameter | STPMIC25A | STPMIC25B | SPMIC25D | Comments |
|---|---|---|---|---|
| VINOK_Rise | 4.0V | 3.3V | 4.0V | Default value of VIN_OK rising threshold |
| VINOK_HYST | 0.5V | 0.5V | 0.5V | Default VIN_OK hysteresis |
| AUTO_TURN_ON | ON | ON | ON | Auto turn-ON functionality enabled by default |
| RANK_DLY | 1.5ms | 1.5ms | 1.5ms | power-up/power-down step (RANK) duration time |
| RST_DLY | 0 | 0 | 0 | RESET release delay after POWER_UP sequence |
| I²C_ADDR | 0x33 | 0x33 | 0x33 | I²C device address |
| NVM_USERx | 0 | 0 | 0 | 2 free NVM bytes for user |

Table 4 shows the safety management settings at startup of STPMIC25A, STPMIC25B and STPMIC25D:

**Table 4. Safety management settings of STPMIC25A, STPMIC25B and STPMIC25D at startup**

| Parameter | STPMIC25A | STPMIC25B | STPMIC25D | Comments |
|---|---|---|---|---|
| NVM_WDG_EN | OFF | OFF | OFF | Watchdog is disabled by default |
| PKEY_LKP_OFF | ON | ON | ON | A long PONKEY key press produce a restart cycle of STPMIC25 |
| PKEY_LKP_FSLS | OFF | OFF | OFF | If PKEY_LKP_FSLS is disabled, the STPMIC25 will be stacked in fail-safe lock state until a VIN power OFF → ON cycle is done |
| PKEY_LKP_TMR | 10s | 10s | 10s | Long PONKEY key press time duration settings |
| HICCUP_DLY | 100ms | 100ms | 100ms | Hiccup mode OFF delay programmed by default |
| VIN_FLT_CNT_MAX | ∞ restart | ∞ restart | ∞ restart | VINOK fault counter |
| TSHDN_FLT_CNT_MAX | ∞ restart | ∞ restart | ∞ restart | Thermal shutdown protection fault counter |
| OCP_FLT_CNT_MAX | ∞ restart | ∞ restart | ∞ restart | Over current protection fault counter |
| WDG_FLT_CNT_MAX | ∞ restart | ∞ restart | ∞ restart | Watchdog fault counter |
| PKEY_FLT_CNT_MAX | ∞ restart | ∞ restart | ∞ restart | PONKEY fault counter |
| RST_FLT_CNT_TMR | 60m | 60m | 60m | Fault counter time reset |
| FAIL_SAFE_LOCK_DIS | Disabled | Disabled | Disabled | Fail-safe lock state is disabled by default |

Table 5 shows the Fail Safe/Hiccup regulator OCP settings at startup of STPMIC25A, STPMIC25B and STPMIC25D:

**Table 5. Fail Safe/Hiccup regulator OCP settings of STPMIC25A, STPMIC25B and STPMIC25D at startup**

| Parameter | STPMIC25A OCP mgt / OCP lim | STPMIC25B OCP mgt / OCP lim | STPMIC25D OCP mgt / OCP lim | Comments |
|---|---|---|---|---|
| **BUCK1 (VDDCPU)** | FS / 1A | FS / 1A | FS / 1A | STPMIC25 switch-off in case of OCP triggered |
| **BUCK2 (VDDCORE)** | FS / 2A | FS / 2A | FS / 2A | STPMIC25 switch-off in case of OCP triggered |
| **BUCK3 (VDDGPU)** | Hiccup / 2A | Hiccup / 2A | Hiccup / 2A | |
| **BUCK4 (VDDIO)** | FS / 0.5A | FS / 0.5A | FS / 0.5A | STPMIC25 switch-off in case of OCP triggered |
| **BUCK5 (VDDA)** | FS / 0.5A | FS / 0.5A | FS / 0.5A | STPMIC25 switch-off in case of OCP triggered |
| **BUCK6 (VDD_DDR)** | Hiccup / 1.5A | Hiccup / 1.5A | Hiccup / 1.5A | |
| **BUCK7 (Peripherals)** | Hiccup / 2.5A | Hiccup / 2.5A | Hiccup / 2.5A | |
| **LDO1 (VDDA18AON)** | FS | FS | FS | STPMIC25 switch-off in case of OCP triggered |
| **LDO2 (VDD_FLASH)** | Hiccup / 400mA | Hiccup / 400mA | Hiccup / 400mA | |
| **LDO3 (VTT/VDD1_DDR)** | Hiccup | Hiccup | Hiccup | |
| **LDO4 (VDD33USB)** | Hiccup | Hiccup | Hiccup | |
| **LDO5 (GP LDO)** | Hiccup / 400mA | Hiccup / 400mA | Hiccup / 400mA | |
| **LDO6 (GP LDO)** | Hiccup / 400mA | Hiccup / 400mA | Hiccup / 400mA | |
| **LDO7 (GP LDO)** | Hiccup / 400mA | Hiccup / 400mA | Hiccup / 400mA | |
| **LDO8 (GP LDO)** | Hiccup | Hiccup | Hiccup | |

Table 6 shows the complete NVM register maps of STPMIC25A, STPMIC25B and STPMIC25D versions:

Table 6. STPMIC25A, STPMIC25B and STPMIC25D NVM configuration maps

| Register (hex) | STPMIC25A Value (hex) | STPMIC25B Value (hex) | STPMIC25D Value (hex) |
|---|---|---|---|
| **0x90** | 0xF1 | 0xD1 | 0xF1 |
| **0x91** | 0x0A | 0x0A | 0x0A |
| **0x92** | 0x13 | 0x13 | 0x13 |
| **0x93** | 0x08 | 0x08 | 0x08 |
| **0x94** | 0x03 | 0x03 | 0x03 |
| **0x95** | 0x04 | 0x00 | 0x04 |
| **0x96** | 0x21 | 0x21 | 0x21 |
| **0x97** | 0x28 | 0x28 | 0x28 |
| **0x98** | 0x00 | 0x00 | 0x00 |
| **0x99** | 0x00 | 0x00 | 0x24 |
| **0x9A** | 0x00 | 0x00 | 0x00 |
| **0x9B** | 0x00 | 0x00 | 0x00 |
| **0x9C** | 0x1E | 0x1E | 0x1E |
| **0x9D** | 0x20 | 0x20 | 0x20 |
| **0x9E** | 0x00 | 0x00 | 0x00 |
| **0x9F** | 0x76 | 0x67 | 0x76 |
| **0xA0** | 0x67 | 0x67 | 0x67 |
| **0xA1** | 0x00 | 0x00 | 0x00 |
| **0xA2** | 0x76 | 0x00 | 0x76 |
| **0xA3** | 0x30 | 0x28 | 0x30 |
| **0xA4** | 0x00 | 0x00 | 0x00 |
| **0xA5** | 0x00 | 0x00 | 0x00 |
| **0xA6** | 0x00 | 0x00 | 0x00 |
| **0xA7** | 0x00 | 0x00 | 0x40 |
| **0xA8** | 0x00 | 0x00 | 0x40 |
| **0xA9** | 0x55 | 0x55 | 0x55 |
| **0xAA** | 0x99 | 0x99 | 0x99 |
| **0xAB** | 0xFF | 0xFF | 0xFF |
| **0xAC** | 0xBD | 0x7D | 0xBD |
| **0xAD** | 0x79 | 0x79 | 0x79 |
| **0xAE** | 0xFF | 0xFF | 0xFF |
| **0xAF** | 0x1B | 0x1B | 0x1B |
| **0xB0** | 0x01 | 0x01 | 0x01 |
| **0xB1** | 0xFF | 0xFF | 0xFF |
| **0xB2** | 0xFF | 0xFF | 0xFF |
| **0xB3** | 0x7F | 0x7F | 0x7F |
| **0xB5** | 0x33 | 0x33 | 0x33 |
| **0xB6** | 0x00 | 0x00 | 0x00 |
| **0xB7** | 0x00 | 0x00 | 0x00 |

The STPMIC25A version is soldered in STEVAL-PMIC25M1.

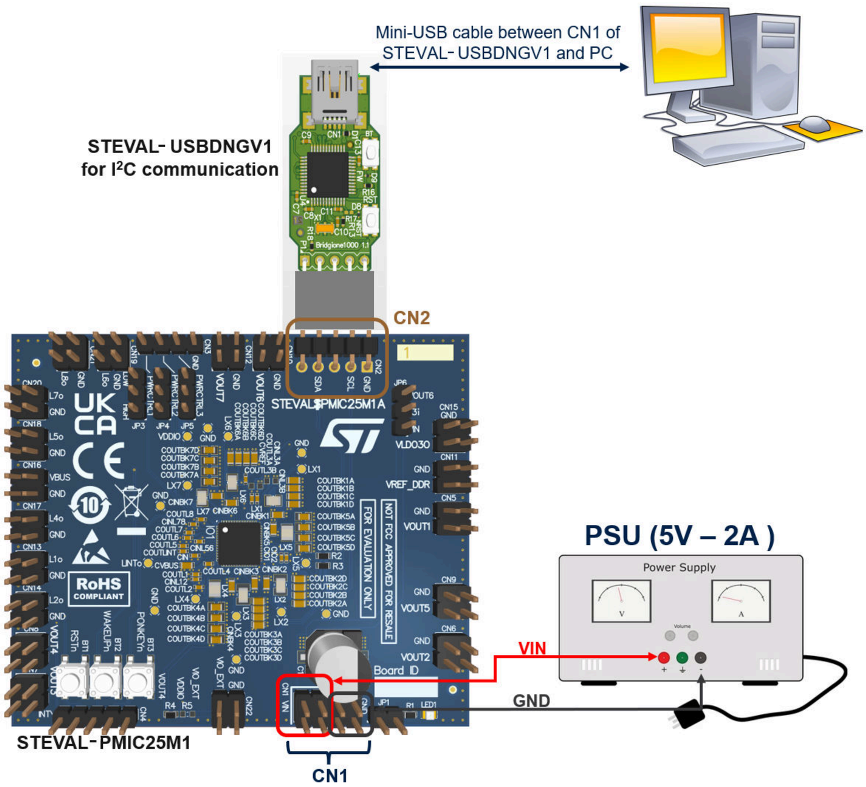
For more details regarding the STPMIC25 features, please refer to STPMIC25 datasheet DS14278.

# 3 Get started with STEVAL-PMIC25V1 kit

To get started with the STEVAL-PMIC25V1 kit, proceed as follows:

1. Connect the STEVAL-USBDNGV1 on STEVAL-PMIC25M1 through the connector CN2
2. Connect a mini-USB cable between the PC and the connector CN1 of STEVAL-USBDNGV1
3. Apply the power supply VIN to the connector CN1 of the STEVAL-PMIC25M1 (a power supply capable of 2A minimum is required)

**Figure 3. STEVAL-PMIC25V1 kit configuration**



## 3.1 Input/Output connector description

The below table shows the list and the relative description of all input/output connectors present in the STEVAL-PMIC25M1:

**Table 7. STEVAL-PMIC25M1 input/output connectors description**

| STEVAL-PMIC25M1 connectors | | |
|---|---|---|
| **Name** | **Functionality** | **Details** |
| CN1 | Main input power supply | VIN: Positive input power force/sense |
| | | GND: Ground input force/sense |
| CN2 | $I^2C$ bus connector | SCL: Clock |
| | | SDA: Data |
| | | GND: Ground |
| CN3 | PWRCTRL1,2,3 output voltage connector | PWRCTRL1: output voltage sense |
| | | PWRCTRL2: output voltage sense |
| | | PWRCTRL3: output voltage sense |
| CN4 | INTn, RSTn, WAKEUPn, PONKEYn output voltage connector | INTn: Output voltage sense |
| | | RSTn: Output voltage sense |
| | | WAKEUPn: Output voltage sense |
| | | PONKEYn: Output voltage sense |
| CN5 | BUCK1 output voltage Connector | VOUT1: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN6 | BUCK2 output voltage Connector | VOUT2: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN7 | BUCK3 output voltage Connector | VOUT3: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN8 | BUCK4 output voltage Connector | VOUT4: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN9 | BUCK5 output voltage Connector | VOUT5: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN10 | BUCK6 output voltage Connector | VOUT6: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN11 | VREFDDR output voltage Connector | VREF_DDR: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN12 | BUCK7 output voltage Connector | VOUT7: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN13 | LDO1 output voltage Connector | L1o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN14 | LDO2 output voltage Connector | L2o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN15 | LDO3 output voltage Connector | L3o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN16 | LDO4 additional input supply through VBUS | VBUS: Positive input power force/sense |
| | | GND: Ground output force/sense |

| STEVAL-PMIC25M1 connectors | | |
|---|---|---|
| Name | Functionality | Details |
| CN17 | LDO4 output voltage Connector | L4o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN18 | LDO5 output voltage Connector | L5o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN19 | LDO6 output voltage Connector | L6o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN20 | LDO7 output voltage Connector | L7o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN21 | LDO8 output voltage Connector | L8o: output voltage force/sense |
| | | GND: Ground output force/sense |
| CN22 | VIO output voltage Connector from external supply | VIO_EXT: output voltage force/sense |
| | | GND: Ground output force/sense |
| JP1 | Manual bridge for VIN “LED1” connection | If LED1 is ON, VIN is applied to the STEVAL$PMIC25M1 |
| JP3 | Manual bridge for PWRCTRL1 connection | HIGH position: PWRTCTRL1 forced to VIO |
| | | LOW position: PWRTCTRL1 forced to GND |
| JP4 | Manual bridge for PWRCTRL2 connection | HIGH position: PWRTCTRL2 forced to VIO |
| | | LOW position: PWRTCTRL2 forced to GND |
| JP5 | Manual bridge for PWRCTRL3 connection | HIGH position: PWRTCTRL3 forced to VIO |
| | | LOW position: PWRTCTRL3 forced to GND |
| JP6 | Manual bridge for LDO3 input connection | L3i-VIN position: LDO3 input forced to main input voltage supply “VIN” |
| | | L3i-VOUT6 position: LDO3 input forced to BUCK6 output |
| R4-R5 | 0 Ohm resistors: Allow VIO connection to BUCK4 output or to external supply (VIO_EXT pin) | If R4 (0 Ohm) is soldered: VIO is connected to BUCK4 output. By default R4 is soldered |
| | | If R5 (0 Ohm) is soldered: VIO is connected to VIO_EXT output; in this case VIO must be supplied externally on CN22 connector (VIO_EXT pin). |
| BT1 | RSTn button | RSTn pin is connected to GND when BT1 is pushed |
| BT2 | WAKEUPn button | WAKEUPn pin is connected to GND when BT2 is pushed |
| BT3 | PONKEYn button | PONKEYn pin is connected to GND when BT3 is pushed |

Figure 4, Figure 5, Figure 6 and Figure 7 show the connectors details of the STEVAL-PMIC25M1.

Referring to Figure 4, be sure that:

- A PSU (5V – 2A) is connected to CN1 connector
- R4 (0 Ω) is soldered → in this way VIO is provided by BUCK4 output

- The STEVAL-USBDNGV1 is connected to CN2 (as show in Figure 3)
- The STEVAL-USBDNGV1 is connected to PC through a micro-USB connector plugged on CN1

**Figure 4. VIN and VIO connectors details of STEVAL-PMIC25M1**

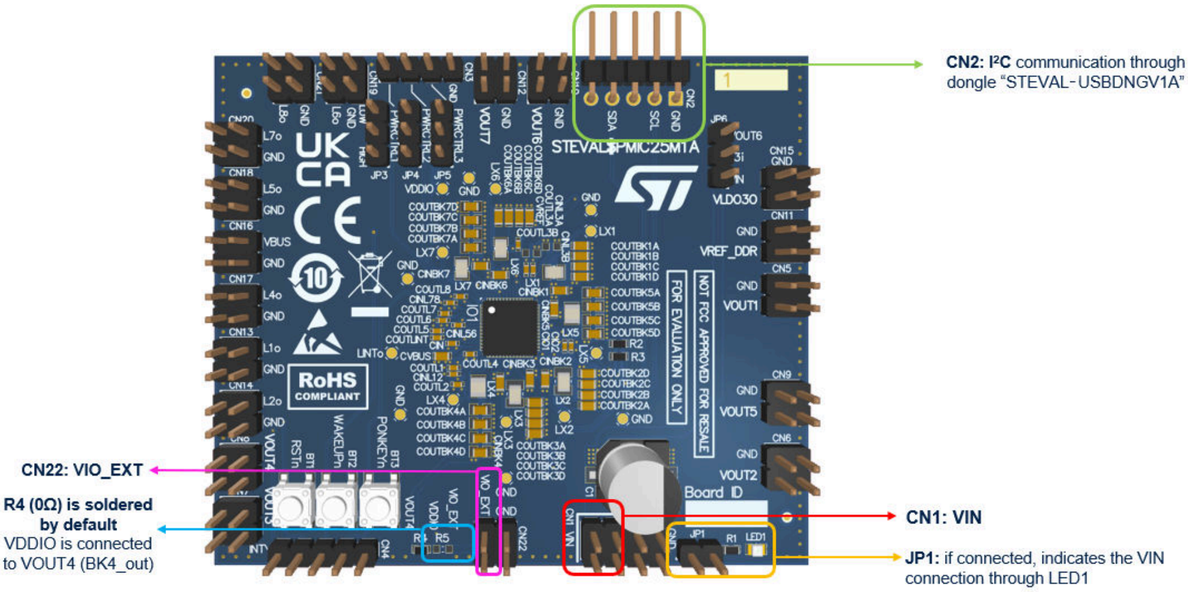
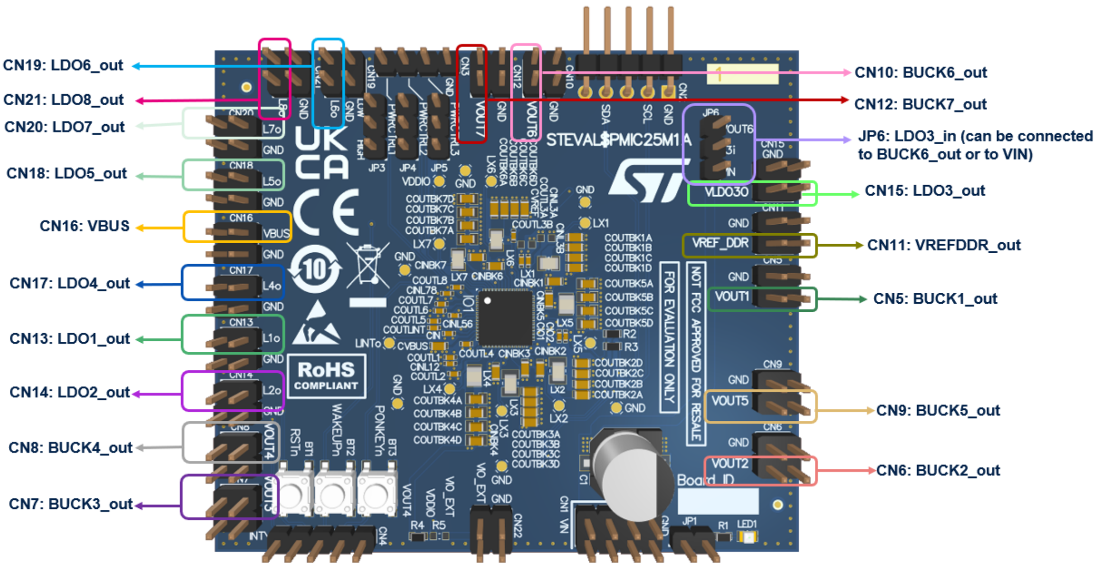



Figure 5 shows the I/O connector of:

- all BUCK converters (from BK1 to BK7)
- all LDO regulators (from LDO1 to LDO8)
- VREFDDR regulator
- JP6, which is a connector that allow to switch LDO3 input between BUCK6 output and the main input supply (VIN)

**Figure 5. BUCKs and LDOs connectors details of STEVAL-PMIC25M1**




*Note: All BUCKs and LDOs input supply pins (except LDO3 input) are connected by default in the board layout to the main input supply (VIN).*

Figure 6 shows the VLX test points from BUCK1 to BUCK7:

**Figure 6. BUCKs VLX test points details of STEVAL-PMIC25M1**

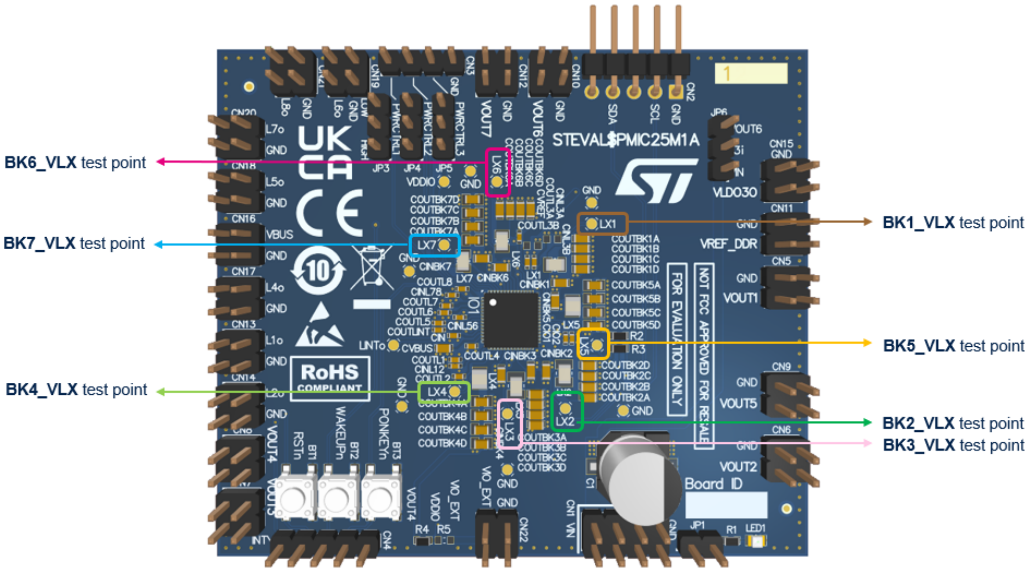
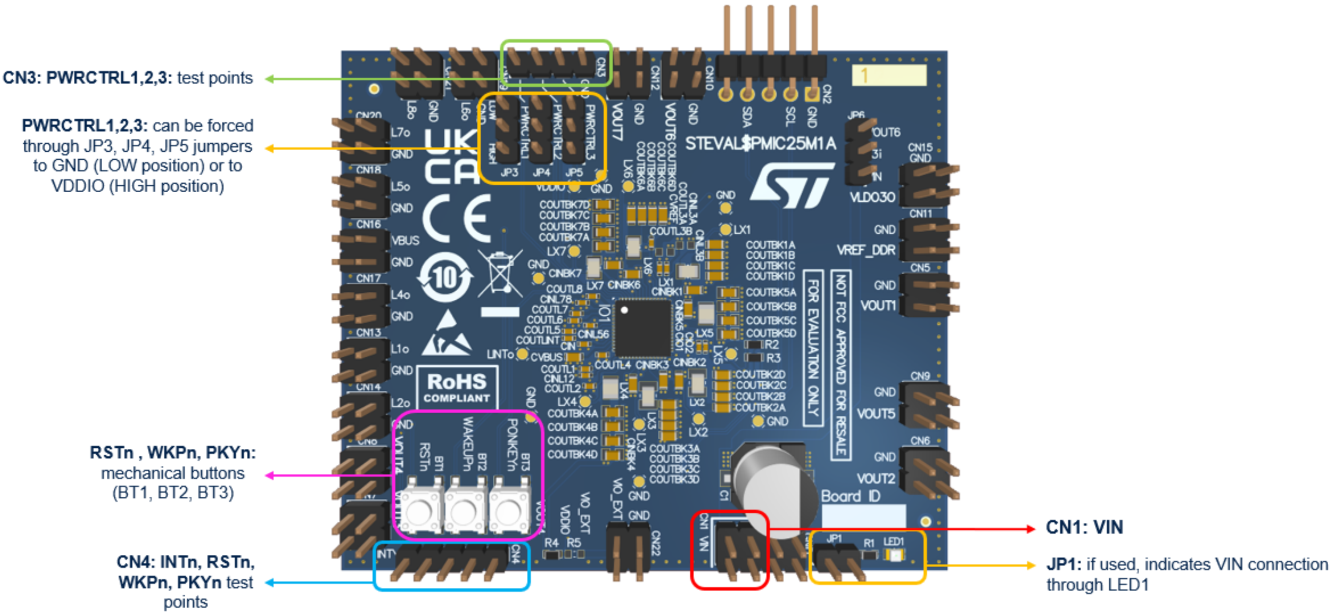


Figure 7 shows the I/O connectors of the digital pins:

- PWRCTRL1,2,3
  - CN3 are test points
  - JP3, JP4 and JP5 allow to force respectively PWRCTRL1, PWRCTRL2 and PWRCTRL3 to VDDIO (in HIGH position) or to GND (in LOW position) using a manual bridge
- INTn, RSTn, WKPn, PKEYn
  - CN4 are test points
  - BT1, BT2 and BT3 are mechanical buttons that if pressed force RSTn, WKPn and PKYn to GND.
- JP1 → if manual bridge is placed over JP1, LED1 will automatically switch on when VIN is provided to the STEVAL-PMIC25M1 on CN1

**Figure 7. Digital connectors details (PWRCTRL1,2,3; WAKEUPn, RSTn, INTn) of STEVAL-PMIC25M1**



# 4 Getting started with STPMIC25 GUI

To get started with the STPMIC25 GUI consult the STSW-PMIC25GUI user manual.

# 5 Board Layout

The STPMIC25 evaluation board is based on a 4-layer PCB, 2s2p, to be compliant with the JEDEC JESD51-2 standard.

## 5.1 Stack-up layer

Figure 8 shows the PCB stack-up layer used for the STPMIC25 evaluation board.

Figure 8. STEVAL-PMIC25M1: PCB stack-up layer

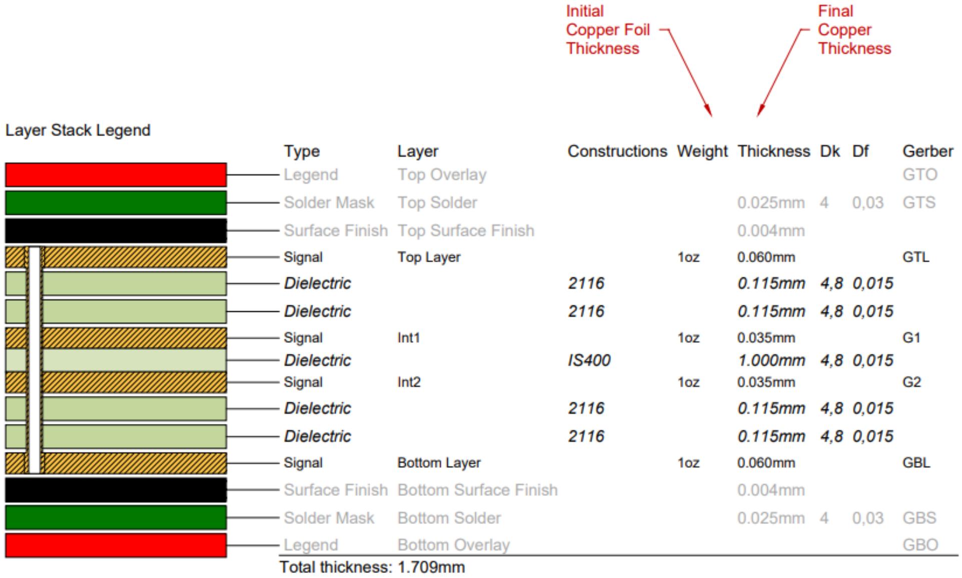


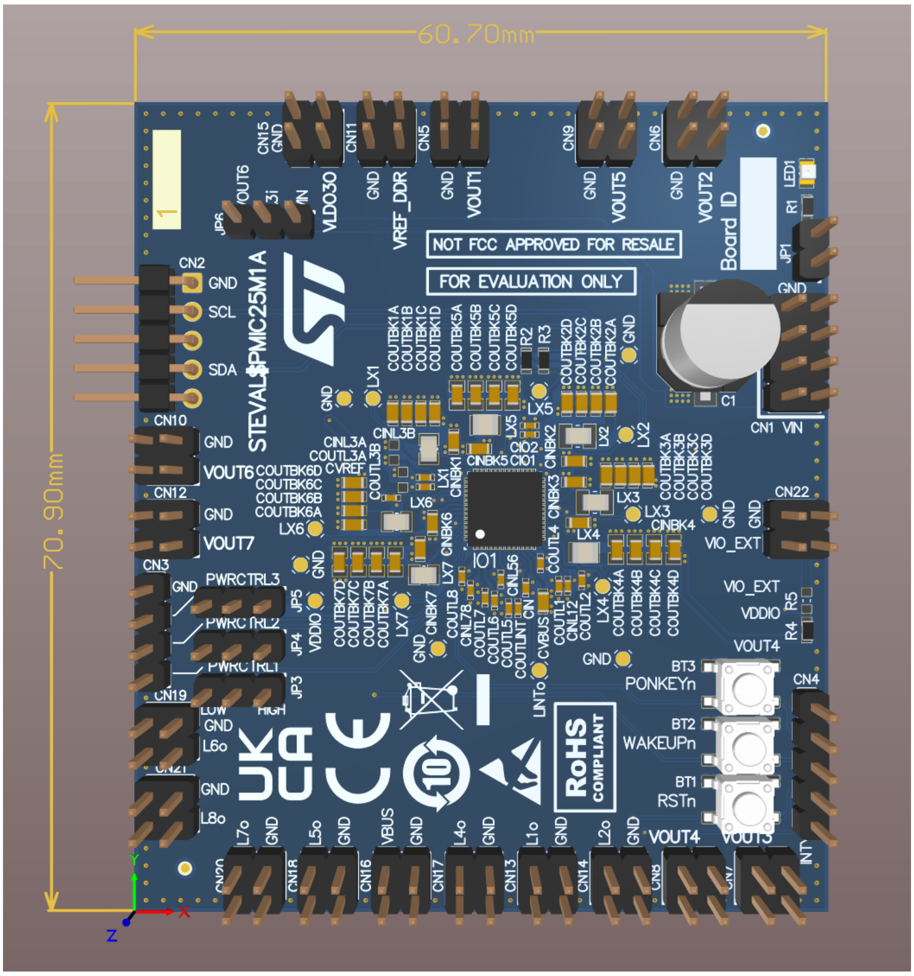

Table 8. STEVAL-PMIC25M1: stack-up layer details

| Layer | Stack-up |
|---|---|
| Top | Component/power/signal |
| Mid signal 1 | GND |
| Mid signal 2 | Power/GND |
| Bottom | Power/GND |

## 5.2 Layout details

Figure 9 shows the board dimensions in mm.

**Figure 9. STEVAL$PMIC25M1: 3D layout**




The dimensions of the board are 70.90mm x 60.70mm.

Figure 10, Figure 11, Figure 12 and Figure 13 show the details of the top, mid1, mid2 and bottom layers of the STEVAL-PMIC25M1.

Figure 10. STEVAL-PMIC25M1: Top layer (components/power/signal)

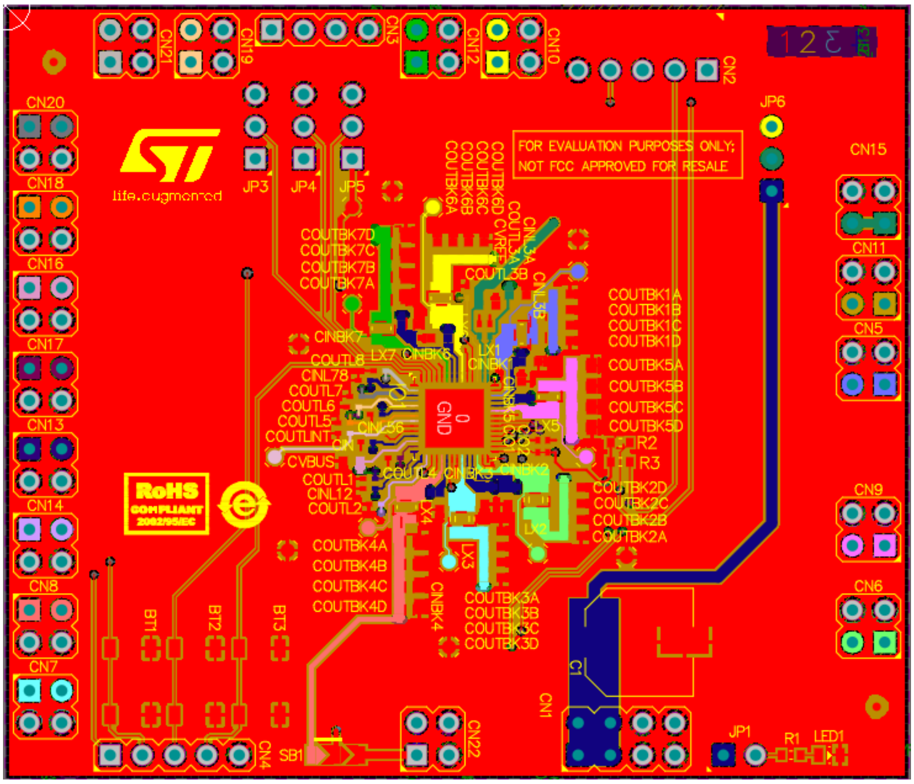
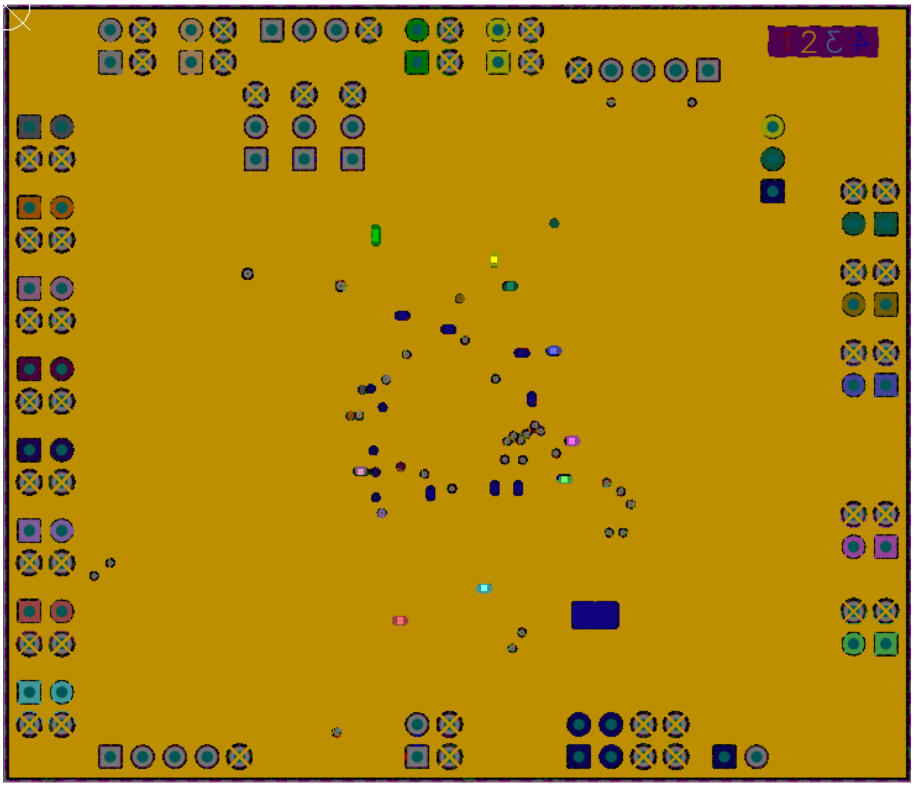


Figure 11. STEVAL-PMIC25M1: Mid layer 1 (GND)



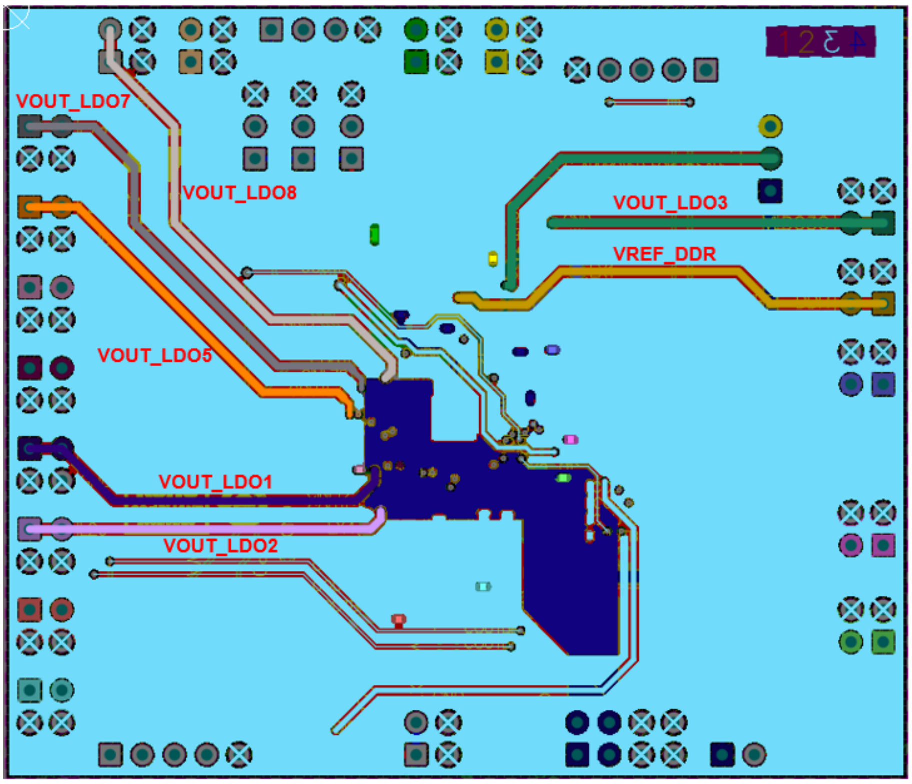



Figure 12. STEVAL-PMIC25M1: Mid layer 2 (Power/GND)

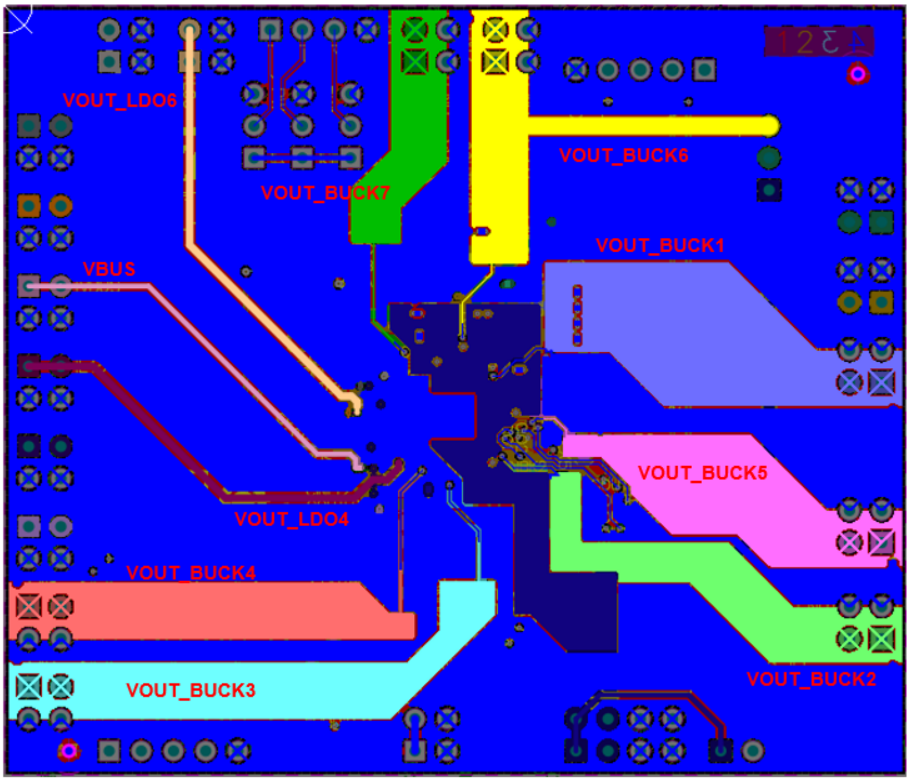


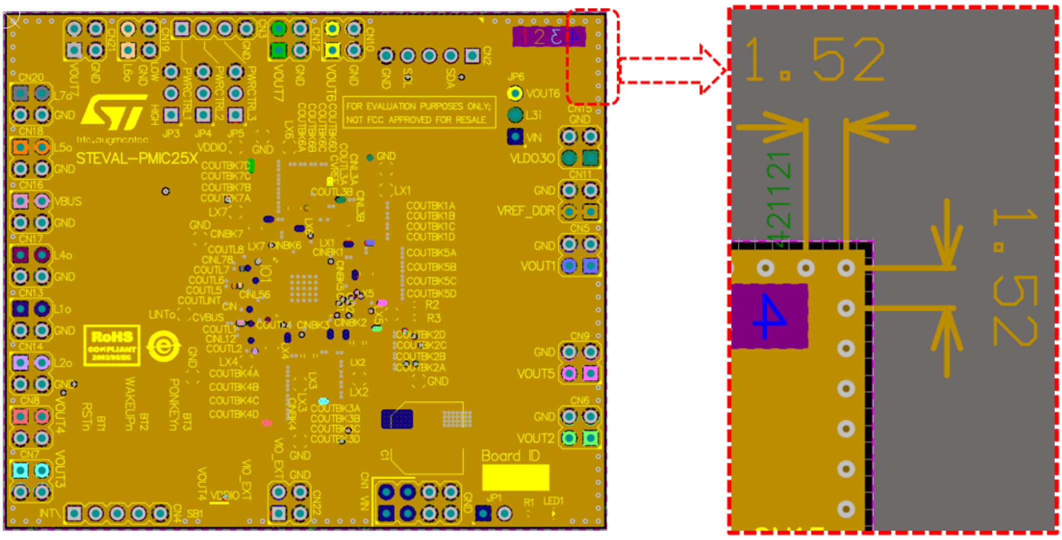

Figure 13. STEVAL-PMIC25M1: Bottom layer (Power/GND)

## 5.3 Power and ground planes

Since both POWER and GROUND are planes, inductive effects are minimized, providing a very low impedance path to the STPMIC25 evaluation board. The use of a continuous ground layer with multiple via holes is a good method to achieve low impedance ground returns, but to keep low impedance over all areas of the PCB, it should never be neither narrowed nor partitioned.

Figure 14 shows the mid layer 1 of the STPMIC25 evaluation board layout, with the detail on GND vias placed all around the PCB edge with 2mm spacing.

Figure 14. **STEVAL-PMIC25M1: Mid layer 1 (GND plane)**




The usage of flat and large shapes, whether possible, is recommended for all high current power supplies such as VIN, VOUT and VBUS. This will help to reduce the power losses. When examining the ground and power planes, make sure that the plane continuity is not affected by too many vias.

Examples of power planes, vias placement and plane shapes are shown in Section 5.5 (mid-layer 2), in which they are used to route VIN and all VOUT of the regulators out to connector headers.

## 5.4 Via holes

Though the ground plane is a good ground reference, the presence of the vias along ground returns introduces some stray inductances at high frequency. Placing multiple via holes in a plane reduces this effect considering that the stray inductances are in parallel. Those via holes must be spaced in such a way that the power plane is not excessively cut up.

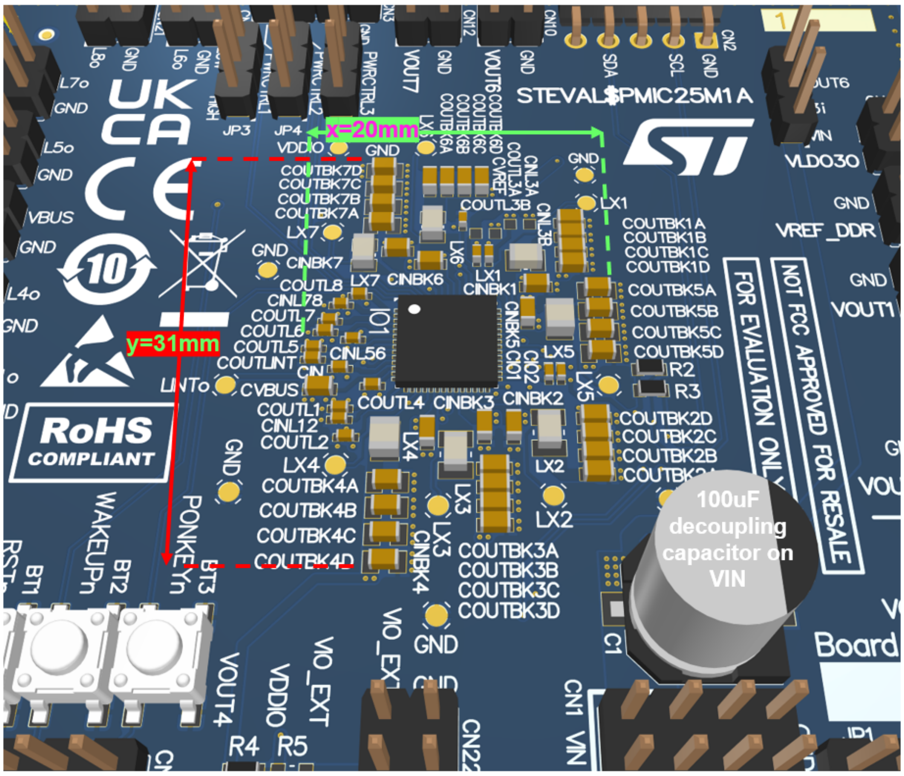
Table 9. **STEVAL-PMIC25M1: via size**

| Via type | Hole size | Pad size |
|---|---|---|
| Via holes | 0.2mm | 0.5mm |

## 5.5 Passive components placement

Figure 15 shows the STPMIC25 passive components arrangement (input and capacitors, output coils and resistors) around the STPMIC25 in the evaluation board. The aim was to shrink all the BOM in the smallest aera around the STPMIC25 device (20mm x 31mm).

**Figure 15.** **STEVAL-PMIC25M1: passive components placement**




In STPMIC25 evaluation board all the suggestions described in this application note have been met.

Moreover, it’s good practice to put all passive components on top of the layout and to use the bottom side only if it is really needed by the application/board size.

A decoupling capacitor of 100μF was placed on the input supply rail for two reasons:

- In case of input voltage drop, it provides adequate power to the STPMIC25 to maintain the voltage level
- In case of voltage surge, it prevents the excess current from flowing through the STPMIC25 to keep the voltage stable

# 6 Schematic diagrams

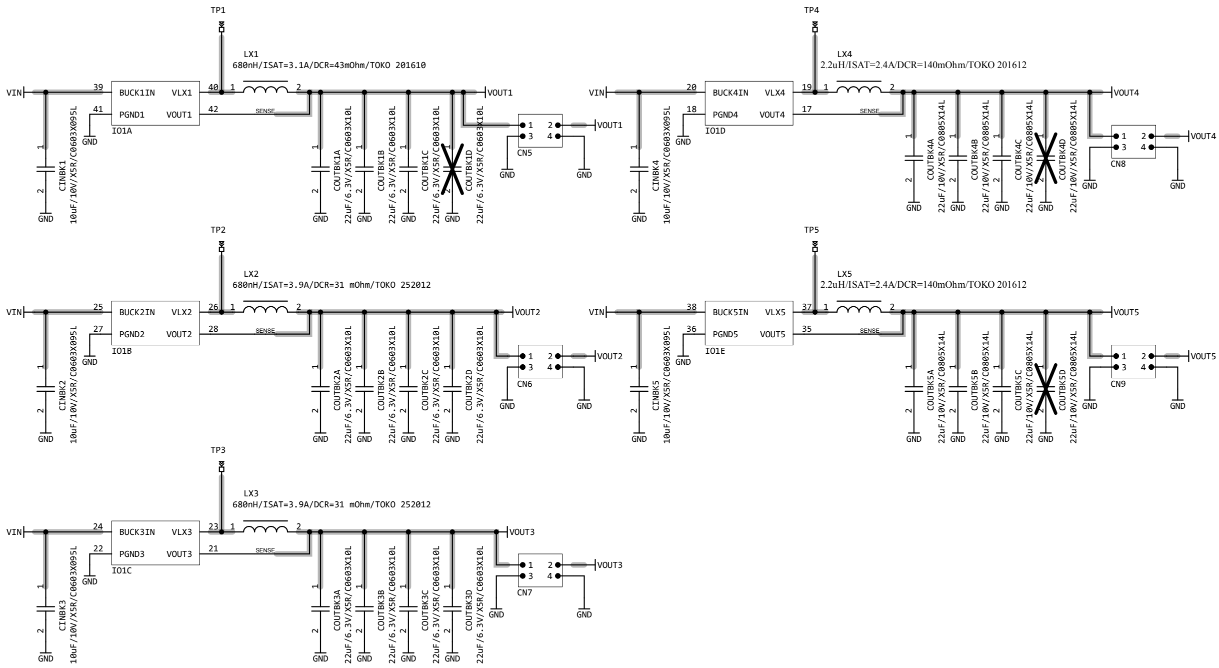
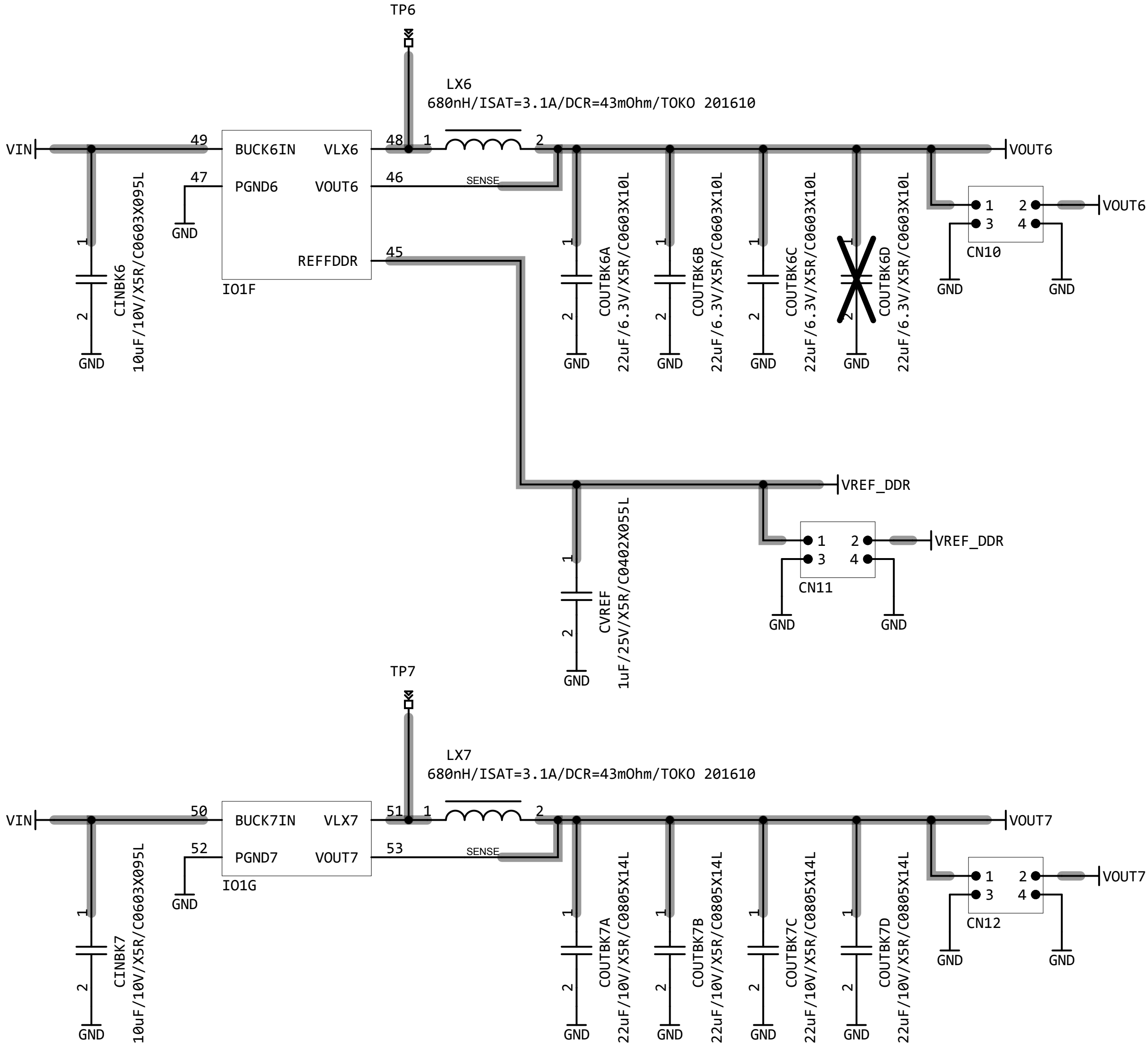


**Figure 16.** STEVAL-PMIC25M1 circuit schematic (1 of 5)

**Figure 17.** STEVAL-PMIC25M1 circuit schematic (2 of 5)



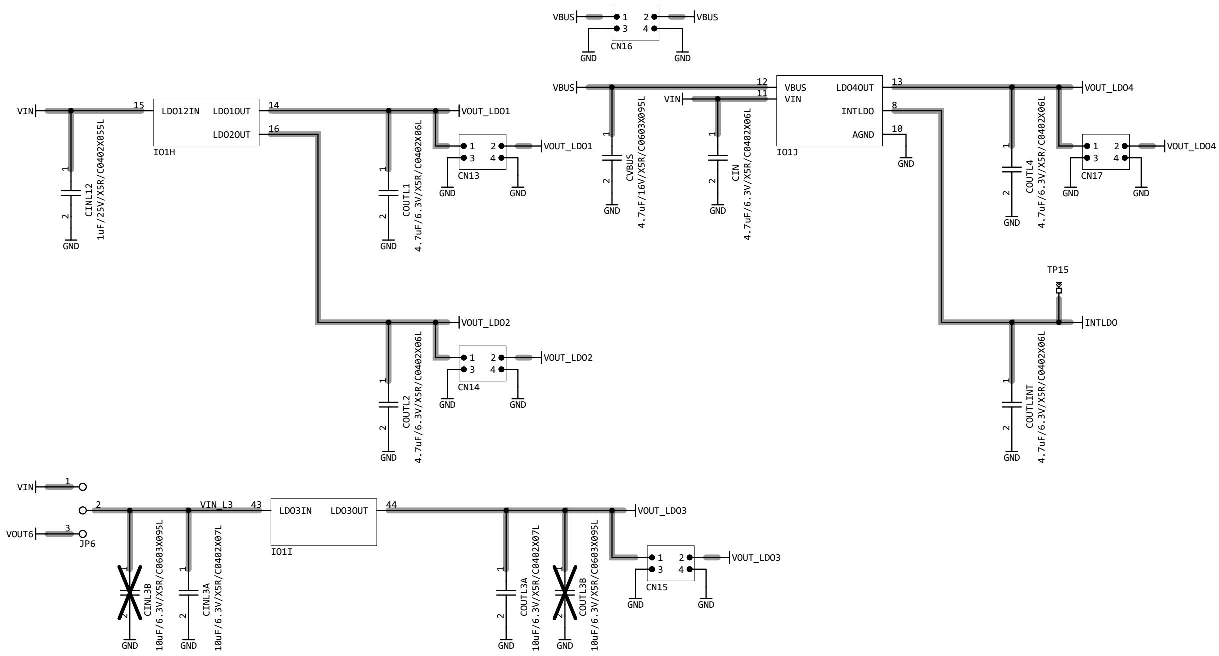



**Figure 18. STEVAL-PMIC25M1 circuit schematic (3 of 5)**

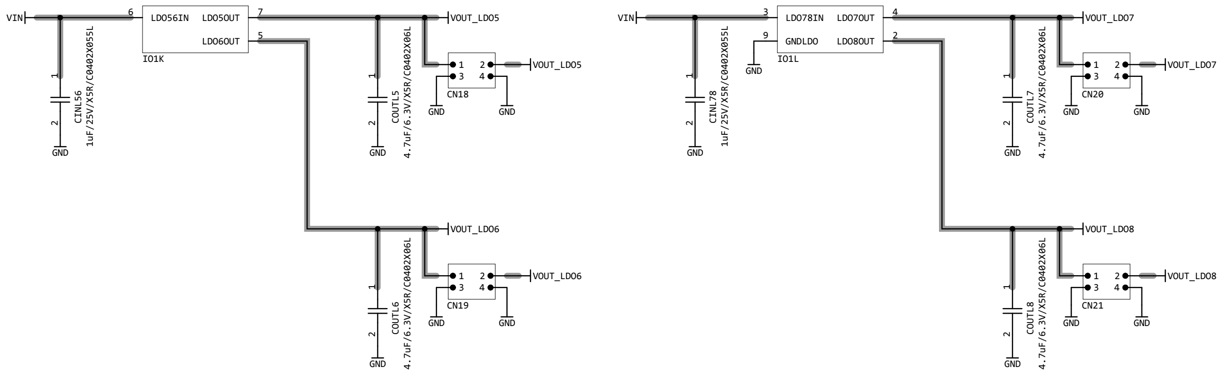
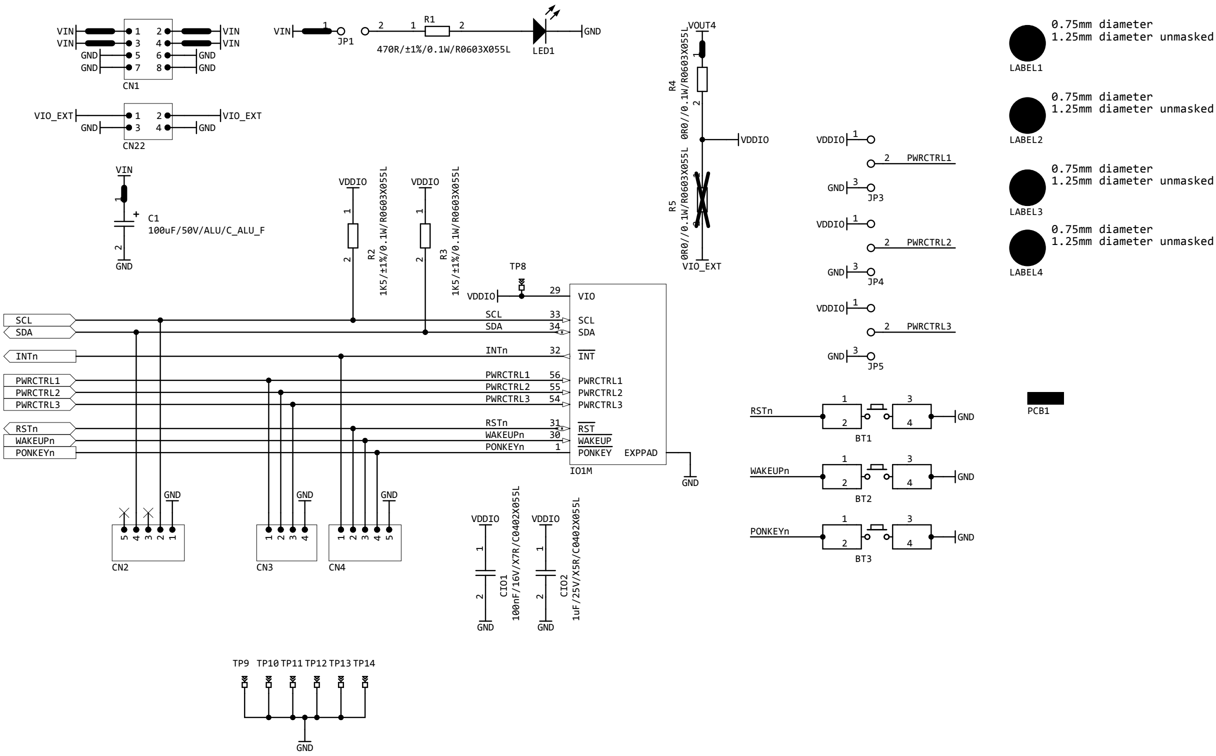



**Figure 19. STEVAL-PMIC25M1 circuit schematic (4 of 5)**

**Figure 20.** STEVAL-PMIC25M1 circuit schematic (5 of 5)



# 7 Bill of materials

Table 10. STEVAL-PMIC25V1 bill of materials

| Item | Q.ty | Ref. | Part / Value | Description | Manufacturer | Order code |
|---|---|---|---|---|---|---|
| 1 | 1 | - | Table 11. STEVAL-PMIC25M1 | - | ST | Not available for separate sale |
| 2 | 1 | - | Table 12. STEVAL-USBDNGV1 | - | ST | Not available for separate sale |

Table 11. STEVAL-PMIC25M1 bill of materials

| Item | Q.ty | Ref. | Part / Value | Description | Manufacturer | Order code |
|---|---|---|---|---|---|---|
| 1 | 3 | BT1, BT2, BT3 | - | Tactile Switches | C&K | PTS647SK38SMTR2LFS |
| 2 | 1 | C1 | 100µF 50V | Aluminium Electrolytic Capacitor | Panasonic Electronic Components | EEE1HA101UP |
| 3 | 9 | CIN, COUTL1, COUTL2, COUTL4, COUTL5, COUTL6, COUTL7, COUTL8, COUTLINT | 4.7µF 6.3V | Multilayer Ceramic Capacitors X5R | Murata Electronics North America | GRM155R60J475ME47 |
| 4 | 7 | CINBK1, CINBK2, CINBK3, CINBK4, CINBK5, CINBK6, CINBK7 | 10µF 10V | Multilayer Ceramic Capacitors X5R | Murata Electronics North America | GRM188R61A106ME69D |
| 5 | 2 | CINL3A, COUTL3A | 10µF 6.3V | Multilayer Ceramic Capacitors X5R | Murata Electronics North America | GRM155R60J106ME05D |
| 6 | 4 | CINL12, CINL56, CINL78, CVREF | 1µF 25V | Multilayer Ceramic Capacitors X5R | Murata Electronics North America | GRM155R61E105KA12D |
| 7 | 1 | CIO1 | 0.1µF 16V | Multilayer Ceramic Capacitor X5R | Murata Electronics North America | GRM155R71C104KA88 |
| 8 | 1 | CIO2 | 1µF 25V | Multilayer Ceramic Capacitor X5R | Murata Electronics North America | GRM155R61E105KA12 |
| 9 | 14 | COUTBK1A, COUTBK1B, COUTBK1C, COUTBK2A, COUTBK2B, COUTBK2C, COUTBK2D, COUTBK3A, COUTBK3B, COUTBK3C, COUTBK3D, COUTBK6A, COUTBK6B, COUTBK6C | 22µF 6.3V | Multilayer Ceramic Capacitors X5R | Murata Electronics North America | GRM188R60J226MEA0 |

| Item | Q.ty | Ref. | Part / Value | Description | Manufacturer | Order code |
|---|---|---|---|---|---|---|
| 10 | 10 | COUTBK4A, COUTBK4B, COUTBK4C, COUTBK5A, COUTBK5B, COUTBK5C, COUTBK7A, COUTBK7B, COUTBK7C, COUTBK7D | 22µF 10V | Multilayer Ceramic Capacitors X5R | Murata Electronics North America | GRM21BR61A226ME51L |
| 11 | 1 | CVBUS | 4.7µF 16V | Multilayer Ceramic Capacitor X5R | Murata Electronics North America | GRM188R61C475KE11D |
| 12 | 3 | LX1, LX6, LX7 | 0.68µH | Power Inductors | Murata Electronics North America | DFE201610E-R68M |
| 13 | 2 | LX2, LX3 | 0.68µH | Power Inductors | Murata Electronics North America | DFE252012F-R68M |
| 14 | 2 | LX4, LX5 | 2.2µH | Power Inductors | Murata Electronics North America | DFE201610E-2R2M |
| 15 | 1 | R1 | 470Ω | Thick Film Resistor | YAGEO | RC0603FR-07470RL |
| 16 | 2 | R2, R3 | 1.5kΩ | Thick Film Resistor | YAGEO | AF0603FR-071K5L |
| 17 | 1 | R4 | 0Ω | Thick Film Resistor | YAGEO | RC0603FR-070RL |
| 18 | 1 | LED1 | Green Led | Standard LEDs - SMD GREEN WATER CLEAR | Kingbright | APT2012SGC |
| 19 | 1 | CN1 | - | Headers & Wire Housings WR-PHD 2.54mm Hdr 8P Dual Str Gold | Wurth Electronics Inc. | 61300821121 |
| 20 | 1 | CN2 | - | Headers & Wire Housings WR-PHD 2.54mm Hdr 5P Single RA Gold | Wurth Electronics Inc. | 61300511021 |
| 21 | 1 | CN3 | - | Headers & Wire Housings WR-PHD 2.54mm Hdr 4P Single Str Gold | Wurth Electronics Inc. | 61300411121 |
| 22 | 1 | CN4 | - | Headers & Wire Housings WR-PHD 2.54mm Hdr 5P Single Str Gold | Wurth Electronics Inc. | 61300511121 |
| 23 | 18 | CN5, CN6, CN7, CN8, CN9, CN10, CN11, CN12, CN13, CN14, CN15, CN16, CN17, CN18, CN19, CN20, CN21, CN22 | - | Headers & Wire Housings WR-PHD 2.54mm Hdr 4P Dual Str Gold | Wurth Electronics Inc. | 61300421121 |
| 24 | 5 | JP1, JP3, JP4, JP5, JP6 | - | Headers & Wire Housings JUMPER SOCKET OPEN TOP BLUE | Harwin | M7583-05 |
| 25 | 1 | IO1 | VQFN6.5X6.5X0.9 56L PITCH 0.40 | STPMIC25A, WFQFN 56L (6.5x6.5x0.9 mm) | ST | STPMIC25APQR |

**Table 12. STEVAL-USBDNGV1 bill of materials**

| Item | Q.ty | Ref. | Part / Value | Description | Manufacturer | Order code |
|---|---|---|---|---|---|---|
| 1 | 9 | C1, C4, C6, C7, C8, C9, C10, C11, C13 | 0.10µF 50V | Capacitor | Murata Electronics North America | GRM155R61H104KE14 |
| 2 | 2 | C2, C5 | 1.0µF 16V | Capacitor | Murata Electronics North America | GRM155R61C105KA12 |
| 3 | 1 | C3 | 2.2µF 6.3V | Capacitor | Murata Electronics North America | GRM155R60J225KE01 |
| 4 | 1 | CN1 | USB 2.0, 30V/1A | Connector | Wurth Electronics Inc. | 65100516121 |
| 5 | 1 | D1 | | BidirTVSDiode | Kyocera AVX | GG0402055R042P |
| 6 | 4 | D2, D3, D4, D5 | | LED | Kingbright | APT1608LVBC/D |
| 7 | 1 | D6 | | LED | Kingbright | APT1608SYCK |
| 8 | 1 | D7 | | LED | Kingbright | APT1608SURCK |
| 9 | 2 | D8, D9 | ST0201 | TVSDiode | ST | ESDALC6V1-1U2 |
| 10 | 1 | F1 | | Fuse | Littelfuse Inc. | 0466.250NRHF |
| 11 | 1 | FL1 | QFN-6L | ESD | ST | ECMF02-2AMX6 |
| 12 | 1 | P1 | | Connector | Sullins Connector Solutions | PPPC051LGBN-RC |
| 13 | 4 | R1, R8, R12, R18 | 0 Ohms | Resistor | Rohm Semiconductor | PMR01ZZPJ000 |
| 14 | 4 | R3, R5, R6, R10 | 1.5 kOhms | Resistor | Yageo | RC0402FR-071K5L |
| 15 | 1 | R11 | 180 Ohms | Resistor | Yageo | RC0402FR-07180RL |
| 16 | 1 | R13 | 100 Ohms | Resistor | Yageo | RC0402FR-07100RL |
| 17 | 1 | R14 | 220 Ohms | Resistor | Yageo | RC0402FR-07220RL |
| 18 | 1 | R15 | 270 Ohms | Resistor | Yageo | RC0402FR-07270RL |
| 19 | 1 | R16 | 10 kOhms | Resistor | Yageo | RC0402FR-0710KL |
| 20 | 2 | SW1, SW2 | | Button | C&K | KMR432NGULCLFS |
| 21 | 1 | U1 | | Level Translator BiDir | TI | LSF0204DRUTR |
| 22 | 1 | U2 | SOT323-5L | LDO | ST | LDK120C33R |
| 23 | 1 | U3 | SOT323-5L | LDO | ST | LDK120C10R |
| 24 | 1 | U4 | LQFP 48 7x7x1.4 mm | MCU | ST | STM32F303CCT6 |
| 25 | 1 | X1 | 8 MHz | Resonator | Murata Electronics | CSTNE8M00GH5L000R0 |

# 8 Kit versions

**Table 13. STEVAL-SPMIC25V1 versions**

| Finished good | Schematic diagrams | Bill of materials |
|---|---|---|
| STEVALSPMIC25V1A[(1)] | STEVALSPMIC25V1A schematic diagrams | STEVALSPMIC25V1A bill of materials |

1. *This code identifies the STEVAL-PMIC25V1 evaluation kit first version. The kit consists of the STEVAL-PMIC25M1 expansion board whose version is identified by the code STEVAL$PMIC25M1A and the STEVAL-USBDNGV1 expansion board whose version is identified by the code STEVAL$USBDNGV1A.*

# 9 Regulatory compliance information

### Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

### Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

### Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2015/863/EU (RoHS).

### Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

## Revision history

Table 14. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-Jun-2024 | 1 | Initial release. |
| 07-Nov-2024 | 2 | Updated Section 2: STPMIC25 NVM settings. |

# Contents

# List of tables

# List of figures