How to use the AEK-COM-10BASET two-channel 10BASE-T1S packet converter evaluation board

Introduction

New megatrends in the automotive industry, such as personalization, electrification, autonomy, and full connectivity are moving in-vehicle networks away from domain-based solutions, gravitating towards new zonal architectures.

Unlike domain-based architectures, zonal-based architectures exploit connectivity based on physical location rather than function, significantly reducing the number of electronic control units (ECUs) in vehicles and the cabling harness weight. As existing legacy connectivity technologies (such as FlexRay and CAN) have exceeded the maximum acceptable latency, Time Sensitive Networks (TSN) based on Ethernet connectivity represent the best alternative to fully leverage the advantages of this new architecture, all the way to edge sensors and actuators.

As cars become more autonomous and interconnected, the automotive field is becoming increasingly software-defined, making in-vehicle electronics grow in volume and complexity to support the goal for autonomous driving. In this context, 10BASE-T1S automotive Ethernet enhances in-vehicle network (IVN) architectures by connecting sensors, car body and infotainment engine control units (ECUs).

10BASE-T1S protocol supports half-duplex and full-duplex communication, allowing either a point-to-point direct connection between two nodes, or use of a multidrop topology with up-to-eight nodes connected on a single 25 m bus segment.

10BASE-T1S reduces total system cost by using a single pair of wires and a multidrop bus architecture. It also increases system scalability since several nodes can operate on the same bus line with high data throughput. Thanks to the multidrop topology, multiple heterogeneous end points can be connected on a single cable in zonal architectures (for example, the door zone, the window lifter, the mirror control, speakers, car locks, ultrasonic sensors, ambient light sensor, and indicator light). This bus implementation provides an optimized Bill –of-Material (BOM) only requiring a single Ethernet PHY in each node, removing the need for a switch or star topology implementation associated with typical Ethernet technologies. Furthermore, the physical layer collision avoidance (PLCA) technology minimizes dead time and avoids collisions. PLCA allows only the PHY device that owns the transmit opportunity to send data. PHY devices with no data to transmit will be given minimal opportunity to send data, increasing the bandwidth of your network.

Our AEK-COM-10BASET evaluation board perfectly meets the requirements of these new automotive megatrends, representing a powerful tool to explore various vehicle network architectures. By combining 10BASE-T1S automotive Ethernet protocol and other legacy automotive interfaces (CAN, CAN-FD, and SPI), it allows using a single software framework throughout the vehicle from the lowest to the highest speed ranges.

This board merges the innovations brought by the new 10BASE-T1S specification with the high-performance dual-core SPC58EC80E5 Chorus family microcontroller.

The AEK-COM-10BASET essentially acts as a gateway to interconnect heterogeneous communication systems, allowing a vehicle zone sensor/actuator to receive messages in the 10BASE-T1S protocol format even if the zone components are not able to communicate via Ethernet.

The board features a PHY-MAC transceiver, which communicates with the MCU via SPI, and a PHY only transceiver requiring an Ethernet MAC to run in the MCU.

In our board, these transceivers support only half-duplex communication. Both are connected to the MCU, one using the MII port while the other using a SPI channel. The firmware embedded in the board can manage a software-implemented Ethernet MAC and runs under FreeRTOS operating system.

The board is very flexible, allowing several gateway packet conversions to and from 10BASE-T1S, CAN-FD, and SPI. The function can be limited to gateway purposes or can also be extended to decode actuation commands and forward them to several daughter boards via the available ports. For example, a Power Distribution Unit (PDU) daughter board containing E-fuses can be controlled via CAN or SPI by decoding 10BASE-T1S frames.

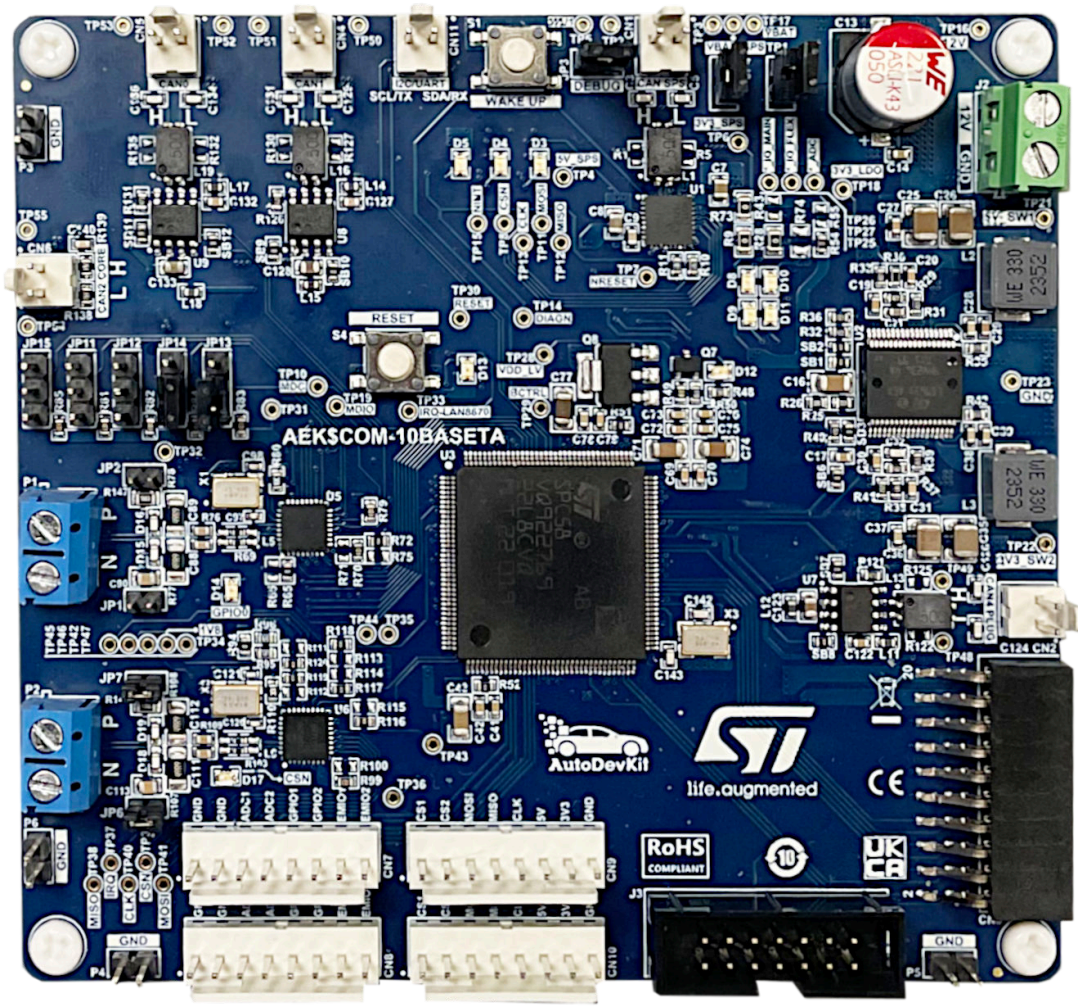
The board features a pre-loaded demo example. This example involves a loopback test among the two 10BASE-T1S channels and two CAN channels. The message is sent via CAN sender port, packed in 10BASE-T1S sent to the other 10BASE-T1S channel, and finally unpacked for a CAN receiving port.

The AEK-COM-10BASET also hosts an OpenOCD debugger/programmer, MCU peripheral connectors, wakeup and reset buttons.

The MCU ADC reference voltage is provided by a stable linear voltage regulator (LDO) embedded in the L5963 IC.

Moreover, a reverse battery protection circuit has been integrated for higher safety.

Figure 1. **AEK-COM-10BASET evaluation board**



Warning: *The AEK-COM-10BASET evaluation board is designed for R&D laboratory use only. It is not intended for field use in vehicles. Moreover, it is not a reference design. Its purpose is evaluation and not production as stated in our Terms of use*

Note: For dedicated assistance, please submit a request in our AutoDevKit Community

1 Hardware overview

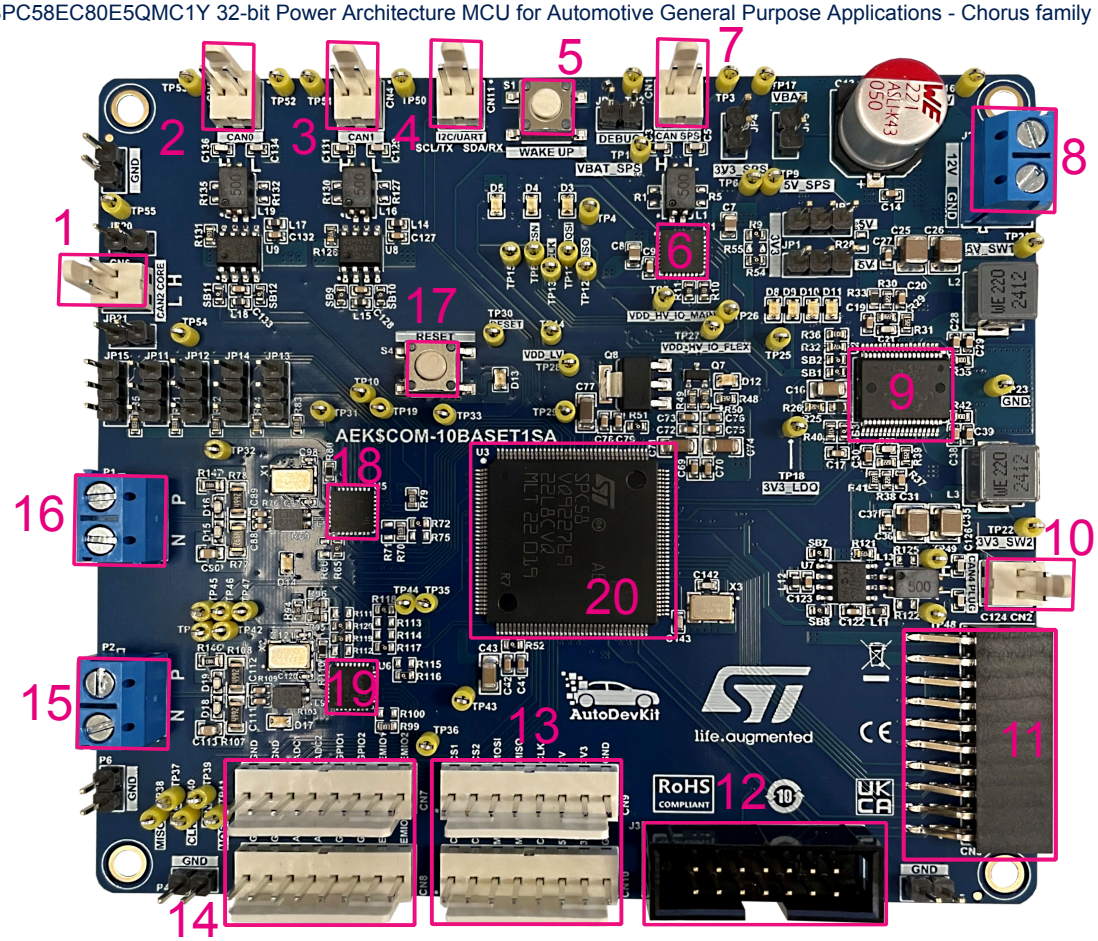
1.1 Features

- 2 x 10BASE-T1S ports:
  - 1x port with PHY-MAC transceiver converting from 10BASE-T1S to SPI
  - 1x port with PHY transceiver converting from 10BASE-T1S to Media-Independent interface (MII)
- The two transceivers are connected with the main board SPC58EC80E5 MCU
- The MCU firmware supports both transceivers at the same time allowing them to work in parallel
- For the transceiver with PHY, we implement a dedicated Ethernet MAC inside the MCU firmware.
- The MCU firmware runs under FreeRTOS implementation on SPC58EC80E5
- 10BASE-T1S according to standard protocol:
  - Point-to-point direct connection or multidrop topology with up-to-eight nodes
  - Up to 10 Mbit/s data transfer over a single pair of wires
  - Physical layer collision avoidance (PLCA)
  - Carrier sense multiple access/Collision detection (CSMA/CD) media access control
- SPSB0813 automotive Power Management IC (PMIC) with CAN-FD transceiver
- JTAG integrated programmer anddebugger
- 5 CAN-FD transceivers (including the one integrated in the SPSB0813 PMIC)
- 1 connector for I2C/UART serial communication
- Wakeup and reset buttons
- 2 general-purpose connectors (8 pins each)
- 2 SPI ports
- One plug connector to plug in an eventual daughter board (e.g., a power distribution unit (PDU))
- Reverse battery-protection dedicated circuit
- L5963 integrated DC-DC converter for potential system supply
- Compact size: 110 mm x 100 mm
- The board belongs to the AutoDevkit ecosystem

1.2 Main components

Figure 2. AEK-COM-10BASET evaluation board, top view: main components

1. CAN line
2. CAN line
3. CAN line
4. I2C/UART
5. Wake-up button
6. SPSB0813 Automotive Power management IC with LIN and CAN-FD
7. CAN line integrated in the SPSB0813 PMIC
8. 12 V power supply
9. L5963DN automotive dual monolithic switching regulator with LDO
10. CAN line
11. Daughter board connector
12. JTAG connector
13. SPI connectors
14. General-purpose connectors
15. Ethernet connector
16. Ethernet connector
17. Reset button
18. 10BASE-T1S Ethernet PHY transceiver
19. 10BASE-T1S MAC-PHY Ethernet Controller with SPI
20. SPC58EC80E5QMC1Y 32-bit Power Architecture MCU for Automotive General Purpose Applications - Chorus family



1.3 Embedded devices

1.3.1 SPC58EC80E

This SPC58EC line, 32-bit Power Architecture automotive microcontroller embeds two processor cores as well as a hardware security module.

The main features are:

- Two main cores
- Single-precision floating point operations
- High performance e200z420n3 dual core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 180 MHz
- 4224 KB (4096 KB code flash + 128 KB data flash) on-chip flash memory: it supports reading during program and erase operations, while multiple blocks allow performing the EEPROM emulation
- 176 KB HSM dedicated flash memory
- 384 KB on-chip general-purpose SRAM
- Multichannel direct memory access controllers
- One interrupt controller (INTC)
- Comprehensive new generation ASIL-B safety concept
  - ASIL-B of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Hardware security module (HSM) with HW cryptographic co-processor
- System integration unit lite (SIUL)
- Enhanced modular IO subsystem (eMIOS): up to 64 timed I/O channels with 16-bit counter resolution
- Enhanced analog-to-digital converter system:
  - Three independent fast 12-bit SAR analog converters
  - One supervisor 12-bit SAR analog converter
  - One 10-bit SAR analog converter with STDBY mode support
- Communication interfaces:
  - Eight CAN interfaces with advanced shared memory scheme and ISO CAN-FD support
  - Eight serial peripheral interface (DSPI) modules
  - Eighteen LIN and UART communication interface (LINFlexD) modules
  - Eight modular controller area network (MCAN) modules, all supporting flexible data rate (ISO CAN-FD compliant)
  - One Ethernet controller 10/100 Mbps compliant with IEEE 802.3-2008 standard
  - Dual-channel FlexRay controller
- Device and board test support for JTAG
- Low power capabilities:
  - Standby power domain with smart wake-up sequence

Note: For further information, refer to RM0407 or to the SPC58ECx datasheet.

1.3.1.1 *Features implemented on the AEK-COM-10BASET for communication with external peripherals/boards*

The MCU external peripherals implemented on the AEK-COM-10BASET are:

- Five CAN interfaces
- A UART communication interface shared with an I^2C interface
- Two serial peripheral interface (DSPI) modules
- Twenty-six general-purpose pins (ADCs, EMIOSs, INTERRUPTs, GPIO, and DSPIs)
- A JTAG interface
- A 10/100 Mbps Ethernet controller compliant with IEEE 802.3-2008 standard
- A DSPI to control the 10Mbps Ethernet

1.3.2 SPSB0813

The SPSB0813 is a power management system IC providing electronic control modules with enhanced power management functionality, including various standby modes to minimize the power consumption with programmable local and remote wake-up capability, as well as LIN and CAN-FD physical communication layers.

The device has one low-drop voltage regulator to supply the system microcontroller and one voltage tracker to supply external peripheral loads such as sensors. V1 is available with a fixed rail 3.3 V and V1 overvoltage detection and protection solution, while V2 is a low dropout tracking regulator that embeds one 5 V or 3.3 V regulator, configurable via SPI. It can be configured as tracker of V1 or a linear independent LDO. Moreover, the device features four high-side drivers to supply LEDs and sensors. All outputs are short-circuit protected and implement open-load diagnosis.

The AEK-COM-10BASET host an SPSB0813 device that supplies the microcontroller and the remaining part of the board.

The main features of the SPSB0813 are:

- AEC-Q100 qualified
- One 3.3 V low-drop voltage regulator (V1) for microcontroller
- One configurable 3.3V or 5V, selectable via SPI, low-drop voltage regulator V2 tracker for V1 and with off-board protection
- Maximum current capability of 250 mA for V1 and 100 mA for V2
- No electrolytic capacitor required on regulator outputs
- Very low quiescent current in standby modes (typ. 15 µA)
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog
- ISO 17987-4/2016-compliant LIN transceiver
- CAN-FD transceiver with local failure and bus failure diagnosis
- Complete 2-channel contact monitoring interface (WU1 and WU2 input pins) with programmable cyclic sense functionality. WU2 also with DIR functionality
- Programmable periodic system wake-up feature
- STM standard serial peripheral interface (32Bit/ST-SPI)
- 4 HS drivers for 0.14 A (RON = 7 Ω) suitable to drive external LED modules with high input capacitance value or to also supply external contacts
- Internal 10-bit PWM timer for each standalone high-side driver
- Buffered supply for all voltage regulators
- DIAGN output pin for fail-safe signalization
- Current monitor output for all internal high-side drivers
- Open-load diagnosis for all outputs
- Overcurrent protection for all outputs
- V1 overvoltage detection and protection
- Device contains temperature warning and protection
- Thermal cluster

Note: For further information, refer to SPSB081 datasheet.

1.3.2.1 *Features implemented on the AEK-COM-10BASET*

All SPSB0813 features have been implemented on the board, except high-side driver functionalities, which are out of our application scope. The main implemented features are:

- A 3.3 V low-drop voltage regulator (V1) for microcontroller
- A 5 V low-drop voltage regulator (V2) to supply the internal CAN, configurable via SPI
- WU1 pin to implement the local wake-up

Note: To exploit the device full potential, refer to AEK-POW-SPSB081.

1.3.3 L5963

The L5963 chip belongs to the STMicroelectronics Power Management IC and System Basis Chip family. It is a dual step-down switching regulator with internal power switches, high-side driver and a low drop-out linear regulator that can operate as standby regulator or normal LDO.

In addition to an adjustable voltage detector, voltage supervisors are available. The two DC-DC converters can work in free-run condition or synchronize themselves to an external clock. This IC is fit for the automotive segment, where load dump protection and wide input voltage range are mandatory. The AEK-COM-10BASET hosts an L5963 device that supplies the ethernet devices of the board, the internal ADC of the microcontroller and the external CAN transceiver. Alternatively, by using a different combination of the resistances available on the board, L5963 can be used to power the entire board instead of the SPSB0813.

The two switching regulators are exploited in order to have a maximum 2 A of current capability and can be controlled directly from a GPIO of the microcontroller. In order to exploit the full current capability and features please refer to AEK-MCU-C4MINI1, having two independent L5963 ICs where one is standalone compared to the other one.

The main features are:

- AEC-Q100 qualified
- Two step-down synchronous switching voltage regulators with internal power switches:
  - Wide input voltage range (from 3.5 V to 26 V)
  - Internal high-side/ low-side NDMOS
  - 3.0 A load current
  - 250 kHz free-run frequency
  - 250 kHz < f < 2 MHz synchronization range
  - Integrated soft-start
  - 180° PWM output phase shift
  - Programmable switching frequency divider by 1, 2, 4 or 8 between the two DC/DC regulators
  - Power good function
- One standby / linear regulator
  - Output voltage programmable with external resistor divider
  - 250 mA maximum current capability
- One high side driver
- All the regulators come with the following protections:
  - Independent thermal protection on all regulators
  - Independent current limit on all regulators
- Protected against short to ground and battery, loss of ground and battery, unsupplied short to battery
- Programmable under voltage battery detector
- Load dump protection
- Extremely low quiescent current in standby conditions
- Power good/adjustable voltage detector outputs to realize customized power up/down sequences

Note: For further information, refer to L5963 datasheet.

1.3.3.1 *Features implemented on the AEK-COM-10BASET*

All the features listed above have been implemented on the AEK-COM-10BASET board, except:

- The Power-good reset, the Power-good function, and the low voltage warning monitor that monitor, respectively, the linear regulator, DC/DC1 output and DC/DC2.

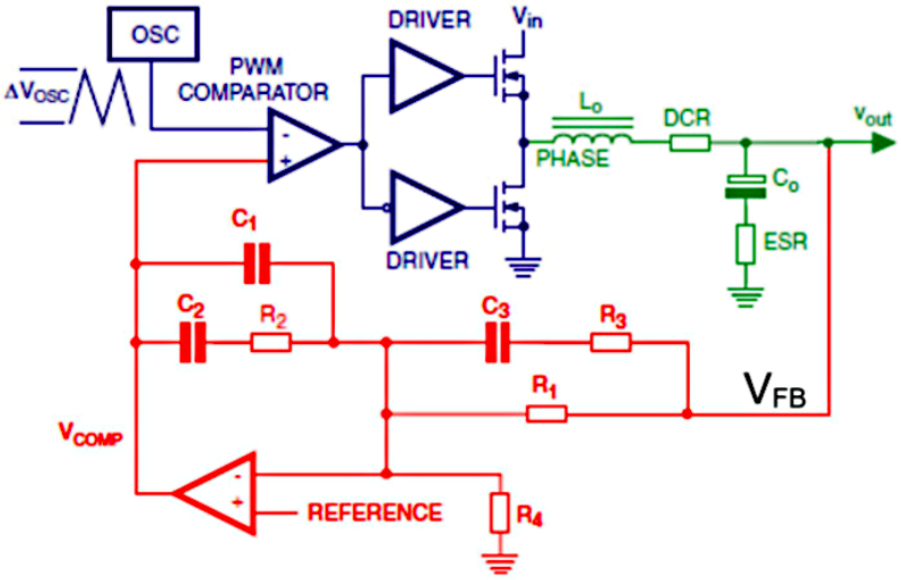
- The high-side output is not connected and left floating.

The external free running frequency is not connected and left floating.

1.3.3.2 *L5963 control*

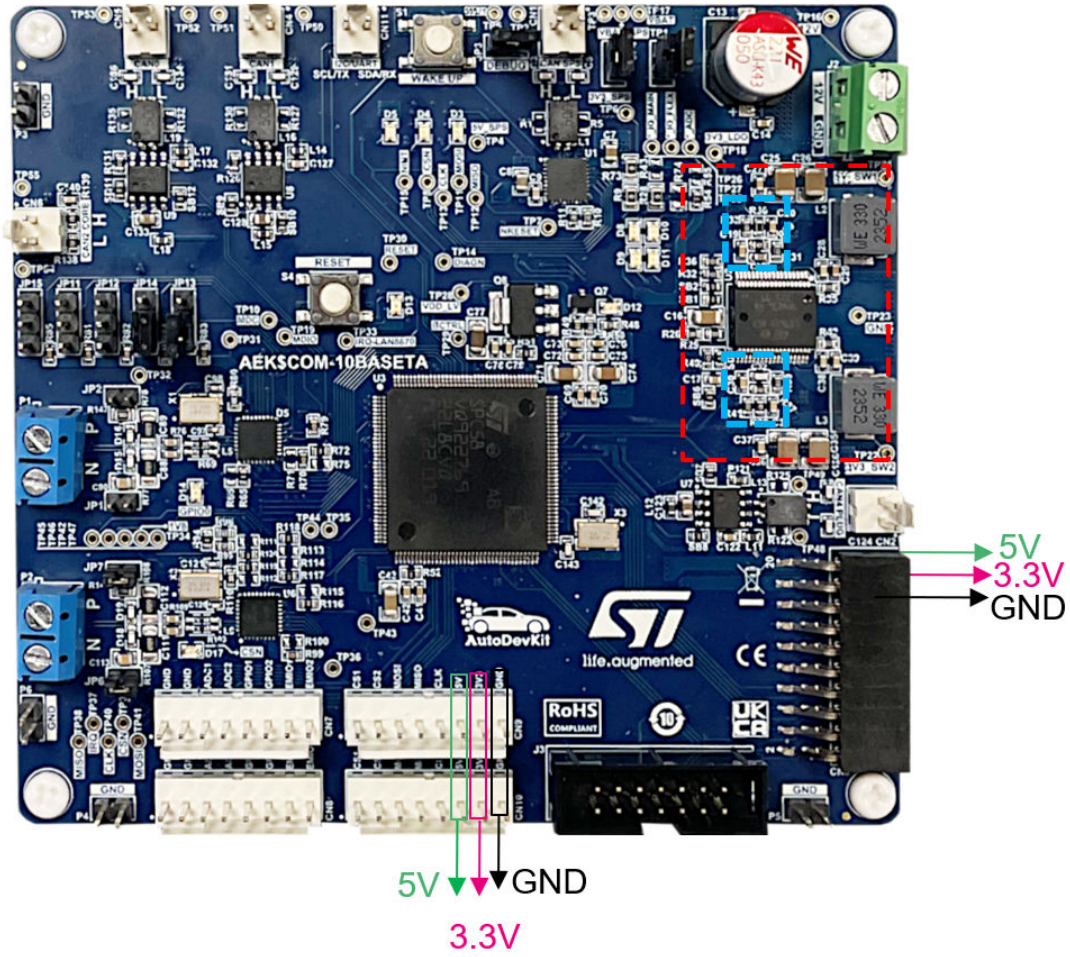
To ensure stability and dynamic performance, the L5963 output voltage can be regulated through a closed feedback loop system with a TYPE III compensation network, as shown in the figure below. The relative stability control was built to manage a load up to 2 A.

Figure 3. Closed loop system with TYPE III network



For example, in the figure above, when the output voltage V_{OUT} increases, the feedback voltage V_{FB} increases as well and the output of the negative feedback error amplifier decreases. So, the duty cycle decreases. As a result, V_{OUT} is pulled back to make V_{FB} = REFERENCE. The compensation network of the error op-amp can be a Type I, Type II or Type III feedback amplifier network. To optimize a voltage mode PWM converter, a Type III compensation network is usually needed to design a fast loop with a sufficient phase margin that ensures robustness and stability.

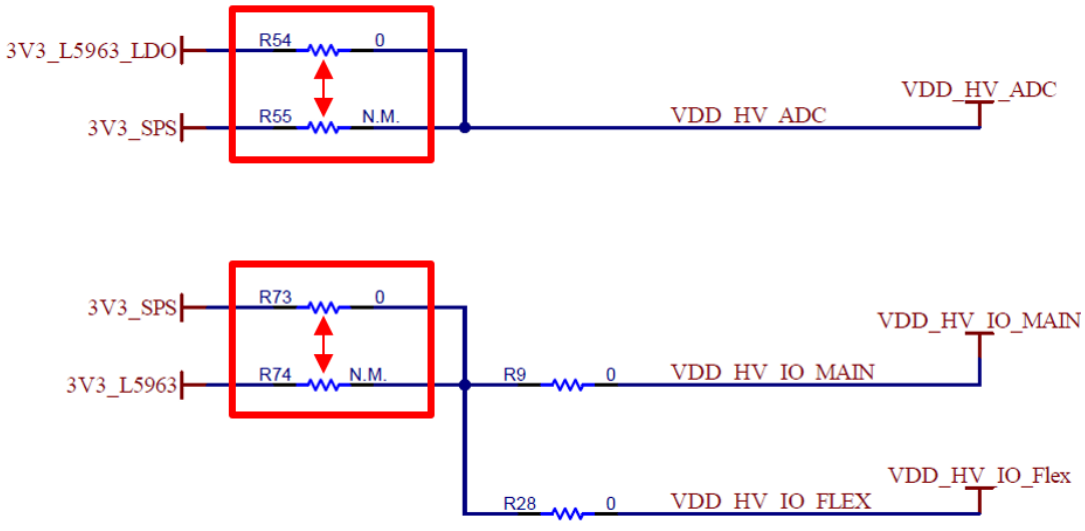
Figure 4. **L5963 supply system**



The device supplies internal peripherals. It also provides 3.3 V and 5 V externally, through CN3 plug connector, CN9 KK connector, and CN10 connector. Moreover, the 5 V supplies the CAN peripheral, while the L5963 internal LDO supplies the MCU ADC and Ethernet.

In applications not requiring full safety standards, the L5963 could supply the entire board just by changing some resistors, as shown in the images below.

Figure 5. **L5963 supply configuration**



As we can see in the figure above, the actual configuration involves the SPSB0813 supply related to the microcontroller. By replacing R74 with R73 and R54 with R55, we could exploit the L5963 supply. In our board, this configuration is not exploited as, through SPSB0813, we can access a higher level of safety and monitor the microcontroller thanks to the SPSB0813 internal diagnostic and watchdog.

1.4 AEK-COM-10BASET supply configuration

Figure 6. AEK-COM-10BASET scheme

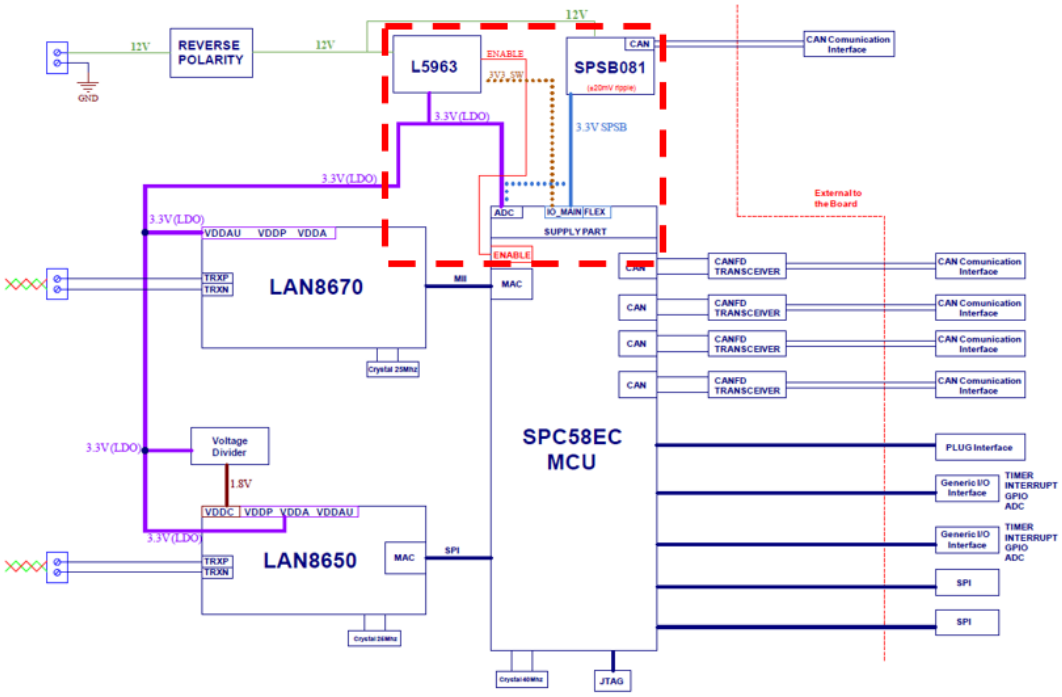
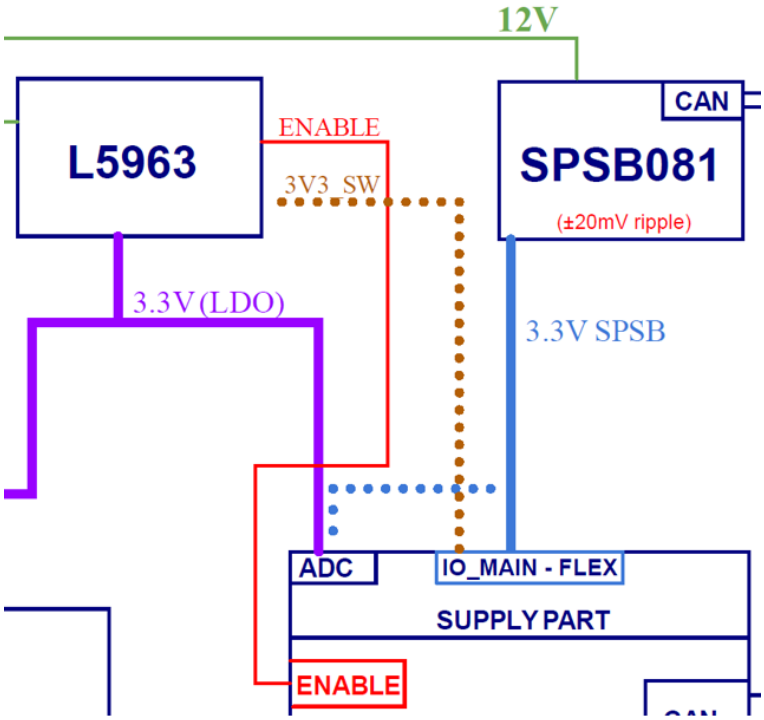


Figure 6. AEK-COM-10BASET scheme shows the AEK-COM-10BASET whole scheme, while Figure 7. Supply part zoom zooms the dotted red line area, which represents the supply configuration described in the previous paragraph.

Figure 7. **Supply part zoom**



1.5 10BASE-T1S protocol implementation

The AEK-COM-10BASET implements the 10BASE-T1S protocol key features highlighted in the introduction paragraph.

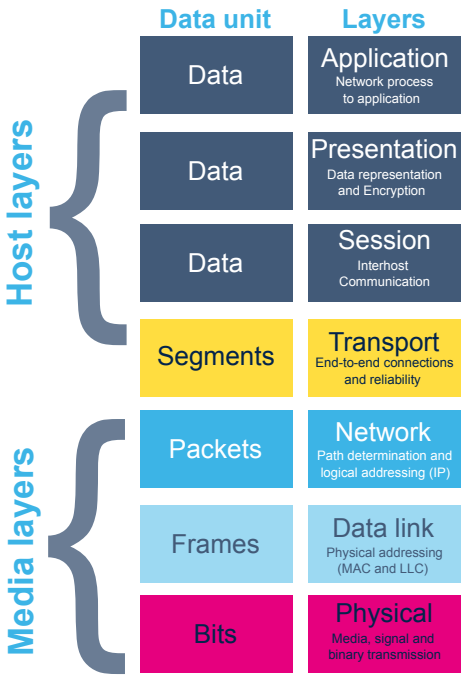
Our dedicated demo (Section 2.1: Available demos) effectively shows this protocol functionality, implementation, and potential.

The Open Systems Interconnection (OSI) reference model shown in figure 8 is a conceptual framework developed by the International Organization for Standardization (ISO).

This model splits the data flow of a communication system into seven abstraction layers to describe networked communication from the physical implementation of transmitting bits across a communication medium to the highest-level representation of data of a distributed application. Layers are interconnected with each other, according to the model structure.

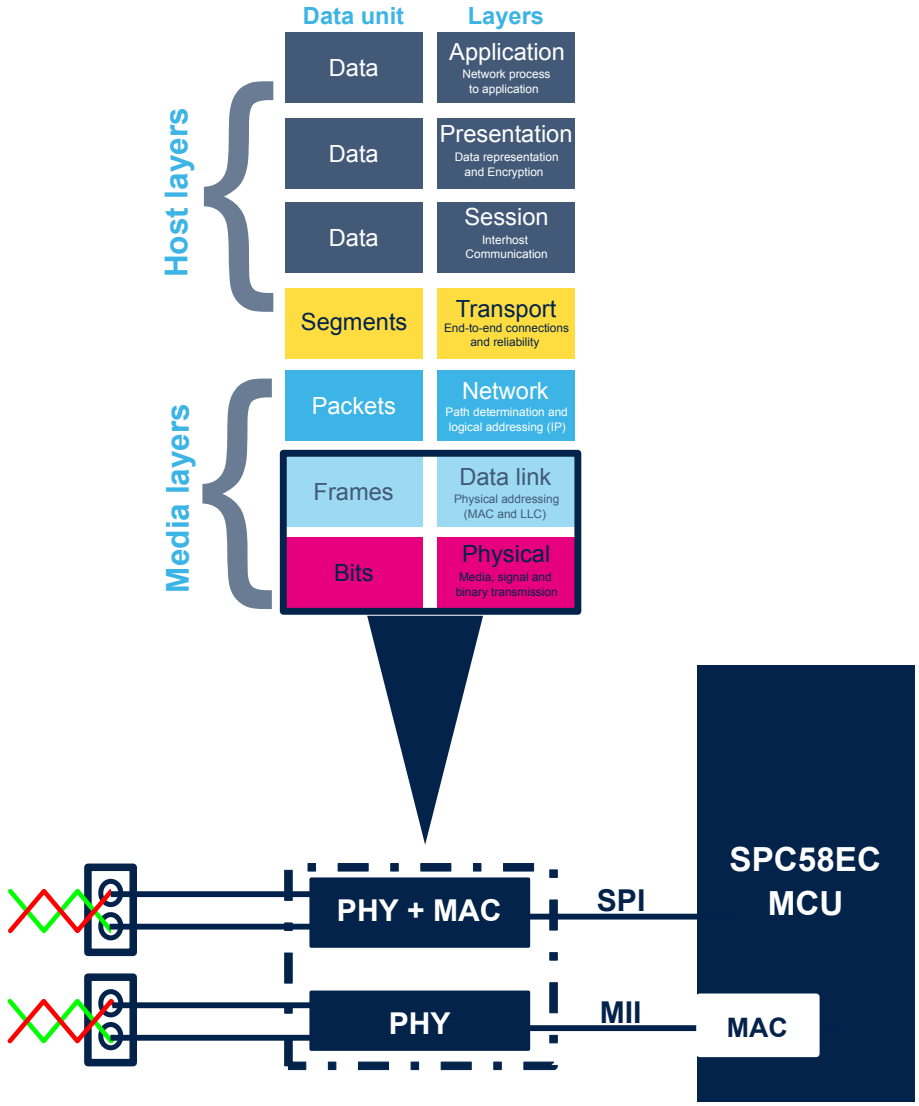
With reference to this model, our board implements the physical part and the physical part plus MAC in two different transceivers.

Figure 8. **OSI model**



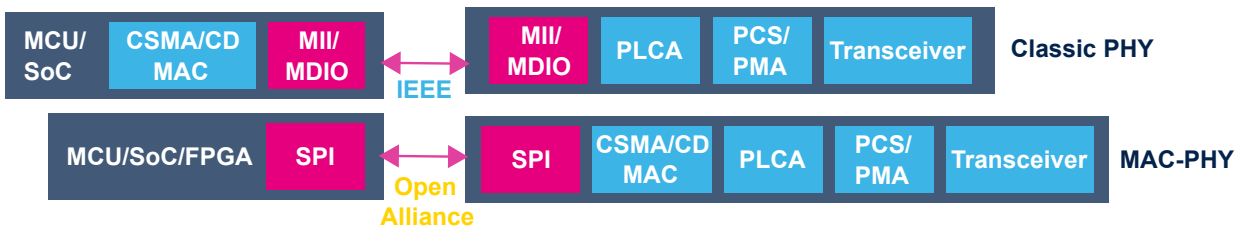
The first transceiver emulates the model last level, takes data bits coming from Ethernet, decodes them according to Manchester decoding, and through the Media-independent interface (MII), transmits them to the upper level, that is the Media Access Control (MAC), which is embedded in the SPC58EC80E5 microcontroller. The second transceiver encapsulates the physical part and the MAC within a single device that communicates with the microcontroller via SPI according to the OPEN Alliance 10BASE-T1x MAC PHY Serial Interface specification, Version 1.1.

Figure 9. **MAC-PHY and PHY transceiver implemented on the AEK-COM-10BASET**



The AEK-COM-10BASET allows you to manage two different 10BASE-T1s networks.
These two networks implement two different architecture types: classic PHY and MAC-PHY.

Figure 10. **Classic PHY and MAC-PHY architectures**



The classic PHY architecture is based on a Media Access Control (MAC), responsible for routing, CRC error identification, and access to the transmission means to avoid collisions. This MAC is implemented and managed by a microcontroller and, through an MII interface, communicates with any PHY transceiver.

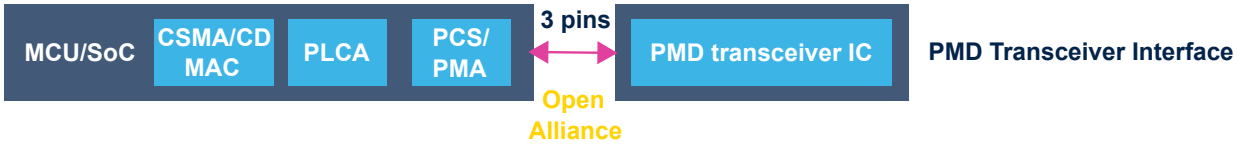
The MAC-PHY architecture, according to the Open Alliance specification, is based on a MAC entirely implemented and managed by a PHY device, aiming to replace proprietary communication technologies with standardized solutions. In fact, the microcontroller firmware has the only goal of configuring the MAC-PHY through SPI messages, without implementing the MAC, thus allowing to standardize its implementation.

Note: A new specification, called 10BASE-T1S PMD Transceiver (not implemented in our board), has been defined by Open Alliance.

The 10BASE-T1S PMD Transceiver is suited for embedded systems where the digital portion of the PHY is fully integrated into an MCU, an Ethernet switch core, or any other suitable host where only the analog part is left into a separate chip (i.e., the PMD transceiver).

This solution features a simple and cost-effective 3-pin clock-less interface between the host controller and the PMD transceiver chip. The PMD transceiver supports half-duplex, full-duplex, or both operation modes.

Figure 11. PMD transceiver interface



1.5.1 Classic PHY transceiver

The embedded Ethernet PHY, designed according to the IEEE Std 802.3cg-2019 specification,

Provides 10 Mbit/s half duplex transmit and receive capabilities over a single balanced pair of conductors.

This device interfaces with the Ethernet MAC via standard media-independent interface (MII). The MII is standardized by IEEE 802.3u and connects different types of PHYs to MACs. Being media independent means that different types of PHY devices for connecting to different media (i.e. twisted pair, fiber optic, etc.) can be used without redesigning or replacing the MAC hardware.

This PHY transceiver provides low power 10BASE-T1S PHY operation along with an ultra-low power sleep mode with flexible wake options.

Advanced PHY diagnostics are also provided for cable defect detection of shorts or opens, PLCA diagnostics, over-temperature, under-voltage detection, comprehensive status interrupt support, and various loopback and test modes.

The main features are:

- AEC-Q100 qualification
- High-performance 10BASE-T1S Ethernet PHY designed according to IEEE Std 802.3cg™-2019
  - 10 Mbit/s over single balanced pair
  - Half-duplex multidrop mixing segments up to at least 25 meters with up to at least 8 PHYs
  - Half-duplex point-to-point link segments up to at least 15 meters
- Media Independent Interface (MII)
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) media access control
- Physical Layer Collision Avoidance (PLCA)
  - Allows for high bandwidth utilization by avoiding collisions on the medium
  - Burst mode for transmission of multiple packets for latency-sensitive applications
  - Minimizes latency for time-sensitive applications by assigning multiple PLCA IDs per node
- Cable fault (open/short) diagnostics and Signal
- Single 3.3 V supply with integrated 1.8 V regulator
- Quality Indication (SQI) support
- Over-temperature and under-voltage detection
- Over-temperature and under-voltage protection

1.5.1.1 *Features implemented on the AEK-COM-10BASET*

The AEK-COM-10BASET features the characteristics listed above. They are partially used in the evaluation demo we developed. The CSMA/CD medium access control has been implemented.

The transceiver allows the physical part of the ISO/OSI stack to be implemented. This stack

encodes the digital signal on a transmission medium. It provides a standardized interface to the transmission medium, including a mechanical specification of electrical connectors and cables (for example, maximum cable length, an electrical specification of transmission line signal level, and impedance).

1.5.2 MAC-PHY transceiver

The board embeds a stand-alone Ethernet controller, which includes a 10BASET1S Ethernet physical layer transceiver (PHY), a Medium Access Controller (MAC), and a Serial Peripheral Interface (SPI) to enable low-cost microcontrollers to support standard networking software stacks over one inexpensive balanced pair of conductors (UTP cable).

The 10BASE-T1S PHY is designed according to the IEEE Std 802.3cgTM-2019 specification and provides 10 Mbit/s half-duplex transmit and receive.

The Carrier Sense Multiple Access/Collision Detection (CSMA/CD) manages access to the physical medium. Physical Layer Collision Avoidance (PLCA) is implemented to configure the transceiver with up to 9 transmit opportunities per bus cycle.

Advanced PHY diagnostics is provided for PLCA, over-temperature, under-voltage detection, status interrupts, and various loopback and test modes.

The main features are:

- High-performance 10BASET1S single-pair Ethernet PHY designed to IEEE Std. 802.3cg™ - 2019
- 10 Mbit/s over a single balanced pair
- Half-duplex multidrop mixing segments up to at least 25 metres with up to at least 8 PHYs
- Half-duplex point-to-point link segments up to at least 15 metres
- Physical Layer Collision Avoidance (PLCA):
  - Burst mode for transmission of multiple packets for latency-sensitive applications
  - Minimize latency for time-sensitive applications by assigning multiple PLCA IDs per node
- Carrier Sense Multiple Access/Collision Detection (CSMA/CD) media access control
- Integrated Media Access Controller (MAC)
- Support for Time Sensitive Networks (IEEE Std 802.1AS™/IEEE 1588™)
- Industry standard Serial Peripheral Interface (SPI)
- Over-temperature and under-voltage protection
- Cable fault diagnostics and Signal Quality Indication (SQI) support

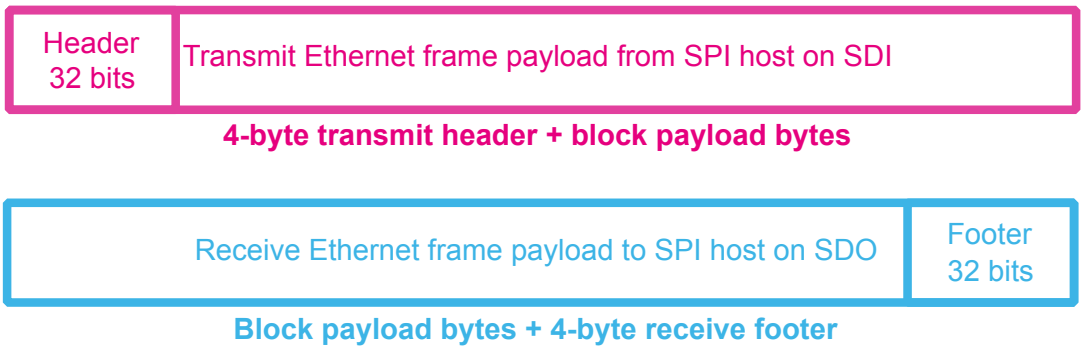
1.5.2.1 *Features implemented on the AEK-COM-10BASET*

This transceiver enables the physical part and the MAC part of the ISO/OSI stack. Its purpose is to regulate multiple nodes' access to a shared communication channel by preventing or managing collision occurrences. A collision occurs when two or more nodes simultaneously transmit data over the shared channel.

Our board implements the CSMA/CD medium access control and PLCA, solving transmission conflicts or collisions, thanks to broadcast or point-to-point wired local networks.

Moreover, this transceiver is responsible for packing and unpacking data to be sent or received through the physical layer, which decodes physical data, encapsulating the packet from the upper or lower layer into a new packet with a new header and tail, also used for control sequences. This data fragmentation into specific packets is called framing and individual packets are called frames.

Figure 12. Transmit and receive data block formats



Since this transceiver communicates with the microcontroller via SPI, based on the OPEN Alliance 10BASE-T1x MAC-PHY Serial Interface specification, data transactions are called *chunks*, with block payload data of 64 bytes.

The AEK-COM-10BASET features the characteristics listed above. They are partially utilized in the evaluation demo we developed. For example, our demo uses a LED to signal successful transmission of an Ethernet frame at the maximum velocity allowed. The transceiver acts as a gateway that allows a message to travel and be translated through multiple protocols, such as CAN-FD and 10BASE-T1S, to seamlessly implement automotive zonal architecture.

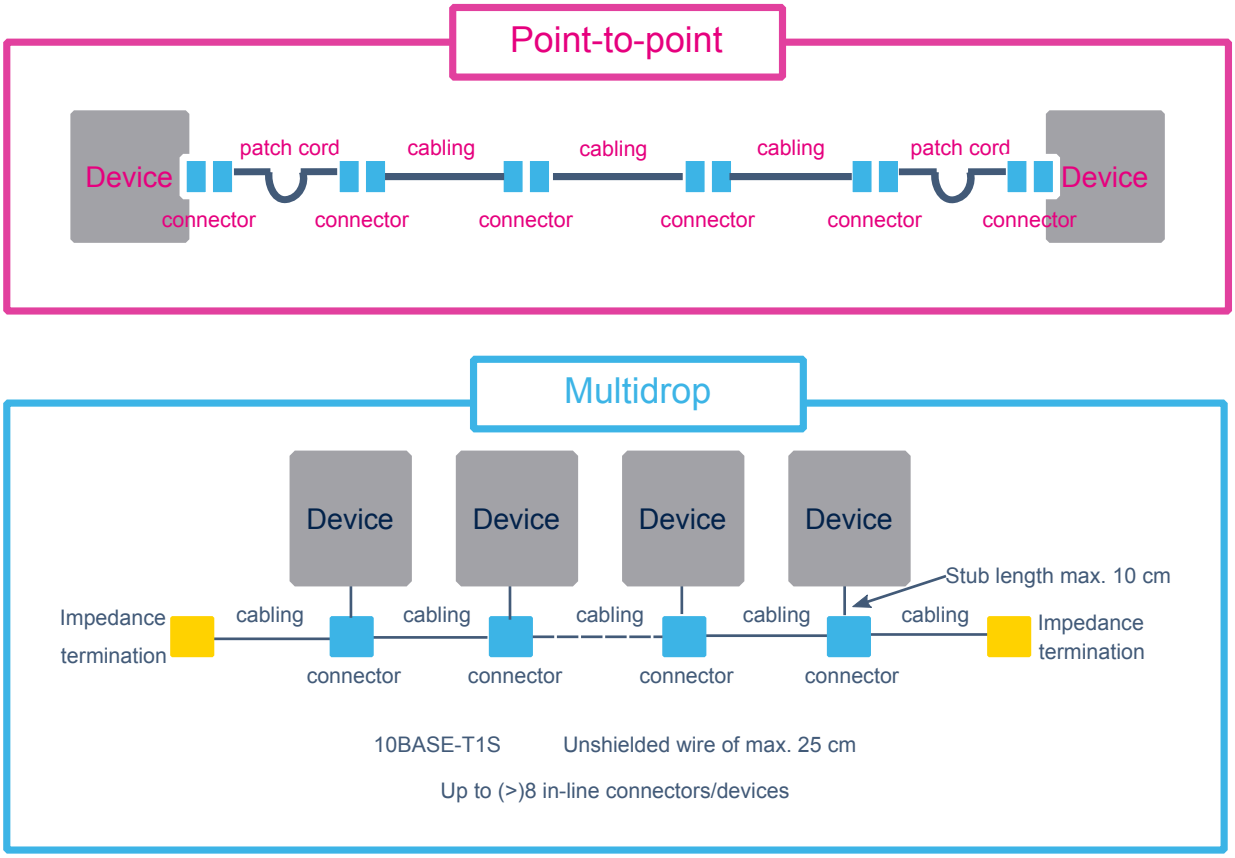
1.5.2.1.1 Physical layer collision avoidance (PLCA)

The physical layer collision avoidance (PLCA) is used for network access. Here a participant, referred to as the “head node”, sends a “beacon”, which signals a transmission cycle initialization. Each participant is assigned a fixed transmission slot in which it is authorized to transmit. Thus, bus access collisions are effectively prevented and the maximum time until the next transmission slot is known. Since a participant does not necessarily have to use its transmission slot to transmit an Ethernet frame, the cycle duration is not fixed. This represents an advantage compared to Flexray TDMA, where there is always a fixed slot for communication.

1.6 Example of Ethernet bus on the AEK-COM-10BASET

Using the two transceivers described previously, it is possible to build two types of networks: multidrop and point-to-point, as shown in the figure below.

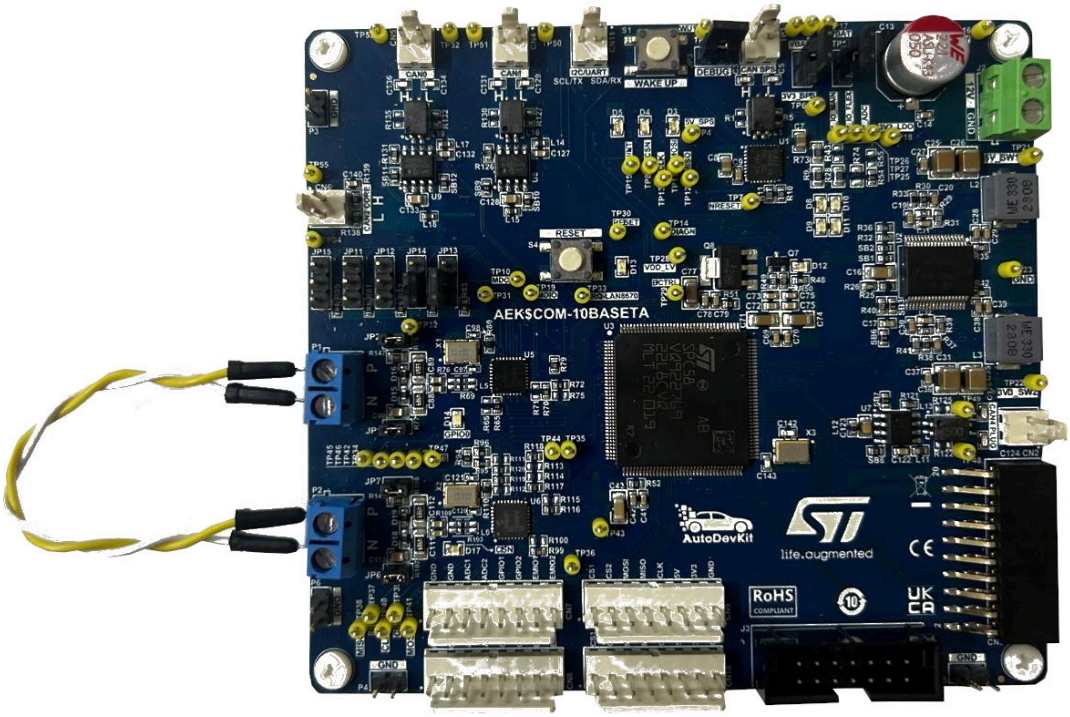
Figure 13. Comparison of P2P (top) and multidrop (bottom) configuration



10BASE-T1S protocol supports both configurations while other Ethernet protocols, notwithstanding higher data rates, only support point-to-point configuration with higher energy consumption. Additionally, using 10BASE-T1S, the combination of CSMA/CD and PLCA ensures greater efficiency.

The figure below shows the two internal transceivers used to emulate a P2P network.

Figure 14. **P2P configuration on the AEK-COM-10BASET**



1.7 Other ICs

The AEK-COM-10BASET hosts other noteworthy third-party integrated circuits (ICs).

1.7.1 CAN-FD transceiver chip

The CAN transceiver IC is designed for high-speed CAN-FD applications. It supports also CAN 2.0. The device meets the automotive requirements for CAN-FD bit rates exceeding 2 Mbps, low quiescent current, electromagnetic compatibility (EMC) and electrostatic discharge (ESD). The AEK-COM-10BASET features four CAN transceivers of this type.

1.8 Connector overview

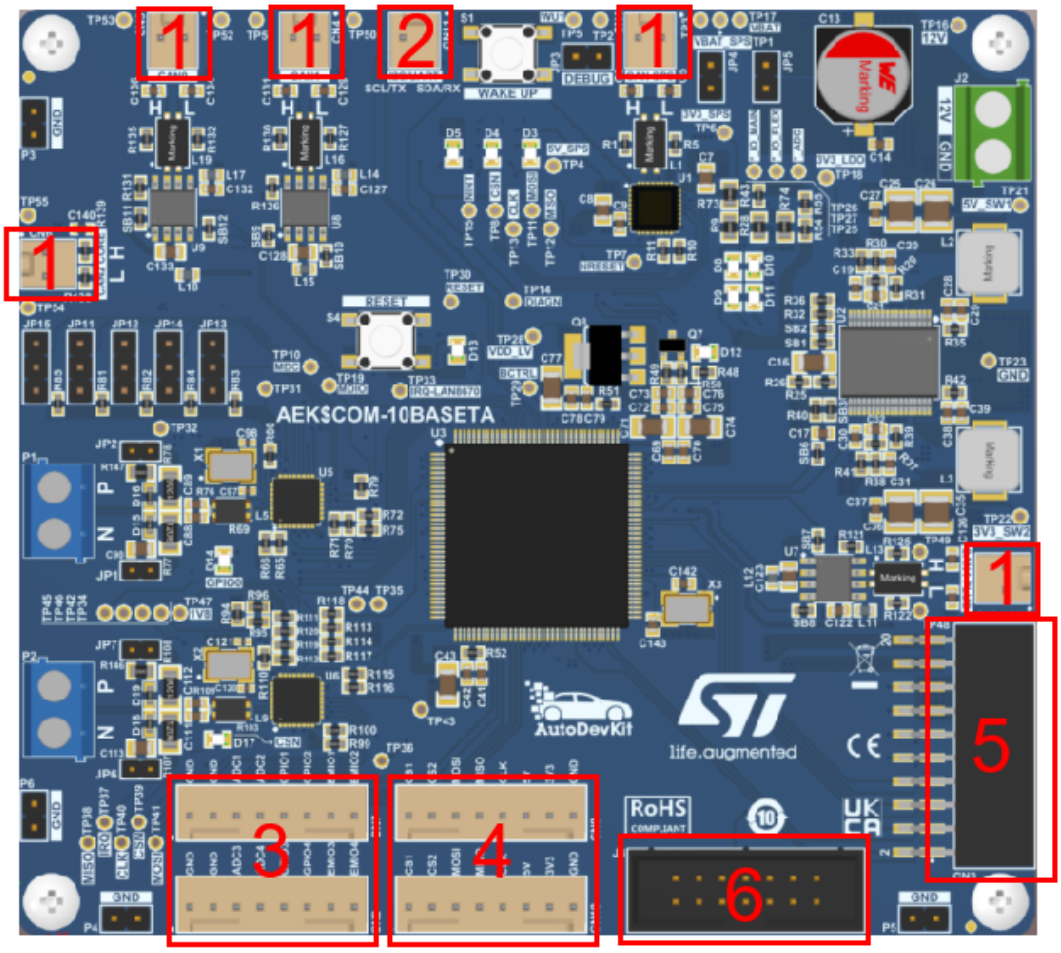
Connectors are grouped by type, to facilitate the connection and simplify the identification of the pins that can be used according to the user's application. The microcontroller peripherals are already mapped on the connector by pin direct connections.

1. CAN connectors
   - CN5: CAN0 peripheral
   - CN4: CAN1 peripheral
   - CN6: CAN2 peripheral
   - CN2: CAN4 peripheral
   - CN1: CAN3 peripheral
2. Serial connector:
   - CN11: UART/I2C peripheral
3. Generic I/O connectors:
   - CN7: ADC, GPIO, EMIOS and GND
   - CN8: ADC, GPIO, EMIOS and GND

4. SPI connectors:
   - CN9: DSPI2 peripheral (master-slave config.) and 5V&3.3V&GND supply voltage
   - CN10: DSPI5 peripheral (master-slave config.) and 5V&3.3V&GND supply voltage
5. PLUG connector:
   - DSPI0 peripheral (master-slave configuration): x6
   - INTERRUPT: x2
   - GPIO: x2
   - EMIOS: x2
   - ADC: x2
   - SUPPLY:
     - 3.3V: x2
     - 5V: x2
     - GND: x2

   This plug connector can be used for standalone pins or to connect a daughter board.
6. JTAG connector

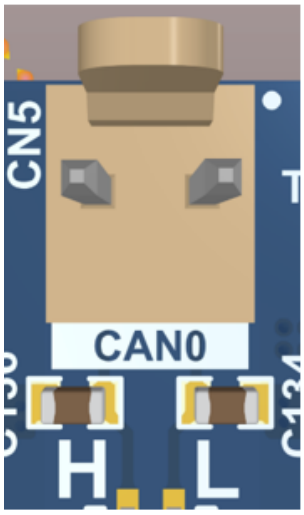
Figure 15. Connector overview



1.8.1 CAN connectors

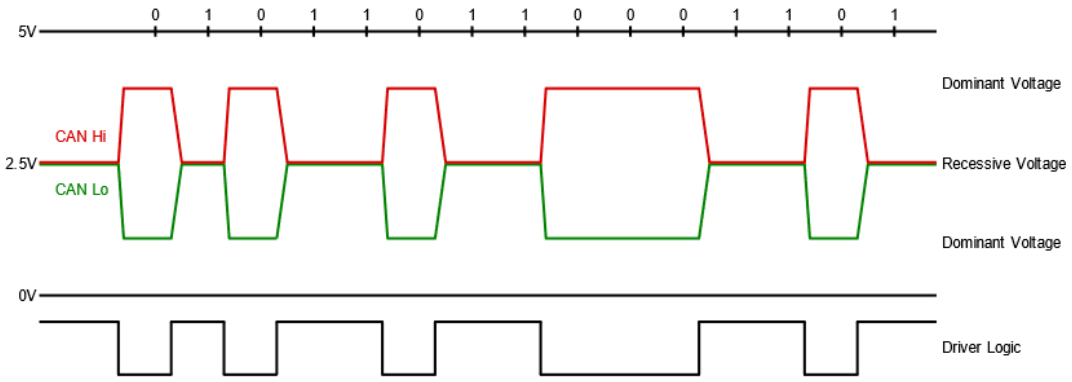
CAN connectors implement the CAN protocol, a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other. All the nodes are connected through a physically conventional two-wire bus, with a (nominal) characteristic impedance of 120 Ω. Thus, on our board, each CAN line has a resistor of 120 Ω. The same applies to the other onboard CAN connectors.

Figure 16. **Example of CAN connector**



The CAN protocol enables two signals, CAN high (CANH) and CAN low (CANL), which are either driven to a "dominant" state with CANH > CANL or not driven and pulled by passive resistors to a "recessive" state with CANH ≤ CANL. A 0 data bit encodes a dominant state, while a 1 data bit encodes a recessive state.

Figure 17. **Example of CAN signals**

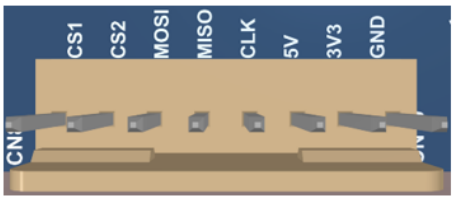


The AEK-COM-10BASET hosts four CAN connectors with CAN-FD transceivers to support high-speed applications. Another CAN-FD transceiver is available on the SPSB0813 device. Each connector has two pins that indicate high and low signals, as shown in the figure above.

1.8.2 SPI connectors

SPI connectors implement the SPI protocol for synchronous serial communication, used primarily in embedded systems for short distance wired communication between integrated circuits. SPI uses a master-slave architecture, where one main device (master) manages communication among peripheral devices (slaves) by driving clock and chip select signals. In our case, we can drive a maximum of two slaves through CS1 and CS2 signals through only one master.

Figure 18. **Example of SPI connector**



- CLK: Serial Clock (clock signal from master)
- MOSI: Master Output Slave Input (data output from master)
- MISO: Master Input Slave Output (data output from slave)
- CS: Chip Select (active low signal from master to address the slave and initiate)

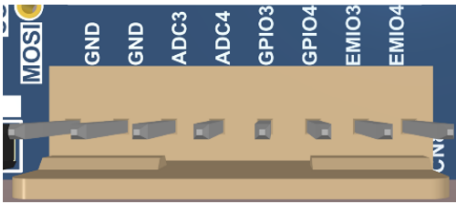
To start communication, the main SPI selects a slave device by pulling its CS low. During each SPI clock cycle, full-duplex transmission of a single bit occurs. The master sends a bit to the MOSI line while the slave sends a bit to the MISO line. Then, they read the corresponding incoming bit. This sequence is maintained even when only one-directional data transfer is intended. The AEK-COM-10BASET hosts two SPI connectors. Each connector has 8 pins. 5 pins are dedicated to the SPI protocol. 3.3 V and 5 V power supplies and a GND pin are also present.

Important: To connect the various KK connectors, use a cable with the maximum current capability allowed on the board, based on to 3.3 V and 5 V supply voltages.

1.8.3 Generic I/O connectors

The AEK-COM-10BASET hosts two generic I/O connectors. These connectors are a combination of the microcontroller different functionalities: general purpose I/O, ADC, EMIOS (e.g. timers), as shown below.

Figure 19. **Example of generic I/O connector**

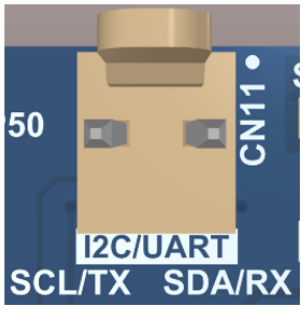


On this board, these pin numbers and types offer a wide range of options to take advantage of the microcontroller potential and to meet the final user's programming needs. A more experienced user may decide to re-map the MCU functionality through these pins. For example, a GPIO can be transformed into an INTERRUPT by configuring the microcontroller pin map editor through AutoDevKit Studio. CN7 and CN8 connectors also host GND pins.

1.8.4 Serial connector: UART and I²C

This connector implements UART and I²C communication protocols.

Figure 20. **UART and I²C connector**



UART protocol is used for asynchronous serial communication, which allows configuring data format and transmission speeds. It sends data bits one by one, from the least significant to the most significant, framed by start and stop bits so that precise timing is handled by the communication channel.

The onboard UART connector TX pin is used for data transmission, while RX pin is used for data reception.

This connector also implements I^2C protocol that is a synchronous, multi-master/multi-slave, single-ended, serial communication bus. It is widely used to connect lower-speed peripheral ICs to microcontrollers in short distance (i.e., for intra-board communication).

The onboard I^2C connector has two pins that indicate the SDA (serial data line) and SCL signal (serial clock line), as shown in the figure above. Both signals need pull-up resistors (not mounted on the board).

Note: The two protocols cannot be used simultaneously.

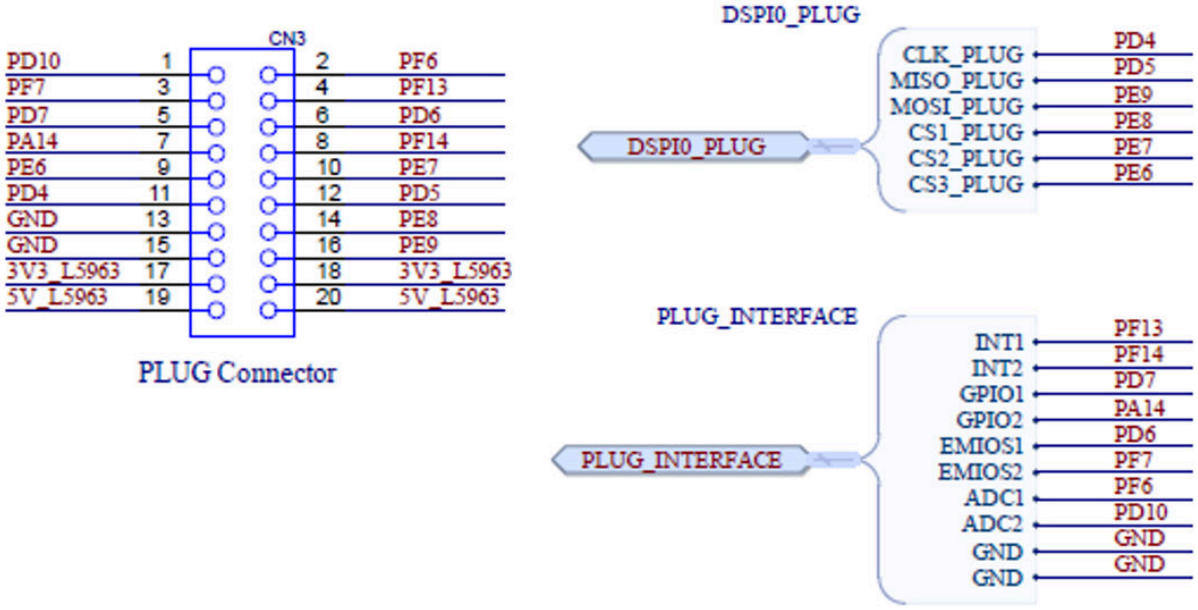
1.8.5 Plug connector

The AEK-COM-10BASET hosts a generic plug I/O connector. This connector is a combination of the microcontroller different functionalities: general purpose I/O, ADC, EMIOS (e.g., timers), INTERRUPT and SPI, as shown below.

Figure 21. Plug connector

The figure below shows this connector pins: one SPI with three chips select, two interrupts, two GPIOs, two EMIOSs and two ADCs. Moreover, there are two pins connected with 5 V and 3.3 V supply voltage lines. All these pins can be used to connect the AEK-COM-10BASET to a daughter board, as, for example, a Power distribution unit (PDU) evaluation board. As already said, a more experienced user may decide to re-map the MCU functionality through these pins, using AutoDevKit Studio.

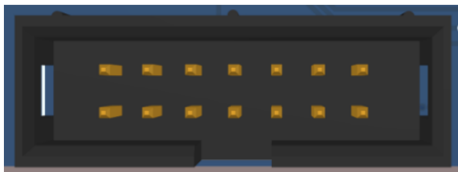
Figure 22. **Plug connector and related MCU pins**



1.8.6 JTAG connector

The JTAG connector allows application programming/debugging, by connecting the AEK-MCU-SPC5LNK dongle.

Figure 23. **JTAG connector**



2 AutoDevKit ecosystem

The application development employing our AEK-COM-10BASET evaluation board takes full advantage of the AutoDevKit ecosystem, whose basic components are:

- AutoDevKit Studio IDE (STSW-AUTODEVKIT)
- OpenOCD programmer and debugger

2.1 Available demos

In the AutoDevKit ecosystem, starting from release 2.4.0, the “SPC58ECxx_RLA AEK-COM-10BASET CAN-ETH Gateway” demo is available for the AEK-COM-10BASET evaluation board testing.

This demo simulates a domain control zone application as well as routing node among all the involved protocols showing how different messages are encapsulated and transferred to peripherals.

The figure below shows the demo application functional blocks. The remote task reads CAN messages from the external CAN sender board (at a speed of 125 kbps) and dispatches them to the Ethernet Client using the receiving queue. The gateway reads messages from the receiving queue and dispatches them by using the CAN protocol to send packets to the External CAN receiver board (at a speed of 125 kbps).

The gateway dispatches data messages among different communication protocols, with different message transmission speeds, communication paradigms, and message frames.

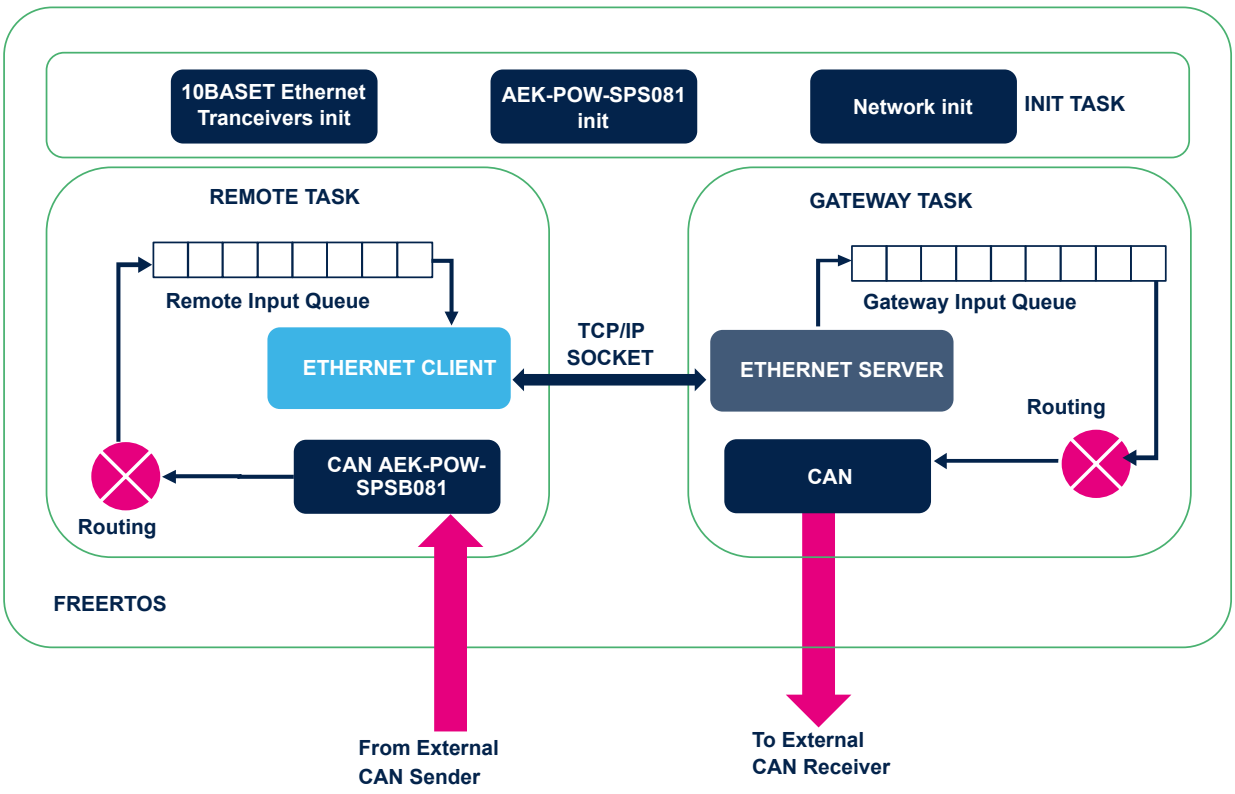
The application demo covers two scenarios:

- Ethernet to CAN;
- CAN to Ethernet

Client and server have been implemented on the same microcontroller. Message packets are sent via Ethernet through the TCP/IP stack, from the application layer to the PHY layer.

The PHY-MAC transceiver acquires messages through MII and transmits them via Ethernet. Instead, the PHY transceiver acquires messages through SPI and transmits them via Ethernet.

Figure 24. Demo application block scheme



The “initialization” task running in FreeRTOS:

- Initializes the AEK-COM-10BASET transceivers by invoking the low-level *DSPI* APIs in AutoDevKit and low-level *DWMAC* APIs.
- Initializes the AEK-POW-SPSB081 task by invoking watchdog activation through DSPI low-level driver activation (refer to SPSB081 datasheet for further information)
- Initializes the Network component to configure TCP/IP settings for server and client

The application software runs on a single core that is designed to implement a gateway. To simulate this gateway, FreeRTOS operating system schedules the remote device emulation task to start transferring messages among different protocols. The gateway device emulation task runs concurrently on the board.

The “remoteDevTask” (client) performs the following functions:

- Initializes CAN0 and CAN_SPS instances, by invoking the `can_lld_start()` low-level CAN API in AutoDevKit.
- Starts the Ethernet client to:
  - create a socket by using the `FreeRTOS_socket()` API
  - let the gateway task start the Ethernet server
  - connect a TCP socket to the gateway socket (`FreeRTOS_connect()`)
  - create a new task to receive (`FreeRTOS_recv()`)
- Waits on CAN_SPS peripheral for a CAN message sent from the external CAN sender board. CAN_SPS peripheral can receive two messages:
  - 0x7F, dispatched to the Ethernet Client and received by the Server
  - 0x7E, not dispatched to the Ethernet Client, but used to enable the AEK-COM-10BASET board low-power mode

Before creating its own task, the gateway prepares a dedicated queue (gatewayQueue), which is the returned handler used by all protocols:

```
gatewayQueue = xQueueCreate(GATEWAY_QUEUE_SIZE, GATEWAY_QUEUE_ITEM_SIZE);
```

Note: The operating system can dynamically allocate memory to support queues, even if this is normally not allowed in automotive safety compliant code.

The “gatewayTask" (server) performs the following functions:

- Starts the CAN0 instance;
- Starts the Ethernet server by opening a new listener socket and binding the server to this socket
- Waits for connection and starts the server task. Then, it:
  - receives packets;
  - adds messages to the queue;
  - notifies the gatewayTask that there is a pending job;

The gatewayTask will wait for a new message to route. On this event, it will:

- Get the message from the queue
- Route the data (invoking `send_to_can` to call the low-level API and transfer the message to the device)

Every time a new gateway message is inserted into the gateway queue, a specific task is woken up from the block state (in this state, the task does not consume any CPU time).

This task takes the gateway message from the queue and, depending on its type, extracts a routing table from the array of routing tables and uses it to forward the message appropriately to the peripheral device (CAN, LIN, SPI, ETH).

To summarize, the demo works as described in the following steps.

Step 1. The AEK-MCU-C4MINI1 sends a message to CAN1, which is then sent by the server as an Ethernet frame via the first Ethernet line.

Step 2. The client receives the Ethernet packet and checks its content, to verify that it is identical to the CAN message sent.

Step 3. Upon successful verification, the client sends a new CAN message through the second Ethernet line.

Step 4. The procedure starts again from step 1.

Step 5. To stop the demo, a CAN message is then sent to disable the SPSB0813, exploiting its low-power capabilities, to switch the AEK-COM-10BASET off.

2.2 Hardware configuration for the demo

To run the available demo, you need an AEK-MCU-SPC5LNK and an AEK-MCU-C4MINI1 to be connected to the AEK-COM-10BASET. Then, for the hardware setup, follow the steps below.

Step 1. Check the following jumper setting on the AEK-MCU-C4MINI1:

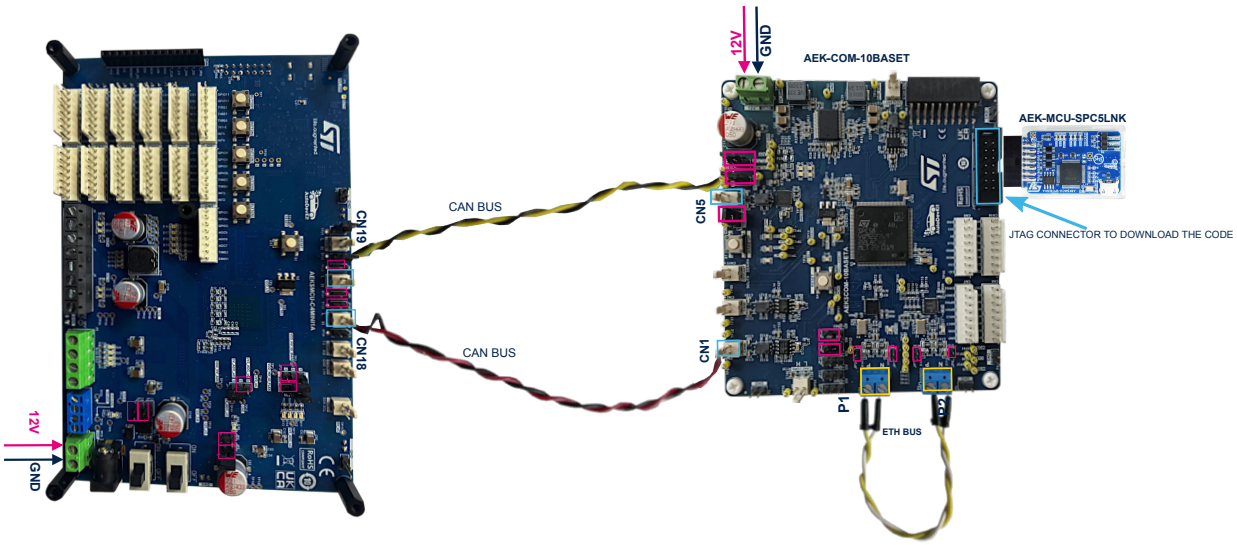
- JP2, JP3: **SHORTED 2-3**
- JP1: **SHORTED 2-3**
- JP4, JP5, JP8, JP9, JP10, JP11 JP12, JP13: **CLOSED**

Step 2. Check the following jumper setting on the AEK-COM-10BASET:

- JP13, JP14: **SHORTED DOWN**
- JP1, JP2, JP3, JP4, JP5, JP6, JP7: **CLOSED**

Step 3. After placing the jumper on the boards, link CAN connectors through a twisted cable pair, as shown in the figure below.

Figure 25. Hardware setup for the demo



Step 3a. Connect cables between the AEK-MCU-C4MINI1 CN18 connector and AEK-COM-10BASET CN1 connectors according to the table below.

Table 1. Connections between AEK-MCU-C4MINI1 CN18 connector and AEK-COM-10BASET CN1 connector

AEK-MCU-C4MINI1 CN18	AEK-COM-10BASET CN1
L	L
H	H

Step 3b. Connect cables between the AEK-MCU-C4MINI1 CN19 connector and AEK-COM-10BASET CN5 connectors according to the table below.

Table 2. Connections between AEK-MCU-C4MINI1 CN19 connector and AEK-COM-10BASET CN5 connector

AEK-MCU-C4MINI1 CN19	AEK-COM-10BASET CN5
L	L
H	H

Step 3c. Connect cables between P1 and P2 Ethernet connectors on the AEK-COM-10BASET according to the table below.

Table 3. Connection between P1 and P2 on the AEK-COM-10BASET

AEK-COM-10BASET P1	AEK-COM-10BASET P2
P	P
N	N

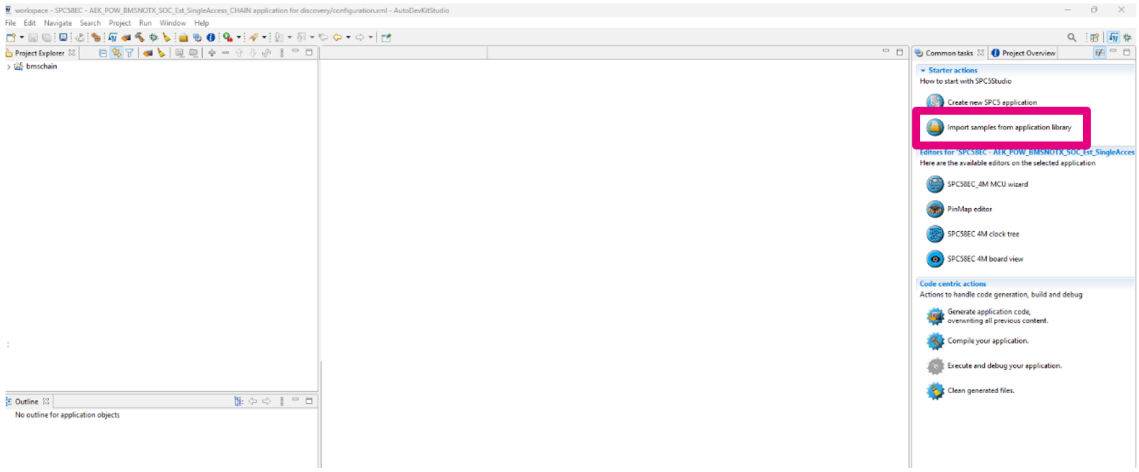
2.3 How to download and run the demo

Step 1. Connect the AEK-MCU-SPC5LNK to the AEK-COM-10BASET JTAG connector. Then, connect the AEK-MCU-SPC5LNK to your PC/laptop via USB cable.

Note: Remove the debug pin from the AEK-COM-10BASET before launching the demo.

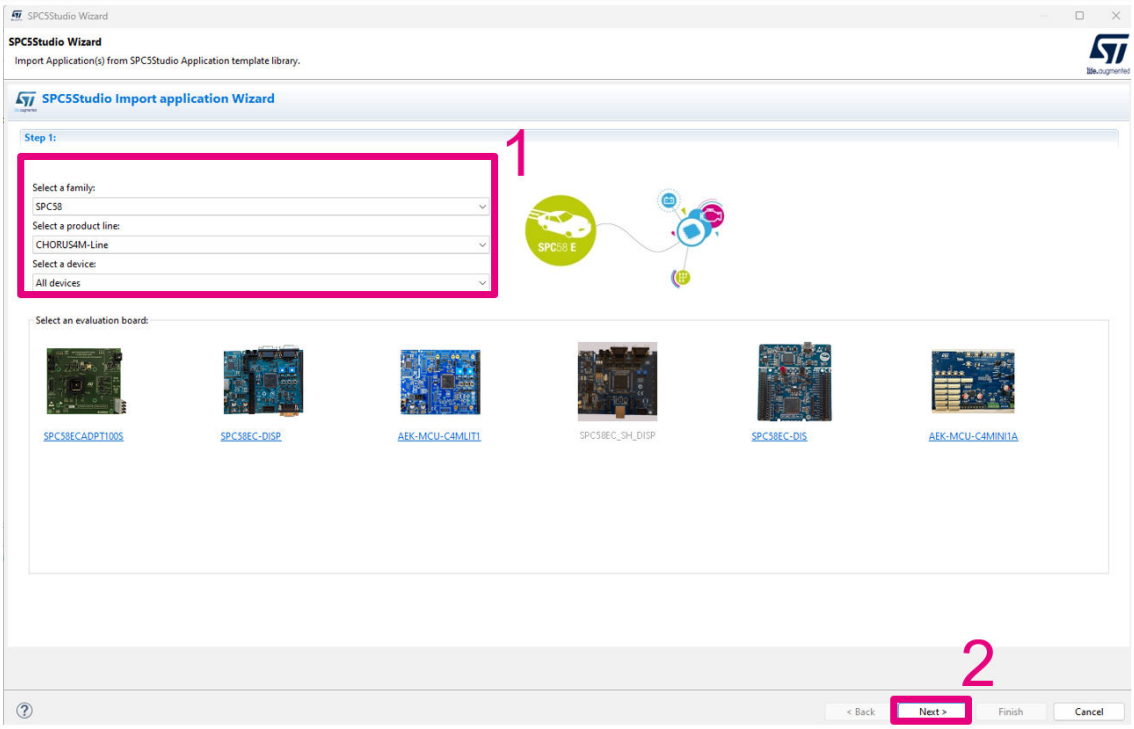
Step 2. Download and install the last version of AutoDevKit Studio. Then, click on “Import samples from application library”.

Figure 26. Importing sample from AutoDevkit library



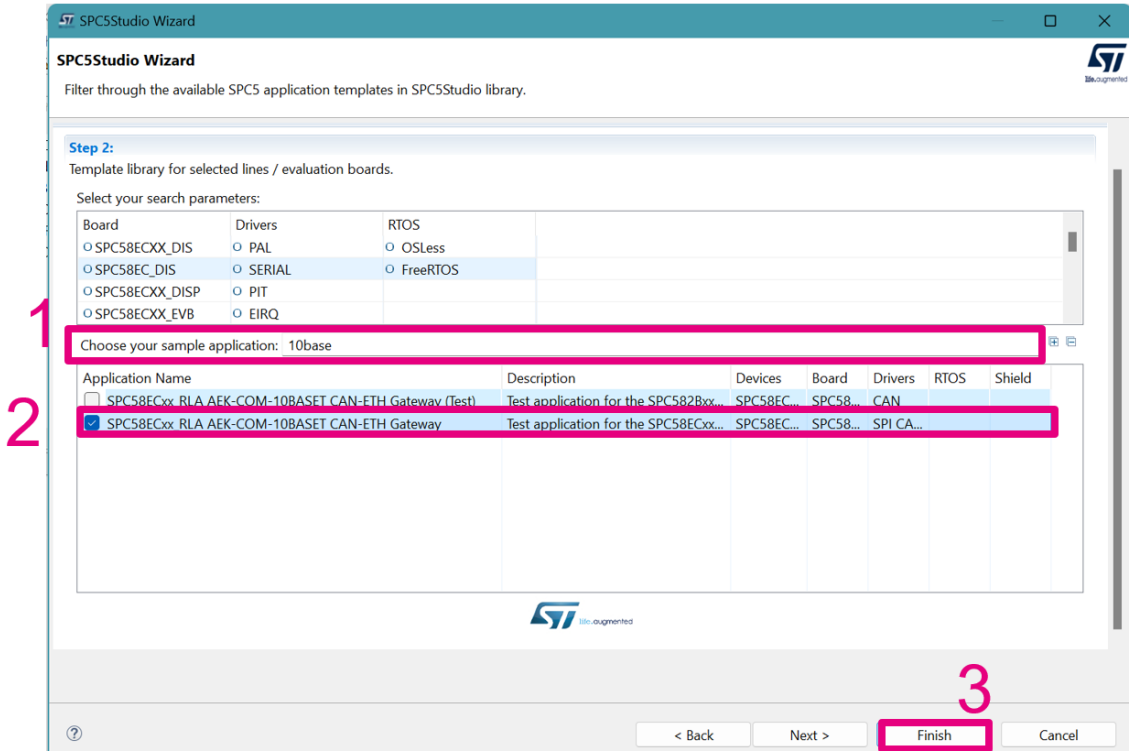
Step 3. Select the microcontroller family and the product line as shown below. Then, click on “Next”.

Figure 27. Selecting microcontroller family and product line



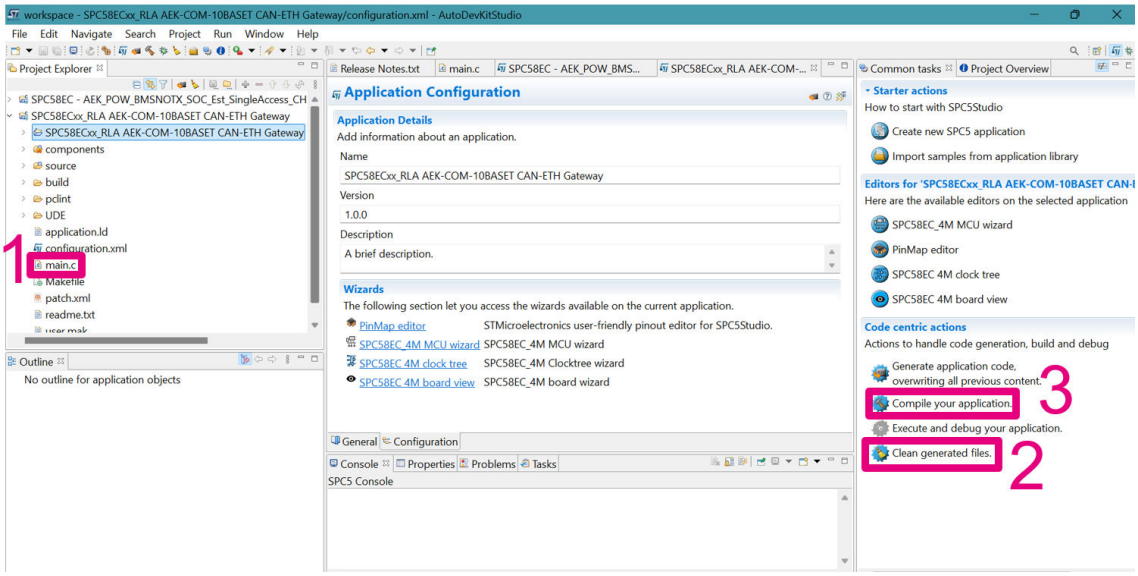
Step 4. Type “10baset” in the field highlighted below and select “SPC58ECxx_RLA AEK-COM-10BASET CAN-ETH Gateway” application. Then, click on “Finish”.

Figure 28. Selecting the application demo



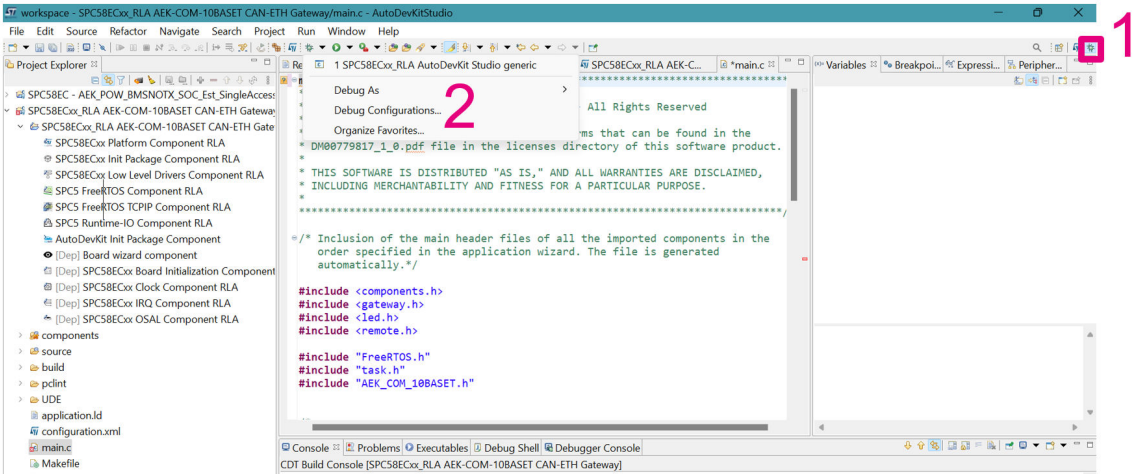
Step 5. Double-click on the main.c file. Then, clean and compile the selected project.

Figure 29. Cleaning and compiling the project



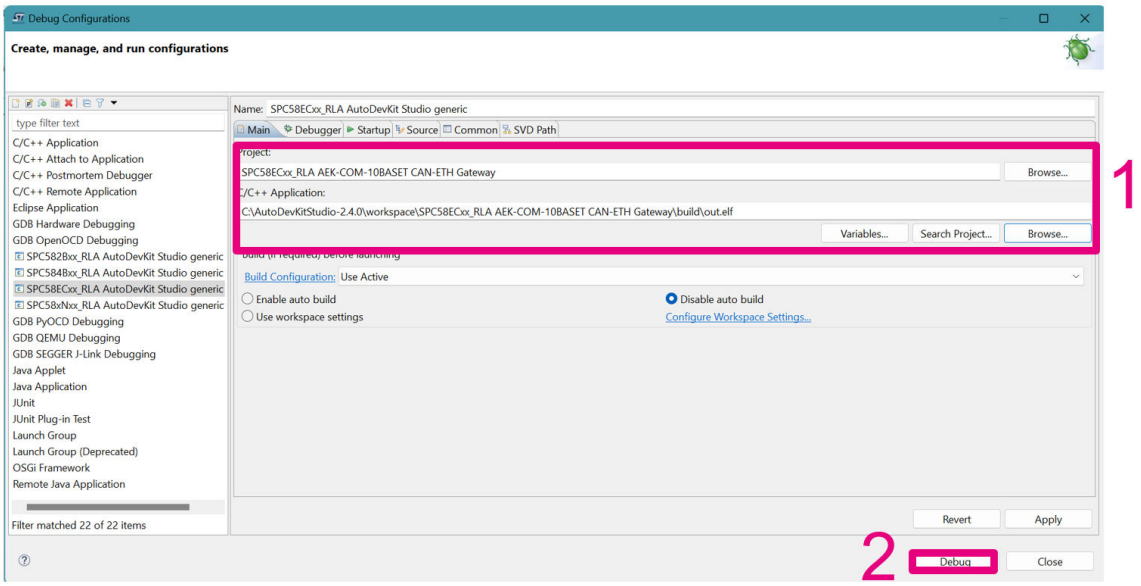
Step 6. Switch to “Debug” by clicking on the green beetle icon and then select “Debug Configurations”.

Figure 30. Debugging the project



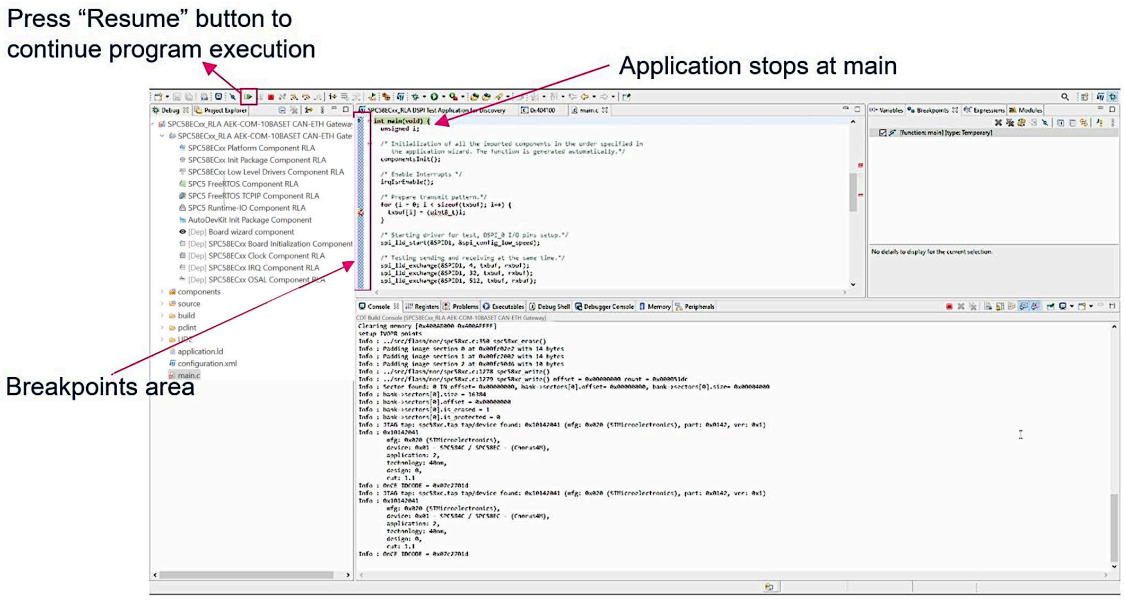
Step 7. Browse to your workspace and insert the path of the elf file in the project field. Click on Debug.

Figure 31. Debugging your out.elf file



Step 8. The console opens and shows your application code execution. The code execution stops at the main file. To continue executing the code, press resume. You can manually insert a breakpoint to stop code execution.

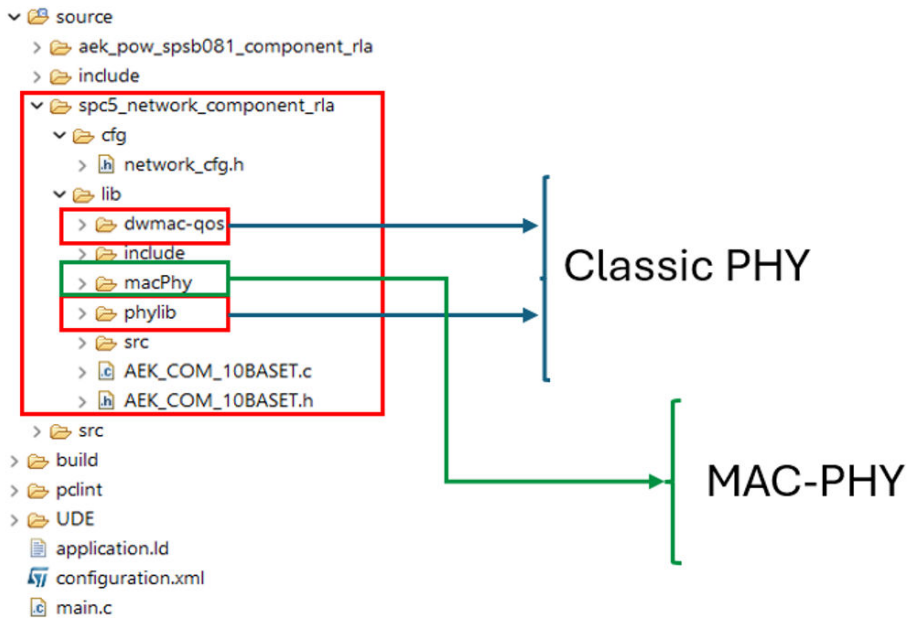
Figure 32. Code execution



2.4 10BASE-T1S software driver implementation

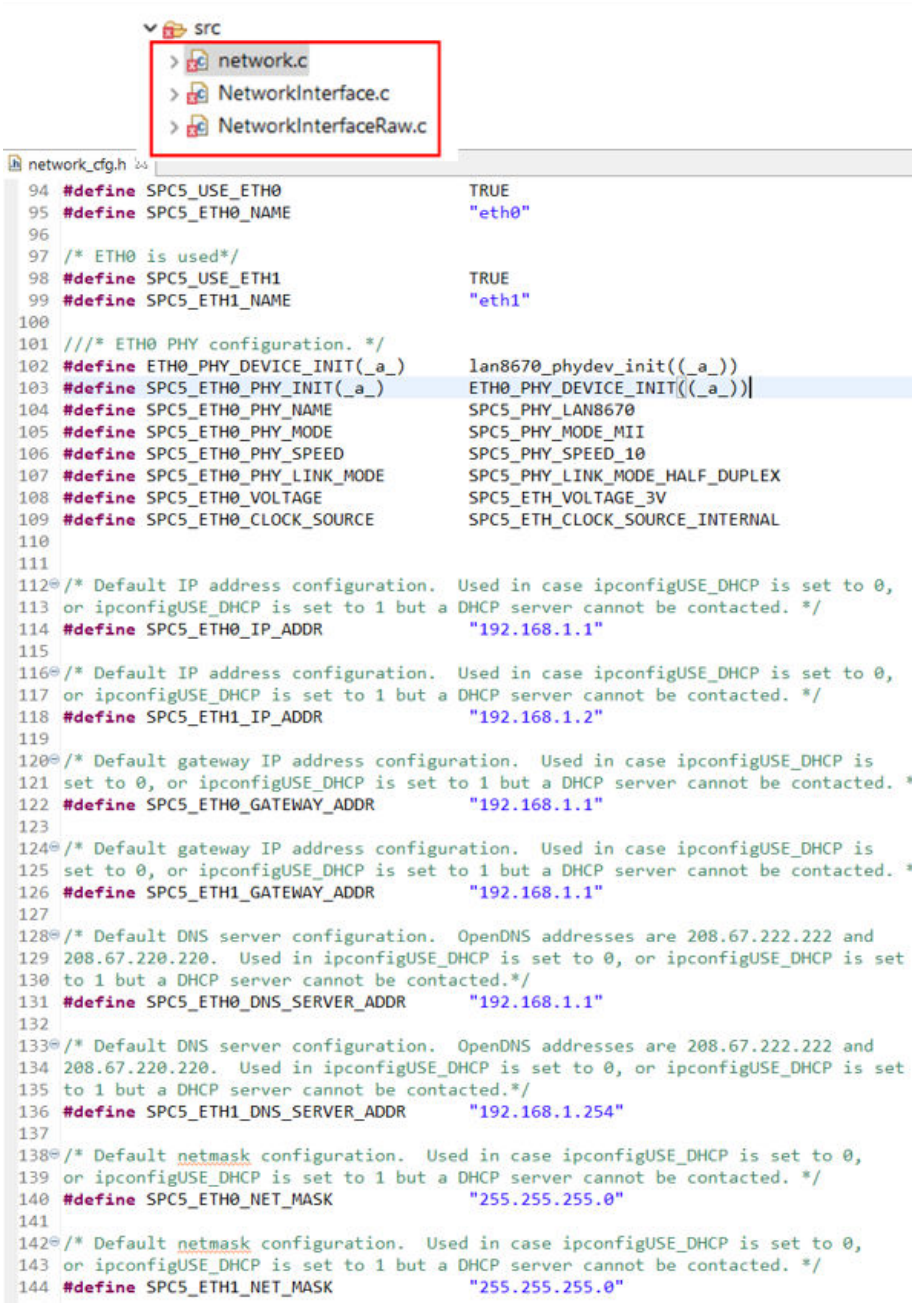
Referring to Section 1.5: 10BASE-T1S protocol implementation, in our “SPC58ECxx_RLA AEK-COM-10BASET CAN-ETH Gateway” demo, “spc5_network_component_rla” (under the “source” folder) includes both architecture drivers, as highlighted in the image below.

Figure 33. "spc5_network_component_rla" folder



Parameter configurations for both architectures are defined in the network_cfg.h file.
Configuration settings are included in the src folder.

Figure 34. **"src" folder**



Note: In the demo code, the ETH0 variable refers to the classic PHY architecture, whereas the ETH1 variable refers to the MAC-PHY architecture.

MAC/PHY Initialization

The `phy_init()` function initializes the PHY. This function is called by the `xNetworkInterfaceInitialise()` function included in the "NetworkInterface.c" file.

According to the network solution selected, the initialization phase can be summarized as shown in the following sequence diagram flows.

Figure 35. **ETH0 sequence diagram flow**

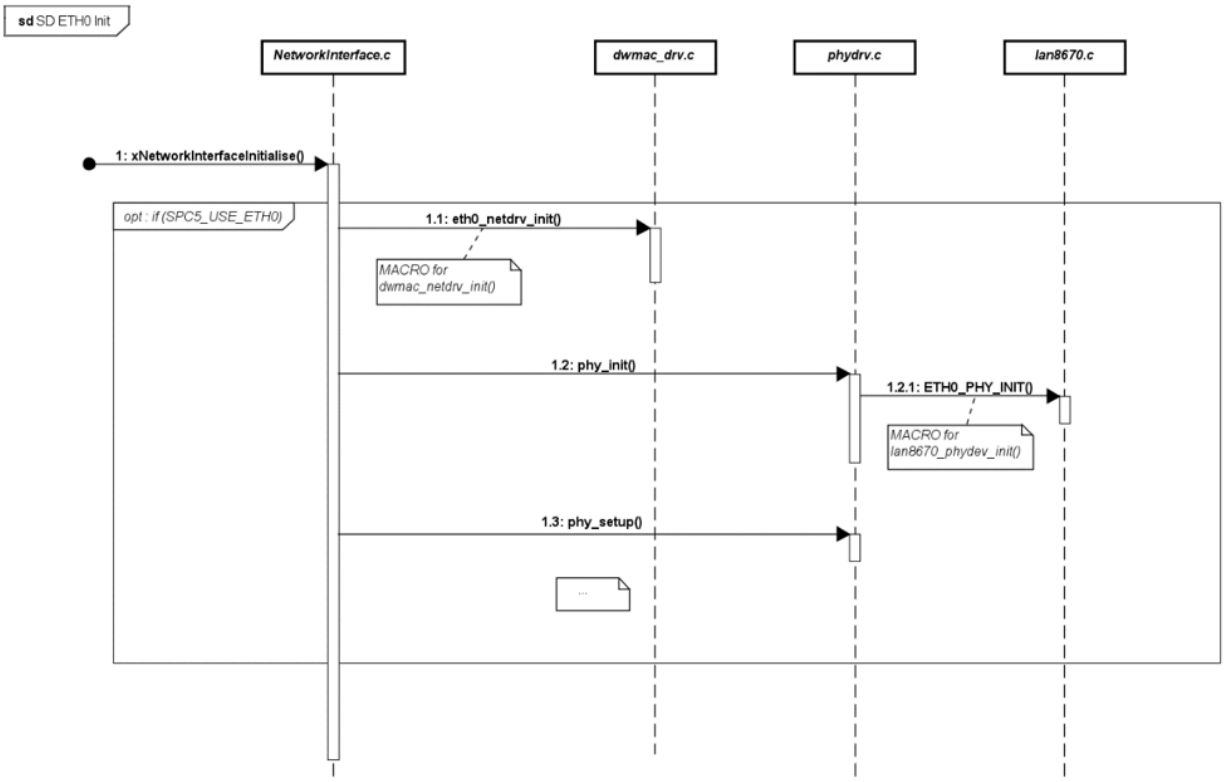
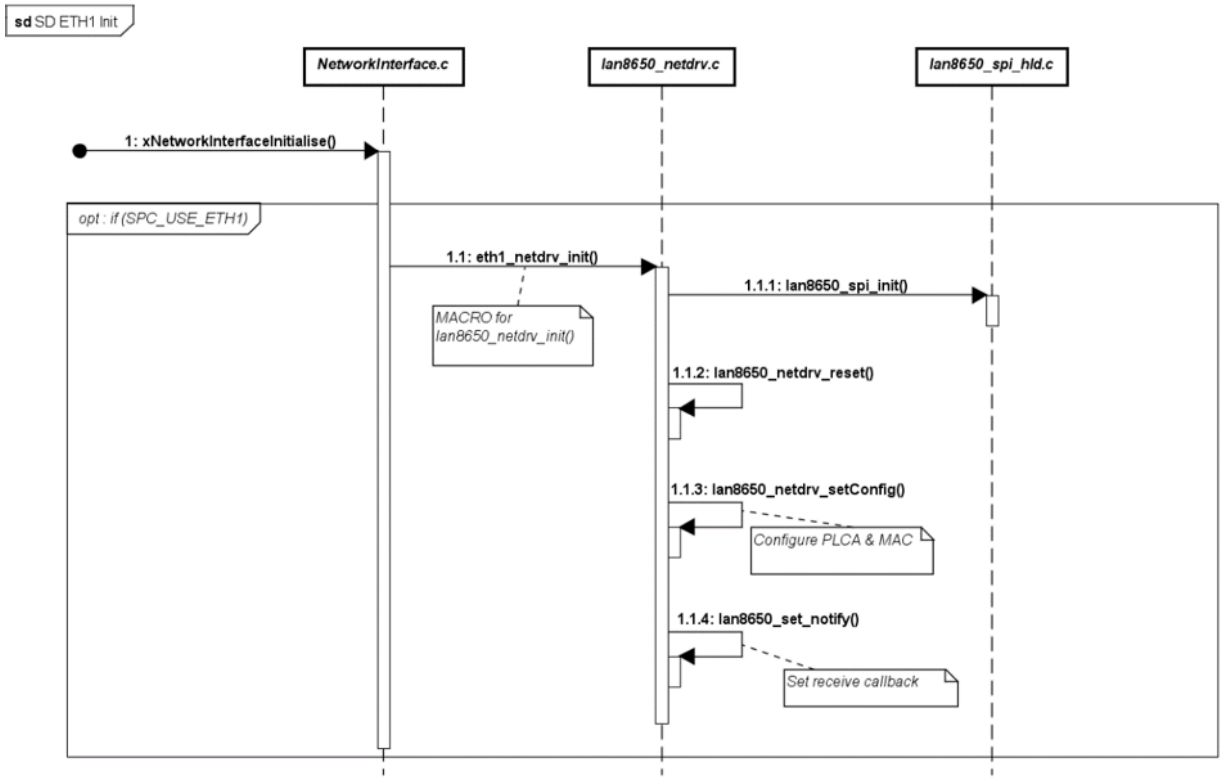


Figure 36. **ETH1 sequence diagram flow**

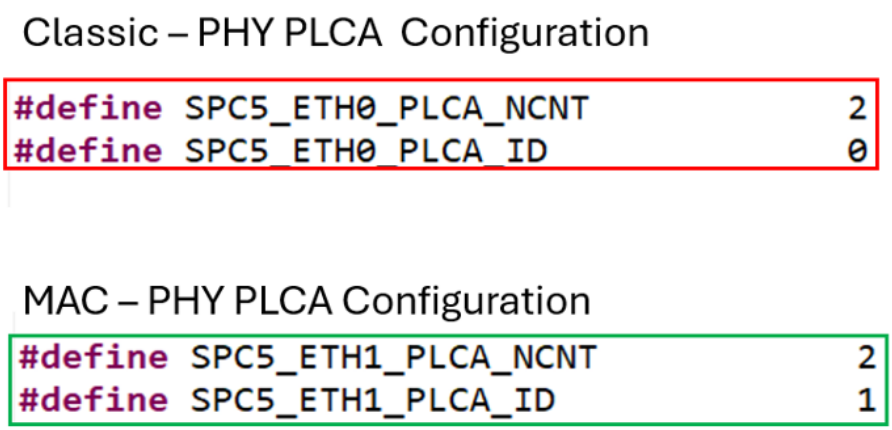


2.5 How to change PLCA configuration for network nodes

In the "network_cfg.h" file, you can configure the transceivers as coordinator or follower.

In our demo, we implemented a point-to-point network topology among the transceivers. The classic PHY transceiver has been defined as coordinator (`PLCA Node ID == 0`), whereas the MAC-PHY transceiver has been defined as follower (`PLCA Node ID != 0`).

Figure 37. PLCA configuration



`SPC5_ETH0_PLCA_NCNT` and `SPC5_ETH1_PLCA_NCNT` parameters are identical to each other and have been set at 2, as the two transceivers are the only components fo the point-to-point network implemented in our demo.

The classic PHY transceiver is the coordinator, whose PLCA Node ID corresponds to `SPC5_ETH0_PLCA_ID` set at 0.

The MAC-PHY transceiver is the follower, whose PLCA Node ID corresponds to `SPC5_ETH1_PLCA_ID` set at 1.

To change the network configuration (for example, to implement a multidrop topology), you have to change the parameter values described above in the "network_cfg.h" file.

Note: The ID that identifies each network node has to be unique and the coordinator ID is always equal to 0.

3 Schematic diagrams

Figure 38. **AEK-COM-10BASET circuit schematic (1 of 10)**

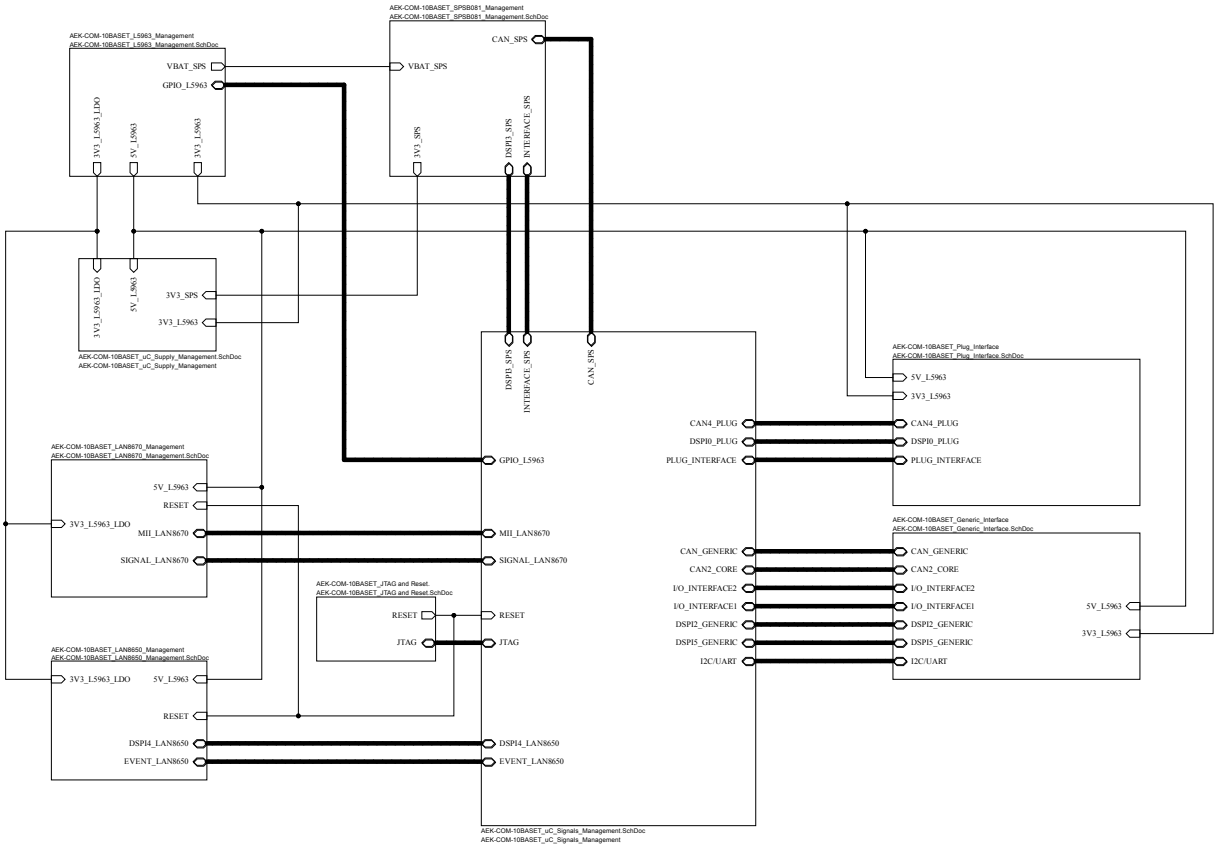


Figure 39. **AEK-COM-10BASET circuit schematic (2 of 10)**

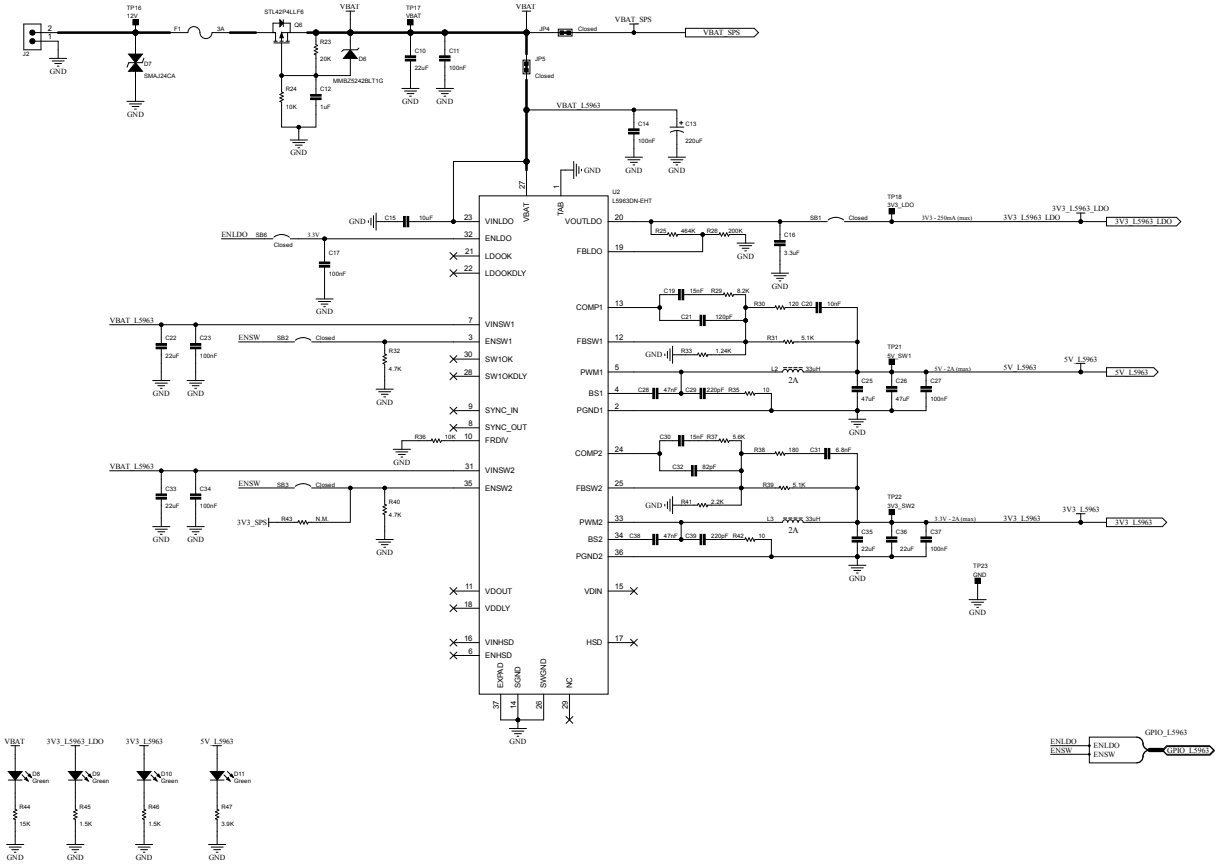


Figure 40. **AEK-COM-10BASET circuit schematic (3 of 10)**

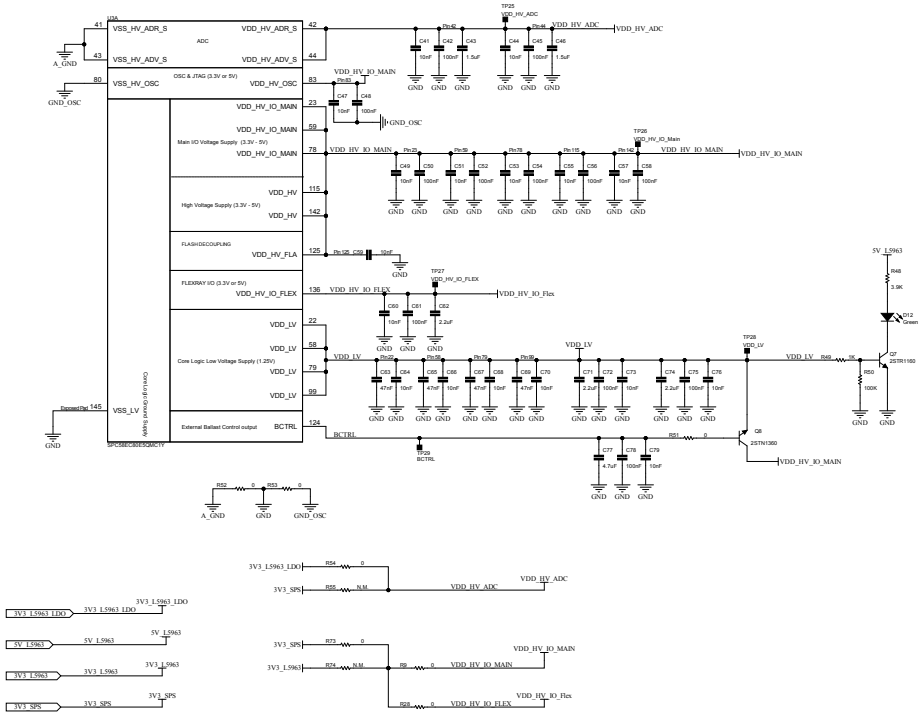


Figure 41. **AEK-COM-10BASET circuit schematic (4 of 10)**

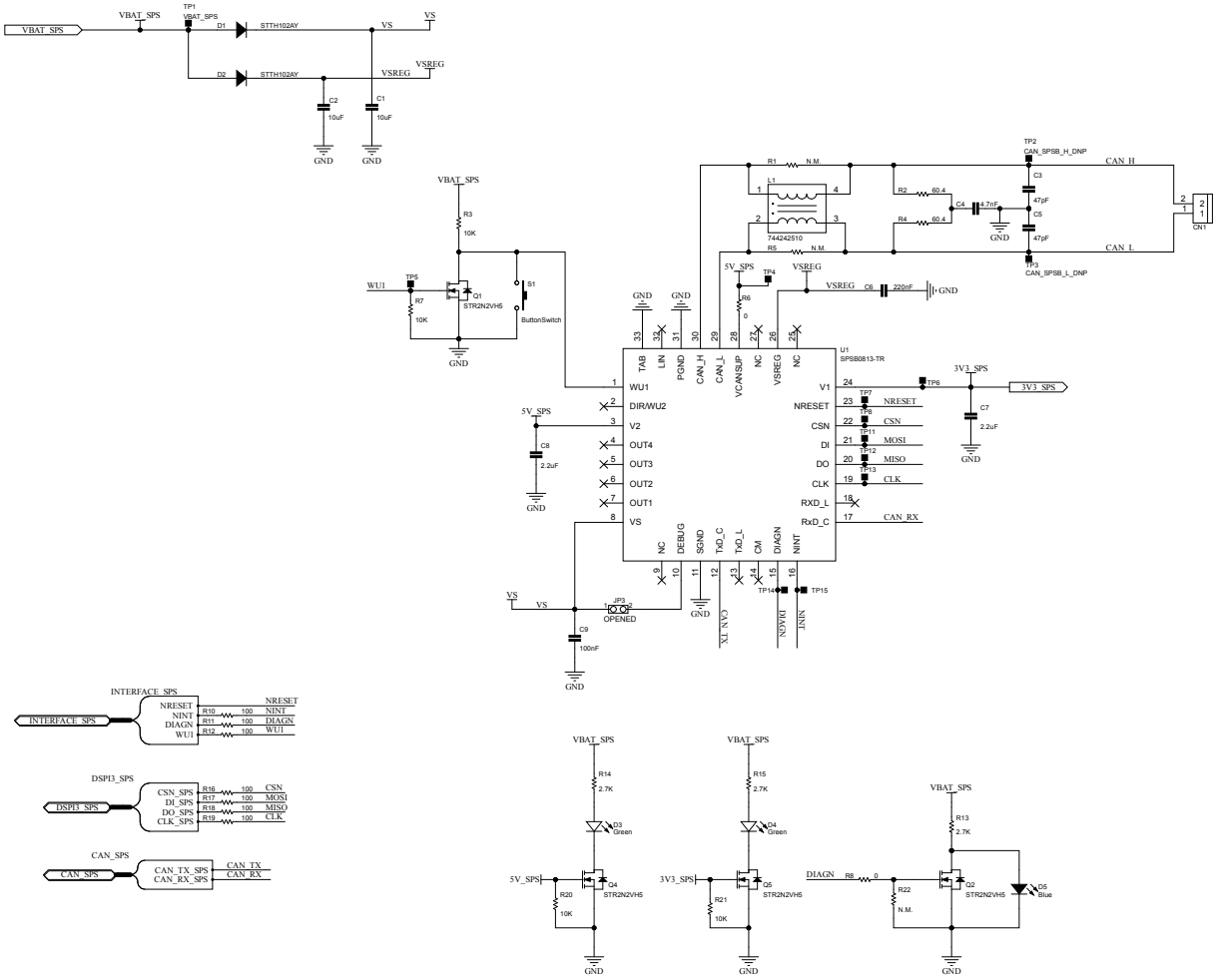
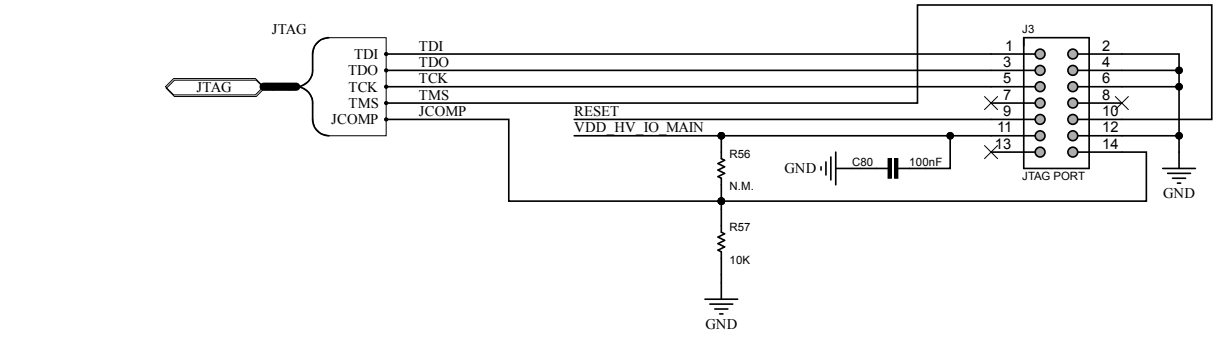


Figure 42. **AEK-COM-10BASET circuit schematic (5 of 10)**



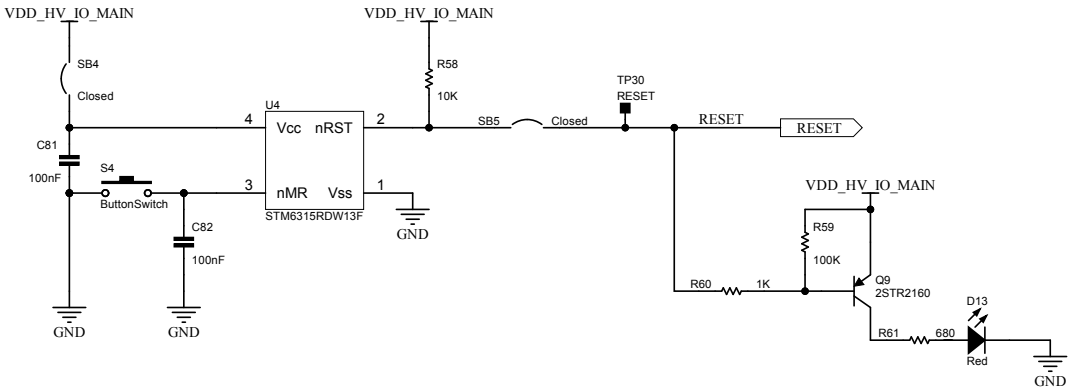


Figure 43. **AEK-COM-10BASET circuit schematic (6 of 10)**

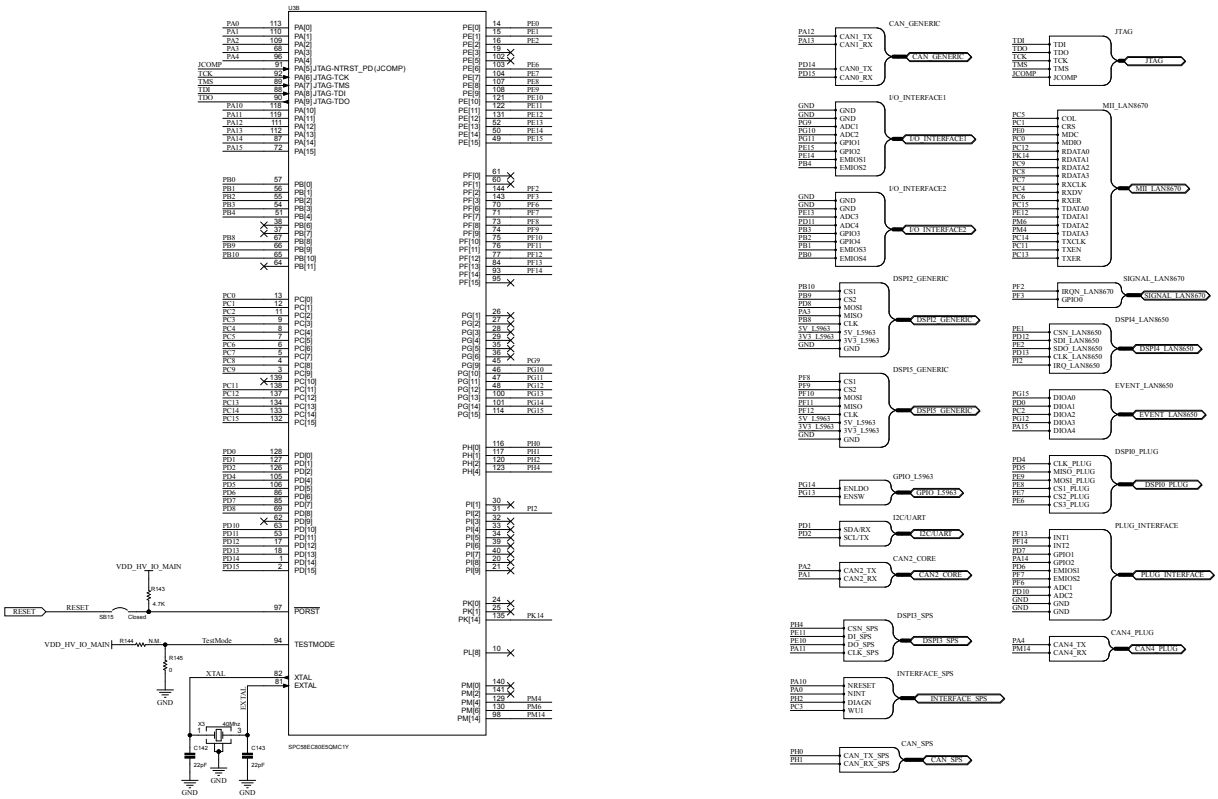


Figure 44. **AEK-COM-10BASET circuit schematic (7 of 10)**

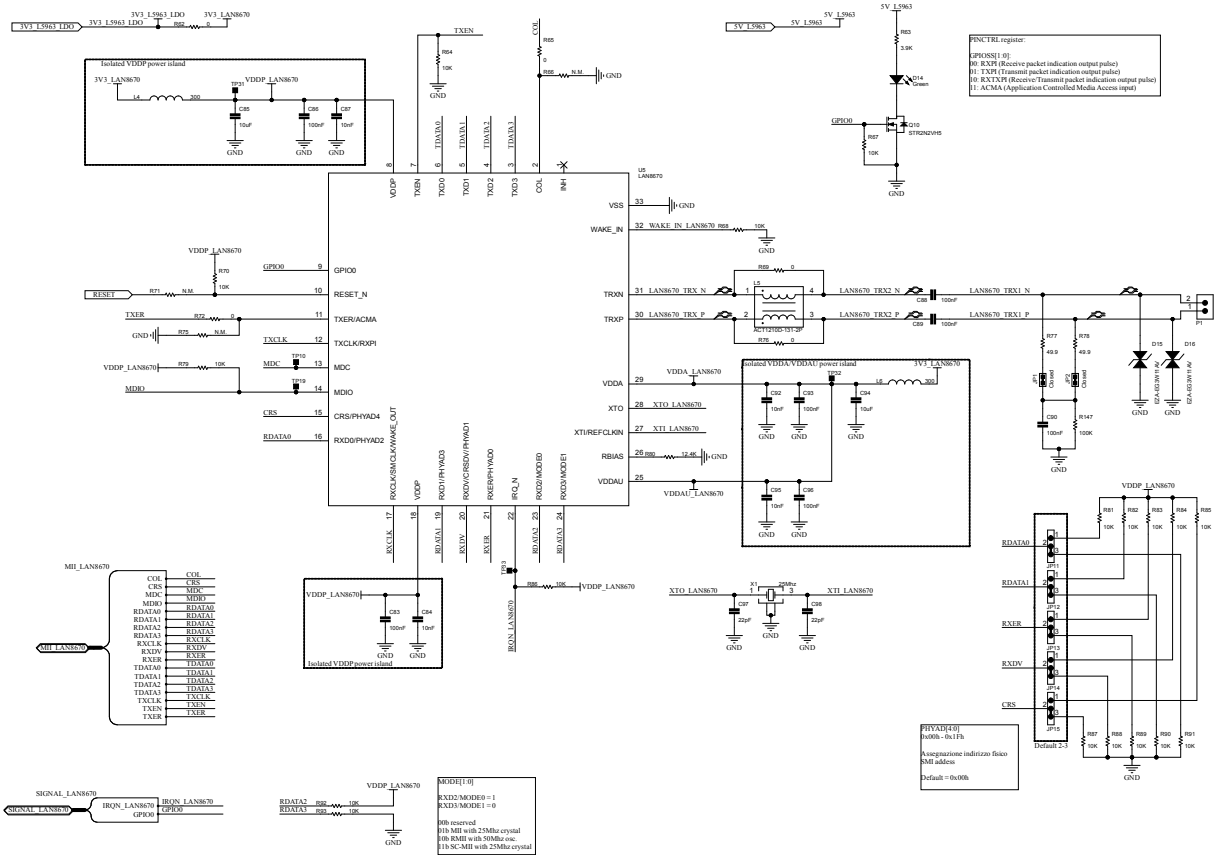


Figure 45. **AEK-COM-10BASET circuit schematic (8 of 10)**

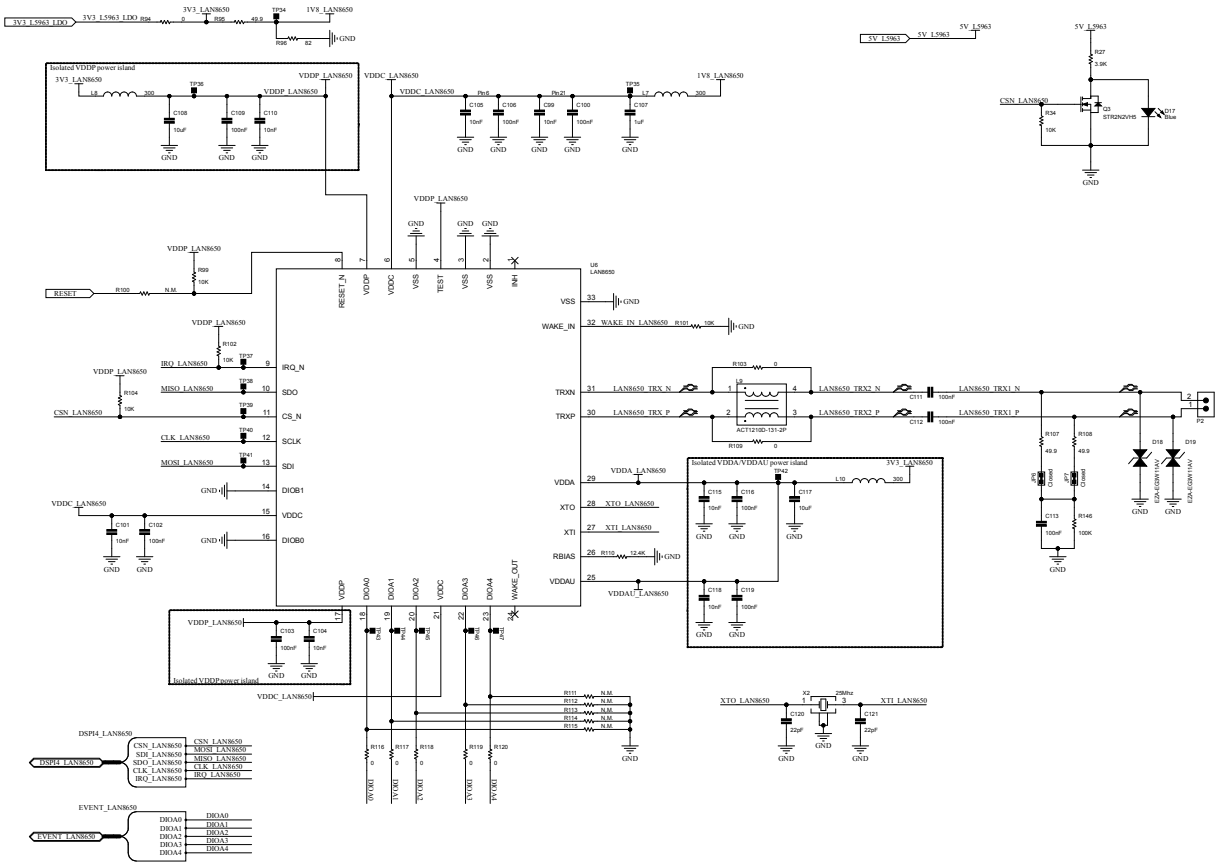


Figure 46. **AEK-COM-10BASET circuit schematic (9 of 10)**

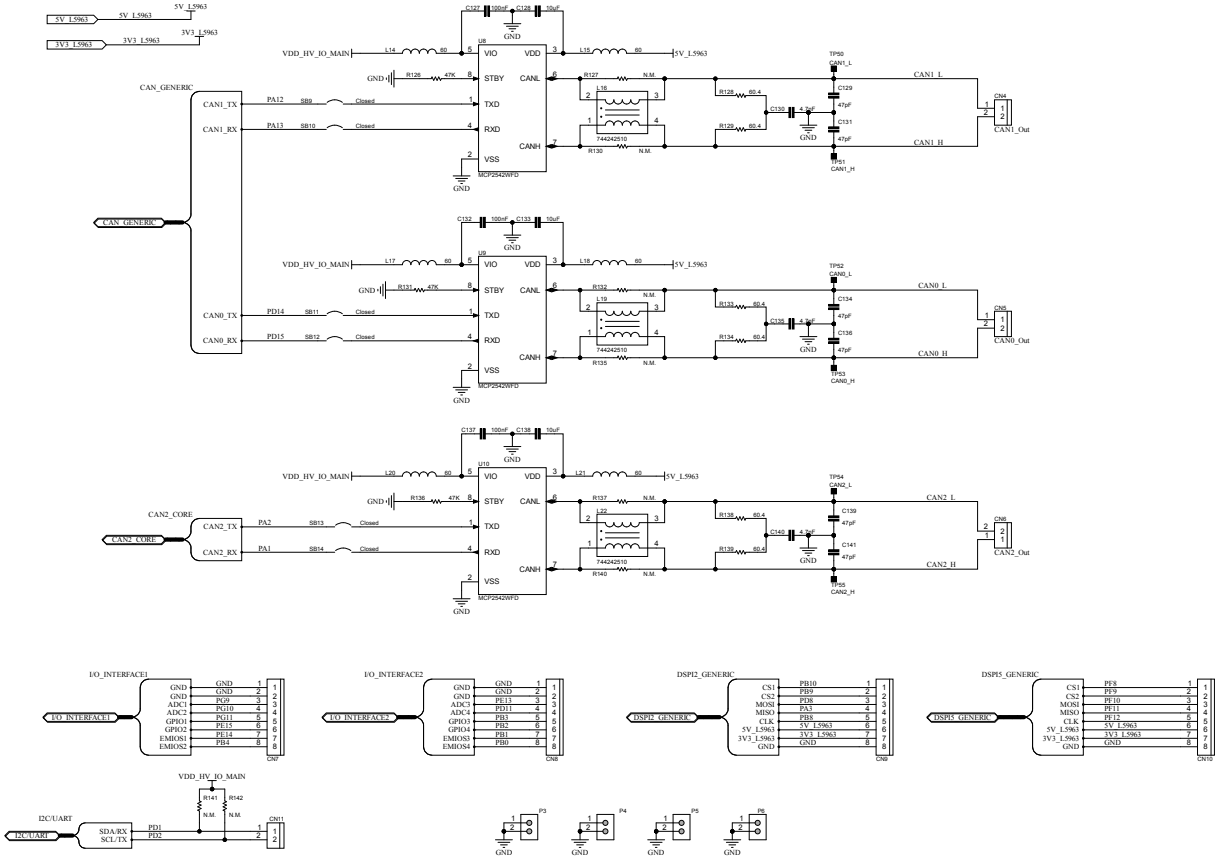
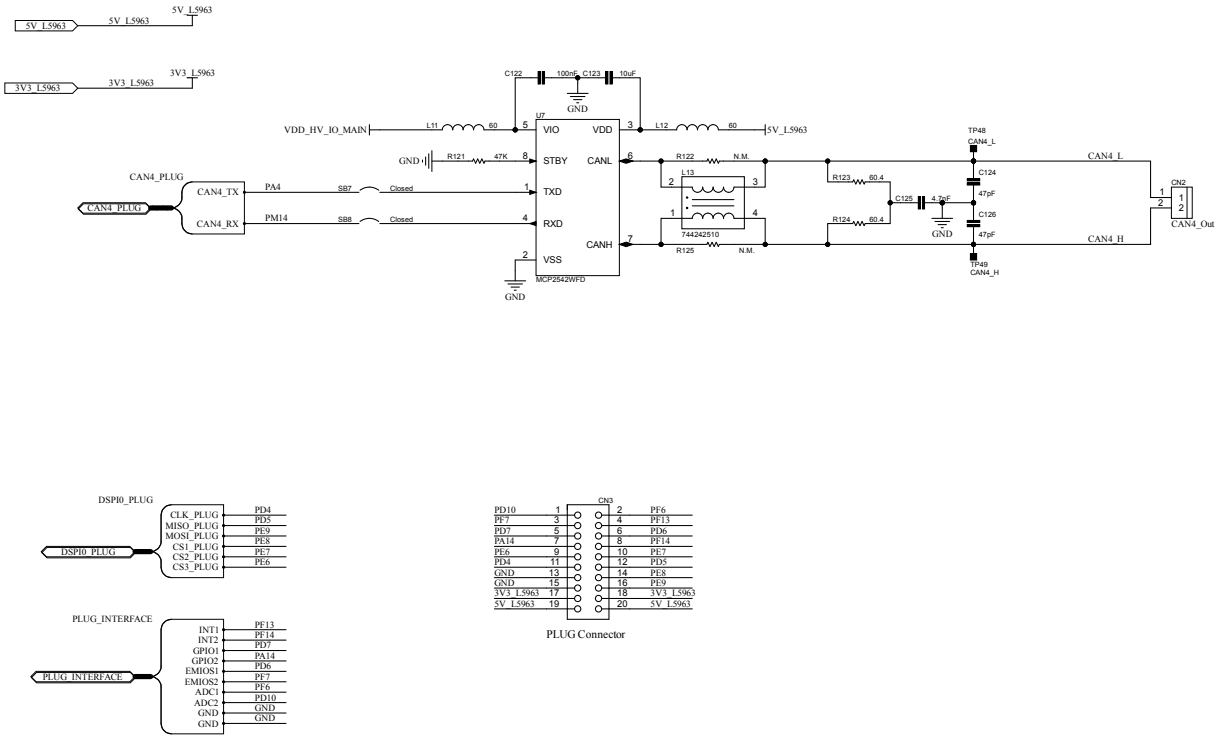


Figure 47. **AEK-COM-10BASET circuit schematic (10 of 10)**



4 Bill of materials

Table 4. **AEK-COM-10BASET bill of materials**

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	7	C1, C2, C15, C85, C94, C108, C117	10uF	1206 - 50V - X5R	WE	885012108022
2	10	C3, C5, C124, C126, C129, C131, C134, C136, C139, C141	47pF	0603 - 50V - NP0 Class I	WE	885012006055
3	5	C4, C125, C130, C135, C140	4.7nF	0603 - 50V - X7R Class II	WE	885012206087
4	1	C6	220nF	0603 - 50V - X7R Class II	WE	885012206125
5	2	C7, C8	2.2uF	0805 - 25V - X7R Class II	WE	885012207079
6	42	C9, C11, C14, C17, C23, C27, C34, C37, C42, C45, C48, C50, C52, C54, C56, C58, C61, C72, C75, C78, C80, C81, C82, C83, C86, C88, C89, C93, C96, C100, C102, C103, C106, C109, C111, C112, C116, C119, C122, C127, C132, C137	100nF	0603 - 50V - X7R Class II	WE	885012206095
7	3	C10, C22, C33	22uF	0805 - 25V - X5R Class II	WE	885012107019
8	1	C12	1uF	0603 - 25V - X7R Class II	WE	885012206076
9	1	C13	220uF	Electrolytic Cap - 50V - 10x10.5	WE	865080657018
10	1	C16	3.3uF	1206 - 25V - X7R Class II	WE	885012208067
11	2	C19, C30	15nF	0603 - 50V - X7R Class II	WE	885012206090
12	29	C20, C41, C44, C47, C49, C51, C53, C55, C57, C59, C60, C64, C66, C68, C70, C73, C76, C79, C84, C87, C92, C95, C99, C101, C104, C105, C110, C115, C118	10nF	0603 - 50V - X7R Class II	WE	885012206089
13	1	C21	120pF	0603 - 50V - X7R	Vishay	VJ0603Y121KXACW1BC
14	2	C25, C26	47uF	1210 - 16V - X5R Class II	WE	885012109011

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
15	6	C28, C38, C63, C65, C67, C69	47nF	0603 - 50V - X7R Class II	WE	885012206093
16	2	C29, C39	220pF	0603 - 50V - X7R Class II	WE	885012206079
17	1	C31	6.8nF	0603 - 50V - X7R Class II	WE	885012206088
18	1	C32	82pF	0603 - 50V - C0G	Murata	GRM1885C1H820JA01D
19	2	C35, C36	22uF	1210 - 25V - X7R Class II	WE	885012209074
20	2	C43, C46	1.5uF	1206 - 25V - X7R Class II	WE	885012208065
21	3	C62, C71, C74	2.2uF	1206 - 25V - X7R Class II	WE	885012208066
22	1	C77	4.7uF	1206 - 50V - X7R Class II	WE	885012208094
23	2	C90, C113	100nF	0805 - 100V - X7R Class II	WE	885012207128
24	4	C97, C98, C120, C121	22pF	0402 - 50V - NP0 Class I	WE	885012005057
25	1	C107	1uF	1206 - 50V - X7R Class II	WE	885012208093
26	4	C123, C128, C133, C138	10uF	0805 - 25V - X5R Class II	WE	885012107027
27	2	C142, C143	22pF	0603 - 50V - NP0 Class I	WE	885012006053
28	6	CN1, CN2, CN4, CN5, CN6, CN11	Con 2P	2.54mm - 1 row - KK254 - Male	WE	61900211121
29	1	CN3	610120249221	WR-PHD 2.54 mm PCB Socket Header - SMT Type - Double Row - Right Angle - 20pins	WE	610120249221
30	4	CN7, CN8, CN9, CN10	Con 8p	2.54mm - 1 row - KK254 - Male	WE	61900811121
31	2	D1, D2	STTH102AY, SMA	Automotive high efficiency ultrafast diode	ST	STTH102AY
32	8	D3, D4, D8, D9, D10, D11, D12, D14	Green	0805 - Led Green - 3.2V	WE	150080GS75000
33	2	D5, D17	Blue	0805 - Led Blue - 3.2V	WE	150080BS75000
34	1	D6	MMBZ5242BLT 1G	12V Zener Voltage Regulators, 225mW	Onsemi	MMBZ5242BLT1G
35	1	D7	SMAJ24CA, SMA	SMA TVS - 24VDC - Bidrectional	ST	SMAJ24CA-TR
36	1	D13	Red	0805 - Led Red - 2V	WE	150080RS75000

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
37	4	D15, D16, D18, D19	EZA-EG3W11AV	ESD Suppressor, High Withstanding Type	Panasonic	EZA-EG3W11AV
38	1	F1	0437003.WRA	437 Series – 1206 Fast-Acting Fuse	LittleFuse	0437003.WRA
39	1	J2	Con 2p 5.08_green	5.08mm - WR-TBL Series 2135 - Horizontal Entry Modular	WE	691213510002
40	1	J3	JTAG PORT	2.54mm - IDC, Male Box Header WR-BHD, THT, Vertical	WE	61201421621
41	4	JP1, JP2, JP6, JP7	Jumper 2p Closed	2mm - WR-PHD 2.00 mm THT Pin Header Single Row, Vertical, 2p, Closed	WE	62000211121
42	7	JP3, JP4, JP5, P3, P4, P5, P6	Jumper 2p, Jumper 2p Closed, Header 2p 2.54	THT Vertical 2 pins Header, Pitch 2.54 mm, Single Row, 2.54mm - Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 2p, Closed, 2.54mm - WR-PHD Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 2p	WE	61300211121
43	5	JP11, JP12, JP13, JP14, JP15	Jumper 3p	THT Vertical 3 pins Header, Pitch 2.54 mm, Single Row	WE	61300311121
44	5	L1, L13, L16, L19, L22	51uH	WE-SLM SMT Common Mode Line Filter - 51uH	WE	744242510
45	2	L2, L3	33uH	WE-LHMI SMT Power Inductor – 6.6 x 6.6 x 4.8 - 2.45A	WE	74437349330
46	5	L4, L6, L7, L8, L10	300	WE-CBF SMT EMI Suppression Ferrite Bead. 300 Ohm, 300mA	WE	742792640

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
47	8	L11, L12, L14, L15, L17, L18, L20, L21	60	WE-CBF SMT EMI Suppression Ferrite Bead. 60 Ohm, 500mA	WE	74279267
48	2	P1, P2	Con 2p 5.00_blue	5.00mm - WR-TBL Serie 102 Horizontal Entry Modular	WE	691102710002
49	6	Q1, Q2, Q3, Q4, Q5, Q10	STR2N2VH5, SOT-23	N-channel 20 V, 0.025 Ω typ., 2.3 A STripFET™ H5 Power MOSFET in a SOT-23 package	ST	STR2N2VH5
50	1	Q6	STL42P4LLF6, PowerFLAT 5x6	P-channel -40 V, 0.0155 Ohm, -42 A, Power MOSFET in a PowerFLAT 5x6 package	ST	STL42P4LLF6
51	1	Q7	2STR1160, SOT-23	Low voltage fast-switching NPN power transistor	ST	2STR1160
52	1	Q8	2STN1360, SOT-223	Low voltage fast-switching NPN power transistors	ST	2STN1360
53	1	Q9	2STR2160, SOT-23	Low voltage fast-switching PNP power transistor	ST	2STR2160
54	26	R1, R5, R22, R43, R55, R56, R66, R71, R75, R100, R111, R112, R113, R114, R115, R122, R125, R127, R130, R132, R135, R137, R140, R141, R142, R144	N.M.	0603	N.M.	N.M.
55	10	R2, R4, R123, R124, R128, R129, R133, R134, R138, R139	60.4	0603 - ±1% - 0.1W	Panasonic	ERJ3EKF60R4V
56	31	R3, R7, R20, R21, R24, R34, R36, R57, R58, R64, R67, R68, R70, R79, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R99, R101, R102, R104	10K	0603 - ±1% - 0.2W	Panasonic	ERJP03F1002V

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
57	31	R6, R8, R51, R52, R53, R54, R62, R65, R72, R94, R116, R117, R118, R119, R120, R145, SB1, SB2, SB3, SB4, SB5, SB6, SB7, SB8, SB9, SB10, SB11, SB12, SB13, SB14, SB15	0, Closed	0603 - ±1% - 0.1W, Circuit Breaker - 0603 - ±1% - 0.1W	Panasonic	ERJ3GEY0R00V
58	3	R9, R28, R73	0	0805 - jumper - 0.25W	Vishay	RCC08050000Z0EA
59	7	R10, R11, R12, R16, R17, R18, R19	100	0603 - ±1% - 0.125W	Panasonic	ERJH3EF1000V
60	3	R13, R14, R15	2.7K	0603 - ±1% - 0.1W	Vishay	MCT06030C2701FP500
61	1	R23	20K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF2002V
62	1	R25	464K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF4643V
63	1	R26	200K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF2003V
64	4	R27, R47, R48, R63	3.9K	0603 - ±1% - 0.1W	Panasonic	ERJ3EKF3901V
65	1	R29	8.2K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF8201V
66	1	R30	120	0603 - ±1% - 0.25W	Panasonic	ERJPA3F1200V
67	2	R31, R39	5.1K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF5101V
68	3	R32, R40, R143	4.7K	0603 - ±1% - 0.25W	Panasonic	ERJPA3F4701V
69	1	R33	1.24K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF1241V
70	2	R35, R42	10	0603 - ±1% - 0.25W	Panasonic	ERJPA3F10R0V
71	1	R37	5.6K	0603 - ±1% - 0.2W	Panasonic	ERJ-P03F5601V
72	1	R38	180	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF1800V
73	1	R41	2.2K	0603 - ±1% - 0.1W	Panasonic	ERJ-3EKF2201V
74	1	R44	15K	0603 - ±1% - 0.25W	Panasonic	ERJ-PA3F1502V
75	2	R45, R46	1.5K	0603 - ±1% - 0.25W	Panasonic	ERJ-PA3F1501V
76	2	R49, R60	1K	0603 - ±1% - 0.25W	Panasonic	ERJPA3F1001V
77	2	R50, R59	100K	0603 - ±1% - 0.2W	Panasonic	ERJP03F1003V

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
78	1	R61	680	0603 - ±1% - 0.25W	Panasonic	ERJPA3F6800V
79	4	R69, R76, R103, R109	0	0402 - 0.1W	Panasonic	ERJ-2GE0R00X
80	1	R74	N.M.	0805	N.M.	N.M.
81	4	R77, R78, R107, R108	49.9	1206 - ±1% - 0.66W	Panasonic	ERJP08F49R9V
82	2	R80, R110	12.4K	0603 - ±1% - 0.2W	Panasonic	ERJP03F1242V
83	1	R95	49.9	0603 - ±1% - 0.25W	Panasonic	ERJ-UP3F49R9V
84	1	R96	82	0603 - ±0.5% - 0.2W	Panasonic	ERJ-P03D82R0V
85	4	R121, R126, R131, R136	47K	0603 - ±1% - 0.25W	Panasonic	ERJPA3F4702V
86	2	R146, R147	100K	0805 - ±5% - 0.25W	Panasonic	ERJT06J104V
87	2	S1, S4	ButtonSwitch	Switch	WE	430152043826
88	52	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP21, TP22, TP23, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP54, TP55		Test point_hole	N.A.	N.A.
89	1	U1	SPSB0813, QFN-32L WF	Automotive power management IC with LIN and CAN-FD	ST	SPSB0813-TR
90	1	U2	L5963DN-EHT, PowerSSO 36	Automotive dual monolithic switching regulator with LDO and HSD	ST	L5963DN-EHT

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
91	1	U3	SPC58EC80E5 QMC1Y, TQFP 144 20x20x1.0	32-bit Power Architecture MCU for Automotive General Purpose Applications - Chorus family	ST	SPC58EC80E5QMC1Y
92	1	U4	STM6315RDW1 3F, SOT-143 4	STMICROELEC TRONICS - STM6315SDW1 3F - Reset Circuit, Active-Low, Open-Drain, 1V to 5.5V, 2.93V Threshold, 1 Monitor	ST	STM6315RDW13F
93	1	U5	LAN8670	10BASE-T1S Ethernet PHY Transceiver	Microchip	LAN8670C2T-E/LMX
94	1	U6	LAN8650	10BASE-T1S MAC-PHY Ethernet Controller with SPI	Microchip	LAN8650B1T-E/LMX
95	4	U7, U8, U9, U10	MCP2542WFD	CAN FD Transceiver with Wake-up Pattern (WUP) Option	Microchip	MCP2542WFD
96	2	X1, X2	25Mhz	WE-XTAL Quartz Crystal, SMT, CFPX-104, 25MHz, +/-50ppm	WE	830033075
97	1	X3	40Mhz	WE-XTAL Quartz Crystal, SMT, CFPX-104, 40MHz, +/-20ppm	WE	830059537
98	4	for blister	970150365	WA-SPAIE Plastic Spacer Stud, metric, internal/ external	WE	970150365
99	4	for blister	97790603211	WA-SCRW Pan Head Screw w. cross slot M3	WE	97790603211
100	4	for blister	61900811621	WR-WTB 2.54 mm Female Terminal Housing	WE	61900811621
101	6	for blister	61900211621	WR-WTB 2.54 mm Female Terminal Housing	WE	61900211621

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
102	44	for blister	61900113722	WR-WTB 2.54 mm Female Crimp Contact	WE	61900113722
103	16	for blister	609002115121	WR-PHD 2.54 mm Jumper with Test Point & Pullback	WE	609002115121
104	4	for blister	60800213421	WR-PHD 2.00 mm Jumper with Test Point	WE	60800213421

4.1 Appendix A: Board robustness enhancements

To make the board more robust, we suggest implementing the following changes in the layout:

- For D7 TVS on battery connector, mount SM4T28CAY instead of the onboard SMAJ24CA.
  The SM4T28CAY device is automotive-grade and is designed to protect sensitive automotive circuits against surges defined in ISO 7637-2 and against electrostatic discharges according to ISO 10605.
  For further information, see the related datasheet at https://www.st.com/resource/en/datasheet/sm4t28cay.pdf
- For U1, U7, U8, U9 and U10 CAN transceivers, enhance CAN link ESD/EOS protection by adding ESDCAN protections on CAN-L and CAN-H:
  - ESDCAN in a SOT23 or a SOT323 package.
    These dual-line CAN transceiver protection devices protect both CAN-H and CAN-L signals of automotive CAN PHY against ISO 7637-3 transients and ESD (electrostatic discharge). This ESDCAN series complies with all the physical layer constraints (jump start, reverse polarity, …) without compromising the low clamping voltage for an efficient CAN or LIN bus protection.
    For further information, see https://www.st.com/resource/en/datasheet/esdcan04-2bly.pdf for ESDCAN in a SOT23 package or https://www.st.com/resource/en/datasheet/esdcan03-2bwy.pdf for ESDCAN in a SOT323 package.

5 Board versions

Table 5. AEK-COM-10BASET versions

Finished good	Schematic diagrams	Bill of materials
AEK$COM-10BASETA(1)	AEK$COM-10BASETA schematic diagrams	AEK$COM-10BASETA bill of materials

1. *This code identifies the AEK-COM-10BASET evaluation board first version.*

6 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
16-Dec-2024	1	Initial release.
22-Sep-2025	2	Added Section 4.1: Appendix A: Board robustness enhancements.

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