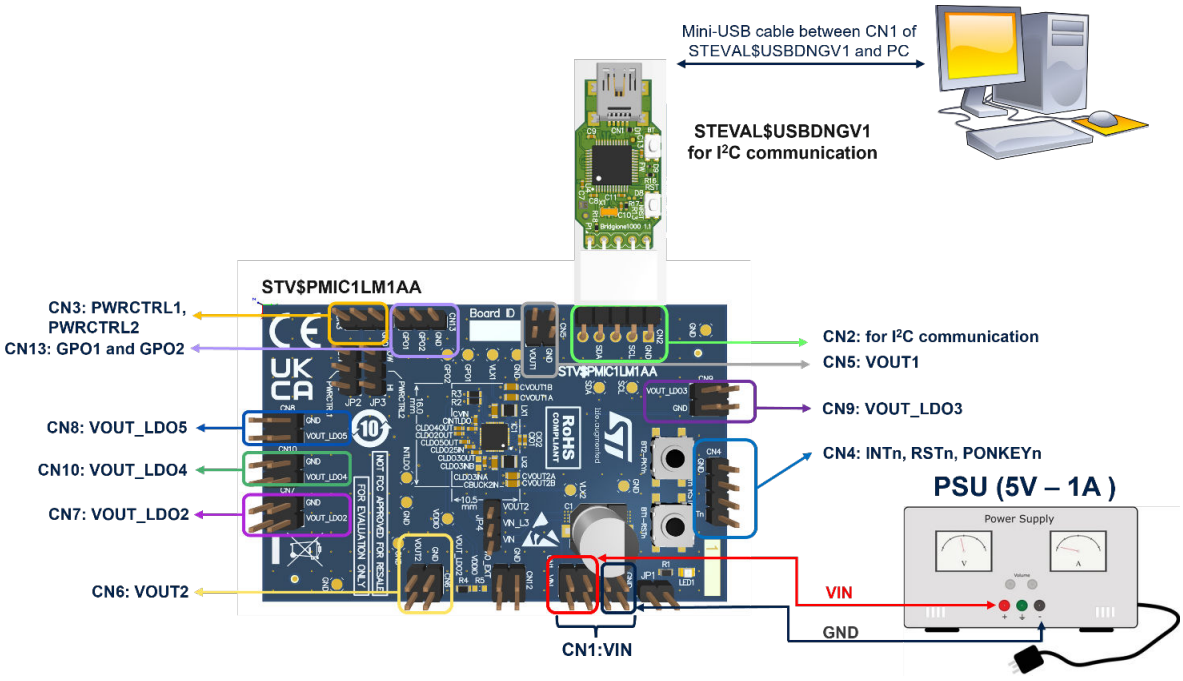
User manual for STEVAL-PMIC1LKV1 based on STPMIC1LA

Introduction

This user manual provides detailed instructions for configuring and using the STEVAL-PMIC1LKV1 kit. The kit includes the following components:

- STEVAL-PMIC1LM1A evaluation board: designed specifically for the STPMIC1LA.
- STEVAL-USBDNGV1 USB dongle: used for programming the STPMIC1L via the I²C bus protocol, in conjunction with the STSW-PMIC1LGUI software.

Figure 1. STEVAL-PMIC1LKV1 kit



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1 STPMIC1L overview

The STPMIC1L is a fully integrated power management IC designed for the STM32MP1x MPU family applications requiring low power and high efficiency.

The device integrates advanced low-power features controlled by a host processor via I²C and I/O interfaces.

STPMIC1L regulators are designed to supply power to the application processor as well as to the external system peripherals like DDR, flash memories, and other system devices.

Two buck SMPS are optimized to provide an excellent transient response and output voltage precision for a wide range of operating conditions. An advanced PWM phase shift synchronization technique with an integrated PLL ensures low noise and reduced EMI.

The main features of the STPMIC1L are:

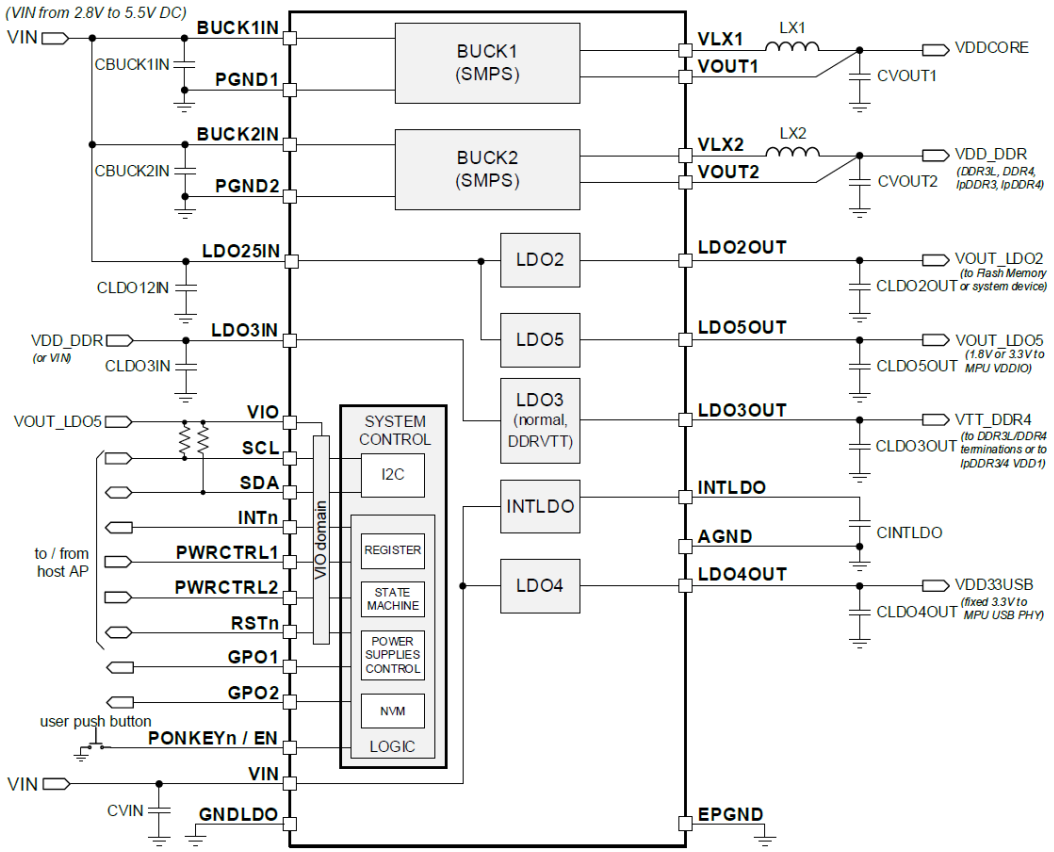
- 2.8 V to 5.5 V input voltage range
- 2 buck SMPS converters with adaptive constant on-time (COT) topology
- 2 MHz switching frequency with forced PWM feature available
- 2 adjustable general purpose LDOs
- 1 LDO for DDR3L/DDR4 termination (sink-source) or as a general purpose LDO
- 1 LDO with fixed output voltage of 3.3 V
- User programmable nonvolatile memory (NVM), enabling scalability to support a wide range of applications
- Immediate output alternate settings toggle by dedicated power control pins
- Programmable output voltages turn ON/OFF sequences
- I²C and digital I/O control interfaces
- 2 GPO output control for external command
- Advanced customizable safety managements
- VFQFPN 28L package (4.0 x 4.0 x 1.0 mm)

Typical applications of the STPMIC25 include:

- Power management for embedded microprocessor units
- Wearable and IoT
- Portable devices
- Man-machine interfaces
- Smart home
- Power management unit companion chip of the STM32MP13/15 MPUs

A typical application schematic of STPMIC1L is shown in the following figure:

Figure 2. STPMIC1L typical application schematic



The STPMIC1L features a large input voltage range from 2.8 V to 5.5 V to supply:

- 5 V DC wall adapter applications
- 1-cell 3.6 V Li-Ion/LiPo battery applications

The STPMIC1L provides all the regulators needed to power supply a complete application:

- 4 LDOs
- 2 step-down (buck) converters

Table 1 describes each regulator and their typical application use (in STM32MP1x MPU applications).

Table 1. General description of STPMIC1L regulators

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Application use
LDO2, LDO5	0.9 to 4.0	100	400 / 200 / 100 / 50	General purpose (eMMC, DDR4 VPP, SD card, LCD camera, etc.)
LDO3 normal mode	0.9 to 4.0	100	120	General purpose / lpDDR VDD1
LDO3 sink-source mode	VOUT2/2	-	±120 (rms), ±-230 (peak)	DDR3L/DDR4 terminations (VTT)
LDO4	3.3	-	40	VDD33USB VDD33UCPD
BUCK1	LV range: 0.5 to 1.5	10	2000, 1500, 1000, 500	VDDCORE
	HV range: 1.5 V to 4.2	100		
BUCK2	0.5 to 1.5	10	2000, 1500, 1000, 500	VDDQ (DDR3L, DDR, lpDDR3, lpDDR4)
GPO1, GPO2				External control 1,2

V_{IN} is the main STPMIC1L supply. All step-down converters and linear regulators have dedicated or shared power supply pins. The dedicated V_{IO} supply is for all digital interface pins.

No other supply voltages must be applied before V_{IN} or set higher than V_{IN}.

2 STPMIC1L NVM settings

The STPMIC1L has a nonvolatile memory (NVM) that can be (re)programmed via I²C directly in target applications to facilitate mass production, enabling scalability to support a wide range of applications. The main settings of STPMIC1L are stored in the NVM memory:

- VIN voltage threshold
- Auto turn-on feature
- Default I²C slave device address
- Default output voltages at startup of the regulators
- Power-up sequence at startup (rank) of the regulators
- Safety management (behavior in case of failure) → overcurrent protection, overtemperature protection, VIN_low, watchdog, and ponkey fault counters
- Possibility to lock the NVM content to prevent further reprogramming by writing the LOCK_NVM bit
- Other features (see STPMIC1L datasheet DS14839 for further details)

The STPMIC1LA, STPMIC1LB and STPMIC1LD are the three standard NVM configurations that support the STM32MP13/15 lines of MPU application versions with a minimum set of regulators enabled by default:

- STPMIC1LA:
  - Typical use case: 5V continuous input voltage (wall adapter) applications
  - VDDIO at 3.3V (LDO2 output)
- STPMIC1LB:
  - Typical use case: Li-Ion/Li-PO single cell battery applications
  - VDDIO at 1.8V (LDO2 output)
- STPMIC1LD:
  - Typical use case: 5V continuous input voltage (wall adapter) applications
  - VDDIO at 3.3V (LDO2 output)

Note: – This NVM version ensures compatibility with the STM32MP13 in an overdrive CPU setup. A dedicated GPO powers on an external buck converter (the ST1S31) with the proper rank to supply the DDR3L memory.

The main settings of STPMIC1LA, STPMIC1LB, and STPMIC1LD are listed in the table below:

Table 2. Main settings of STPMIC1LA, STPMIC1LB, and STPMIC1LD

IP	STPMIC1LA				STPMIC1LB				STPMIC1LD			
	Voltage	Mode	Pull-down	Rank	Voltage	Mode	Pull-down	Rank	Voltage	Mode	Pull-down	Rank
BUCK1	1.22V	HP	SLOW	2	1.22V	HP	SLOW	2	1.25V	HP	SLOW	2
BUCK2	OFF	OFF	FAST	0	OFF	OFF	FAST	0	1.25V	HP	SLOW	3
LDO2	3.3V	-	YES	1	1.8V	-	YES	1	3.3V	-	YES	1
LDO3	OFF	-	YES	0	OFF	-	YES	0	OFF	-	YES	0
LDO4	3.3V	-	YES	5	3.3V	-	YES	5	3.3V	-	YES	5
LDO5	3.3V	-	YES	4	2.9V	-	YES	4	3.3V	-	YES	4
GPO1	VIN	Active High	-	3	VIN	Active High	-	3	VIN	Active High	-	5
GPO2	OFF	Active High	-	0	OFF	Active High	-	0	OFF	Active High	-	0

The startup sequence of STPMIC1L is divided into four steps (Rank0 to Rank5).

Each BUCK, LDO regulator and GPO can be programmed to be automatically turned ON in one of these ranks. Each rank phase is separated by a delay, which is by default 1.5 ms. This rank delay can be programmed in NVM (Reg0x91[7:6]) at 1.5 ms, 3 ms, 4.5 ms, or 6 ms (RANK_DLY[1:0]).

- Rank=0: rail not turned ON automatically, no output voltage appears after POWER-UP sequence
- Rank=1: rail automatically turned ON after 7 ms (which is the fixed delay from VIN>VINOK_rise to the start of IPs with rank1), following a Turn_ON condition
- Rank=2: rail automatically turned ON after a further 1.5 ms compared to Rank1 output rails
- Rank=3: rail automatically turned ON after a further 1.5 ms compared to Rank2 output rails
- Rank=4: rail automatically turned ON after a further 1.5 ms compared to Rank3 output rails
- Rank=5: rail automatically turned ON after a further 1.5 ms compared to Rank4 output rails

Regardless of the STPMIC1L version the AUTO_TURN_ON option is set.

Table 3 shows the miscellaneous settings at startup of STPMIC1LA, STPMIC1LB and STPMIC1LD:

Table 3. Miscellaneous settings of STPMIC1LA, STPMIC1LB, and STPMIC1LD at startup

Parameter	STPMIC1LA	STPMIC1LB	STPMIC1LD	Comments
VINOK_Rise	4.0V	3.3V	4.0V	Default value of VIN_OK rising threshold
VINOK_HYST	0.5V	0.5V	0.5V	Default VIN_OK hysteresis
AUTO_TURN_ON	ON	ON	ON	Auto turn-ON functionality enabled by default
RANK_DLY	1.5ms	1.5ms	1.5ms	power-up/power-down step (RANK) duration time
RST_DLY	0	0	0	RESET release delay after POWER_UP sequence
I²C ADDR	0x33	0x33	0x33	I²C device address
NVM_USER	0	0	0	2 free NVM bytes for user

Table 4 shows the safety management and miscellaneous settings at startup of STPMIC1LA, STPMIC1LB and STPMIC1LD:

Table 4. Safety management and miscellaneous settings of STPMIC1LA, STPMIC1LB, and STPMIC1LD at startup

Parameter	STPMIC1LA	STPMIC1LB	STPMIC1LD	Comments
NVM_WDG_EN	OFF	OFF	OFF	Watchdog can be enabled at runtime
PKEY_LKP_OFF	ON	ON	ON	A long PONKEY key press does not switch OFF PMIC25
PKEY_LKP_EN_FSLS	OFF	OFF	OFF	A long PONKEY key press allows PMIC25 to skip the Fail-Safe Lock State
PKEY_LKP_TMR	10s	10s	10s	Long PONKEY key press timer duration settings
HICCUP_DLY	100ms	100ms	100ms	
VIN_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	
TSHDN_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	
OCP_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	If regulator OCP management set in FS (Fail Safe) mode
WDG_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	
PKEY_FLT_CNT_MAX	∞ restart	∞ restart	∞ restart	
RST_FLT_CNT_TMR	60m	60m	60m	
FAIL_SAFE_LOCK_DIS	Disabled	Disabled	Disabled	PMIC will never be locked in FS mode state (will go in OFF mode)
VIN_DLY	10ms	10ms	10ms	VIN additional delay
PKEY_EN_CFG	PONKEY	PONKEY	PONKEY	PONKEYn/EN feature configuration
NVM_PKEY_EN_PULL	pull-up active	pull-up active	pull-up active	PONKEYn/EN pad pull resistor selection

Table 5 shows the Fail Safety OCP management at startup settings of STPMIC1LA, STPMIC1LB, and STPMIC1LD:

Table 5. Fail safety OCP management settings of STPMIC1LA and STPMIC1LB

Parameter	STPMIC1LA OCP mgt / OCP lim	STPMIC1LB OCP mgt / OCP lim	STPMIC1LD OCP mgt / OCP lim	Comments
BUCK1 (VDDCORE/ VDDCPU)	FS / 1.5A	FS / 1.5A	FS / 1.0A	STPMIC1L switch-off in case of OCP triggered
BUCK2 (VDD_DDR)	FS / 1.0A	FS / 1.0A	FS / 1.0A	STPMIC1L switch-off in case of OCP triggered
LDO2 (VDDIO)	FS / 400mA	FS / 400mA	FS / 400mA	STPMIC1L switch-off in case of OCP triggered
LDO3 (VTT/VDD1_DDR)	FS	FS	Hiccup	
LDO4 (VDD33USB)	Hiccup	Hiccup	Hiccup	
LDO5 (VDD_FLASH)	Hiccup / 400mA	Hiccup / 400mA	Hiccup / 400mA	
GPO1	-	-		
GPO2	-	-		

2.1 STPMIC1L NVM shadow register map

Table 6 shows the complete NVM shadow register map of STPMIC1LA, STPMIC1LB and STPMIC1LD versions:

Table 6. STPMIC1LA/B/D NVM shadow register map

Reg (Hex)	Register Name	R/W	STPMIC1LA/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x90	NVM_MAIN_CTRL_SHR1	R/W		VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WD G_EN	AUTO_TU RNON
			A: 0xF1	1	1	1	1	0	0	0	1
			B: 0xD1	1	1	0	1	0	0	0	1
			D: 0xF1	1	1	1	1	0	0	0	1
0x91	NVM_MAIN_CTRL_SHR2	R/W		RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_CONFIG	NVM_PKEY_LKP_FSLS	NVM_PKEY_LKP_TM R[1:0]	
			A: 0x0A	0	0	0	0	1	0	1	0
			B: 0x0A	0	0	0	0	1	0	1	0
			D: 0x0A	0	0	0	0	1	0	1	0
0x92	NVM_RANK_SHR1	R/W		-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
			A: 0x02	0	0	0	0	0	0	1	0
			B: 0x02	0	0	0	0	0	0	1	0
			D: 0x1A	0	0	0	1	1	0	1	0
0x96	NVM_RANK_SHR5	R/W		-	-	LDO2_RANK[2:0]			-	-	-
			A: 0x08	0	0	0	0	1	0	0	0
			B: 0x08	0	0	0	0	1	0	0	0
			D: 0x08	0	0	0	0	1	0	0	0
0x97	NVM_RANK_SHR6	R/W		-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
			A: 0x28	0	0	1	0	1	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
			D: 0x28	0	0	1	0	1	0	0	0

Reg (Hex)	Register Name	R/W	STPMIC1LA/B/D default NVM shadow register map							
			(1) Hex	BITS[7:0]						
				7	6	5	4	3	2	1	0
0x98	NVM_RANK_SHR7	R/W		-	-	-	-	-	LDO5_RANK[2:0]		
			A: 0x04	0	0	0	0	0	1	0	0
			B: 0x04	0	0	0	0	0	1	0	0
			D: 0x04	0	0	0	0	0	1	0	0
0x9A	NVM_BUCK_MODE_SHR1	R/W		-	-	-	-	BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]	
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0x9C	NVM_BUCK1_VOUT_SHR	R/W		BUCK1_VRANGE_CFG	NVM_VOUT[6:0]						
			A: 0x48	0	1	0	0	1	0	0	0
			B: 0x48	0	1	0	0	1	0	0	0
			D: 0x4B	0	1	0	0	1	0	1	1
0x9D	NVM_BUCK2_VOUT_SHR	R/W		BUCK2_IRANGE_CFG	NVM_VOUT[6:0]						
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x4B	0	1	0	0	1	0	1	1
0x9F	NVM_MAIN_CTRL_SHR3	R/W		-	-	-	-	-	-	GPO2_POL_CFG	GPO1_POL_CFG
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA0	NVM_RANK_SHR9	R/W		-	-	GPO2_RANK [2:0]			GPO1_RANK [2:0]		
			A: 0x03	0	0	0	0	0	0	1	1
			B: 0x03	0	0	0	0	0	0	1	1

Reg (Hex)	Register Name	R/W	STPMIC1LA/B/D default NVM shadow register map							
			(1) Hex	BITS[7:0]						
				7	6	5	4	3	2	1	0
0xA0	NVM_RANK_SHR9	R/W	D: 0x05	0	0	0	0	0	1	0	1
0xA3	NVM_LDO2_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x12	0	0	0	1	0	0	1	0
			D: 0x30	0	0	1	1	0	0	0	0
0xA4	NVM_LDO3_SHR	R/W		NVM_SNK_SRC	-	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA5	NVM_LDO5_SHR	R/W		-	-	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
			D: 0x30	0	0	1	1	0	0	0	0
0xA9	NVM_PD_SHR1	R/W		-	-	-	-	NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
			A: 0x09	0	0	0	0	1	0	0	1
			B: 0x09	0	0	0	0	1	0	0	1
			D: 0x05	0	0	0	0	0	1	0	1
0xAB	NVM_PD_SHR3	R/W		-	-	-	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	-
			A: 0x1E	0	0	0	1	1	1	1	0
			B: 0x1E	0	0	0	1	1	1	1	0
			D: 0x1E	0	0	0	1	1	1	1	0
0xAC	NVM_BUCKS_IOUT_SHR1	R/W		-	-	-	-	BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
			A: 0x06	0	0	0	0	0	1	1	0

Reg (Hex)	Register Name	R/W	STPMIC1LA/B/D default NVM shadow register map							
			(1) Hex	BITS[7:0]						
				7	6	5	4	3	2	1	0
0xAC	NVM_BUCKS_IOUT _SHR1	R/W	B: 0x06	0	0	0	0	0	1	1	0
			D: 0x05	0	0	0	0	0	1	0	1
0xAD	NVM_BUCKS_IOUT _SHR2	R/W		HICCUP_DLY[1:0]		-	-	-	-	-	-
			A: 0x40	0	1	0	0	0	0	0	0
			B: 0x40	0	1	0	0	0	0	0	0
			D: 0x40	0	1	0	0	0	0	0	0
0xAE	NVM_LDOS_IOUT _SHR	R/W		-	-	-	-	LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
			A: 0x0F	0	0	0	0	1	1	1	1
			B: 0x0F	0	0	0	0	1	1	1	1
			D: 0x0F	0	0	0	0	1	1	1	1
0xAF	NVM_FS_OCP_SHR1	R/W		-	-	-	-	-	-	NVM_FS_ OCP_BUC K2	NVM_FS_ OCP_BUC K1
			A: 0x03	0	0	0	0	0	0	1	1
			B: 0x03	0	0	0	0	0	0	1	1
			D: 0x03	0	0	0	0	0	0	1	1
0xB0	NVM_FS_OCP_SHR2	R/W		-	-	-	NVM_FS_ OCP_LDO5	NVM_FS_ OCP_LDO4	NVM_FS_ OCP_LDO3	NVM_FS_ OCP_LDO2	-
			A: 0x06	0	0	0	0	0	1	1	0
			B: 0x06	0	0	0	0	0	1	1	0
			D: 0x02	0	0	0	0	0	0	1	0
0xB1	NVM_FS_SHR1	R/W		VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1

Reg (Hex)	Register Name	R/W	STPMIC1LA/B/D default NVM shadow register map							
			(1) Hex	BITS[7:0]						
				7	6	5	4	3	2	1	0
0xB2	NVM_FS_SHR2	R/W		TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1
0xB3	NVM_FS_SHR3	R/W		-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
			A: 0x4F	0	1	0	0	1	1	1	1
			B: 0x4F	0	1	0	0	1	1	1	1
			D: 0x4F	0	1	0	0	1	1	1	1
0xB5	NVM_I²C_ADDR_SHR	R/W		LOCK_NVM	I2C_ADDR[6:0]						
			A: 0x33	0	0	1	1	0	0	1	1
			B: 0x33	0	0	1	1	0	0	1	1
			D: 0x33	0	0	1	1	0	0	1	1
0xB6	NVM_USER_SHR1	R/W		NVM_USER1[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xB7	NVM_USER_SHR2	R/W		NVM_USER2[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xB9	NVM_MAIN_CTRL_SHR4	R/W		VIN_DLY [1:0]		-	-	NVM_PKEY_EN_PULL [1:0]		EN_POL_CFG	PKEY_EN_CFG
			A: 0x46	0	1	0	0	0	1	1	0
			B: 0x46	0	1	0	0	0	1	1	0

Reg (Hex)	Register Name	R/W	STPMIC1LA/B/D default NVM shadow register map							
			(1) Hex	BITS[7:0]						
				7	6	5	4	3	2	1	0
0xB9	NVM_MAIN_CTRL_SHR4	R/W	D: 0x46	0	1	0	0	0	1	1	0

Note: (*) This column contains the STPMIC1L default values of NVM content shadow register in hexadecimal format.
The STPMIC1L version is soldered in STEVAL-PMIC1LM1A.
For more details regarding the STPMIC1L features, refer to the STPMIC1L datasheet DS14839.

3 Get started with STEVAL-PMIC1LKV1 kit

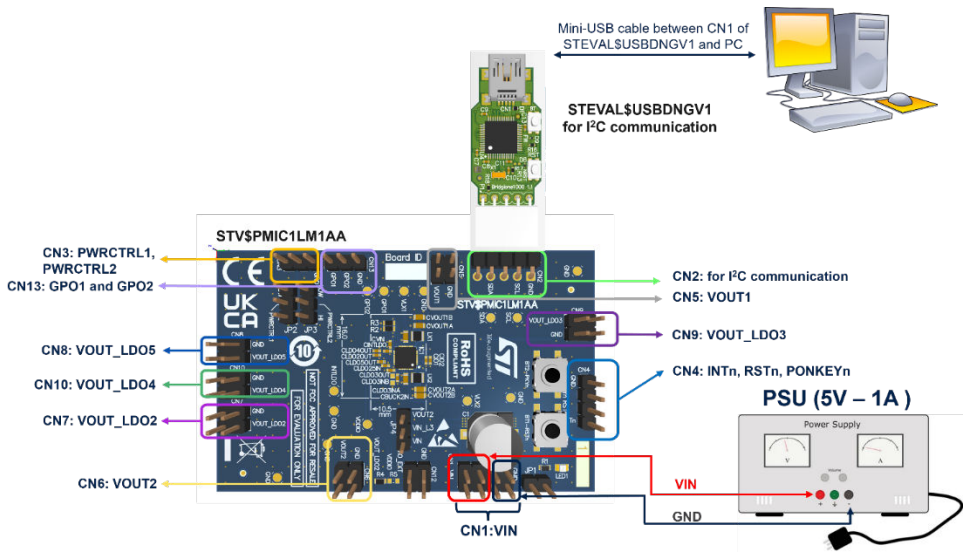
To get started with the STEVAL-PMIC1LKV1 kit, proceed as follows:

Step 1. Connect the STEVAL-USBDNGV1 on STEVAL-PMIC1LM1A through the connector CN2

Step 2. Connect a mini-USB cable between the PC and the connector CN1 of STEVAL-USBDNGV1

Step 3. Apply the power supply VIN to the connector CN1 of the STEVAL-PMIC1LM1A (a power supply capable of 1 A minimum is required)

Figure 3. STEVAL-PMIC1LKV1 kit configuration



3.1 Input/Output connector description

The table below shows the list and the relative description of all input/output connectors present in the STEVAL-PMIC1LM1A:

Table 7. STEVAL-PMIC1LM1A input/output connectors description

Name	Functionality	Details
CN1	Main input power supply	VIN: Positive input power force/sense
		GND: Ground input force/sense
CN2	I²C bus connector	SCL: Clock
		SDA: Data
		GND: Ground
CN3	PWRCTRL1,2 output voltage connector	PWRCTRL1: output voltage sense
		PWRCTRL2: output voltage sense
		GND: Ground sense
CN4	INTn, RSTn, PONKEYn output voltage connector	INTn: Output voltage sense
		RSTn: Output voltage sense
		PONKEYn: Output voltage sense
CN5	BUCK1 output voltage connector	VOUT1: output voltage force/sense
		GND: Ground output force/sense
CN6	BUCK2 output voltage connector	VOUT2: output voltage force/sense
		GND: Ground output force/sense
CN7	LDO2 output voltage connector	VOUT_LDO2: output voltage force/sense
		GND: Ground output force/sense
CN8	LDO5 output voltage connector	VOUT_LDO5: output voltage force/sense
		GND: Ground output force/sense
CN9	LDO3 output voltage connector	VOUT_LDO3: output voltage force/sense
		GND: Ground output force/sense
CN10	LDO4 output voltage connector	VOUT_LDO4: output voltage force/sense
		GND: Ground output force/sense
CN12	VIO output voltage connector from external supply	VIO_EXT: output voltage force/sense
		GND: Ground output force/sense
CN13	GPO1,2 output voltage connector	GPO1: output voltage sense
		GPO2: output voltage sense
		GND: Ground sense
JP1	Manual bridge for VIN “LED1” connection	If LED1 is ON, VIN is applied to the STEVAL-PMIC1LM1A
JP2	Manual bridge for PWRCTRL1 connection	HIGH position: PWRTCTRL1 forced to VIO
		LOW position: PWRTCTRL1 forced to GND
JP3	Manual bridge for PWRCTRL2 connection	HIGH position: PWRTCTRL2 forced to VIO
		LOW position: PWRTCTRL2 forced to GND
JP4	Manual bridge for LDO3 input connection	L3i-VIN position: LDO3 input forced to main input voltage supply “VIN”
		L3i-VOUT2 position: LDO3 input forced to BUCK2 output
R4-R5	0 Ω resistors: Allow VIO connection to BUCK4 output or to external supply (VIO_EXT pin)	If R4 (0 Ω) is soldered: VIO is connected to LDO2 output. By default R4 is soldered
		If R5 (0 Ω) is soldered: VIO is connected to VIO_EXT output; in this case VIO must be supplied externally on CN12 connector (VIO_EXT pin).
BT1	RSTn button	RSTn pin is connected to GND when BT1 is pushed

Name	Functionality	Details
BT2	PONKEYn button	PONKEYn pin is connected to GND when BT2 is pushed

Figure 4, Figure 5, Figure 6, and Figure 7 show the connector details of the STEVAL-PMIC1LM1A.
Referring to Figure 4, be sure that:

- A PSU (5 V – 1A) is connected to the CN1 connector
- R4 (0 ohm) is soldered → in this way VIO is provided by LDO2 output
- The STEVAL-USBDNGV1 is connected to CN2 (as shown in figure 3)
- The STEVAL-USBDNGV1 is connected to the PC through a mini-USB connector plugged on CN1

Figure 4. VIN and VIO connectors details of STEVAL-PMIC1LM1A

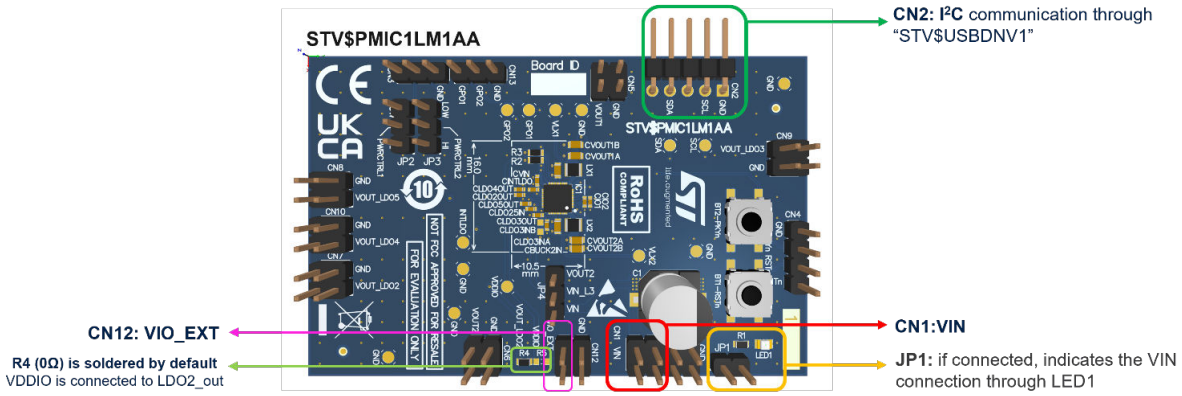
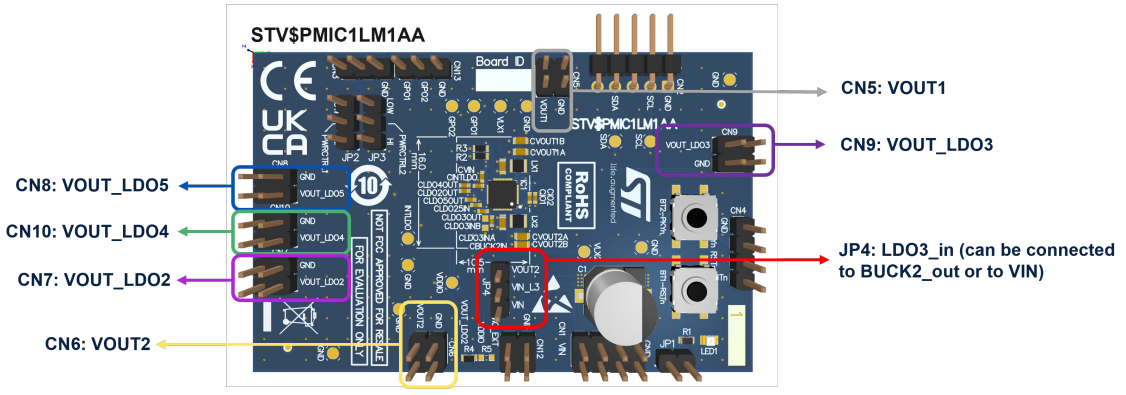


Figure 5 shows the I/O connector of:

- all step-down converters (BUCK1 and BUCK2)
- all LDO regulators (LDO2, LDO3, LDO4, and LDO5)
- JP4, which is a connector that allows to switch LDO3 input between BUCK2 output and the main input supply (VIN)

Figure 5. Buck and LDO connector details of STEVAL-PMIC1LM1A



Note: All buck and LDO input supply pins (except LDO3 input) are connected by default in the board layout to the main input supply (VIN).

Figure 6 shows the VLX test points of BUCK1 and BUCK2:

Figure 6. Buck VLX test point details of STEVAL-PMIC1LM1A

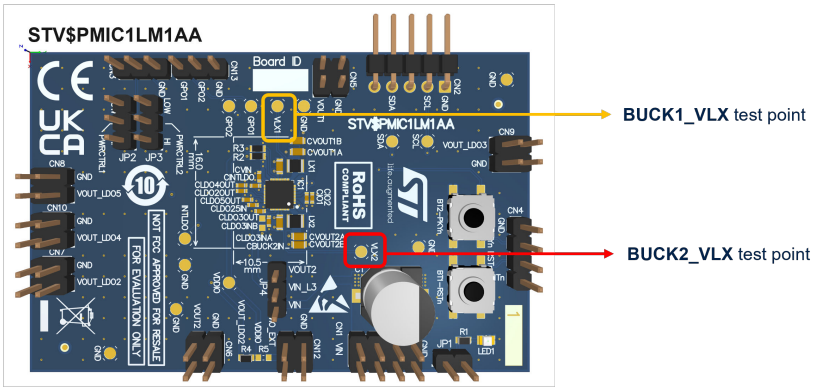


Figure 7 shows the test points of GPO1,2 external controls:

Figure 7. GPO1 and GPO2 test point

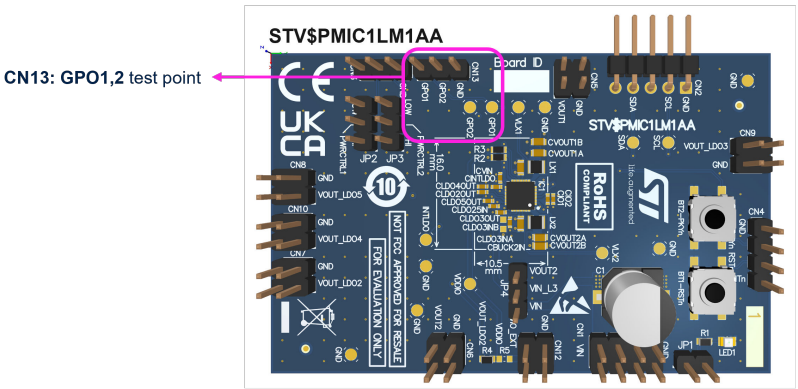
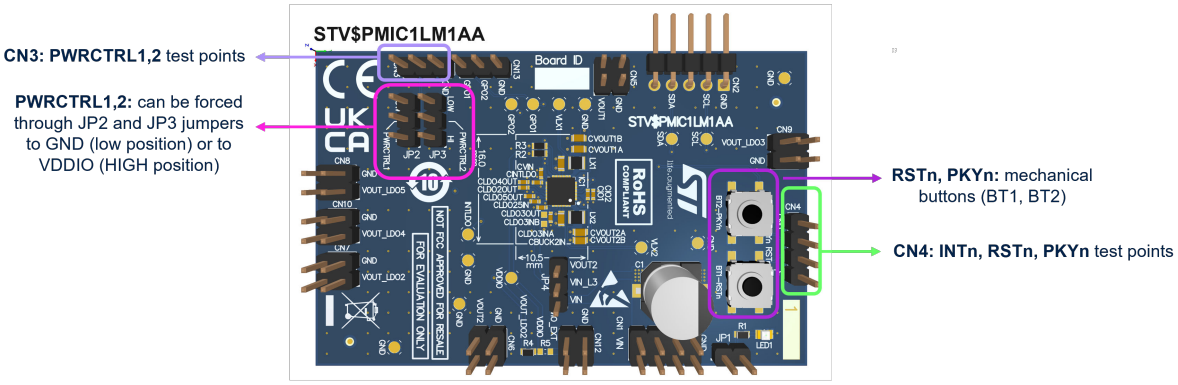


Figure 8 shows the I/O connectors of the digital pins:

- PWRCTRL1,2
  - CN3 are test points
  - JP2 and JP3 allow to force respectively PWRCTRL1 and PWRCTRL2 to VDDIO (in HIGH position) or to GND (in LOW position) using a manual bridge
- INTn, RSTn, PKEYn
  - CN4 are test points
  - BT1 and BT2 are mechanical buttons that if pressed force RSTn and PKYn to GND.
- JP1: if manual bridge is placed over JP1, LED1 will automatically switch on when VIN is provided to the STEVAL-PMIC1LM1A on CN1

Figure 8. Digital connector details (PWRCTRL1, PWRCTRL2, PKYn, RSTn, INTn) of STEVAL-PMIC1LM1A



4 Getting started with STPMIC1L GUI

To get started with the STPMIC1L GUI, see the STSW-PMIC1LGUI user manual.

5 Board layout

The STEVAL-PMIC1LM1A evaluation board is based on a 4-layer PCB, 2s2p, to be compliant with the JEDEC JESD51-2 standard.

5.1 Stack-up layer

Figure 9 shows the PCB stack-up layer used for the STPMIC1L evaluation board.

Figure 9. STEVAL-PMIC1LM1A: PCB stack-up layer

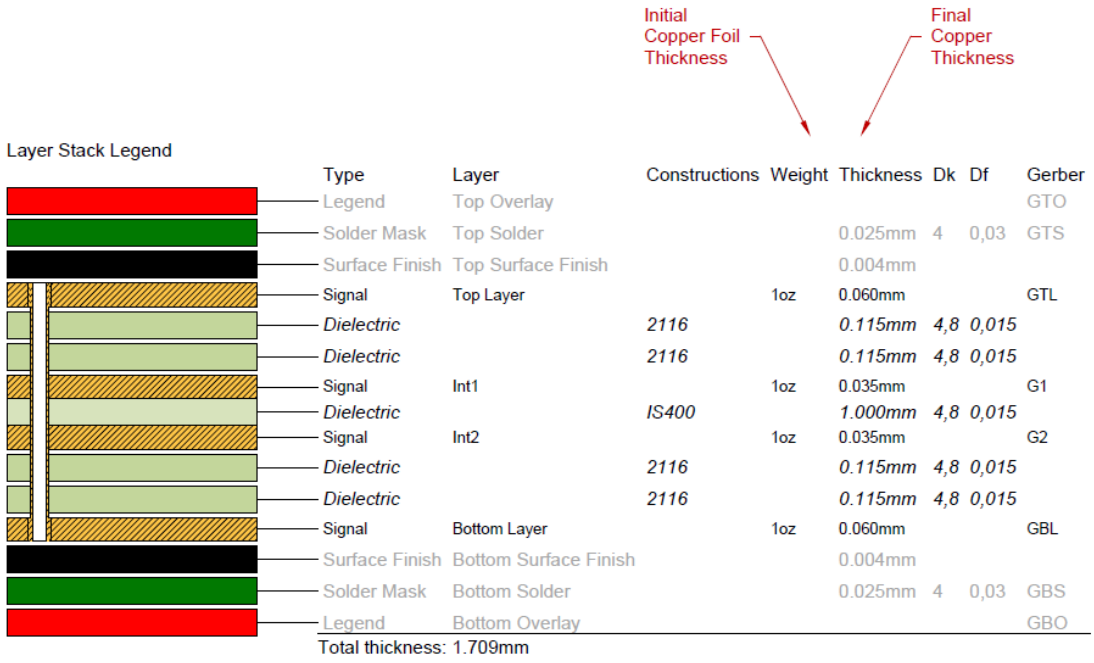


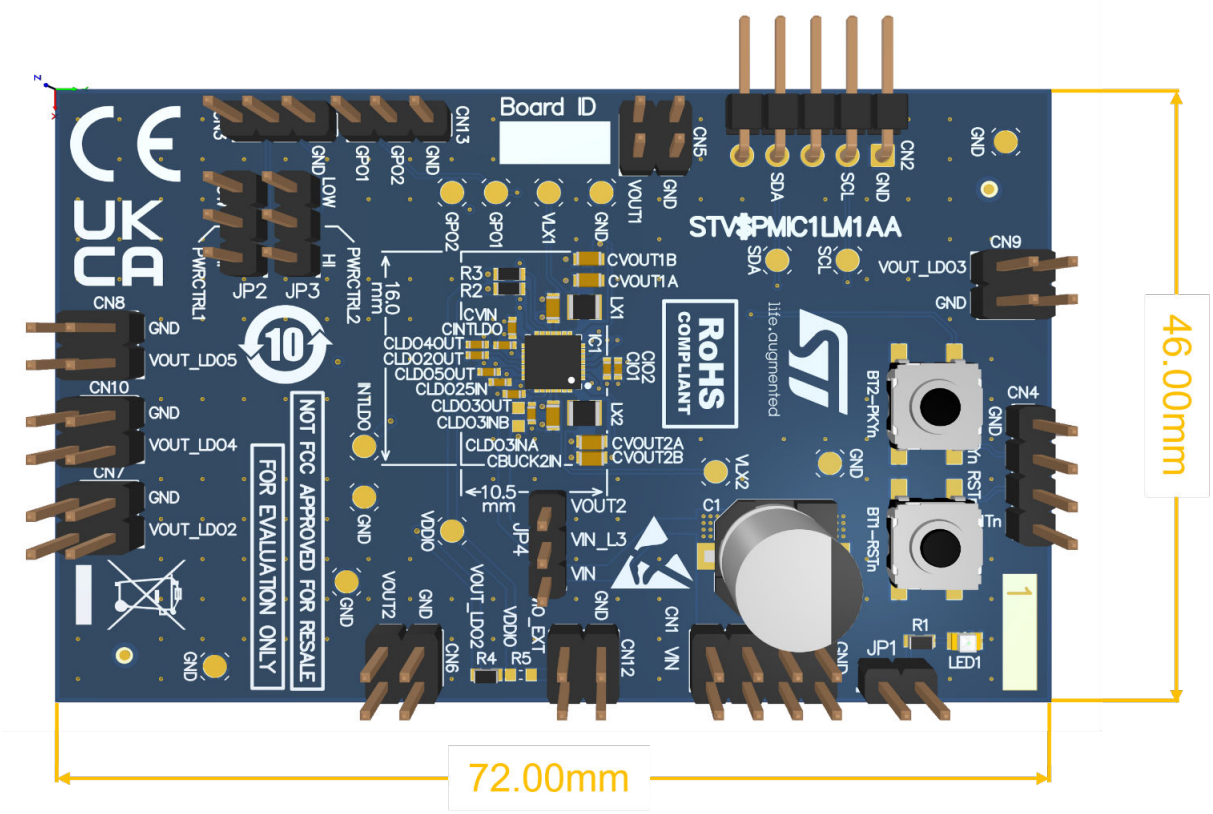
Table 8. STEVAL-PMIC1LM1A evaluation board: stack-up layer details

Layer	Stack-up
Top	Component/power/signal
Mid signal 1	GND
Mid signal 2	Power/GND
Bottom	Power/GND

5.2 Layout details

Figure 10 shows the PCB stack-up layer used for the STPMIC1L evaluation board.

Figure 10. **STEVAL-PMIC1LM1A: 3D layout**



The dimensions of the board are 72 x 46 mm.

Figure 11, Figure 12, Figure 13, and Figure 14 show the details of the top, internal1, internal2, and bottom layers of the STEVAL-PMIC1LM1A, respectively.

Figure 11. **STEVAL-PMIC1LKV1: Top layer (components/power/signal)**

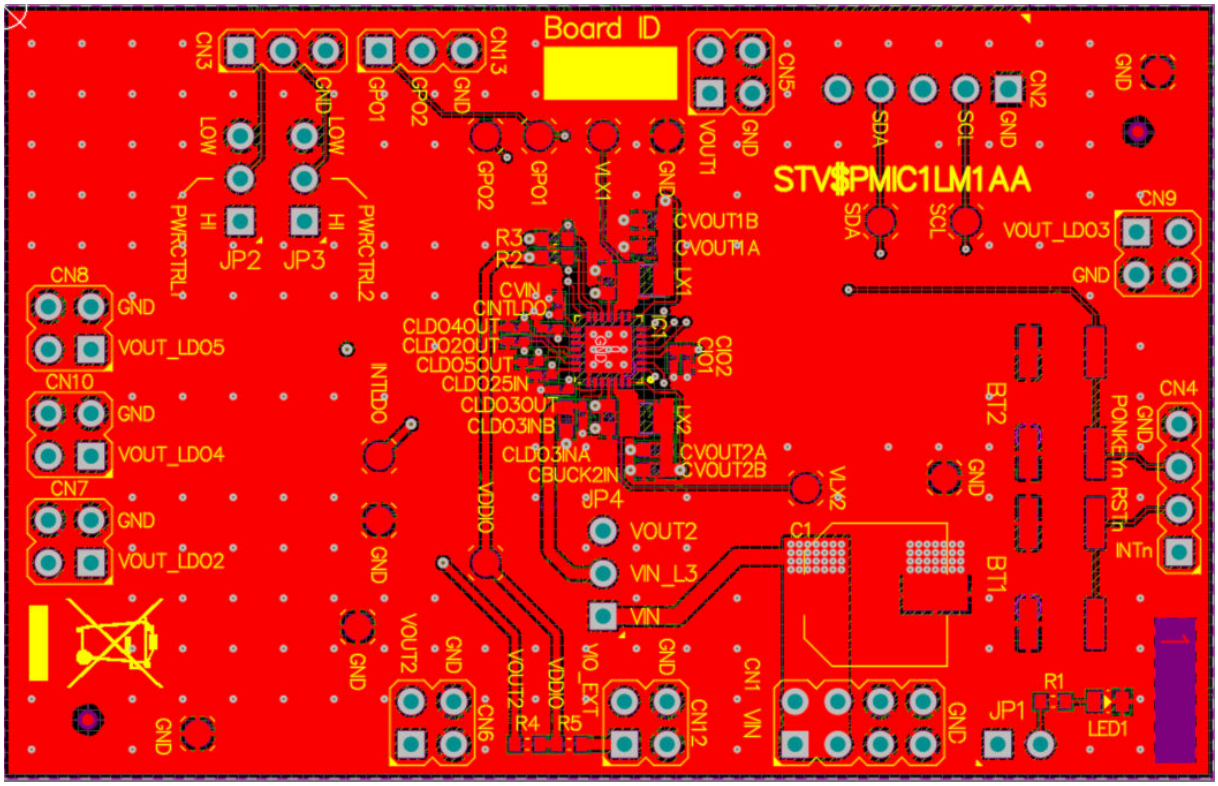


Figure 12. **STEVAL-PMIC1LKV1: Internal layer 1 (GND)**

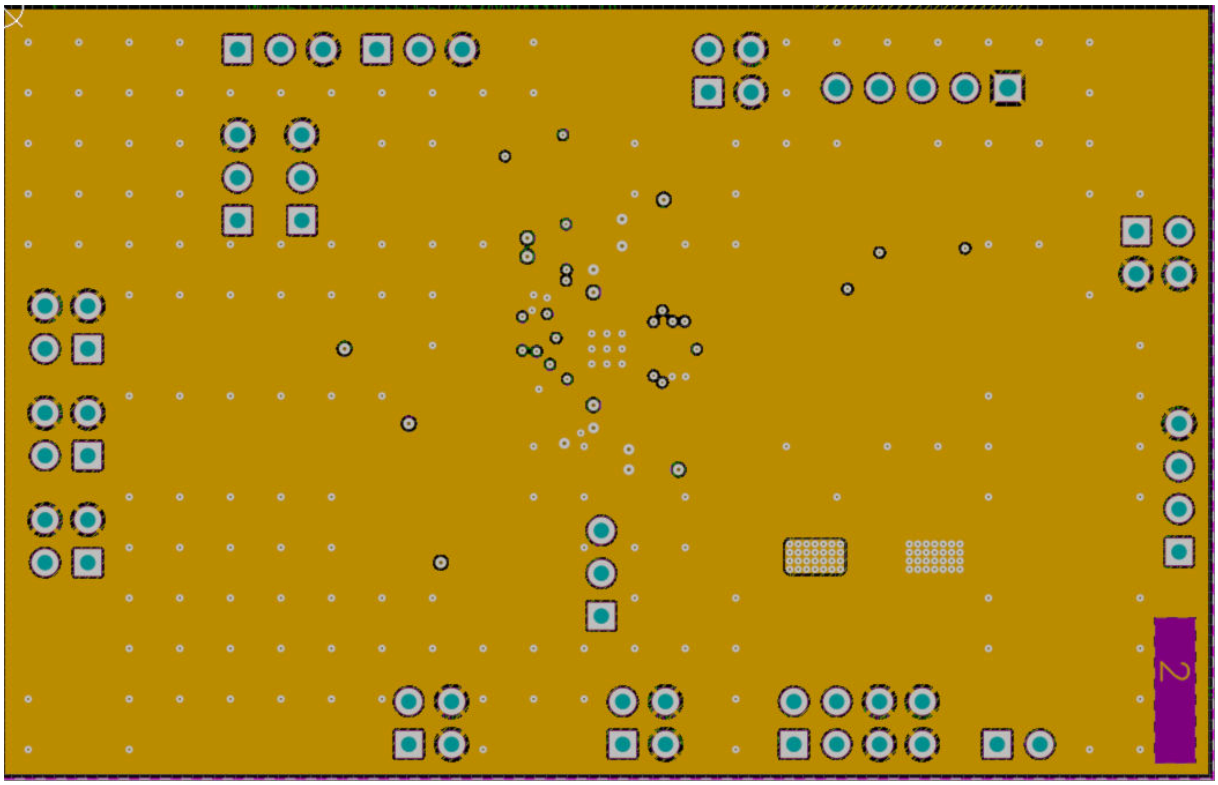


Figure 13. **STEVAL-PMIC1LKV1: Internal layer 2 (Power/GND)**

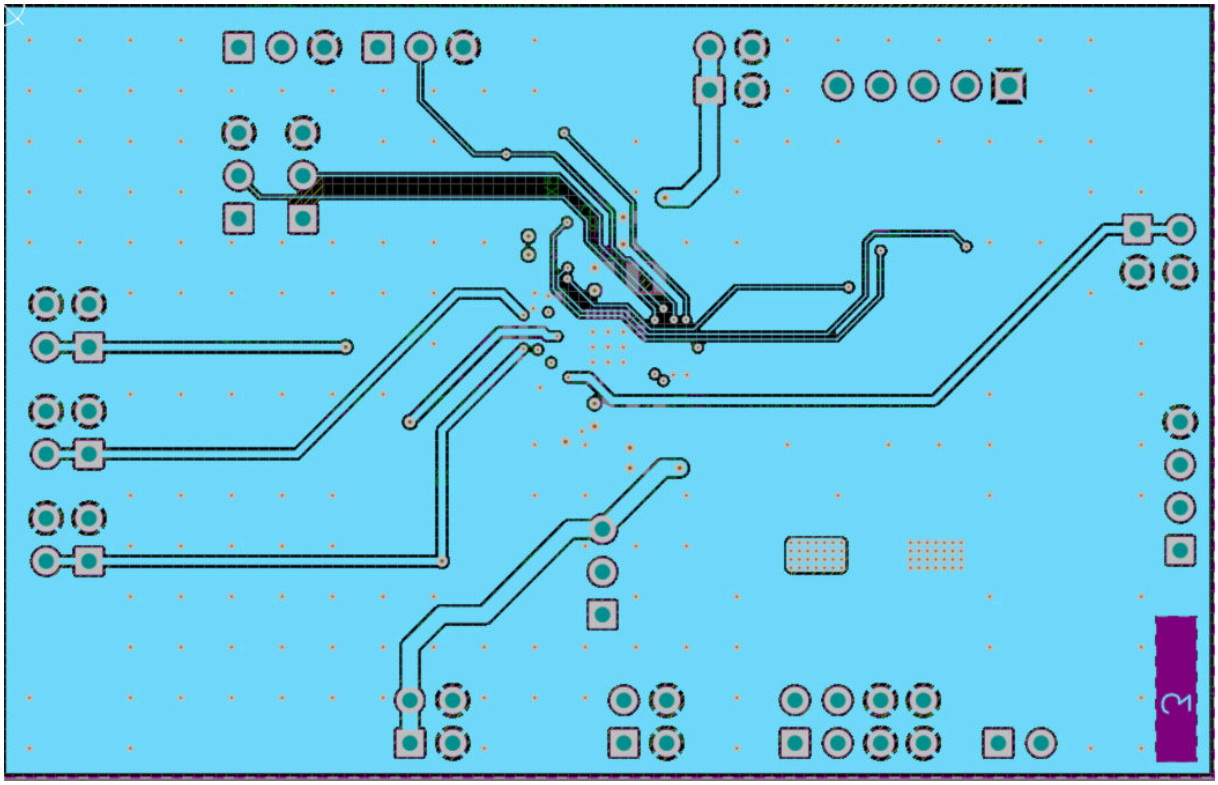
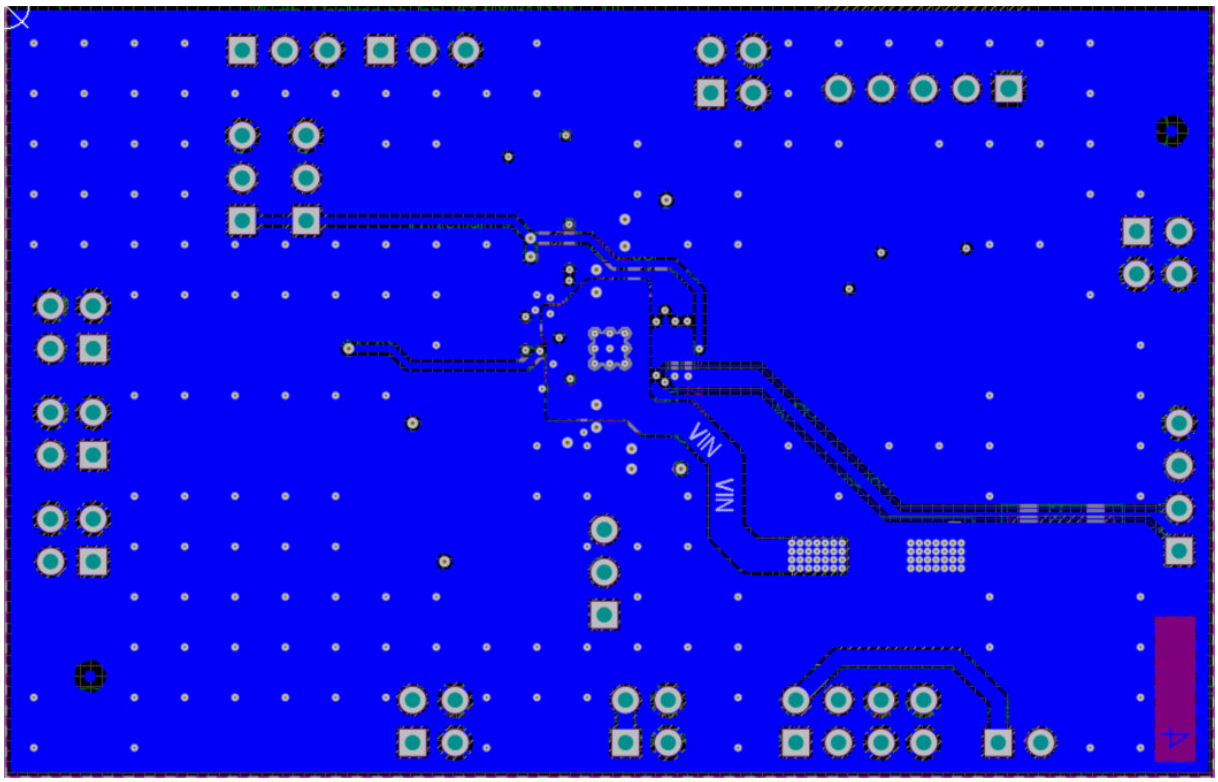


Figure 14. **STEVAL-PMIC1LKV1 evaluation board: Bottom layer (Power/GND)**

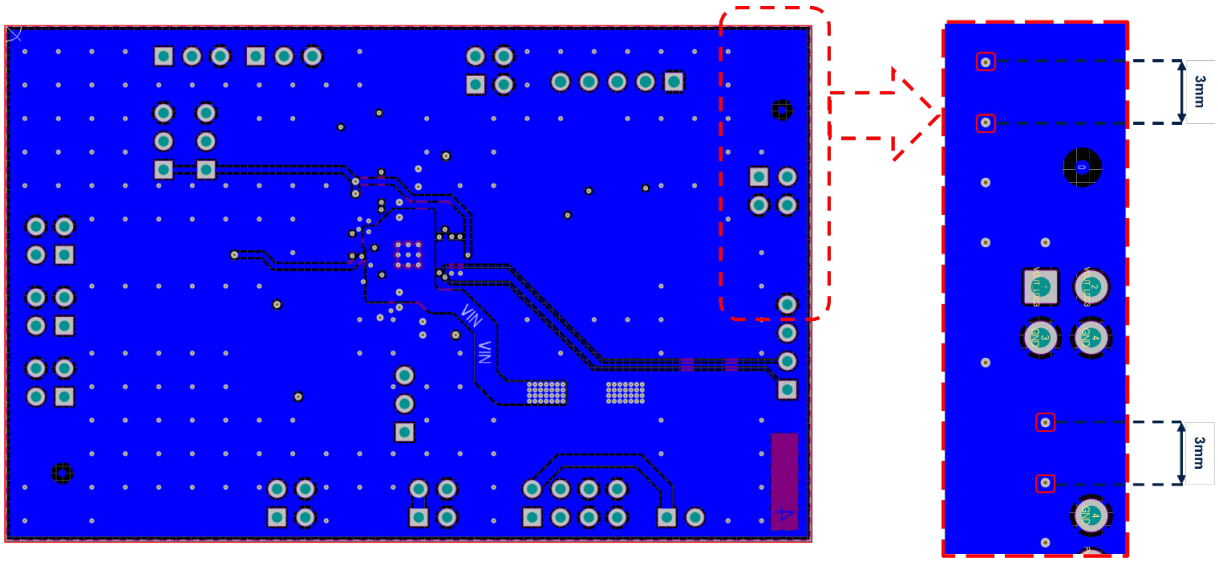


5.3 Power and ground planes

Since both POWER and GROUND are planes, inductive effects are minimized, providing a very low impedance path to the STPMIC1L. The use of a continuous ground layer with multiple via holes is a good method to achieve low impedance ground returns. However, to keep low impedance over all areas of the PCB, the continuous ground layer should never be narrowed or partitioned.

Figure 15 shows the mid layer 1 of the STPMIC1L evaluation board layout, with the detail on GND vias placed all around the PCB edge with 3 mm spacing.

Figure 15. Internal layer 1 (GND plane)



The usage of flat and large shapes, whether possible, is recommended for all high current power supplies such as VIN and VOUT. This helps to reduce the power losses. When examining the ground and power planes, make sure that the plane continuity is not affected by too many vias.

Examples of power planes, vias placement and plane shapes are shown in figure 13 (Internal layer 2), in which they are used to route VIN and all VOUT of the regulators out to connector headers.

5.4 Via holes

Though the ground plane is a good ground reference, the presence of the vias along ground returns introduces some stray inductances at high frequency. Placing multiple via holes in a plane reduces this effect considering that the stray inductances are in parallel. Those via holes must be spaced in such a way that the power plane is not excessively cut up.

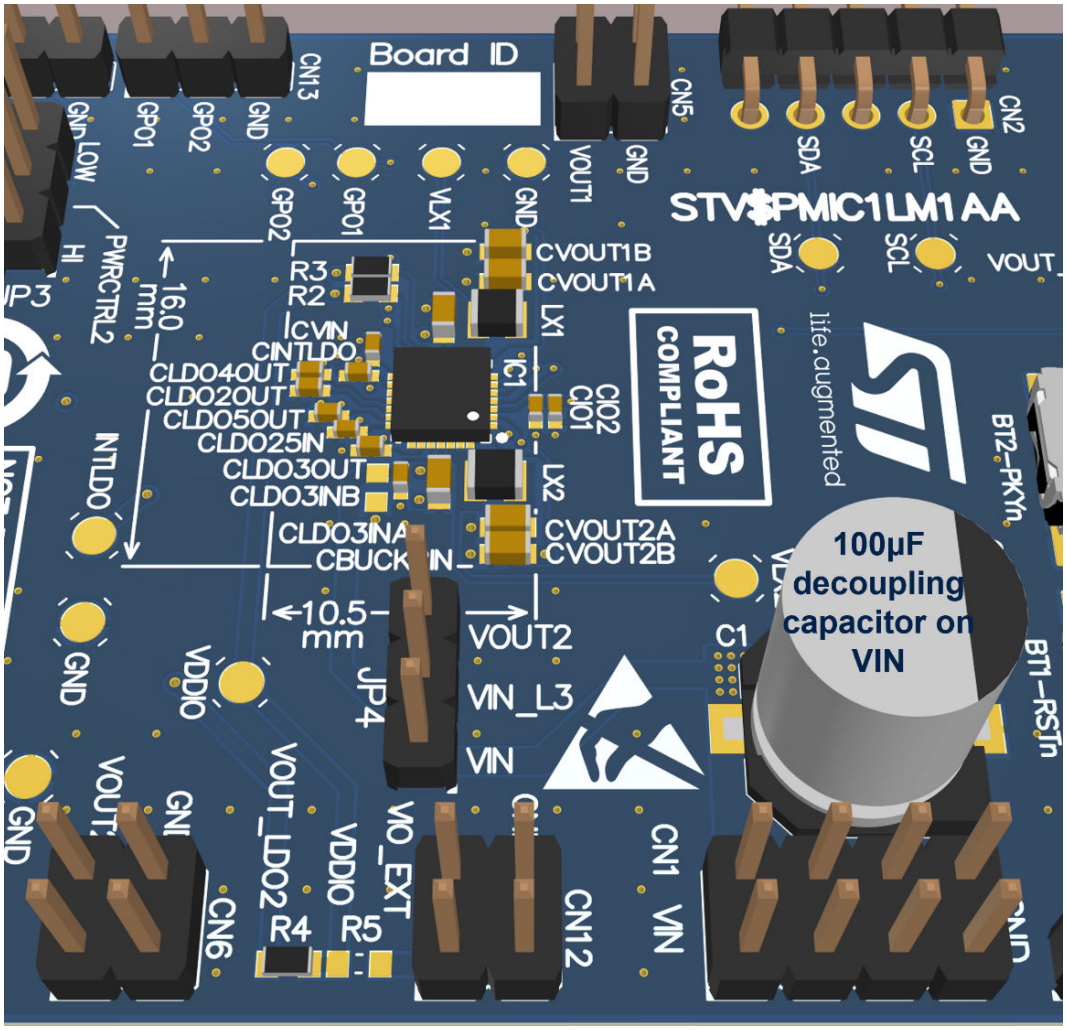
Table 9. Via size

Via type	Hole size	Pad size
Via holes	0.2 mm	0.5 mm

5.5 Passive components placement

Figure 16 shows the arrangement of the passive components (input and capacitors, output coils, and resistors) around the STPMIC1L on the evaluation board with the aim of minimizing the area accupied around the STPMIC1L device (10.5 x 16 mm).

Figure 16. **STEVAL-PMIC1LKV1 evaluation board: passive components placement on the top layer**



All the suggestions described in this document have been applied on the STPMIC1L evaluation board.

It is good practice to place all passive components on top of the layout and to use the bottom side only if necessitated by the application/board size.

A decoupling capacitor of 100 µF is placed on the input supply rail for two reasons:

- In case of an input voltage drop, it provides adequate power to the STPMIC1L to maintain the voltage level.
- In case of a voltage surge, it prevents excess current from flowing through the STPMIC1L to keep the voltage stable.

6 Schematic diagrams

Figure 17. **STEVAL-PMIC1LM1A circuit schematic (1 of 3)**

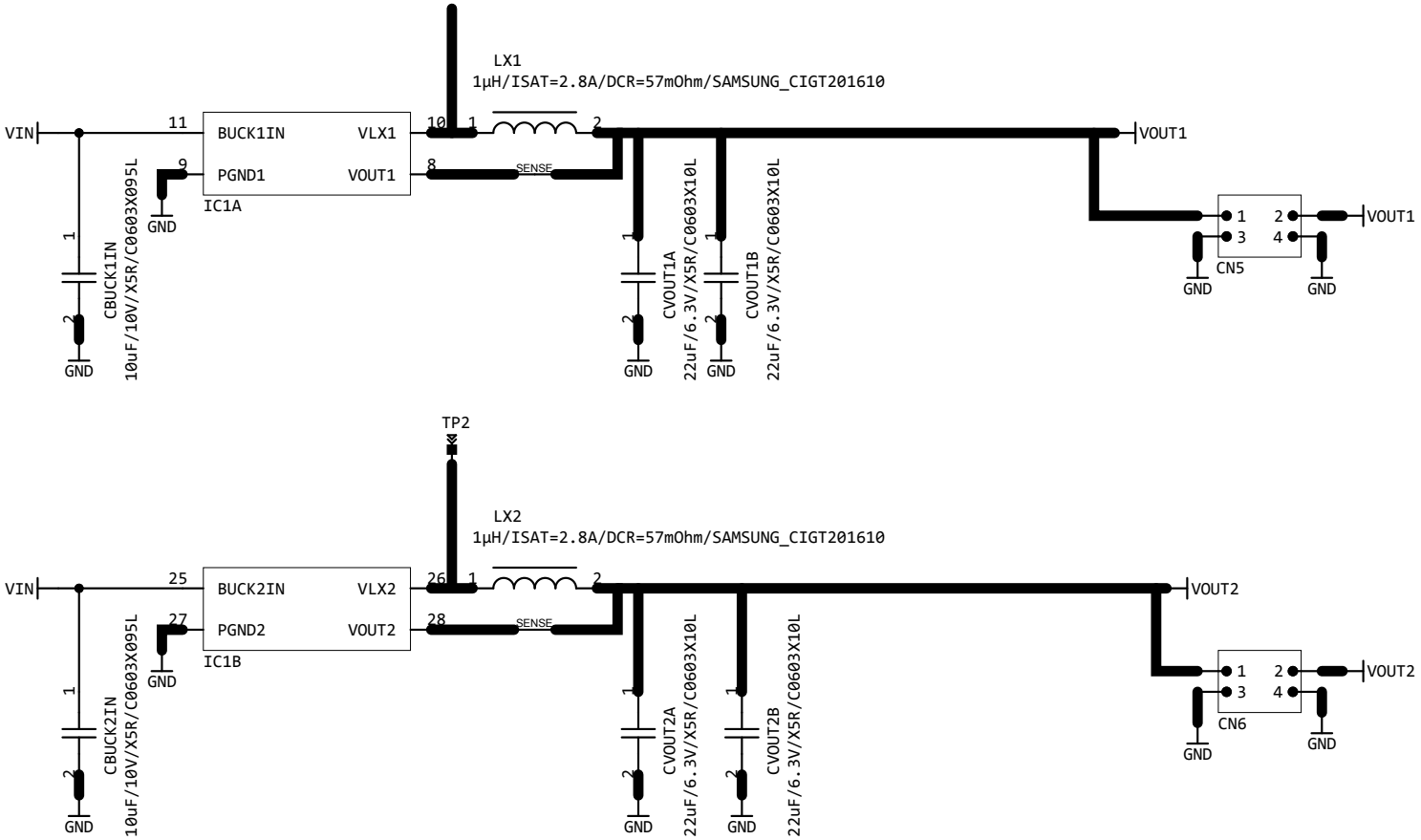


Figure 18. STEVAL-PMIC1LM1A circuit schematic (2 of 3)

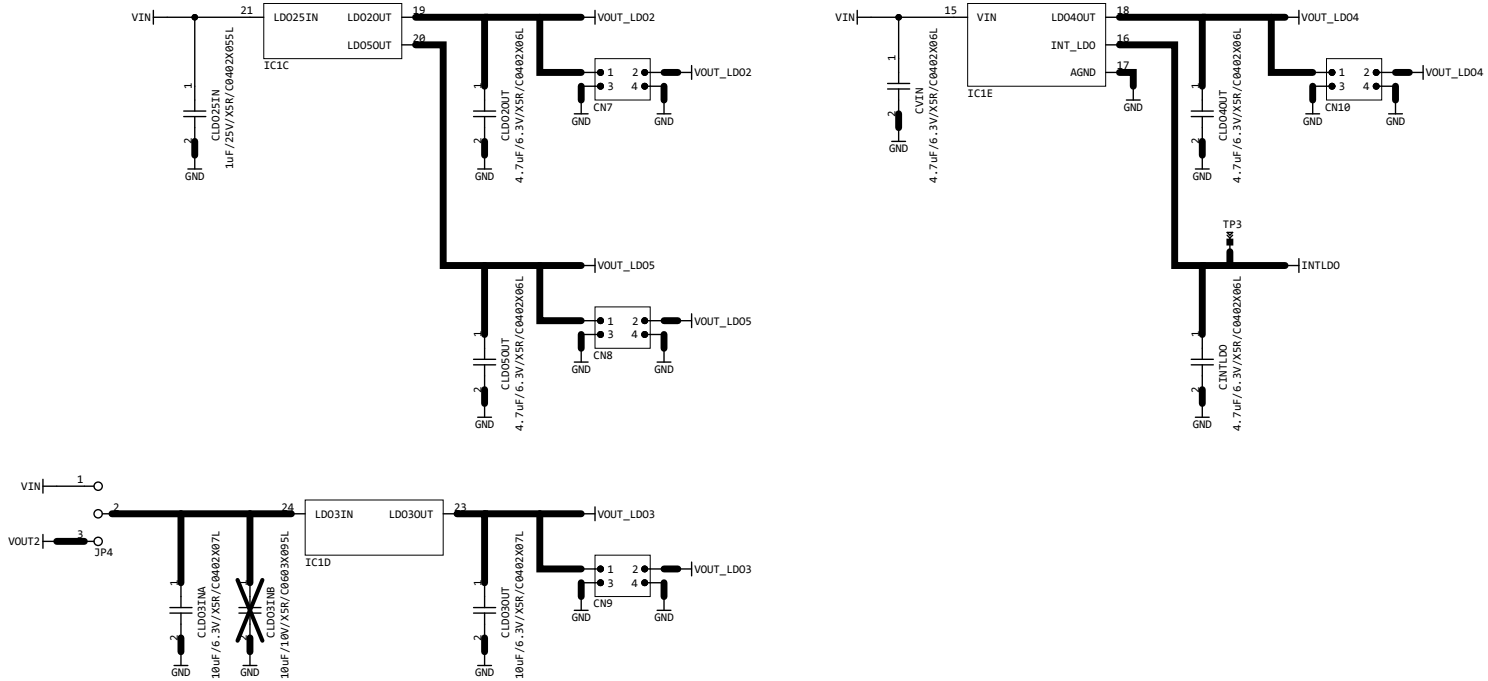


Figure 19. **STEVAL-PMIC1LM1A circuit schematic (3 of 3)**

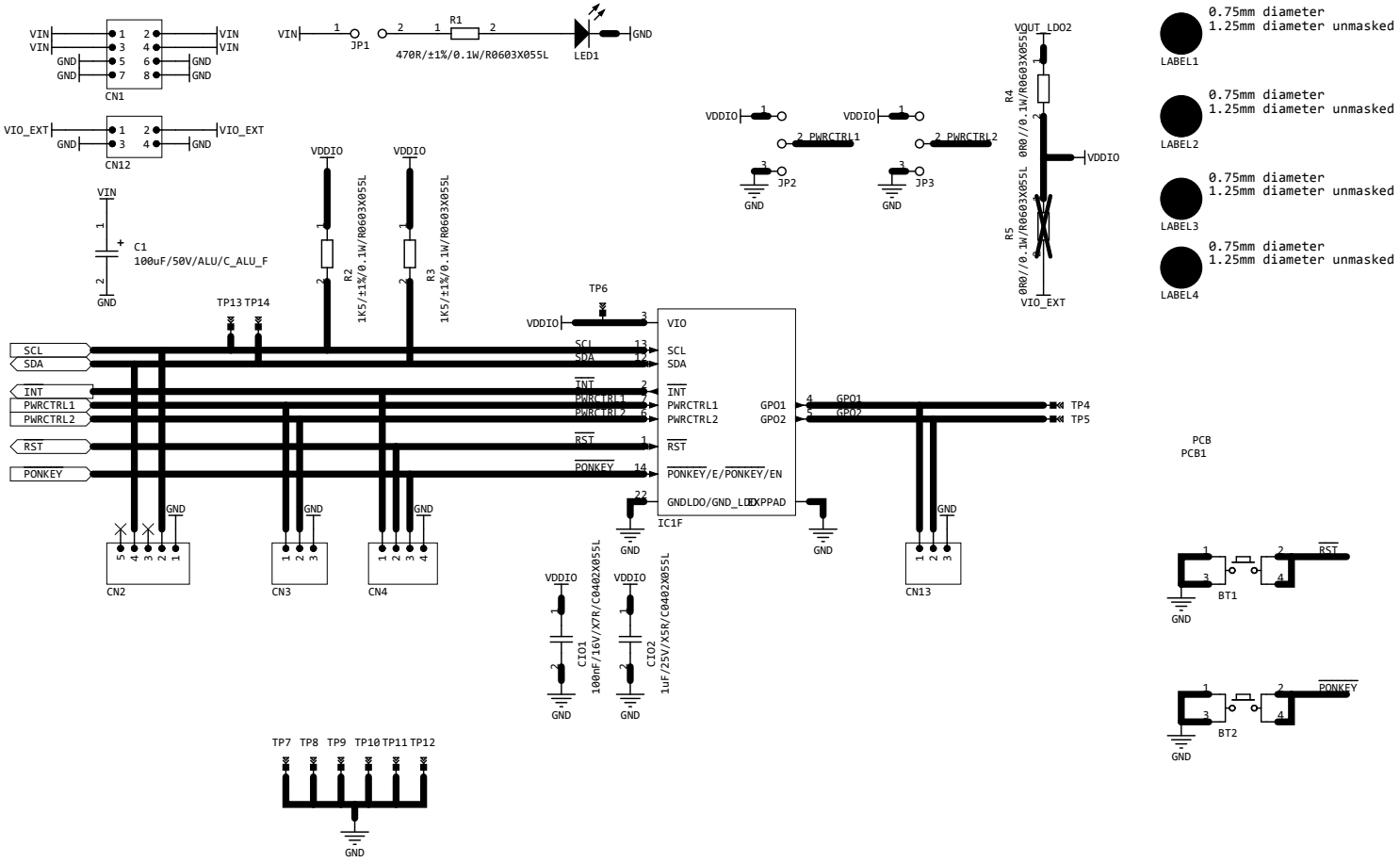
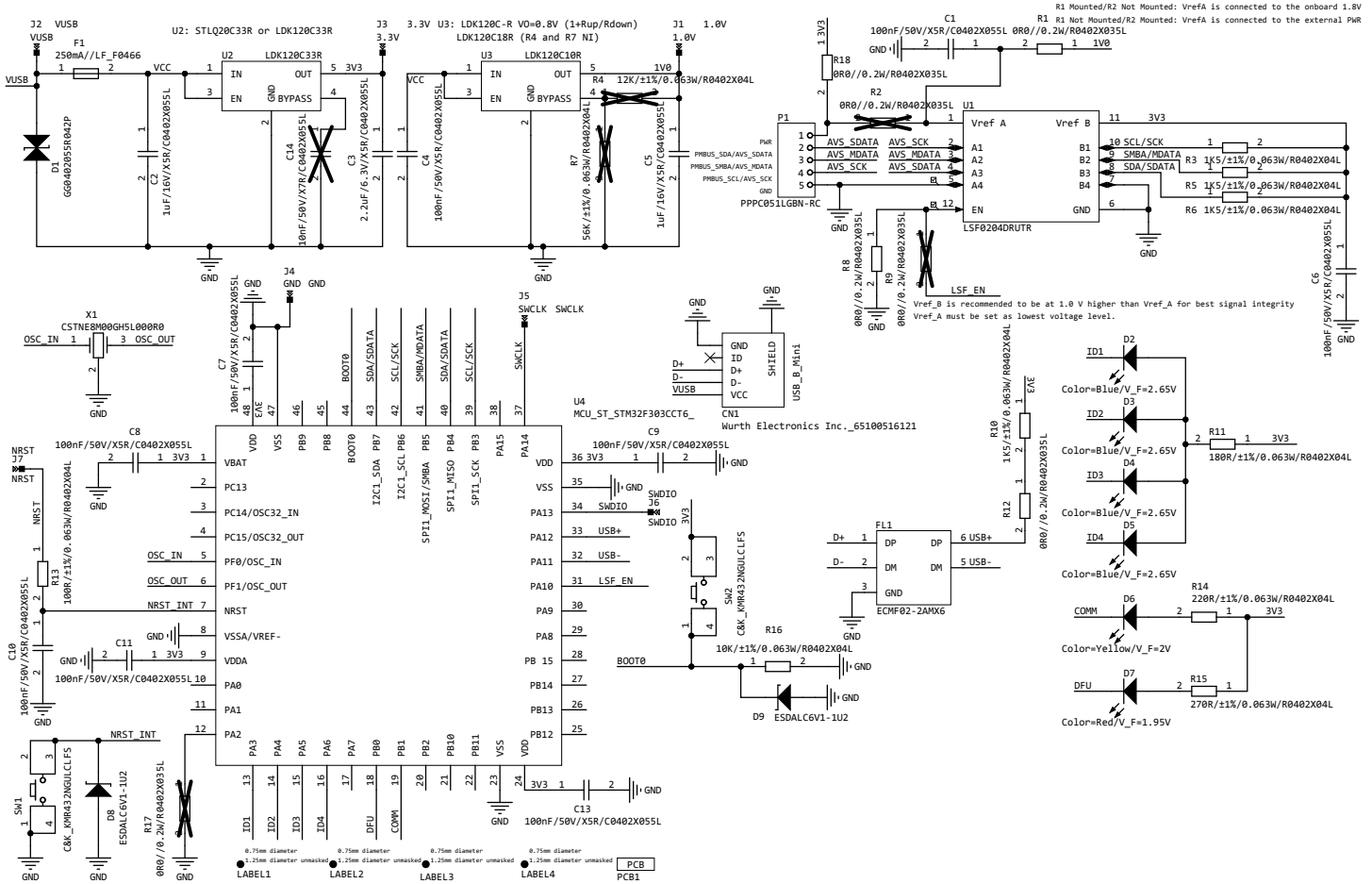


Figure 20. STEVAL-USBDNGV1 circuit schematic



7 Bill of materials

Table 10. STEVAL-PMIC1LKV1 bill of materials

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	-	Table 11. STEVAL-PMIC1LM1A	Evaluation board	ST	Not available for separate sale
2	1	-	Table 12. STEVAL-USBDNGV1	USB dongle	ST	Not available for separate sale

Table 11. STEVAL-PMIC1LM1A bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	2	BT1, BT2	-	Tactile Switches	C&K	KSC351JLFS
2	1	C1	100µF 50V	Aluminium Electrolytic Capacitor	Panasonic Electronic Components	EEE1HA101UP
3	5	CINTLDO, CLDO2OUT, CLDO4OUT, CLDO5OUT, CVIN	4.7µF 6.3V	Multilayer Ceramic Capacitors X5R	Murata Electronics North America	GRM155R60J475ME47
4	2	CBUCK1IN, CBUCK2IN	10µF 10V	Multilayer Ceramic Capacitors X5R	Murata Electronics North America	GRM188R61A106ME69D
5	2	CLDO3INA, CLDO3OUT	10µF 6.3V	Multilayer Ceramic Capacitors X5R	Murata Electronics North America	GRM155R60J106ME05D
6	1	CIO1	0.1µF 16V	Multilayer Ceramic Capacitor X5R	Murata Electronics North America	GRM155R71C104KA88
7	2	CIO2, CLDO25IN	1µF 25V	Multilayer Ceramic Capacitor X5R	Murata Electronics North America	GRM155R61E105KA12
8	4	CVOUT1A, CVOUT1B, CVOUT2A, CVOUT2B	22µF 6.3V	Multilayer Ceramic Capacitors X5R	Murata Electronics North America	GRM188R60J226MEA0
9	2	LX1, LX2	1µH	Power Inductors	Samsung Electro-Mechanics	CIGT201610LH1R0MNE
10	1	R1	470Ω	Thick Film Resistor	YAGEO	RC0603FR-07470RL
11	2	R2, R3	1.5kΩ	Thick Film Resistor	YAGEO	RE0603FRE071K5L
12	1	R4	0Ω	Thick Film Resistor	YAGEO	RC0603FR-070RL
13	1	LED1	Green Led	Standard LEDs - SMD GREEN WATER CLEAR	Kingbright	APT2012SGC
14	1	CN1	-	Headers & Wire Housings WR-PHD 2.54mm Hdr 8P Dual Str Gold	Wurth Electronics Inc.	61300821121

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
15	1	CN2	-	Headers & Wire Housings WR-PHD 2.54mm Hdr 5P Single RA Gold	Wurth Electronics Inc.	61300511021
16	5	CN3, CN13, JP2, JP3, JP4	-	Headers & Wire Housings WR-PHD 2.54mm Hdr 3P Single Str Gold	Wurth Electronics Inc.	61300311121
17	1	CN4	-	Headers & Wire Housings WR-PHD 2.54mm Hdr 4P Single Str Gold	Wurth Electronics Inc.	61300411121
18	7	CN5, CN6, CN7, CN8, CN9, CN10, CN12	-	Headers & Wire Housings WR-PHD 2.54mm Hdr 4P Dual Str Gold	Wurth Electronics Inc.	61300421121
19	1	JP1	-	Headers & Wire Housings WR-PHD 2.54mm 2Pin T HT Header	Wurth Electronics Inc.	61300211121
20	2	B1, B2	Jumpers	Female Straight Black Closed Top 2 Way 1 Row 2.54mm Pitch	RS	251-8503
21	1	IC1	STPMIC1LAPQR, WFQFN 28L	STPMIC1LA	ST	STPMIC1LAPQR

Table 12. STEVAL-USBDNGV1 bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	9	C1, C4, C6, C7, C8, C9, C10, C11, C13	0.10µF 50V	Capacitor	Murata Electronics North America	GRM155R61H104KE14
2	2	C2, C5	1.0µF 16V	Capacitor	Murata Electronics North America	GRM155R61C105KA12
3	1	C3	2.2µF 6.3V	Capacitor	Murata Electronics North America	GRM155R60J225KE01
4	1	CN1	USB 2.0, 30V/1A	Connector	Wurth Electronics Inc.	65100516121
5	1	D1		BidirTVSDiode	Kyocera AVX	GG0402055R042P
6	4	D2, D3, D4, D5		LED	Kingbright	APT1608LVBC/D
7	1	D6		LED	Kingbright	APT1608SYCK
8	1	D7		LED	Kingbright	APT1608SURCK
9	2	D8, D9	ESDALC6V1-1U2, C_0201_0603Metric	TVSDiode	ST	ESDALC6V1-1U2
10	1	F1		Fuse	Littelfuse Inc.	0466.250NRHF

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
11	1	FL1	ECMF02-2AMX6, QFN-6	ESD	ST	ECMF02-2AMX6
12	1	P1		Connector	Sullins Connector Solutions	PPPC051LGBN-RC
13	4	R1, R8, R12, R18	0 Ohms	Resistor	Rohm Semiconductor	PMR01ZZPJ000
14	4	R3, R5, R6, R10	1.5 kOhms	Resistor	Yageo	RC0402FR-071K5L
15	1	R11	180 Ohms	Resistor	Yageo	RC0402FR-07180RL
16	1	R13	100 Ohms	Resistor	Yageo	RC0402FR-07100RL
17	1	R14	220 Ohms	Resistor	Yageo	RC0402FR-07220RL
18	1	R15	270 Ohms	Resistor	Yageo	RC0402FR-07270RL
19	1	R16	10 kOhms	Resistor	Yageo	RC0402FR-0710KL
20	2	SW1, SW2		Button	C&K	KMR432NGULCLFS
21	1	U1		Level Translator BiDir	TI	LSF0204DRUTR
22	1	U2	LDK120C33R, SOT-323-5	LDO	ST	LDK120C33R
23	1	U3	LDK120C10R,SOT-323-5	LDO	ST	LDK120C10R
24	1	U4	STM32F303CCT6, LQFP-48	MCU	ST	STM32F303CCT6
25	1	X1	8 MHz	Resonator	Murata Electronics	CSTNE8M00GH5L000R0

8 Kit versions

Table 13. STEVAL-PMIC1LKV1 kit versions

Finished good	Schematic diagrams	Bill of materials
STV$PMIC1LKV1A(1)	STV$PMIC1LKV1A schematic diagrams	STV$PMIC1LKV1A bill of materials

1. *This code identifies the STEVAL-PMIC1LKV1 evaluation kit first version. The kit consists of a STEVAL-PMIC1LM1A whose version is identified by the code STV$PMIC1LM1AA and a STEVAL-USBDNGV1 whose version is identified by the code STEVAL$USBDNGV1A.*

9 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

Revision history

Table 14. **Document revision history**

Date	Version	Changes
19-Nov-2025	1	Initial release.

Contents

List of figures

List of tables