Radiation Hardened 5 A monolithic synchronous switching regulator

Introduction

The STEVAL-LEOPOL1V1 is created and optimized for a typical application of the LEOPOL1.

LEOPOL1 is a single phase, step-down monolithic switching regulator with high precision internal voltage reference and integrated power MOSFETs for synchronous conversion.

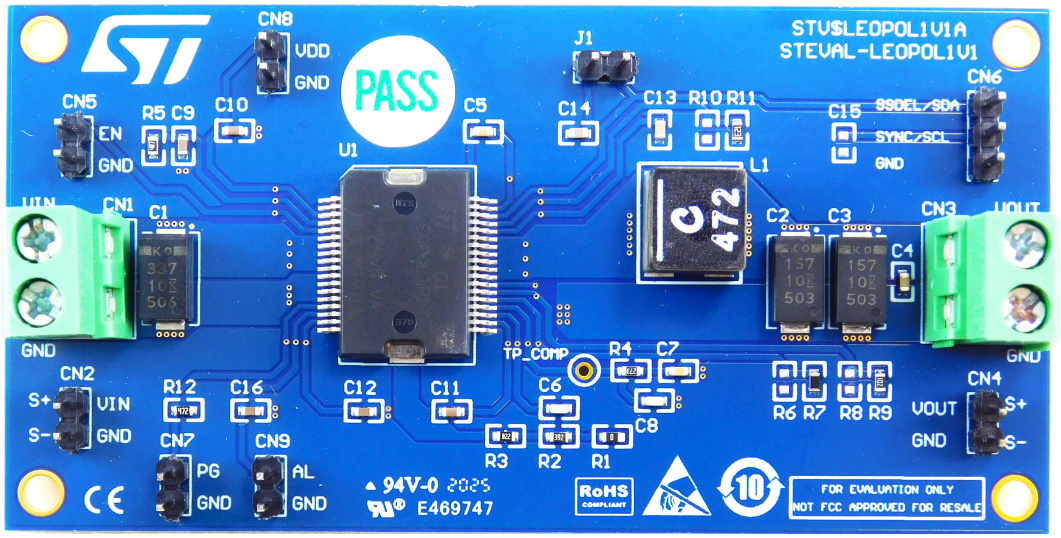
The regulator LEOPOL1 converts 3 ~ 12 V input voltage to 0.8 V ~ (0.85 x VIN) output voltage. The controller is based on a peak current mode architecture, which ensures a fast load transient response and very stable switching frequency. An embedded integrator compensates the DC voltage error due to the output voltage ripple.

The STEVAL-LEOPOL1V1 is optimized to meet the radiation hardness required for low Earth orbit space (LEO).

It can operate in a wide operating temperature condition from -40 to 125°C.

The main applications are: power management in satellites for low Earth orbit (LEO); FPGA, MPU, ASIC, and MCU power supply; and power management in radiative and other harsh environments.

Figure 1. STEVAL-LEOPOL1V1 evaluation board



Notice: *For dedicated assistance, submit a request through our online support portal at **www.st.com/support**.*

1 Features

- Input operating voltage: 5.0 V
- Output voltage: 1.2 V
- Output current: up to 5 A
- Enable input voltage: 2.5 V
- Switching frequency: 500 kHz
- Output overcurrent protection: 10 A
- Easy synchronization with 180° out-of-phase management (up to 2 ICs)
- Target radiation performance:
  - 50 krad (Si) total ionizing dose
  - TNID immune at 3.1011 PROTON / cm²
  - SEL free up to 62 MeV. cm² / mg

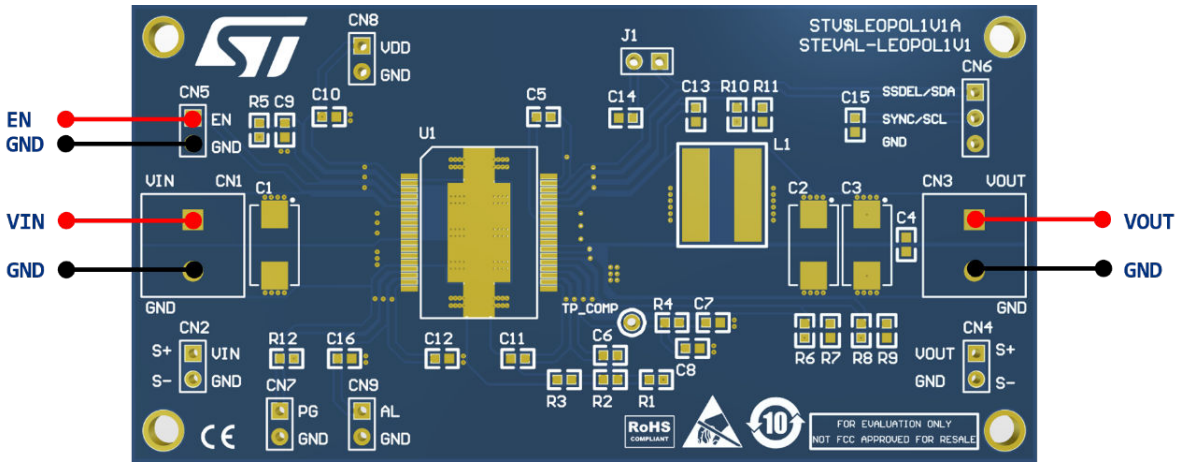
2 Input and output connections

Table 1. Input and output connections

Reference Designator	Name	Description
CN1	VIN	CN1_1: VIN power CN1_2: GND power
CN2	VIN_SENSE	CN2_1: VIN sense (s+) CN2_2: GND sense (s-)
CN3	VOUT	CN3_1: VOUT power CN3_2: GND power
CN4	VOUT_SENSE	CN4_1: VOUT sense (s+) CN4_2: GND sense (s-)
CN5	EN	CN5_1: EN pin CN5_2: GND
CN6	SSDEL/SYNC	CN6_1: SSDEL/SDA pin • J1: through a capacitor to GND CN6_2: SYNC/SCL pin CN6_3: GND
CN7	PGOOD	CN7_1: PGOOD pin CN7_2: GND
CN8	VDD	CN8_1: VDD pin CN8_2: GND
CN9	AL	CN9_1: AL pin CN9_2: GND

3 Connectors

Figure 2. **In/out connectors**



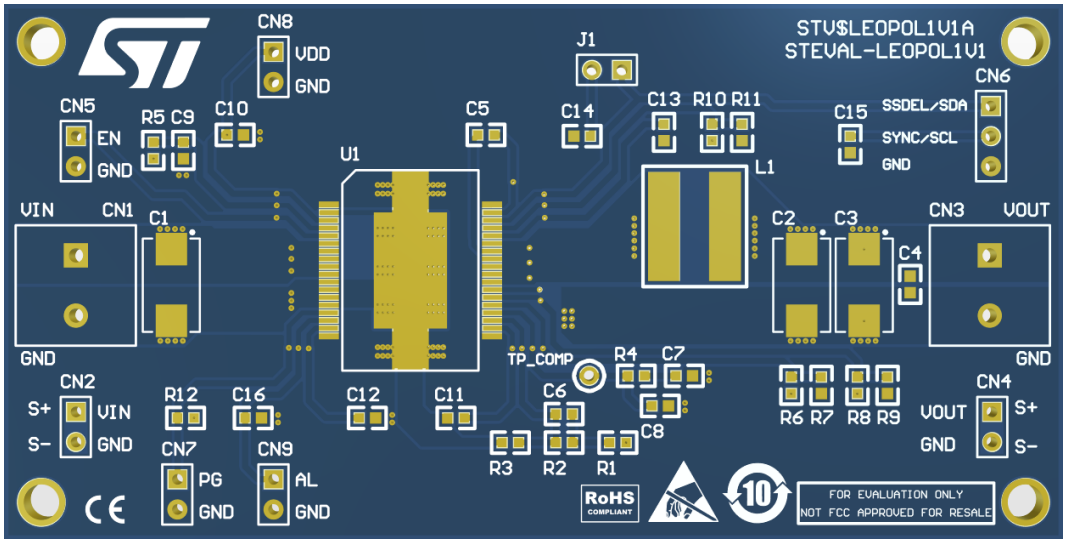
1. Connect a power supply between VIN power (CN1_1) and GND power (CN1_2), and a power supply between EN (CN5_1) and GND (CN5_2). The output voltage is present on the VOUT pin at the voltage value set by R_1 and R_2.
2. Connect a multimeter between VIN (S+) (CN2_1) and GND (S-) (CN2_2) for precise input voltage sensing.
3. Connect a multimeter between VOUT (S+) (CN3_1) and GND (S-) (CN3_2) for precise output voltage sensing.
4. Connect a multimeter between VDD (CN8_1) and GND (CN8_2) for precise VDD voltage sensing. This pin outputs a 2.7 V regulated voltage.
5. R_{10} - R_{11} SLOPE: the slope compensation ramp is programmed by connecting an external R_{SLOPE} resistor (R_{11}) between the SLOPE pin and GND. The default internal slope compensation is also implemented. It can be enabled by pulling up the voltage on the SLOPE pin higher than 2 V or, better, up to VDD by a resistor (R_{10}) or simply by a short. If the SLOPE pin is directly shorted to GND, both ramps, default current slope, and programmed external current slope are disabled.
6. R_8 - R_9 ILIM: the default value for the overcurrent threshold is 10 A, with a second level OCP of 13 A (ILIM pin pulled up to VDD through R_8). If a resistor (R_9) is connected between ILIM pin and GND, the I_{LIM1} threshold can be set to a lower value, and the I_{LIM2} is consequently set at 1.3 x I_{LIM1}.
7. R_6 - R_7 FSW: the regulator switching frequency can be programmed by connecting an external resistor (R_7) between FSW pin and GND. A voltage of 1 V is present on the FSW pin, so a current of 1 V / R_{FSW} is set on the resistor. This current is used to charge an internal capacitor (~20 pF). The switching frequency can range from 100 kHz to 1 MHz. If the FSW pin is connected to a voltage higher than 2 V (it's better if it is shorted to VDD through R_6), the external programmability is turned off and the internal default frequency, tuned at 500 kHz, is enabled. To set "slave mode" configuration, the FSW pin must be forced to a voltage lower than 0.1 V or, better, shorted to ground. The internal clock is normally present to the SYNC pin with 180° phase shifting.
8. CN6 - SSDEL/SYNC: the device can also use the connectors on the demonstration board to directly control the features through an I²C interface. In order to enable the serial interface, the EN pin must be set to -2 V and J1 must be left open. **Be mindful of the capacitive load on pin SYNC**: max allowed capacitive load (equivalent) for SLAVE devices is 150 pF.

4 Board layout guidelines

4.1 Guidelines

The DC-DC converter area is very sensitive, and it is necessary to pay attention to the layout of this part. This is because the DC-DC converter generates GND noise that can get coupled with surrounding ground, therefore reducing the sensitivity and high-frequency components can disturb the RF part of the system. To ensure a correct layout, it is necessary to provide efficient filtering by placing capacitors as close as possible to the device pins. To reduce parasitic inductance and resistance, it is recommended to use connections as wide and short as possible.

Figure 3. Demo boards

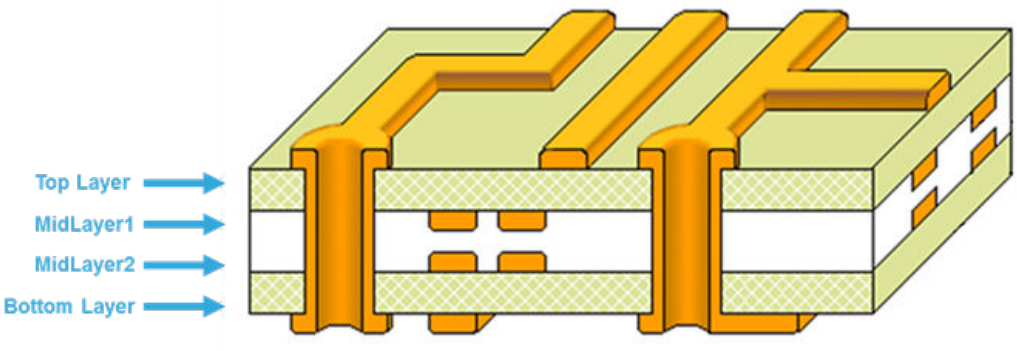


4.2 Four-layer boards

A four-layer board is strongly recommended, with top and bottom layers connected to ground (0 V). Use a ground plane internally (mid layer) to reduce the coupling between the traces. Put this ground layer very close to the top layer to obtain a good ground plane reference. A thickness between the top layer and ground layer of 0.2 mm or 0.3 mm is suggested.

If it is not possible to use a four-layer board, it is recommended to shield the area under the RF part (mainly traces of LX and ground-current return paths) of the board with ground metal to reduce or eliminate radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects and to ensure a good ground reference plane to the RF parts.

Figure 4. Four-layer PCB

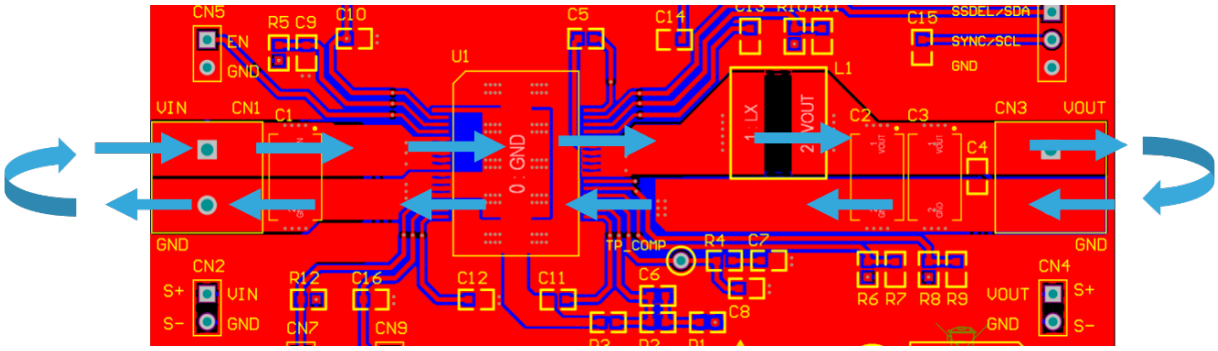


4.3 Ground plane

Any switch-mode power supply requires a good PCB layout in order to achieve maximum performance. Component placement, GND trace routing, and width are the main issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed. All traces carrying current should be drawn on the PCB as short and thick as possible. This should be done to minimize resistive and inductive parasitic effects, and to increase system efficiency. A PCB (ring) ground plane is suggested to avoid spikes on the output voltage. Good soldering of the exposed pad also helps with this issue.

Connect all the ground metallization and/or layers with as many vias as possible. Ground vias between layers should be added liberally throughout the RF portion of the PCB. This helps prevent accrual of parasitic ground inductance due to ground-current return paths. The vias also help to prevent cross-coupling from RF and other signal lines across the PCB.

Figure 5. Ground plane



The layers assigned to system bias (DC supply) and ground must be considered in terms of the return current for the components. The general guidance is not to have signals routed on layers between the bias layer and the ground layer.

Figure 6. Incorrect ground plane assignment

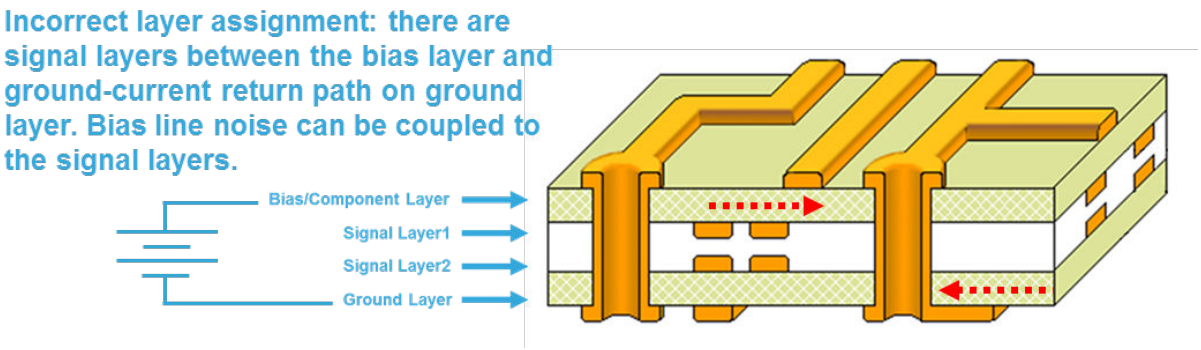
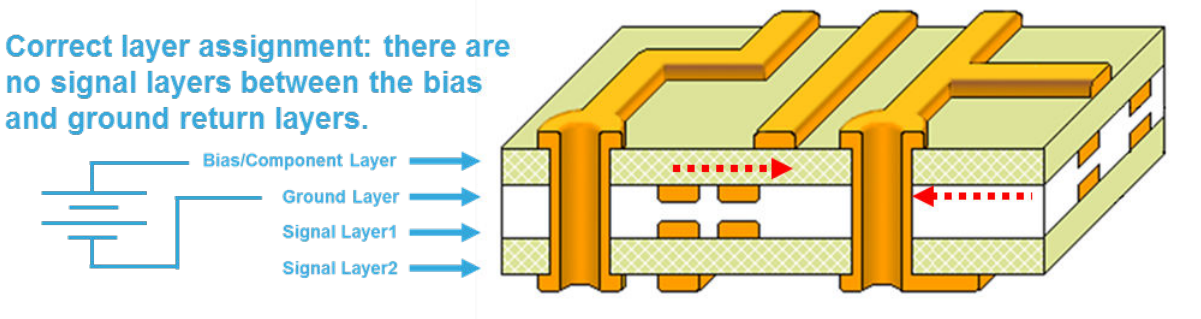


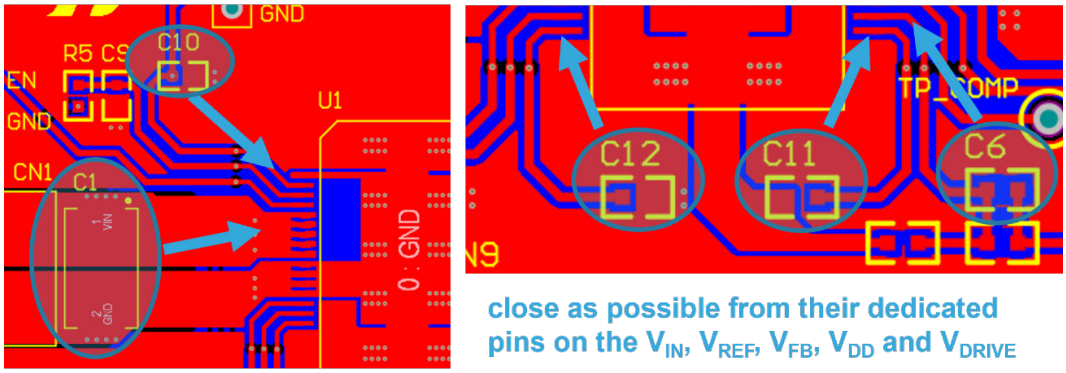
Figure 7. Correct ground plane assignment



4.4 Capacitors placing

Particular care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering by placing these capacitors as close as possible to their dedicated pins on the V_{IN}, V_{REF}, V_{FB}, V_{DD} and V_{DRIVE}.

Figure 8. Capacitors placing

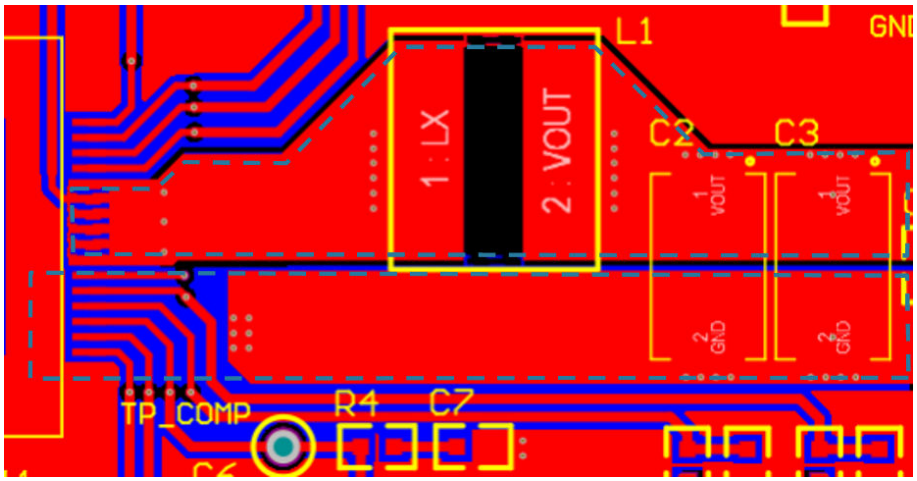


The layout of decoupling capacitors is extremely important to minimize the induction loop formed between the capacitor, the IC power, and the ground. The vias should be placed on the side of the capacitor lands (at the ends). The vias should be located at minimum keepout distance and connected to the capacitor lands with a wide trace, at least as wide as the via pad. Vias of opposite polarity should be placed as close together as possible (minimum keepout distance) and vias of the same polarity should be as separated as possible. If the space allows it, a second pair of vias on the opposite side of the capacitor may be added to further reduce the inductance.

4.5 Inductor placing

The DC-DC converter inductor must be placed as close as possible to the LX pin, with short and thick traces. This should be done to minimize resistive parasitic effects and increase system efficiency.

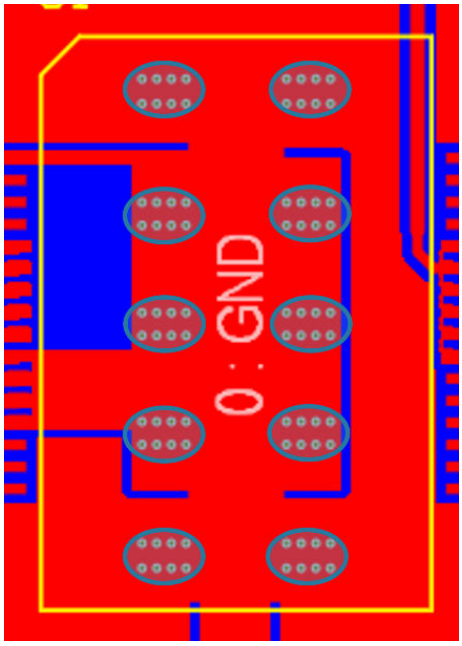
Figure 9. Inductor placing



4.6 Vias placing

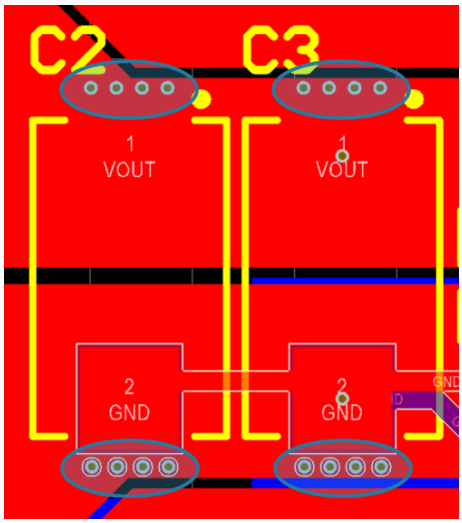
Properly connecting the ground of the exposed pad of the PowerSO 36 to the ground of the application board is crucial. This may be accomplished by placing many vias to ensure that the parasitic inductance introduced from each via is negligible.

Figure 10. Package vias placing



Connect all the ground metallization and/or layers with as many vias as possible. The vias should be located at minimum keepout distance, in order to minimize resistive and inductive parasitic effects.

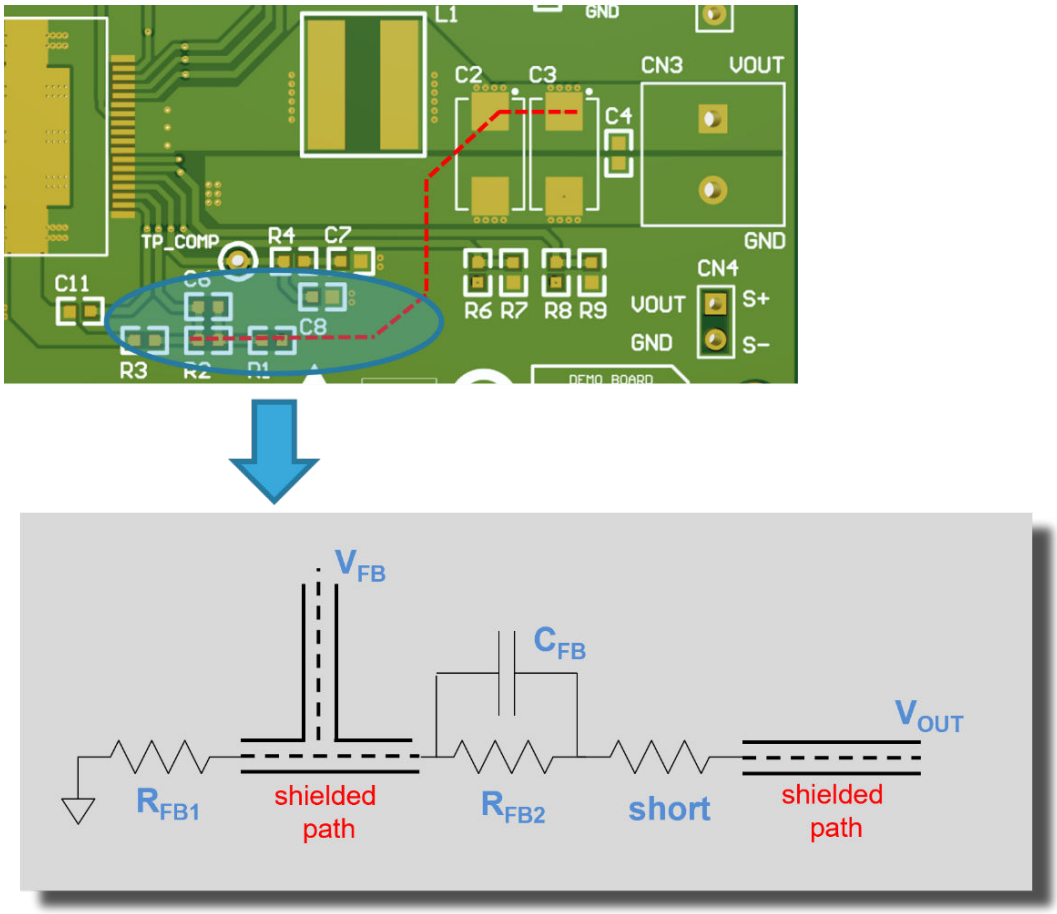
Figure 11. Capacitor vias placing



4.7 Feedback voltage

V_{FB} is generated by a precision voltage divider. The use of low tolerance resistors is recommended. Place a decoupling capacitor very close to the V_{FB} pin. Use good capacitor layout techniques. Place the voltage divider resistors close to the V_{FB} pin to minimize trace length, but not so close that they interfere with other critical signals or power routing. Do not route the V_{FB} trace near noisy traces or planes. Do not place a decoupling capacitor at the junction of the resistors, but only at the V_{FB} pin.

Figure 12. Feedback voltage

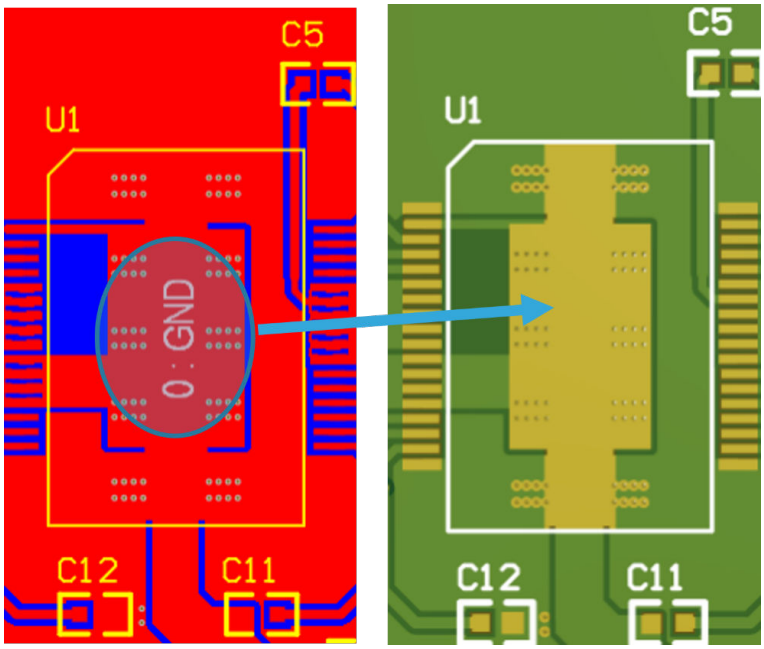


4.8 Thermal aspects

The LEOPOL1 power dissipation inside the IC is mainly due to the DC-DC integrated MOSFETs power loss. The heat generated due to this power dissipation level requires a suitable heatsink to keep the junction temperature below the overtemperature protection threshold at the rated ambient temperature. To improve heat dissipation, where possible, try to increase the number of power planes connected, at least below the IC position. Different layouts are also possible. Basic principles suggest:

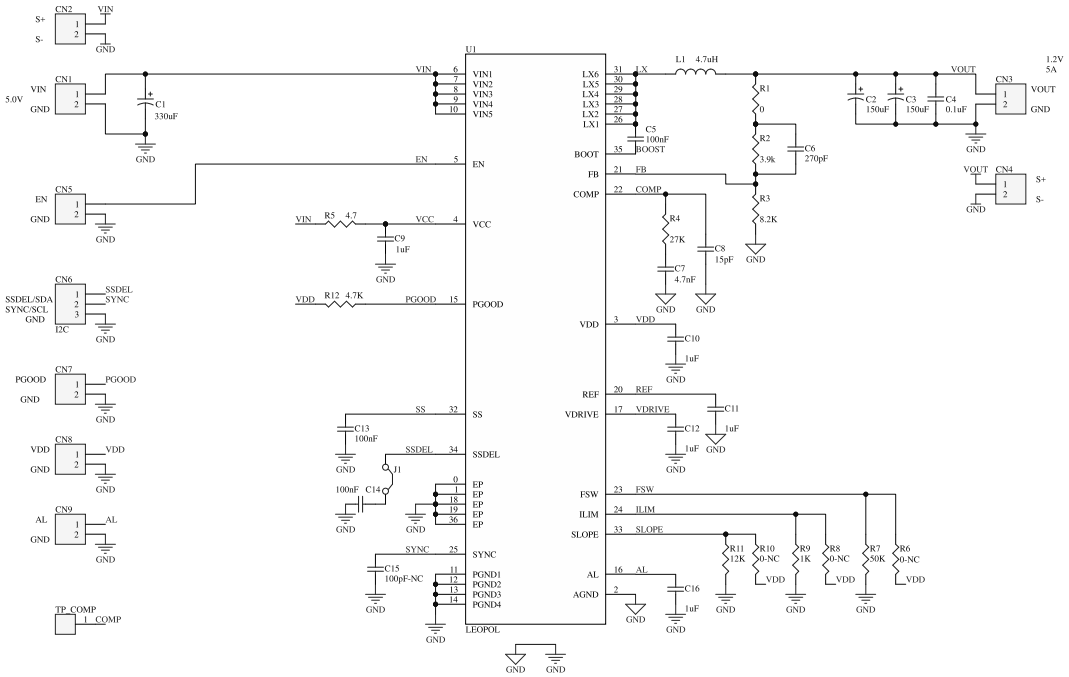
- Keeping the IC and its ground exposed pad approximately in the middle of the dissipating area.
- Providing as many vias as possible.
- Designing a dissipating area with a shape as square as possible and not interrupted by other copper traces.

Figure 13. **Thermal aspects**



5 Schematic diagrams

Figure 14. **STEVAL-LEOPOL1V1 circuit schematic**



6 PCB

Figure 15. **Assembly layer**

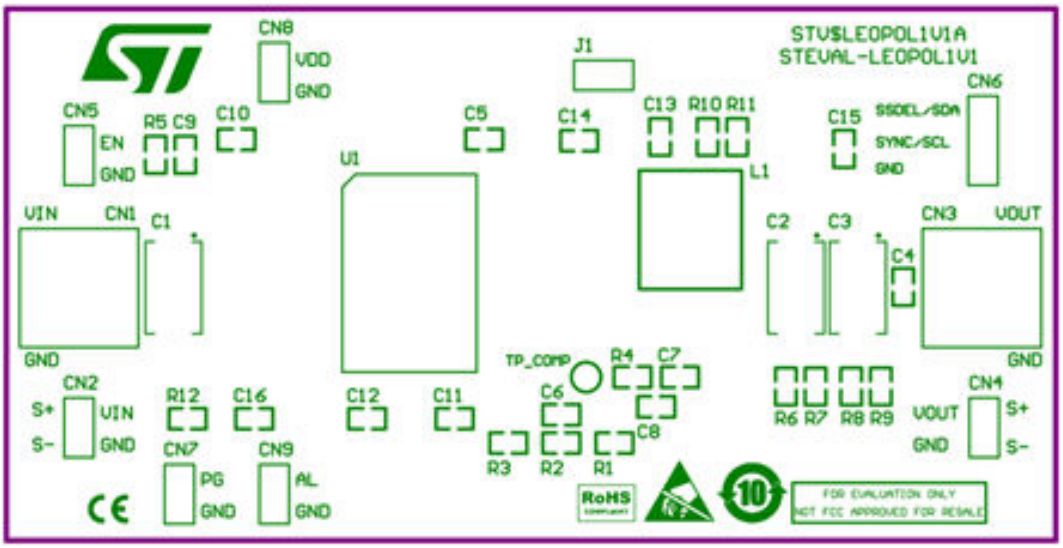


Figure 16. **Top layer**

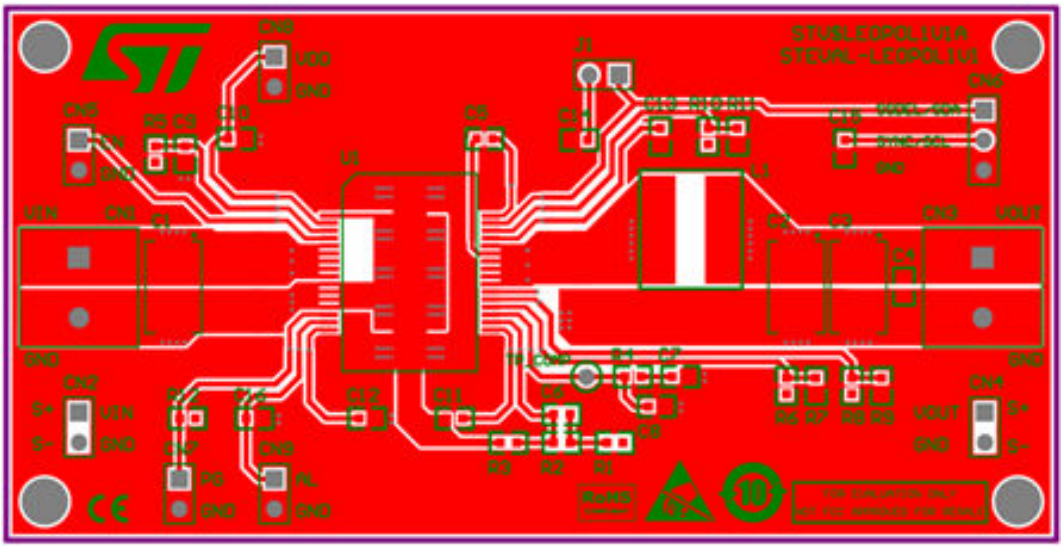


Figure 17. **Mid layer (1)**

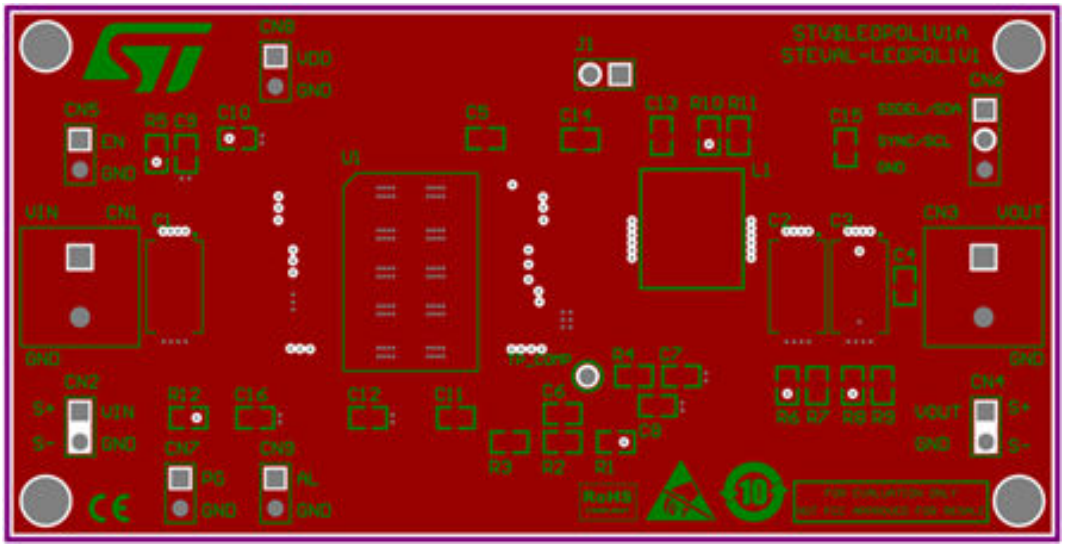


Figure 18. **Mid layer (2)**

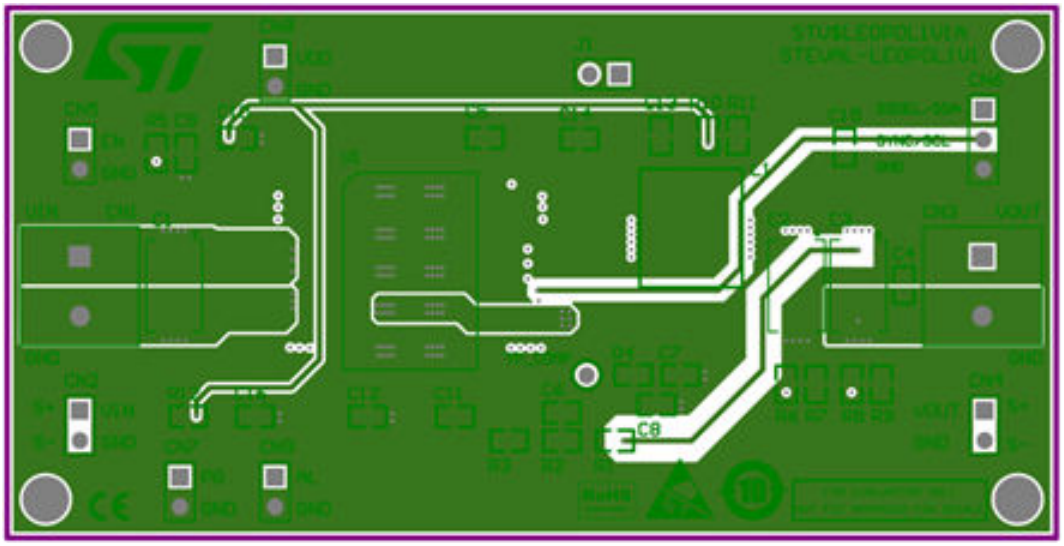
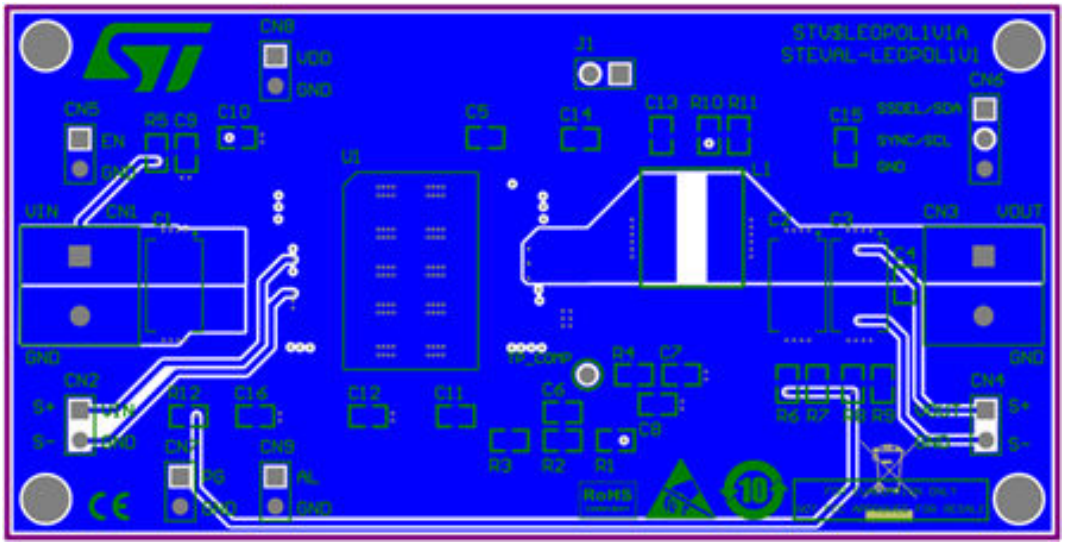


Figure 19. **Bottom layer**



7 Bill of materials

Table 2. **STEVAL-LEOPOL1V1 bill of materials**

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	1	C1	330 µF	Tantalum Polymer Capacitor	KEMET	T530X337M010ATE006
2	2	C2, C3	150 µF	Tantalum Polymer Capacitor	KEMET	T530D157M010ATE006
3	4	C4, C5, C13, C14	100 nF	Multilayer Ceramic Capacitors	MULTICOMP PRO	MC0603B104K500CT
4	5	C9, C10, C11, C12, C16	1 µF	Multilayer Ceramic Capacitors	TDK	C1608X5R1E105K080AC
5	0	C15	100 pF	Multilayer Ceramic Capacitors	Murata	GRM1885C1H101JA01
6	1	C6	270 pF	Multilayer Ceramic Capacitors	KEMET	C0603C271J5GACTU
7	1	C8	15 pF	Multilayer Ceramic Capacitors	KEMET	C0603C150J5GACTU
8	1	C7	4.7 nF	Multilayer Ceramic Capacitors	WALSIN	0603B472K500CT
9	1	R4	27 KΩ	Thick Film Resistor	WALSIN	WR06X2702FTL
10	1	R1	0 Ω	Thick Film Resistor	WALSIN	WR06X000PTL
11	1	R2	3.9 KΩ	Thick Film Resistor	WALSIN	WR06X3901FTL
12	1	R3	8.2 KΩ	Thick Film Resistor	WALSIN	WR06X8201FTL
13	1	R5	4.7 Ω	Thick Film Resistor	ROYALOHM	0603SAF470KT5E
14	1	R12	4.7 KΩ	Thick Film Resistor	WALSIN	WR06X4701FTL
15	0	R6, R8, R10	0 Ω	Thick Film Resistor	MULTICOMP PRO	WR06X000PTL
16	1	R7	50 KΩ	Thick Film Resistor	WELWYN	APC0603AD-50KBT5
17	1	R9	1 KΩ	Thick Film Resistor	WALSIN	WR06X1001FTL
18	1	R11	12 KΩ	Thick Film Resistor	WALSIN	WR06X1202FTL
19	1	J1		2 PIN MALE STRIP LINE, 2.54 mm Pitch	Wurth Electronics Inc.	61300211121
20	2	CN1, CN3		2 Way PCB terminal, 5.08 mm Pitch	Phoenix Contact	1888687

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
21	1	CN6		3 PIN MALE STRIP LINE, 2.54 mm Pitch	Wurth Electronics Inc.	61300311121
22	6	CN2, CN4, CN5, CN7, CN8, CN9		2 PIN MALE STRIP LINE, 2.54 mm Pitch	Wurth Electronics Inc.	61300211121
23	1	L1	4.7 µH	Power Inductors	Coilcraft	XAL8080-472MEB
24	1	TP		Test Point, 0.9 Hole Size	MULTICOMP PRO	TEST-1(W)
25	1	U1	LEOPOL1, PowerSO 36	LEOPOL, PowerSO-36, 36L	ST	LEOPOL1PDT

8 Board versions

Table 3. **STEVAL-LEOPOL1V1 versions**

Finished good	Schematic diagrams	Bill of materials
STV$LEOPOL1V1A(1)	STV$LEOPOL1V1A schematic diagrams	STV$LEOPOL1V1A bill of materials

1. *This code identifies the STEVAL-LEOPOL1V1 evaluation board first version.*

9 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III). Compliance to EMC standards in Class A (industrial intended use).

Notice for the United Kingdom

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III). Compliance to EMC standards in Class A (industrial intended use).

Revision history

Table 4. **Document revision history**

Date	Revision	Changes
18-Jun-2025	1	Initial release.
11-Nov-2025	2	Updated Introduction.

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.