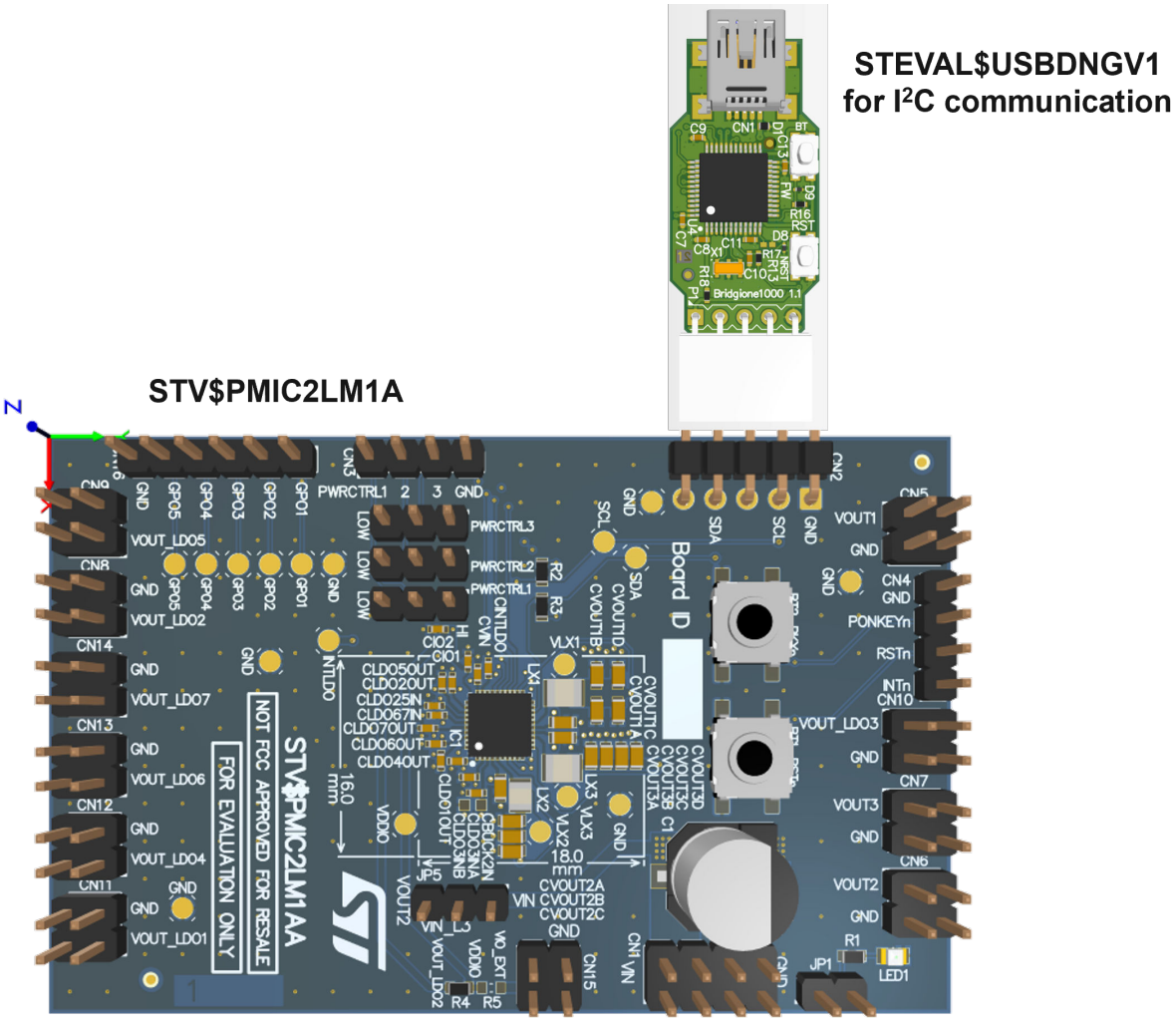
User manual for STEVAL-PMIC2LK1 based on STPMIC2LA

Introduction

This user manual provides detailed instructions on how to configure and use the STEVAL-PMIC2LKV1 kit. The kit includes the following components:

1. The STEVAL-PMIC2LM1A evaluation board, which is designed specifically for the STPMIC2LA.
2. The STEVAL-USBDNGV1 USB dongle, which is used to program the STPMIC2L through I²C bus protocol with the STSW-PMIC2LGUI software.

Figure 1. STEVAL-PMIC2LKV1 kit



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1 STPMIC2L overview

The STPMIC2L is a fully integrated power management IC, designed for STM32MP2x MPUs family applications requiring low power and high efficiency. The device integrates advanced low-power features controlled by a host processor via I²C and I/O interfaces.

The STPMIC2L regulators are designed to supply power to the application processor, as well as to the external system peripherals, such as DDR, flash memories, and other system devices.

3 buck SMPS are optimized to provide an excellent transient response and an output voltage precision for a wide range of operating conditions. Very high efficiency in full output load range is achieved thanks to low power (LPM) and high power (HPM) modes selection. All the buck converters are provided with smooth transition from LPM to HPM. Advanced PWM phase shift synchronization technique is integrated with PLL (low noise and reduced EMI).

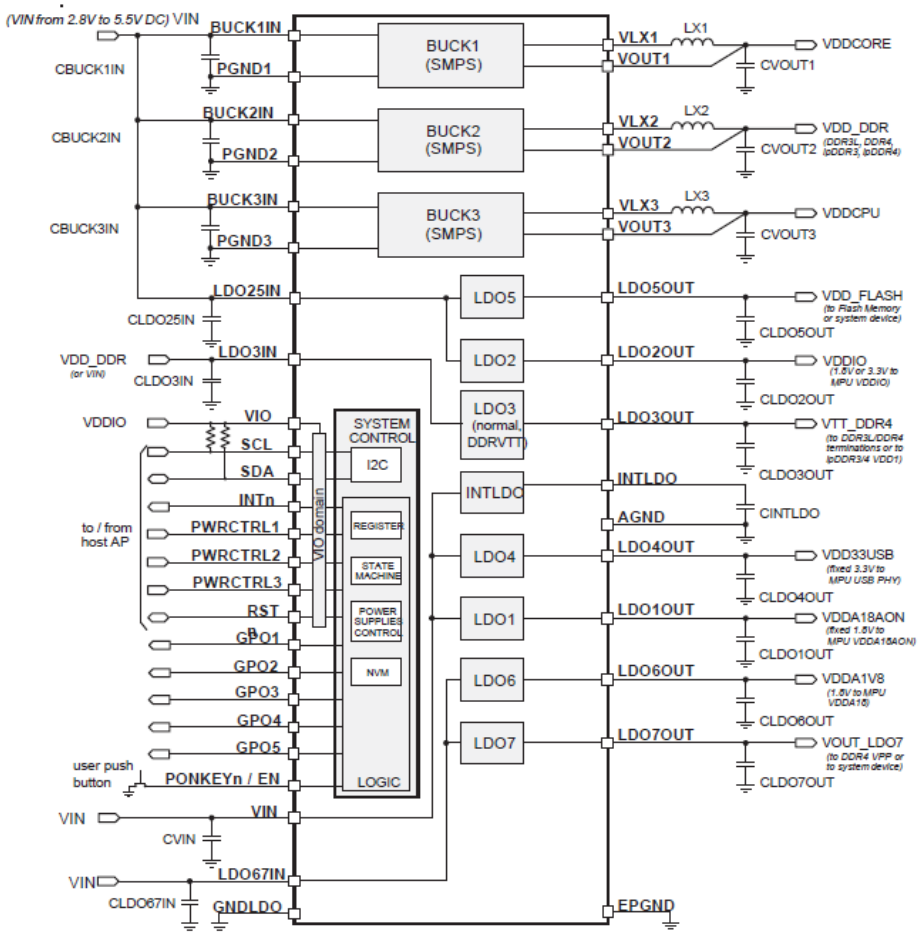
The main features of the STPMIC2L are:

- Input voltage range from 2.8 V to 5.5 V.
- 3 buck converters with adaptive constant on-time (COT) topology.
- 2 MHz switching frequency.
- Selectable forced PWM.
- Spread spectrum function.
- Phase shift synchronization.
- 4 adjustable general purpose LDOs.
- 1 LDO configurable as:
  - Sink/Source mode for DDR4 termination.
  - Adjustable output (normal mode) for general purpose use.
- 5 GPO output controls for external command.
- User programmable nonvolatile memory (NVM), enabling scalability to support a wide range of applications.
- Immediate output alternate settings toggle by dedicated power control pins.
- Programmable output voltages Turn ON/OFF sequences.
- I²C and digital I/O control interface.
- Advanced customizable safety managements.
- WFQFN 40 L package (5.0 x 5.0 x 1.0 mm).

Typical applications of the STPMIC2L are:

- Power management for embedded microprocessor units.
- Wearable and IoT.
- Portable devices.
- Man-machine interfaces.
- Smart home.
- Power management unit companion chip of the STM32MP2x MPUs family.

Figure 2. **STPMIC2L typical application schematic**



Note: all the input voltage pins must be connected at the same voltage supply value except the LDO3 sink/source

The STPMIC2L features a large input voltage range from 2.8 V to 5.5 V to supply:

- 5 V DC wall-adaptor applications.
- 1 cell 3.6 V Li-Ion/LiPo battery applications.
- 5 V USB port (bus-powered) applications.

STPMIC2L provides all regulators needed to power supply a complete application:

- 7 LDOs.
- 3 step-down buck converters.
- 5 GPOs.

Table 1 shows a general description of each regulator and the typical application use (in STM32MP2 MPU application).

Table 1. **General description of STPMIC2L regulators and their typical applications in MPU application**

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Application use
LDO1	1.8	-	20	VDDA18AON
LDO2, LDO5, LDO6, LDO7	0.9 V - 4.0 bypass mode	100	400 / 200 / 100 / 50	General purpose (VDDIO, eMMC, DDR4 VPP, SD card, LCD image sensor…)
LDO3 normal mode	0.9 V - 4.0	100	120	General purpose / lpDDR VDD1

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Application use
LDO3 Sink/Source mode	$V_{OUT2}/2$	-	+/-120 (rms) +/-230 (peak)	DDR3L/DDR4 terminations (VTT)
LDO4	3.3	-	40	VDD33USB VDD33UCPD
BUCK1, BUCK3	0.5 - 1.5	10	2000, 1500, 1000, 500	Buck1 = VDDCORE Buck3 = VDDCPU
BUCK2	0.5 - 1.5	10	2000, 1500, 1000, 500	Buck2 = VDDQ

Note: VIN is the main STPMIC2L supply. All Buck converters and linear regulators have dedicated or shared power supply pins. A dedicated VIO supply is for all digital interface pins.

2 Differences between STPMIC2LA and STPMIC2LB

STPMIC2L has a nonvolatile memory (NVM) that can be reprogrammed via I^2C directly in target applications to facilitate mass production, enabling scalability to support a wide range of applications. The main settings of STPMIC2L are stored in the NVM memory:

- VIN voltage threshold.
- Auto turn-on feature.
- Default I^2C slave device address.
- Regulators default output voltages at startup.
- Regulators power-up sequence at startup (rank).
- Safety management in case of failure: overcurrent protection, overtemperature protection, VIN_low, watchdog, and ponkey fault counters.
- Possibility to lock the NVM content to prevent further reprogramming by writing the LOCK_NVM bit.
- Other features (see DS14940 for further details).

STPMIC2LA and STPMIC2LB are the two standard NVM configurations to support the STM32MP2x series application processor versions, in particular:

- STPMIC2LA version:
  - Typical use case: 5 V continuous input voltage (wall adaptor) applications.
  - VDDIO 3.3 V (LDO2 output).
  - Minimum set of regulators enabled by default.
- STPMIC2LB version:
  - Typical use case: Li-Ion/LiPo single cell battery applications.
  - VDDIO 1.8 V (LDO2 output).
  - Minimum set of regulators enabled by default.

Table 2. Main settings of STPMIC2LA and STPMIC2LB

IP	STPMIC2LA				STPMIC2LB			
	Voltage	Mode	Pull-down	Rank	Voltage	Mode	Pull-down	Rank
LDO1 (VDDA18AON)	1.8 V		YES	1	1.8 V		YES	1
LDO2 (VDDIO)	3.3 V		YES	1	1.8 V		YES	1
LDO3 (VTT/VDD1_DDR)	OFF	OFF	YES	0	OFF	OFF	YES	0
LDO4 (VDD33USB)	3.3 V		YES	5	3.3 V		YES	5
LDO5 (GP LDO)	3.3 V		YES	5	1.8 V		YES	5
LDO6 (GP LDO)	1.8 V		YES	3	2.9 V		YES	3
LDO7 (GP LDO)	OFF		YES	0	OFF		YES	0
BUCK1 (VDDCORE)	0.82 V	HP	SLOW	2	0.82 V	HP	SLOW	2
BUCK2 (VDDDDR)	OFF		FAST	0	OFF		FAST	0
BUCK3 (VDDCPU/VDDGPU)	0.80 V	HP	SLOW	4	0.80 V	HP	SLOW	4
GPO1	OFF	POL_HIGH		0	OFF	POL_HIGH		0
GPO2	OFF	POL_HIGH		0	OFF	POL_HIGH		0
GPO3	OFF	POL_HIGH		0	OFF	POL_HIGH		0
GPO4	VIN	POL_HIGH		5	VIN	POL_HIGH		5
GPO5	VIN	POL_HIGH		5	VIN	POL_HIGH		5

The startup sequence of STPMIC2L is divided into four steps (Rank0 to Rank5).

Each BUCK converter, LDO regulator, or GPO can be programmed to be automatically turned ON in one of these ranks. Each rank phase is separated by a delay, which is by default 1.5 ms. This rank delay can be programmed in NVM (Reg0x91 [7:6]) at 1.5 ms, 3 ms, 4.5 ms, or 6 ms (RANK_DLY [1:0]).

- Rank = 0: rail not turned ON automatically, no output voltage appears after POWER-UP sequence.
- Rank = 1: rail automatically turned ON after 7 ms (which is the fixed delay from VIN>VINOK_rise to the start of IPs with rank1), following a Turn_ON condition.
- Rank = 2: rail automatically turned ON after further 1.5 ms compared to Rank1 output rails.
- Rank = 3: rail automatically turned ON after further 1.5 ms compared to Rank2 output rails.
- Rank = 4: rail automatically turned ON after further 1.5 ms compared to Rank3 output rails.
- Rank = 5: rail automatically turned ON after further 1.5 ms compared to Rank4 output rails.

Regardless of the STPMIC2L version, the AUTO_TURN_ON option is set.

Table 3 shows the miscellaneous settings at startup of STPMIC2LA and STPMIC2LB.

Table 3. Miscellaneous settings of STPMIC2LA and STPMIC2LB at startup

Parameter	STPMIC2LA	STPMIC2LB	Comments
VIN_OK_Rise	4.0 V	3.3 V	VIN threshold enabling PMIC to turn ON
VIN_OK_hysteresis	0.5 V	0.5 V	
Auto_Turn_ON	ON	ON	Automatic PMIC turn-ON when VIN goes higher VIN_OK_Rise
Rank duration	1.5 ms	1.5 ms	Duration of delay between two ranks
NRST delay	0	0	Delay after last rank before PMIC release NRST
I2C address	0x33	0x33	I^2C address
USER NVM byte	0	0	2 free NVM bytes for user

Table 4 shows the safety management settings at startup of STPMIC2LA and STPMIC2LB.

Table 4. Safety management settings of STPMIC2LA and STPMIC2LB at startup

Parameter	STPMIC2LA	STPMIC2LB	Comments
Watchdog	OFF	OFF	Watchdog can be enabled at runtime
PONKEY LKP OFF	ON	ON	A long PONKEY key press does not switch PMIC25 OFF
PONKEYLKP FSLS	OFF	OFF	A long PONKEY key press allows PMIC25 to skip the Fail-Safe Lock State
LKP duration	10 s	10 s	Long PONKEY key press timer duration settings
Hiccup delay restart	100 ms	100 ms	
VINOK fault	∞ restart	∞ restart	
Thermal fault	∞ restart	∞ restart	
OCP FS fault	∞ restart	∞ restart	If regulator OCP management is set in Fail-Safe (FS) mode
Watchdog fault	∞ restart	∞ restart	
PONKEY fault	∞ restart	∞ restart	
Fail-Safe lock state	Disabled	Disabled	PMIC is never locked in FS mode (it goes in OFF mode)
VIN delay	10 ms	10 ms	Delay to wait for VIN stable
PONKEYn/ENABLE	PONKEYn/PU	PONKEYn/PU	PONKEYn function with pullup

Table 5 shows the Fail-Safe/Hiccup regulator OCP settings at startup of STPMIC2LA and STPMIC2LB.

Table 5. Fail-Safe/Hiccup regulator OCP settings of STPMIC2LA and STPMIC2LB at startup

Parameter	STPMIC2LA OCP mgt / OCP lim	STPMIC2LB OCP mgt / OCP lim	Comments
BUCK1 (VDDCORE)	FS / 1.5 A	FS / 1.5 A	STPMIC2L switch-off in case of OCP triggered
BUCK2 (VDDDDR)	FS / 1.5 A	FS / 1.5 A	STPMIC2L switch-off in case of OCP triggered
BUCK3 (VDDCPU/ VDDGPU)	FS / 2 A	FS / 2A	STPMIC2L switch-off in case of OCP triggered
LDO1 (VDDA18AON)	FS	FS	STPMIC2L switch-off in case of OCP triggered
LDO2 (VDD_FLASH)	FS / 400 mA	FS / 400 mA	STPMIC2L switch-off in case of OCP triggered
LDO3 (VTT/ VDD1_DDR)	FS	FS	STPMIC2L switch-off in case of OCP triggered
LDO4 (VDD33USB)	Hiccup	Hiccup	STPMIC2L does not switch-off in case of OCP triggered
LDO5 (GP LDO)	Hiccup / 400 mA	Hiccup / 400 mA	STPMIC2L does not switch-off in case of OCP triggered
LDO6 (GP LDO)	FS / 400 mA	FS / 400 mA	STPMIC2L switch-off in case of OCP triggered
LDO7 (GP LDO)	FS / 400 mA	FS / 400 mA	STPMIC2L switch-off in case of OCP triggered

Table 6 shows the complete NVM register maps of STPMIC2LA and STPMIC2LB version.

Table 6. STPMIC2LA and STPMIC2LB NVM configuration maps

Register (hex)	STPMIC2LA Value (hex)	STPMIC2LB Value (hex)
0x90	0xF1	0xD1
0x91	0x0A	0x0A
0x92	0x02	0x02
0x93	0x04	0x04
0x94	0x00	0x00
0x95	0x00	0x00
0x96	0x09	0x09
0x97	0x28	0x28
0x98	0x1D	0x1D
0x99	0x00	0x00
0x9A	0x00	0x00
0x9B	0x00	0x00
0x9C	0x20	0x20
0x9D	0x00	0x00
0x9E	0x9E	0x9E
0x9F	0x00	0x00
0xA0	0x00	0x00
0xA1	0x28	0x28
0xA2	0x05	0x05
0xA3	0x30	0x12
0xA4	0x00	0x00

Register (hex)	STPMIC2LA Value (hex)	STPMIC2LB Value (hex)
0xA5	0x30	0x28
0xA6	0x12	0x12
0xA7	0x00	0x00
0xA8	0x00	0x00
0xA9	0x19	0x19
0xAA	0x00	0x00
0xAB	0x7F	0x7F
0xAC	0x3A	0x3A
0xAD	0x40	0x40
0xAE	0xFF	0xFF
0xAF	0x07	0x07
0xB0	0x67	0x67
0xB1	0xFF	0xFF
0xB2	0xFF	0xFF
0xB3	0x4F	0x4F
0xB4	0x80	0x80
0xB5	0x33	0x33
0xB6	0x00	0x00
0xB7	0x00	0x00

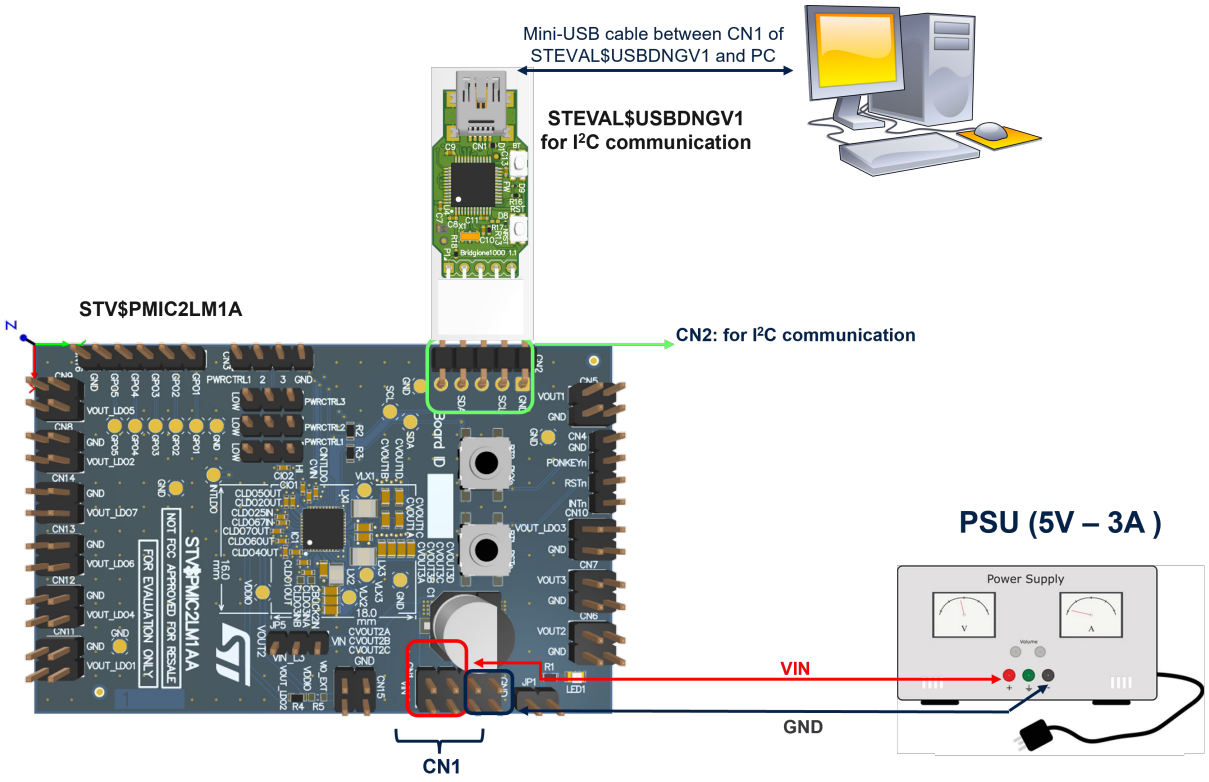
The STPMIC2LA version is soldered on STV-PMIC2LM1AA.
For more details regarding the STPMIC2L features, please refer to DS14940.

3 Getting started with the STEVAL-PMIC2LKV1 kit

To get started with the STEVAL-PMIC2LKV1 kit, proceed as follows:

1. Connect the STEVAL-USBDNGV1 on STV-PMIC2LM1A through the CN2 connector.
2. Connect a mini-USB cable between the PC and the CN1 connector of STEVAL-USBDNGV1.
3. Apply the power supply VIN to the CN1 connector of the STV-PMIC2LM1AA. A power supply capable of 2 A minimum is required.

Figure 3. STEVAL-PMIC2LKV1 kit configuration



3.1 Input/Output connector description

Table 7. STEVAL-PMIC2LM1A input/output connectors description

STEVAL-PMIC2LM1A connectors		
Name	**Functionality**	**Details**
CN1	Main input power supply	VIN: positive input power force/sense
		GND: ground input force/sense
CN2	I^2C bus connector	SCL: clock
		SDA: data
		GND: ground
CN3	PWRCTRL1,2,3 output voltage connector	PWRCTRL1: output voltage sense
		PWRCTRL2: output voltage sense
		PWRCTRL3: output voltage sense
		GND: ground
CN4	INTn, RSTn, PONKEYn output voltage connector	INTn: output voltage sense
		RSTn: output voltage sense
		PONKEYn: output voltage sense
		GND: ground
CN5	BUCK1 output voltage connector	VOUT1: output voltage force/sense
		GND: ground output force/sense
CN6	BUCK2 output voltage connector	VOUT2: output voltage force/sense
		GND: ground output force/sense
CN7	BUCK3 output voltage connector	VOUT3: output voltage force/sense
		GND: ground output force/sense
CN11	LDO1 output voltage connector	VOUT_LDO1: output voltage force/sense
		GND: ground output force/sense
CN8	LDO2 output voltage connector	VOUT_LDO2: output voltage force/sense
		GND: ground output force/sense
CN10	LDO3 output voltage connector	VOUT_LDO3: output voltage force/sense
		GND: ground output force/sense
CN12	LDO4 output voltage connector	VOUT_LDO4: output voltage force/sense
		GND: ground output force/sense
CN9	LDO5 output voltage connector	VOUT_LDO5: output voltage force/sense
		GND: ground output force/sense
CN13	LDO6 output voltage connector	VOUT_LDO6: output voltage force/sense
		GND: ground output force/sense
CN14	LDO7 output voltage connector	VOUT_LDO7: output voltage force/sense
		GND: ground output force/sense
CN16	GPOs connector	GPO1: output voltage
		GPO2: output voltage
		GPO3: output voltage
		GPO4: output voltage

STEVAL-PMIC2LM1A connectors		
CN16	GPOs connector	GPO5: output voltage
		GND: ground output
CN15	VIO output voltage connector from external supply	VIO_EXT: output voltage force/sense
		GND: ground output force/sense
JP1	Manual bridge for VIN “LED1” connection	If LED1 is ON, VIN is applied to the STEVAL
JP2	Manual bridge for PWRCTRL1 connection	HIGH position: PWRTCTRL1 forced to VIO
		LOW position: PWRTCTRL1 forced to GND
JP3	Manual bridge for PWRCTRL2 connection	HIGH position: PWRTCTRL2 forced to VIO
		LOW position: PWRTCTRL2 forced to GND
JP4	Manual bridge for PWRCTRL3 connection	HIGH position: PWRTCTRL3 forced to VIO
		LOW position: PWRTCTRL3 forced to GND
JP5	Manual bridge for LDO3 input connection	VIN_L3-VIN position: LDO3 input forced to main input voltage supply “VIN”
		VIN_L3-VOUT2 position: LDO3 input forced to BUCK2 output
R4-R5	0 Ω resistors allow VIO connection to LDO2 output or to external supply (VIO_EXT pin)	If R4 (0 Ω) is soldered, VIO is connected to LDO2 output
		If R5 (0 Ω) is soldered, VIO is connected to VIO_EXT output. In this case VIO must be supplied externally on CN15 connector (VIO_EXT pin).
BT1	RSTn button	RSTn pin is connected to GND when BT1 is pushed
BT2	PONKEYn button	PONKEYn pin is connected to GND when BT3 is pushed

Referring to Figure 4, be sure that:

- A PSU (5 V - 2 A) is connected to CN1 connector.
- R4 (0 Ω) is soldered. This way, VIO is provided by BUCK4 output.
- STEVAL-USBDNGV1 is connected to CN2 (as shown in Figure 3).
- STEVAL-USBDNGV1 is connected to the PC through a micro-USB connector plugged on CN1.

Figure 4. VIN and VIO connectors details of STEVAL-PMIC2LM1A

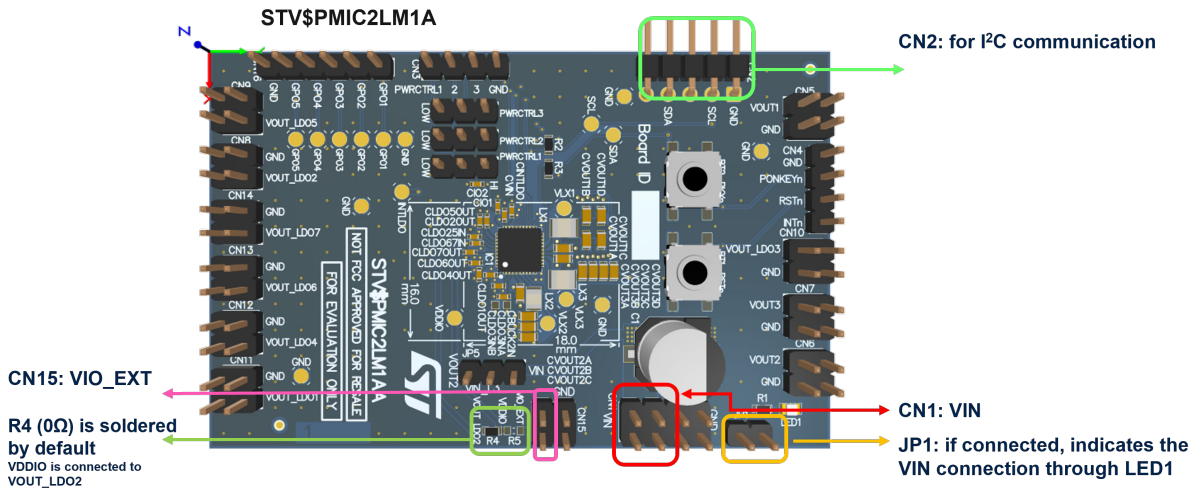
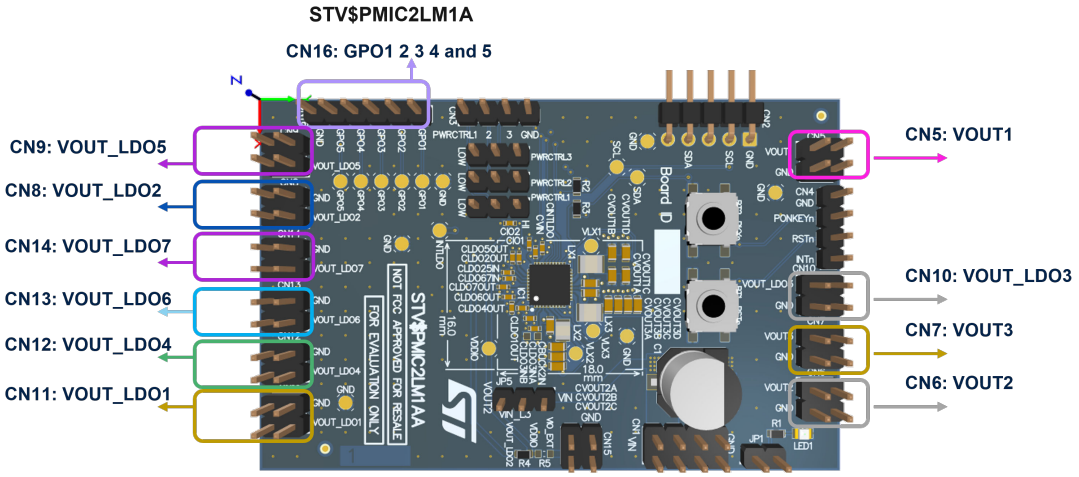


Figure 5 shows the I/O connector of:

- All BUCK converters (from BK1 to BK3).
- All LDO regulators (from LDO1 to LDO7).

- All GPOs (from GPO1 to GPO5).
- JP5, which is a connector that allows to switch LDO3 input between BUCK2 output and the main input supply (VIN).

Figure 5. BUCKs, LDOs, and GPOs connectors details of STEVAL-PMIC2LM1A



Note: All BUCKs and LDOs input supply pins (except LDO3 input) are connected by default in the board layout to the main input supply (VIN).

Figure 6. BUCKs VLX test points details of STEVAL-PMIC2LM1A

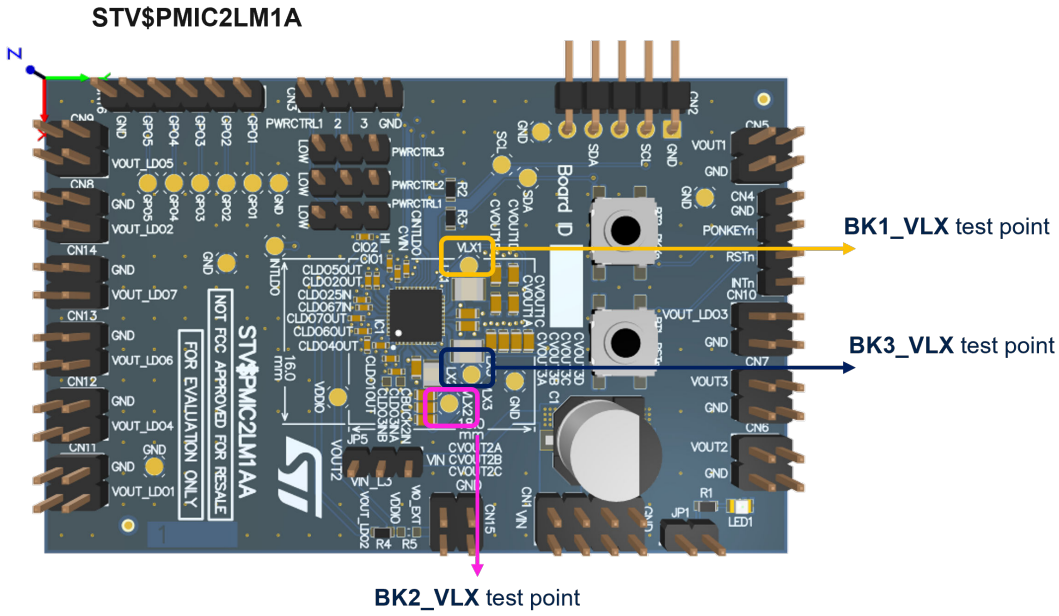
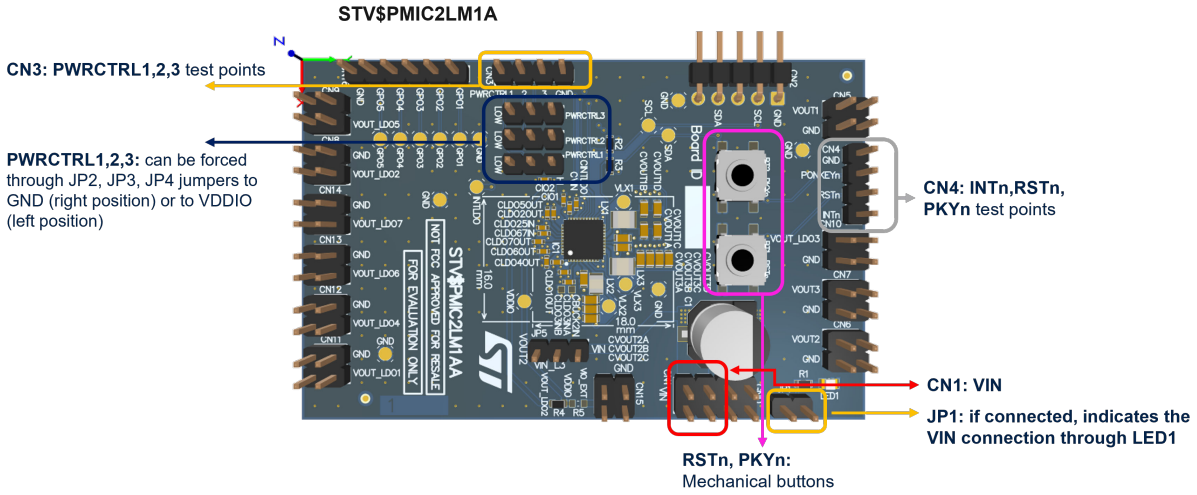


Figure 7 shows the I/O connectors of the digital pins:

- PWRCTRL1,2,3:
  - CN3 are test points.
  - JP2, JP3, and JP4 allow to force respectively PWRCTRL1, PWRCTRL2, and PWRCTRL3 to VDDIO (right position) or to GND (left position) using a manual bridge.
- INTn, RSTn, PKYn:
  - CN4 are test points.
  - BT1 and BT2 are mechanical buttons that, if pressed, force RSTn and PKYn to GND.

- JP1: if manual bridge is placed over it, LED1 automatically switches on when VIN is provided to the STEVAL-PMIC2LM1A on CN1.

Figure 7. Digital connectors details (PWRCTRL1,2,3; RSTn, INTn) of STEVAL-PMIC2LM1A



4 Getting started with STPMIC2L GUI

To get started with the STPMIC2L GUI, consult the STSW-PMIC2LGUI user manual (UM3532).

5 Schematic diagrams

Figure 8. **STEVAL-PMIC2LM1A circuit schematic (1 of 4)**

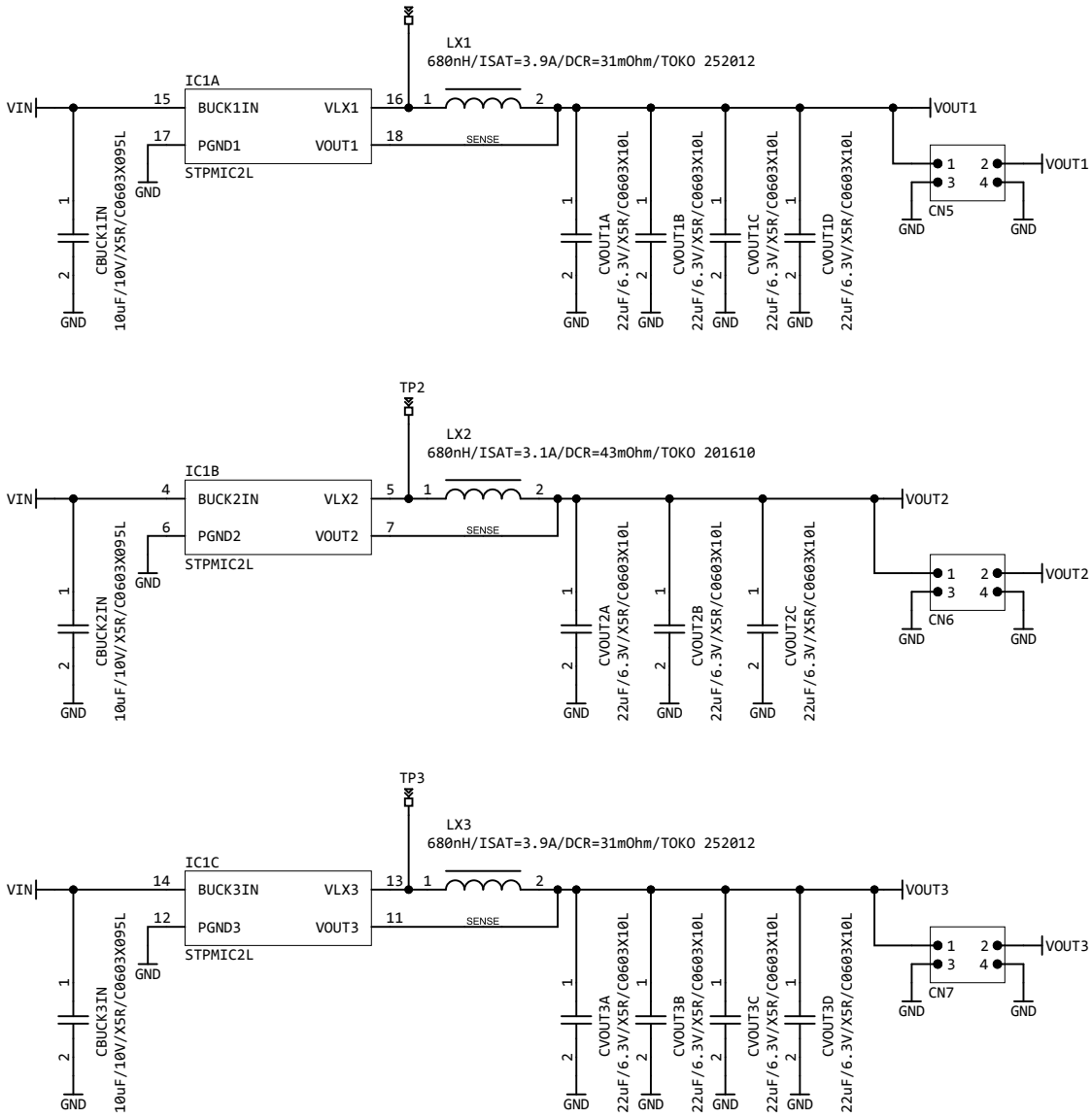


Figure 9. **STEVAL-PMIC2LM1A circuit schematic (2 of 4)**

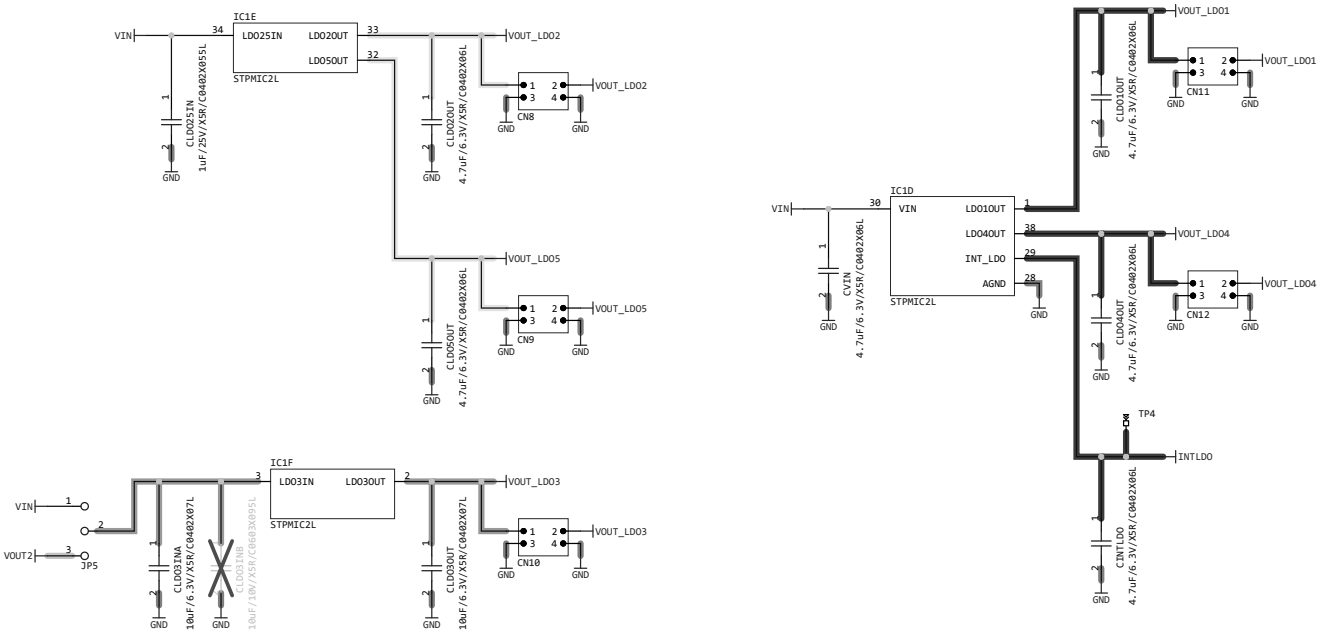


Figure 10. **STEVAL-PMIC2LM1A circuit schematic (3 of 4)**

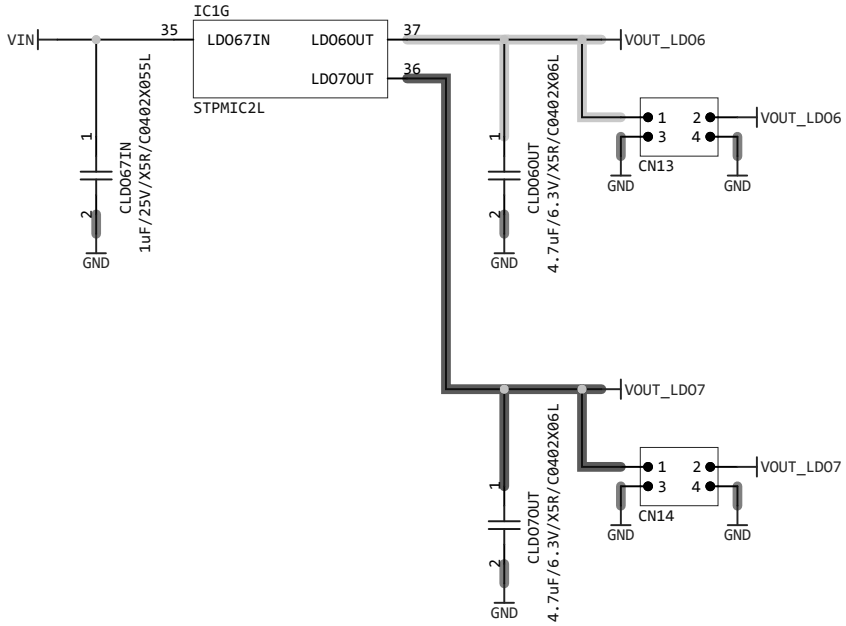
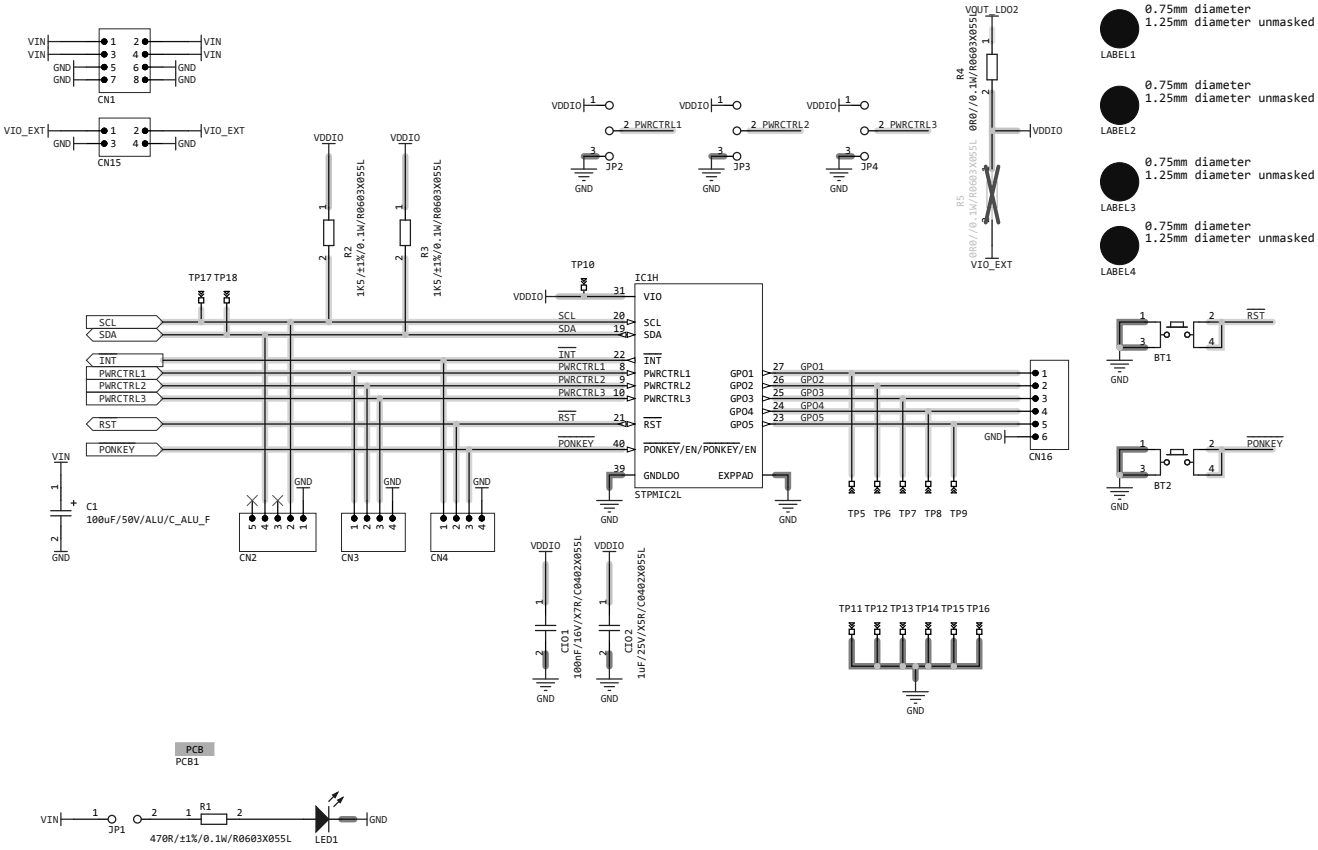


Figure 11. **STEVAL-PMIC2LM1A circuit schematic (4 of 4)**



6 PCB

The STPMIC2L evaluation board is based on a 4-layer PCB.

6.1 Stack-up layer

Figure 12 shows the PCB stack-up layer used for the STPMIC2L evaluation board.

Figure 12. STEVAL-PMIC2LM1A: PCB stack-up layer

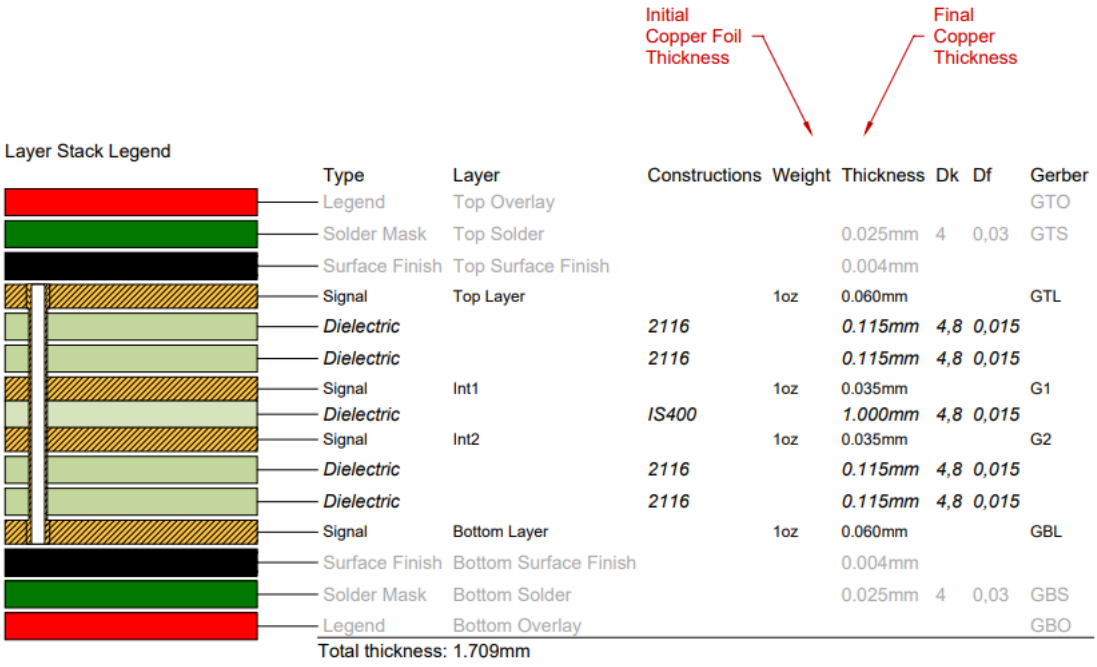


Table 8. STEVAL-PMIC2LM1A: stack-up layer details

Layer	Stack-up
Top	Component/power/signal
Mid layer 1	GND
Mid layer 2	Power/GND
Bottom	Power/GND

6.2 Layout details

Figure 13 shows the board dimensions in mm and Figure 14, Figure 15, Figure 16, and Figure 17 show the details of the top, mid1, mid2 and bottom layers of STEVAL-PMIC2LM1A.

Figure 13. STEVAL-PMIC2LM1A: 3D layout and dimentions

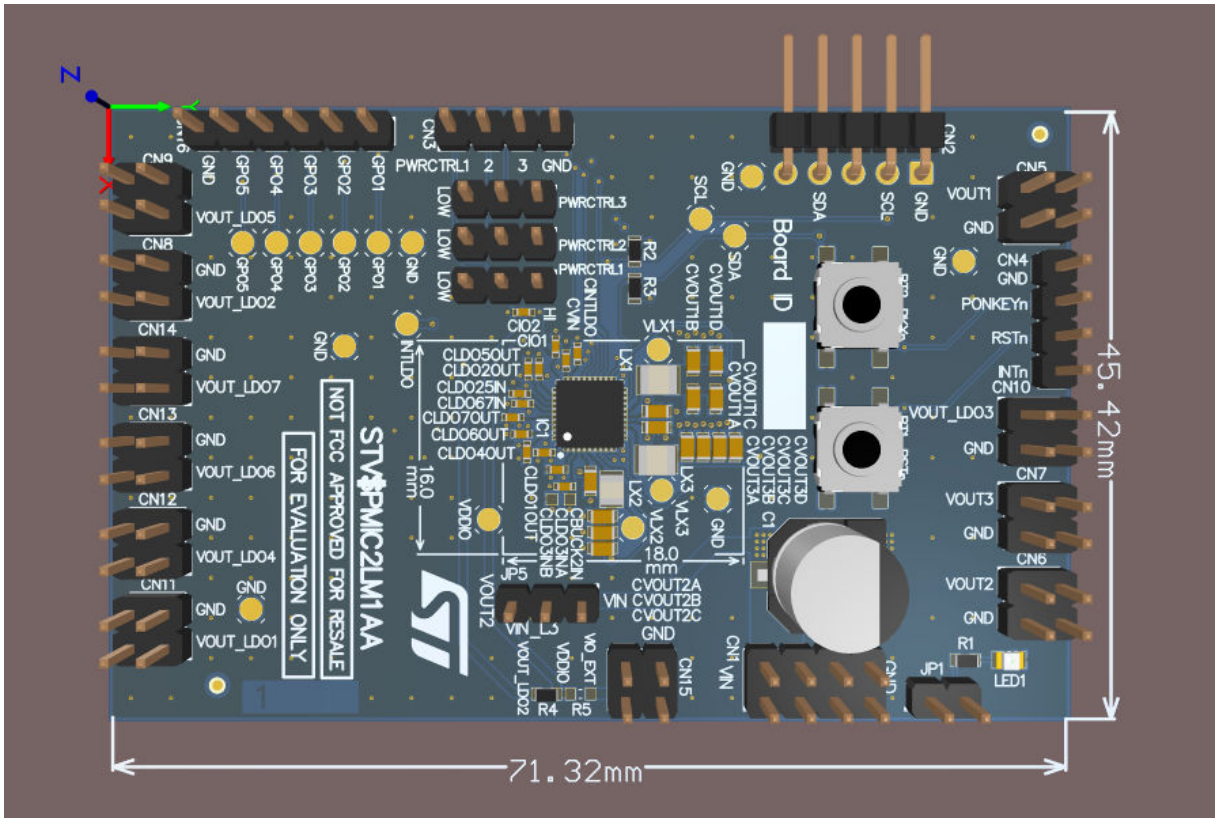


Figure 14. **STEVAL-PMIC2LM1A: top layer (components/power/signal)**

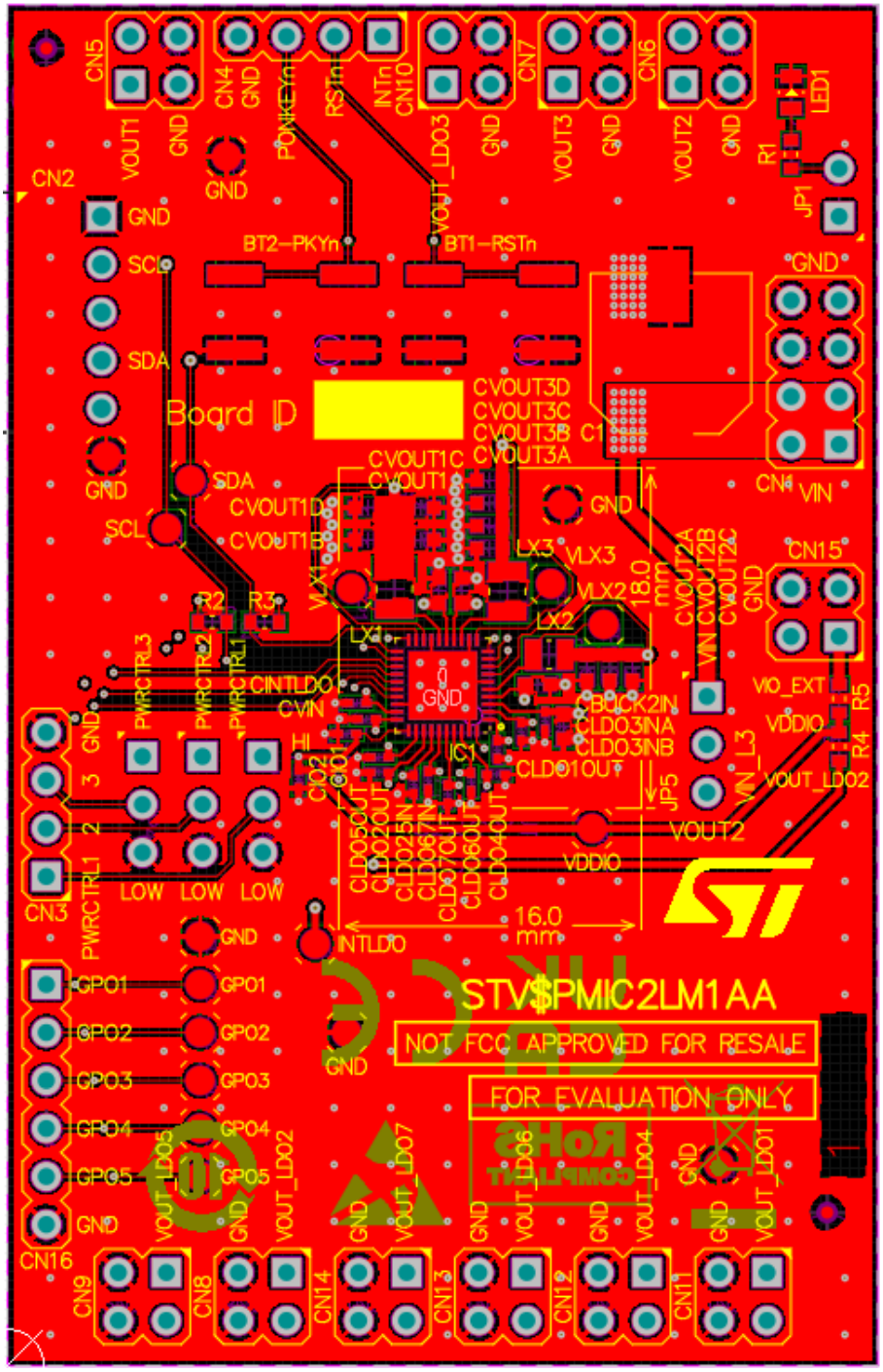


Figure 15. **STEVAL-PMIC2LM1A: mid layer 1 (GND)**

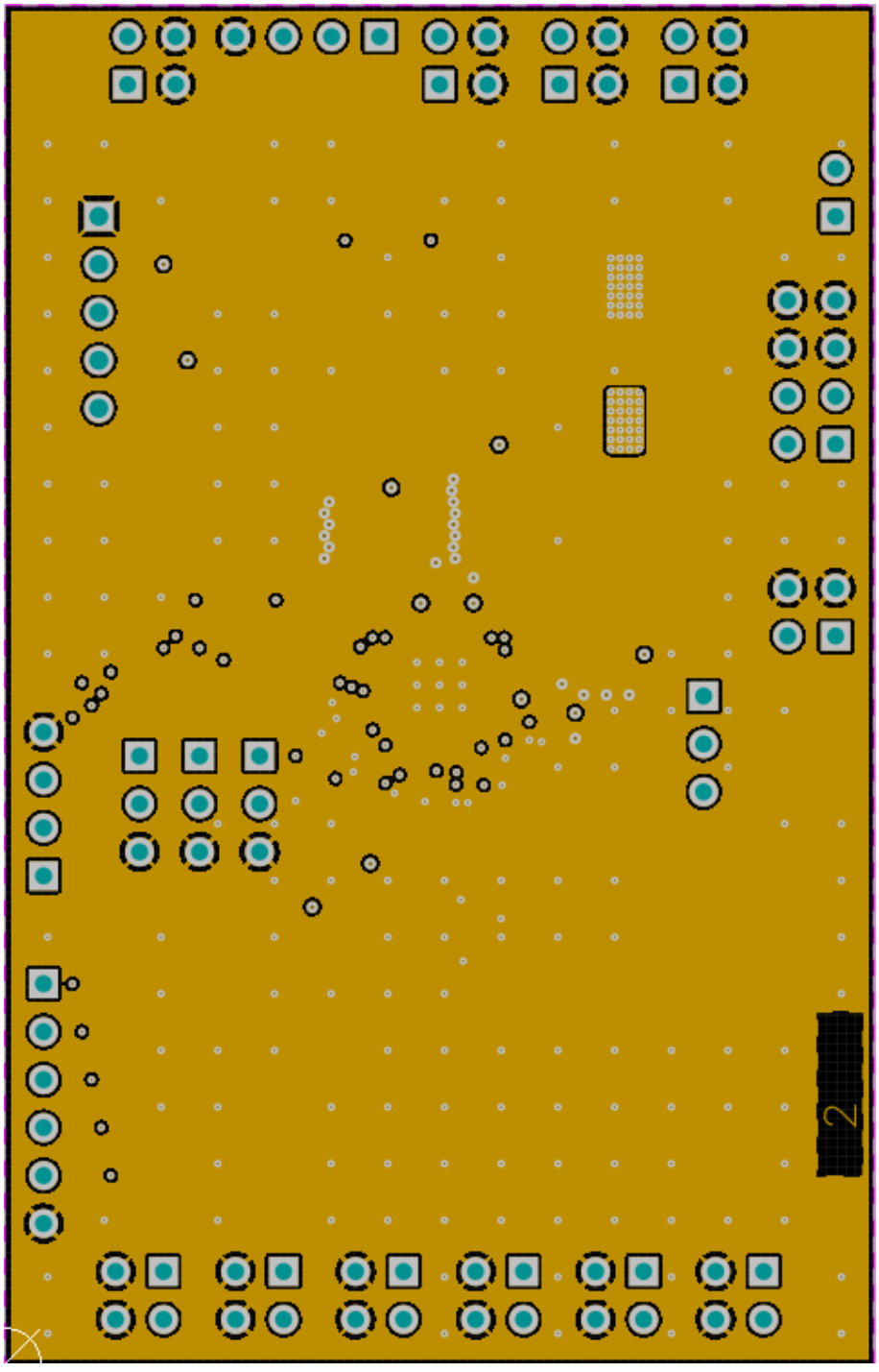


Figure 16. **STEVAL-PMIC2LM1A: mid layer 2 (Power/GND)**

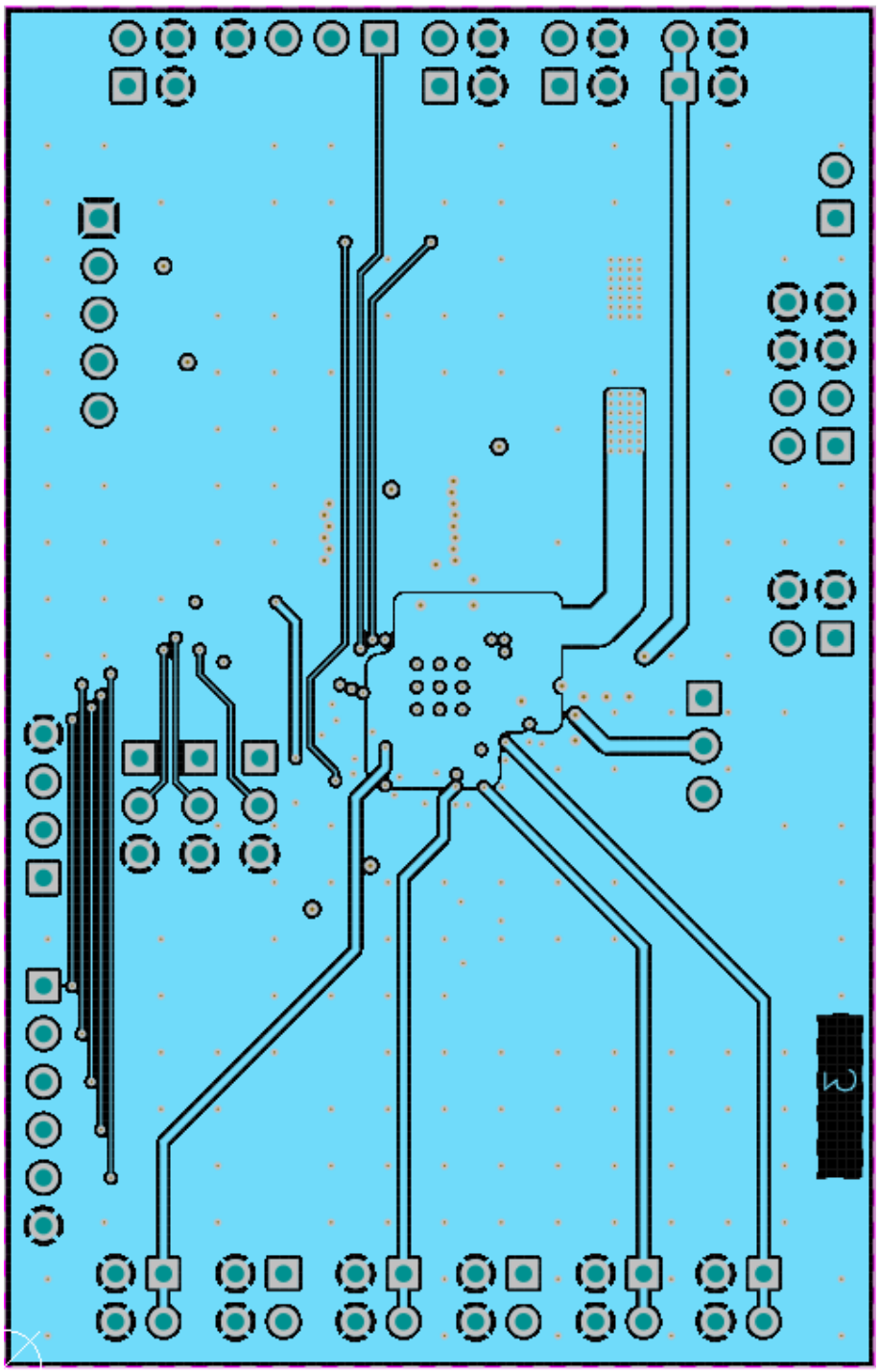
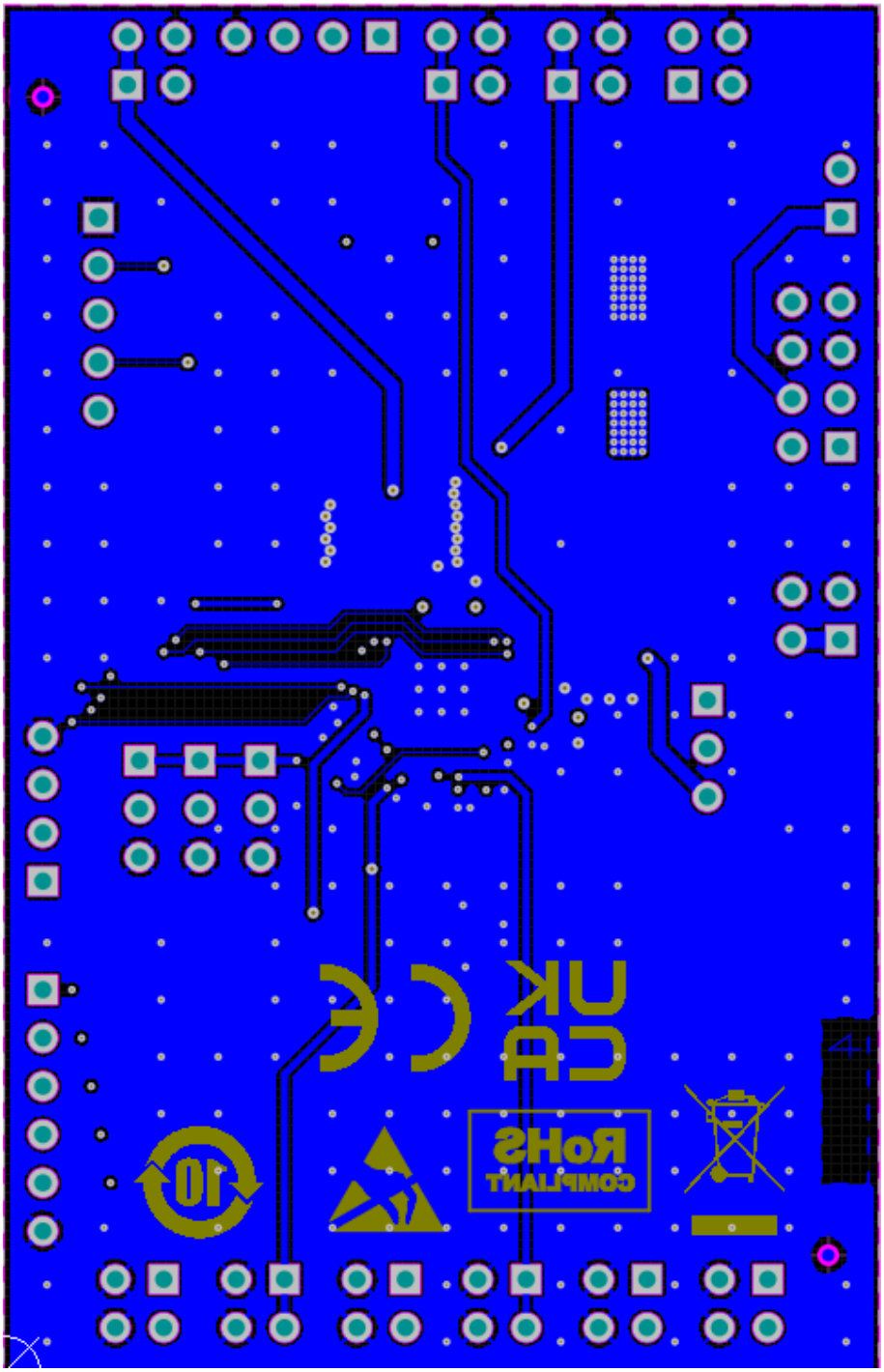


Figure 17. **STEVAL-PMIC2LM1A: bottom layer (Power/GND)**

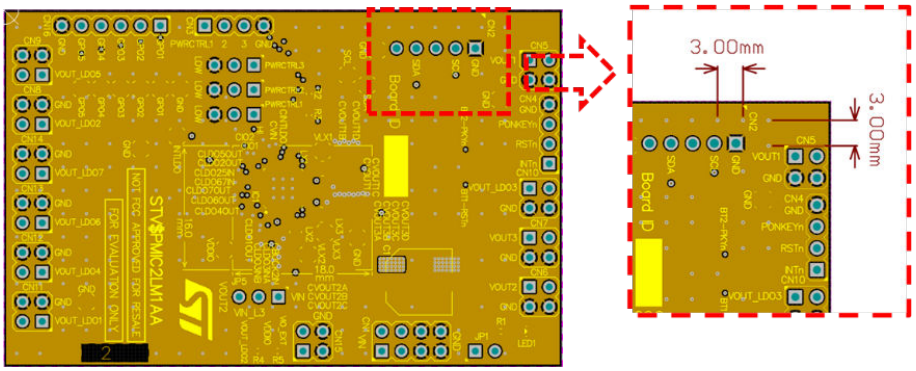


6.3 Power and ground planes

Since both Power and Ground are planes, inductive effects are minimized, providing a very low impedance path to the STPMIC2L evaluation board. The use of a continuous ground layer with multiple via holes is a good method to achieve low impedance ground returns. However, to keep low impedance over all areas of the PCB, it should never be narrowed nor partitioned.

Figure 18 shows the mid layer 1 of the STPMIC2L evaluation board layout, with the detail on GND vias placed all around the PCB edge with 3 mm spacing.

Figure 18. **STEVAL-PMIC2LM1A: mid layer 1 (GND)**



The usage of flat and large shapes, whether possible, is recommended for all high current power supplies, such as VIN and VOUT. This helps reduce power loss. When examining the ground and power planes, make sure that the plane continuity is not affected by too many vias.

Examples of power planes, vias placement and plane shapes are shown in Figure 16, in which they are used to route VIN and all VOUT of the regulators out to connector headers.

6.4 Via holes

Even though the ground plane is a good ground reference, the presence of the vias along ground returns introduces some stray inductances at high frequency. Placing multiple via holes in a plane reduces this effect, considering that the stray inductances are in parallel. Those via holes must be spaced in such a way that the power plane is not excessively cut up.

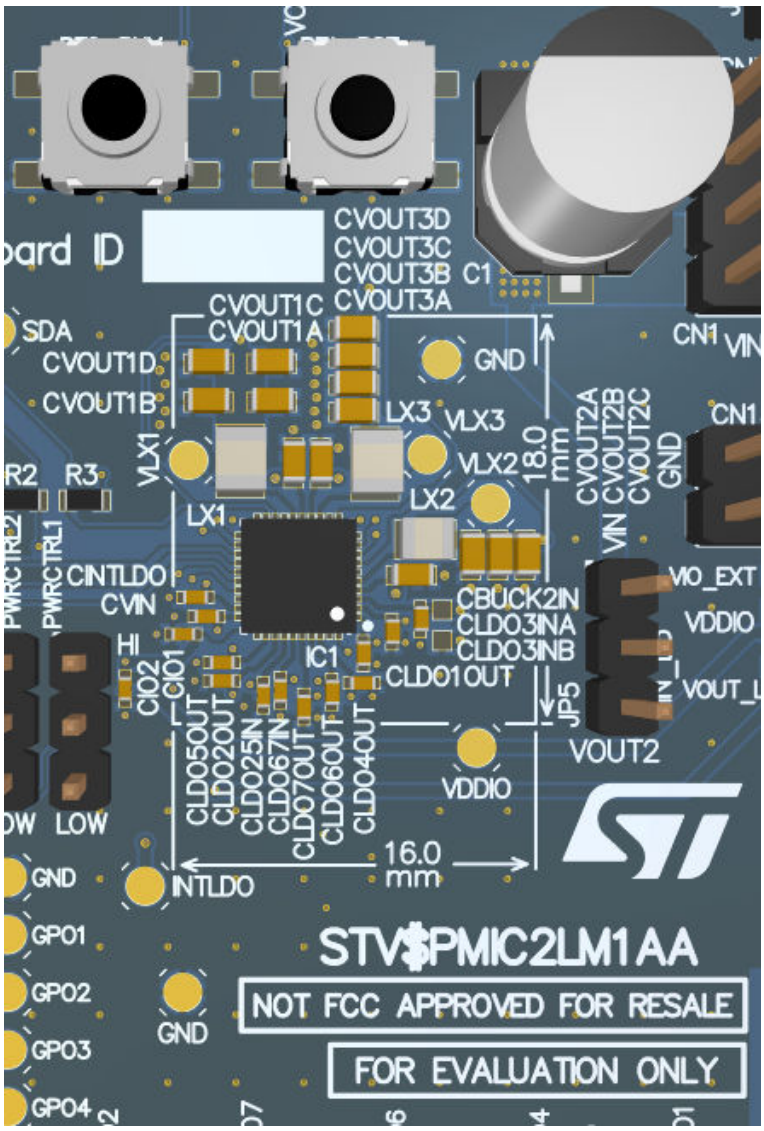
Table 9. **STEVAL-PMIC2LM1A via size**

Via type	Hole size	Pad size
Via holes	0.2 mm	0.5 mm

6.5 Passive components placement

Figure 19 shows the STPMIC2L passive components arrangement (input and capacitors, output coils, and resistors) in the evaluation board. The aim is to shrink all the BOM in the smallest area around the STPMIC2L device (16 mm x 18 mm).

Figure 19. STEVAL-PMIC2LM1A: passive components placement



All the suggestions described in this user manual have been implemented in the STPMIC2L evaluation board.

Moreover, it's good practice to put all the passive components on top of the layout and to use the bottom side only if it is absolutely needed due to the application/board size.

A decoupling capacitor of 100 µF was placed on the input supply rail for two reasons:

- In case of input voltage drop, it provides adequate power to the STPMIC2L to maintain the voltage level.
- In case of voltage surge, in order to keep the voltage stable, it prevents excess current from flowing through the STPMIC2L.

7 Bill of materials

Table 10. STEVAL-PMIC2LKV1 bill of materials

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	-	STEVAL-PMIC2LM1A	Evaluation board	ST	Not available for separate sale
2	1	-	Table 11. STEVAL-USBDNGV1	USB Dongle	ST	Not available for separate sale

Table 11. STEVAL-USBDNGV1 bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	9	C1, C4, C6, C7, C8, C9, C10, C11, C13	0.10 µF 50 V	Capacitor	Murata Electronics North America	GRM155R61H104KE14
2	2	C2, C5	1.0 µF 16 V	Capacitor	Murata Electronics North America	GRM155R61C105KA12
3	1	C3	2.2 µF 6.3 V	Capacitor	Murata Electronics North America	GRM155R60J225KE01
4	1	CN1	USB 2.0, 30 V/1 A	Connector	Wurth Electronics Inc.	65100516121
5	1	D1		BidirTVSDiode	Kyocera AVX	GG0402055R042P
6	4	D2, D3, D4, D5		LED	Kingbright	APT1608LVBC/D
7	1	D6		LED	Kingbright	APT1608SYCK
8	1	D7		LED	Kingbright	APT1608SURCK
9	2	D8, D9		TVSDiode, ST0102	ST	ESDALC6V1-1U2
10	1	F1		Fuse	Littelfuse Inc.	0466.250NRHF
11	1	FL1		ESD, QFN-6L	ST	ECMF02-2AMX6
12	1	P1		Connector	Sullins Connector Solutions	PPPC051LGBN-RC
13	4	R1, R8, R12, R18	0 Ohms	Resistor	Rohm Semiconductor	PMR01ZZPJ000
14	4	R3, R5, R6, R10	1.5 kOhms	Resistor	Yageo	RC0402FR-071K5L
15	1	R11	180 Ohms	Resistor	Yageo	RC0402FR-07180RL
16	1	R13	100 Ohms	Resistor	Yageo	RC0402FR-07100RL
17	1	R14	220 Ohms	Resistor	Yageo	RC0402FR-07220RL
18	1	R15	270 Ohms	Resistor	Yageo	RC0402FR-07270RL
19	1	R16	10 kOhms	Resistor	Yageo	RC0402FR-0710KL
20	2	SW1, SW2		Button	C&K	KMR432NGULCLFS
21	1	U1		Level Translator BiDir	TI	LSF0204DRUTR
22	1	U2		LDO, SOT323-5L	ST	LDK120C33R

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
23	1	U3		LDO, SOT323-5L	ST	LDK120C33R
24	1	U4		MCU, LQFP 48 7x7x1.4 mm	ST	STM32F303CCT6
25	1	X1	8 MHz	Resonator	Murata Electronics	CSTNE8M00GH5L000R0

8 Kit versions

Table 12. STEVAL-PMIC2LKV1 kit versions

Finished good	Schematic diagrams	Bill of materials
STV$PMIC2LKV1A(1)	STV$PMIC2LKV1A schematic diagrams	STV$PMIC2LKV1A bill of materials

1. *This code identifies the STEVAL-PMIC2LKV1 evaluation kit first version. The kit consists of a STEVAL-PMIC2LM1A whose version is identified by the code STV$PMIC2LM1AA and a STEVAL-USBDNGV1 whose version is identified by the code STEVAL$USBDNGV1A.*

9 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
19-Nov-2025	1	Initial release.

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