



XWire12B Device User Manual

Introduction

The XWire12B is an ISO26262 ASIL D compliant application-specific integrated actuation solution for corner wheel control unit (WCU) in 12 V electro-mechanical brake (EMB) systems (mixed wet/dry or pure-dry), developed in advanced BCD technology. It integrates the full actuation stage to accomplish service and parking brake phases through a 3-Phase inverter floating predriver and a flexible H-Bridge predriver. MCU can rely on three integrated high accuracy floating current sense amplifiers for advanced brushless motor control algorithms.

The H-Bridge predriver allows totally independent FET control, granting flexibility in the execution of several parking brake strategies (unidirectional/bidirectional DC motors, single/dual solenoid driver for mechanical locking component control).

The device also integrates a wheel speed sensor interface for sensor data acquisition and decoding to ensure the availability of information to allow the MCU to modulate the braking torque according to the vehicle stability program.

The device is AEC-Q100 Grade 1 qualified.

1 Block diagram and pin description

Figure 1. Block diagram

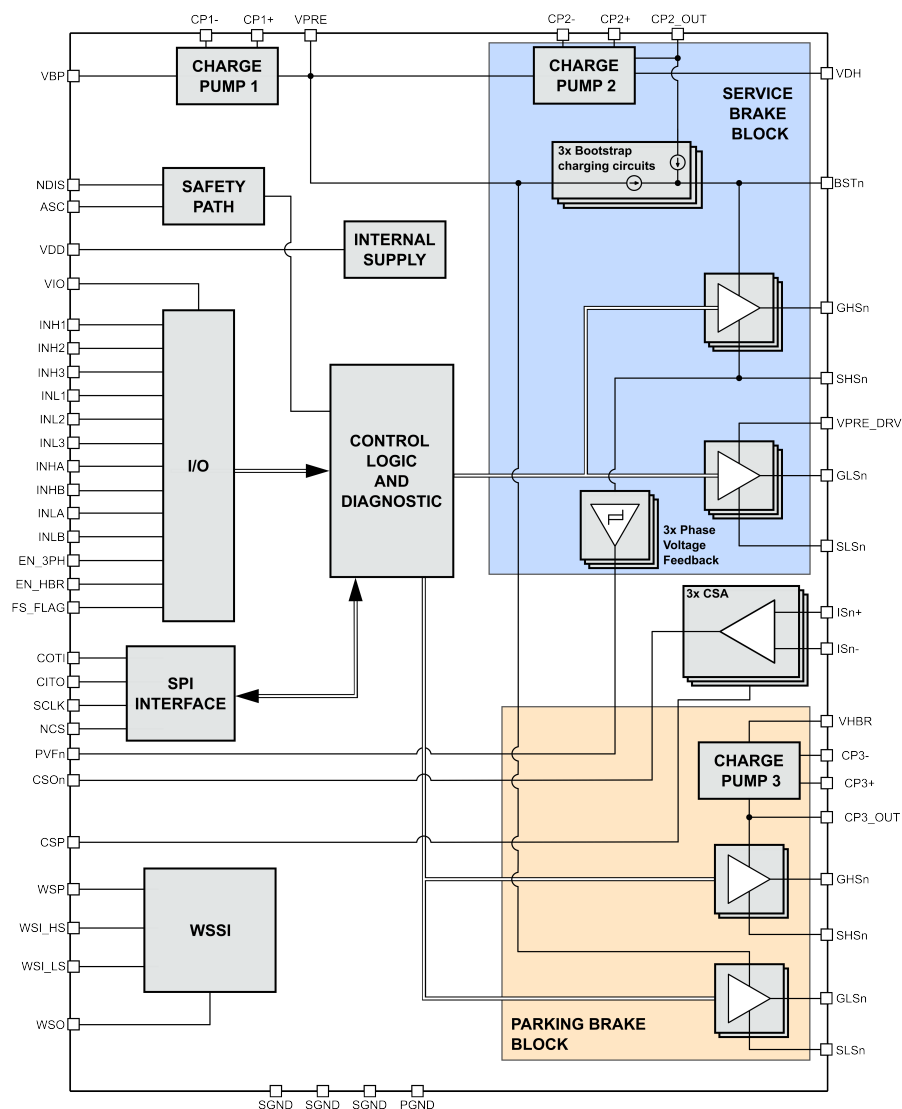


Figure 2. Pin connection (top view)

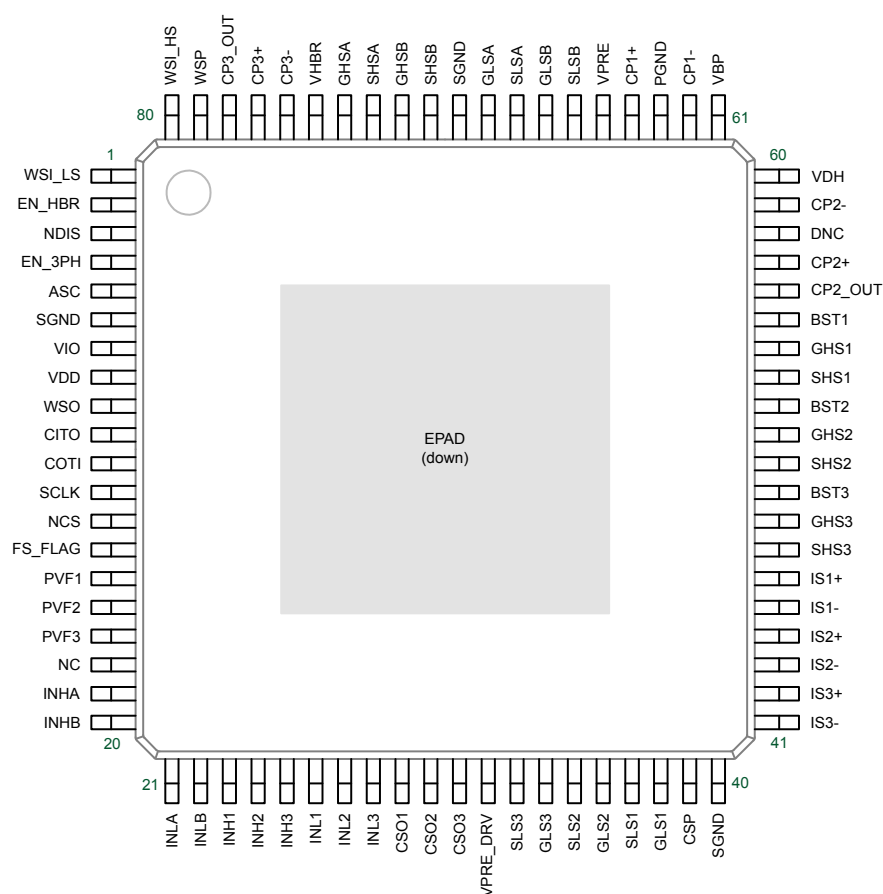


Table 1. Pin function description

Pin number	Pin name	Description	I/O type	Class
1	WSI_LS	Wheel speed sensor LS interface	I	Local
2	EN_HBR	H-Bridge Enable Input (Active HIGH)	DI	Local
3	NDIS	Safe switch-off activation Input (Active LOW)	DI	Local
4	EN_3PH	3-Phase Bridge Enable Input (Active HIGH)	DI	Local
5	ASC	3-Phase Bridge active short circuit input pin	DI	Local
6	SGND	Signal Ground (Analog, Digital, Reference)	G	Local
7	VIO	Digital I/O power supply	S	Local
8	VDD	Power supply input for internal circuitry and VIO	S	Local
9	WSO	Wheel speed sensor output	DO	Local
10	CITO	SPI Controller Input – Target Output	DO	Local
11	COTI	SPI Controller Output – Target Input	DI	Local
12	SCLK	SPI Serial Clock Input	DI	Local
13	NCS	SPI Chip Select Input (Active LOW)	DI	Local

Pin number	Pin name	Description	I/O type	Class
14	FS_FLAG	Fault status flag output (Active LOW)	DO	Local
15	PVF1	Phase voltage feedback 1 output	DO	Local
16	PVF2	Phase voltage feedback 2 output	DO	Local
17	PVF3	Phase voltage feedback 3 output	DO	Local
18	NC	Not connected. Tie to ground potential.	-	-
19	INHA	PWM command for H-Bridge HS, phase A	DI	Local
20	INHB	PWM command for H-Bridge HS, phase B	DI	Local
21	INLA	PWM command for H-Bridge LS, phase A	DI	Local
22	INLB	PWM command for H-Bridge LS, phase B	DI	Local
23	INH1	PWM command for 3-ph HS, phase 1	DI	Local
24	INH2	PWM command for 3-ph HS, phase 2	DI	Local
25	INH3	PWM command for 3-ph HS, phase 3	DI	Local
26	INL1	PWM command for 3-ph LS, phase 1	DI	Local
27	INL2	PWM command for 3-ph LS, phase 2	DI	Local
28	INL3	PWM command for 3-ph LS, phase 3	DI	Local
29	CSO1	Current Sense Amplifier 1 analog output	O	Local
30	CSO2	Current Sense Amplifier 2 analog output	O	Local
31	CSO3	Current Sense Amplifier 3 analog output	O	Local
32	VPRE_DRV	Input pin for pre-driver supply. Shall be connected to VPRE	S/I	Local
33	SLS3	Source connection of 3-ph LS FET, phase 3	I/O	Local
34	GLS3	Gate connection of 3-ph LS FET, phase 3	I/O	Local
35	SLS2	Source connection of 3-ph LS FET, phase 2	I/O	Local
36	GLS2	Gate connection of 3-ph LS FET, phase 2	I/O	Local
37	SLS1	Source connection of 3-ph LS FET, phase 1	I/O	Local
38	GLS1	Gate connection of 3-ph LS FET, phase 1	I/O	Local
39	CSP	Supply for CSO output	S	Local
40	SGND	Signal Ground (Analog, Digital, Reference)	G	Local
41	IS3-	Current Sense Amplifier 3 negative input	I	Global
42	IS3+	Current Sense Amplifier 3 positive input	I	Global
43	IS2-	Current Sense Amplifier 2 negative input	I	Global
44	IS2+	Current Sense Amplifier 2 positive input	I	Global
45	IS1-	Current Sense Amplifier 1 negative input	I	Global
46	IS1+	Current Sense Amplifier 1 positive input	I	Global

Pin number	Pin name	Description	I/O type	Class
47	SHS3	Source connection of 3-ph HS FET, phase 3	I/O	Global
48	GHS3	Gate connection of 3-ph HS FET, phase 3	I/O	Local
49	BST3	Bootstrap capacitor of 3-ph HS, phase 3	I/O	Local
50	SHS2	Source connection of 3-ph HS FET, phase 2	I/O	Global
51	GHS2	Gate connection of 3-ph HS FET, phase 2	I/O	Local
52	BST2	Bootstrap capacitor of 3-ph HS, phase 2	I/O	Local
53	SHS1	Source connection of 3-ph HS FET, phase 1	I/O	Global
54	GHS1	Gate connection of 3-ph HS FET, phase 1	I/O	Local
55	BST1	Bootstrap capacitor of 3-ph HS, phase 1	I/O	Local
56	CP2_OUT	Charge Pump 2 output	S/O	Local
57	CP2+	Charge Pump 2 positive input of fly capacitance	I/O	Local
58	DNC	Do Not Connect	DNC	Local
59	CP2-	Charge Pump 2 negative input of fly capacitance	I/O	Local
60	VDH	Drain connection of 3-Phase driver HS FETs	I	Global
61	VBP	Pre-regulation stage power supply	S	Global
62	CP1-	Charge Pump 1 negative input of fly capacitance	I/O	Local
63	PGND	Power Ground	G	Local
64	CP1+	Charge Pump 1 positive input of fly capacitance	I/O	Local
65	VPRE	Pre-regulated voltage for gate driving	S/O	Local
66	SLSB	Source connection of H-Bridge LS FET	I/O	Local
67	GLSB	Gate connection of H-Bridge LS FET, phase B	I/O	Local
68	SLSA	Source connection of H-Bridge LS FET	I/O	Local
69	GLSA	Gate connection of H-Bridge LS FET, phase A	I/O	Local
70	SGND	Signal Ground (Analog, Digital, Reference)	G	Local
71	SHSB	Source connection of H-Bridge HS FET, phase B	I/O	Local
72	GHSB	Gate connection of H-Bridge HS FET, phase B	I/O	Local
73	SHSA	Source connection of H-Bridge HS FET, phase A	I/O	Local
74	GHSA	Gate connection of H-Bridge HS FET, phase A	I/O	Local
75	VHBR	Drain connection of H-Bridge driver HS FETs	I	Global

Pin number	Pin name	Description	I/O type	Class
76	CP3-	Charge Pump 3 negative input of fly capacitance	I/O	Local
77	CP3+	Charge Pump 3 positive input of fly capacitance	I/O	Local
78	CP3_OUT	Charge Pump 3 output	S/O	Local
79	WSP	Wheel speed sensor Power supply input	S	Global
80	WSI_HS	Wheel speed sensor HS interface	O	Local
	Exp. pad	Cooling slug to be connected to GND plane, no internal electrical connection		Local

Note: pin type legenda:

- I=Input
- DI=Digital Input
- O=Output
- DO=Digital Output
- S=Supply
- G=GND
- DNC=Do Not Connect

2 Reference application circuit

Figure 3. Application circuit

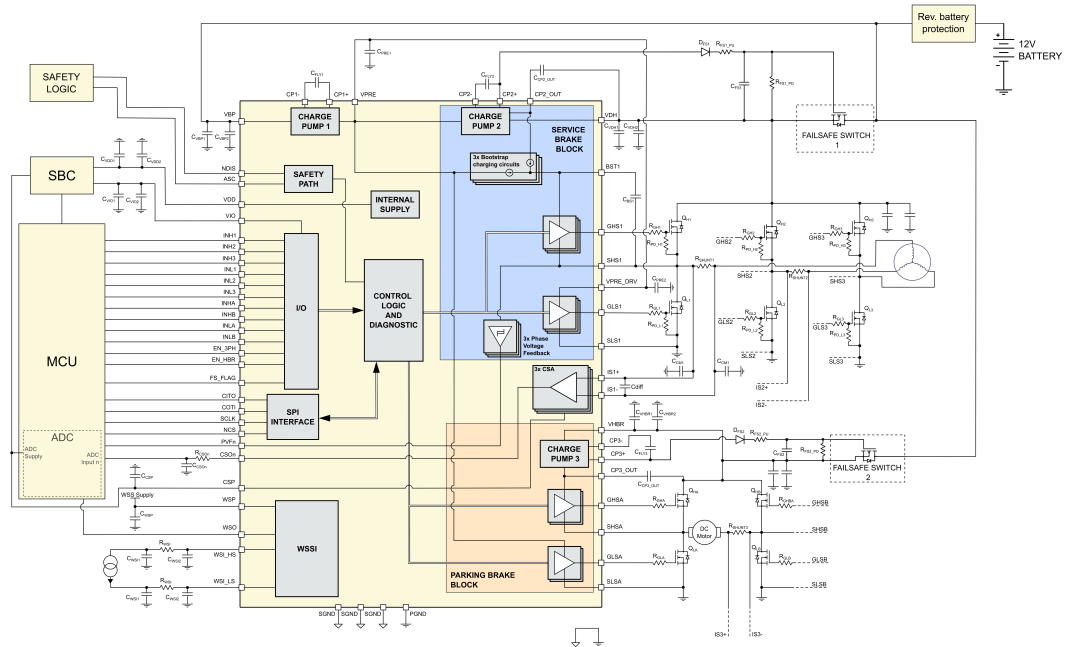


Table 2. Bill of material

Component	Value				Minimum rating	Comment
	Min.	Typ.	Max.	Unit		
CBSn		1		μF	25 V	n=1,2,3
CCSOn		220		pF	6.3 V	n=1,2,3
CFLY1		1		μF	50 V	
CFLY2		1		μF	50 V	
CFLY3		1		μF	50 V	
CCP2_OUT		1		μF	63 V	
CCP3_OUT		1		μF	63 V	
CCM1		10		nF	50 V	To be mounted close to RSHUNTn, n=1,2,3
Cdiff		220		nF	35 V	To be mounted close ISn+, ISn- to pins, n=1,2,3
CVBP1		1		μF	50 V	
CVBP2		100		nF	50 V	
CVDD1		1		μF	6.3 V	
CVDD2		100		nF	6.3 V	
CVDH1		100		nF	50 V	
CVDH2		1		μF	50 V	

Component	Value				Minimum rating	Comment
	Min.	Typ.	Max.	Unit		
C _{FS1}		10		nF	25 V	
C _{VHBR1}		100		nF	50 V	
C _{VHBR2}		1		μF	50 V	
C _{FS2}		10		nF	25 V	
C _{VIO1}		1		μF	6.3 V	
C _{VIO2}		100		nF	6.3 V	
C _{CSP}		1		μF	6.3 V	
C _{VPRE1}		2.2	3.3	μF	16 V	Max tolerance ±20%
C _{VPRE2}		2.2	3.3	μF	16 V	Max tolerance ±20%
C _{WSP}		1		μF	50 V	
C _{WSI1}		1		nF	25 V	x2 if both HS and LS WSS interfaces are used
C _{WSI2}		10		nF	25 V	x2 if both HS and LS WSS interfaces are used
R _{CSOn}		1		kΩ		n=1,2,3
R _{WSI}		10		Ω		x2 if both HS and LS WSS interfaces are used
R _{PD_Hn}		47		kΩ		n=1,2,3
R _{PD_Ln}		47		kΩ		n=1,2,3
R _{GHn}		(1)		Ω		n=1,2,3, A, B
R _{GLn}		(1)		Ω		n=1,2,3, A, B
Q _{Hn}		(2)				n=1,2,3, A, B
Q _{Hn}		(2)				n=1,2,3, A, B
R _{FS1_PU}		100		Ω		
R _{FS1_PD}		47		kΩ		
R _{FS2_PU}		100		Ω		
R _{FS2_PD}		47		kΩ		
D _{FS1}	STPS1L60-Y					
D _{FS2}	STPS1L60-Y					

- Note:**
1. Series gate resistor value must be selected by the user according to application requirements.
 2. MOSFETs part numbers must be selected by the user according to application requirements.

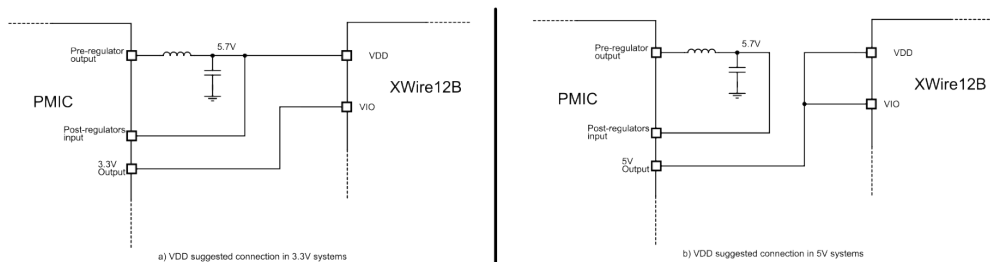
3 Low voltage power supply

The device needs 4 low voltage supplies to supply different device subcircuits: V_{VDD} , V_{VIO} , V_{CSP} and V_{WSP} .

3.1 VDD supply

The V_{VDD} is necessary to supply the device main logic. In systems where the PMIC is regulating a stable 5 V rail the VDD pin must be connected to that rail. When the 5 V rail is not available, for example, in ECUs where the MCU is 3.3 V-based, it is not necessary to add a dedicated regulator to generate the supply voltage but the VDD pin can be connected to the PMIC preregulator output, which is typically between 5.5 V and 7.5 V.

Figure 4. VDD connection in 3.3 V and 5 V systems



3.2 VIO supply

The V_{VIO} is the supply for the device digital I/Os, therefore must be connected to the same rail used to supply MCU I/Os. The XWire12B supports both 3.3 V and 5 V VIO supplies.

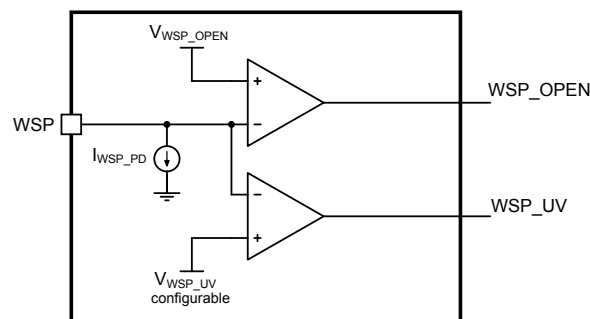
3.3 CSP supply

The V_{CSP} is needed to supply the output stage of the CSAs. Given the impact of the CSP supply voltage on CSO output range, this pin must be connected to a dedicated low-noise supply rail. To prevent ADC acquisition issues, it is strongly recommended to connect the CSP pin to the supply rail dedicated to MCU's ADC so that the two circuits will not show additional error on current reading due to misalignment between the two supply voltages.

3.4 WSP supply

The device contains a 1-channel wheel speed sensor interface that reports the sensor status to the MCU via the SPI. The WSS interface and sensor are supplied by WSP.

Figure 5. WSSI supply monitor



The monitoring unit shall guarantee the detection of undervoltage events/open circuit on WSP pin to guarantee the correct driving of the external wheel speed sensor.

When the WSP pin voltage falls below V_{WSP_OPEN} the WSP_OPEN flag is set and latched.

The undervoltage threshold is configurable by setting the SPI field WSP_UV_CFG as reported in Table 3.

Table 3. WSS supply monitor electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V _{WSP_OPEN}	WSP monitor open circuit threshold		3	3.75	4.5	V
V _{WSP_UV1}	WSP monitor undervoltage 1	WSP_UV_CFG=00	7.25	7.5	7.85	V
V _{WSP_UV2}	WSP monitor undervoltage 2	WSP_UV_CFG=01	6.5	6.7	6.9	V
V _{WSP_UV3}	WSP monitor undervoltage 3	WSP_UV_CFG=10/11	5.88	6	6.12	V
I _{WSP_PD}	WSP monitor pull-down current		10		150	uA
T _{WSP_UV}	Comparator delay			600	1200	ns
T _{WSP_FLT}	WSP monitor filter time	CLK_SSM_EN = 0	8	10	12	us

The WSP_UV monitor has been designed to be compatible with sensors that require a 12 V power supply. To use sensors with a lower power supply voltage, for example 5 V, the user must change the reaction and redirection of the WSP_UV flag, so even a detection of an undervoltage event will not have an impact on the functionality. The WSP_OPEN monitor will still be functional, guaranteeing the detection of a deep undervoltage event.

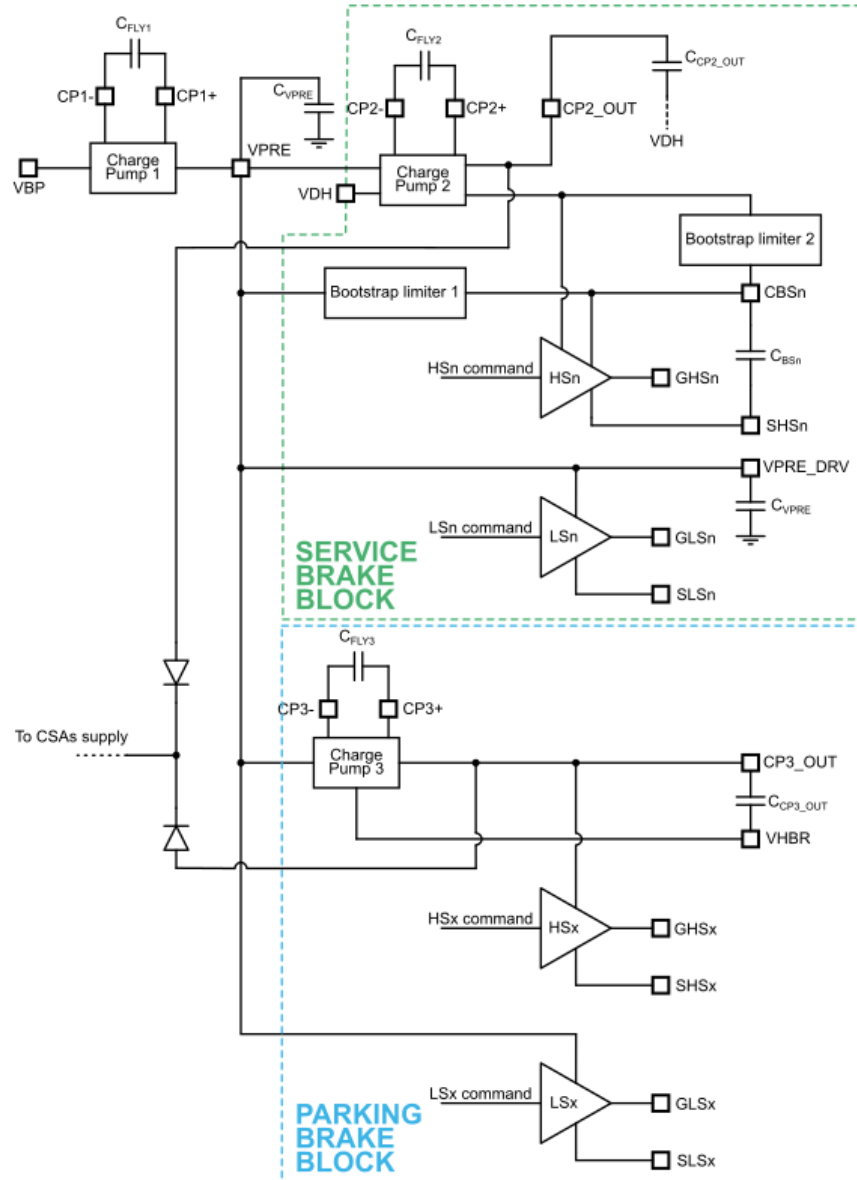
Table 4. Configuration steps for WSS power supply class different from 12 V

# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
1	Enter Normal mode			Refer to section 9.
2	CONFIG mode access (first unlock frame)	0x31	0x55	Enter in configuration mode by writing two SPI frames.
3	CONFIG mode access (second unlock frame)	0x31	0x33	
4	WSP_UV_REDIRECT_CFG=1	0x1F	0x01	WSP undervoltage condition redirected on GWB.
5	CONFIG mode exit	0x31	0xAA	

4 Actuation stages of power supply

XWire12B is equipped with a multiple-stages power supply architecture to provide energy for external FETs driving and CSA operation. A simplified schematic is depicted in Figure 6.

Figure 6. Power supply architecture



The charge pump 1 acts as the main preregulator that converts the battery voltage into a stable VPRE voltage used to supply low-side predrivers, to charge bootstrap capacitors and as a reservoir for charge pump 2 (CP2) and charge pump 3 (CP3).

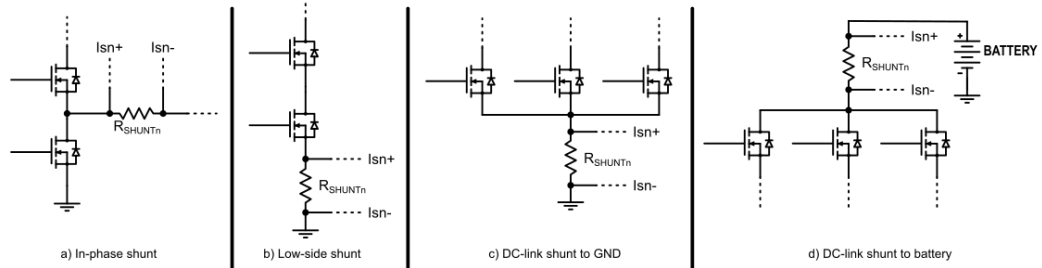
CP2 is dedicated to the service brake block, top-offing the high-side bootstrap capacitors voltage at high duty cycles to ensure correct operation, while CP3 is dedicated to the parking brake block, directly feeding the high-side predrivers.

Both CP2 and CP3 are used to supply the three CSAs, ensuring their functionality when at least one charge pump is enabled.

5 Current sense amplifier

Each CSA can be used independently according to the final application; examples of typical current sensing shunt resistor placement are depicted in Figure 7.

Figure 7. Current sensing shunt resistor connection examples



Where a) and b) connections are applicable to any load connected to the 3-phase inverter or to the H-bridge (3-phase motor, DC motor, solenoid, etc.); while the c) and d) solutions are intended to sense the 3-phase inverter total current, but the same approach can be also used to sense the H bridge total current or even the overall current from the battery.

For suggestions about CSA's input and output external filters sizing refer to Section 5.1

Figure 8. Typical current sense shunt resistor placement

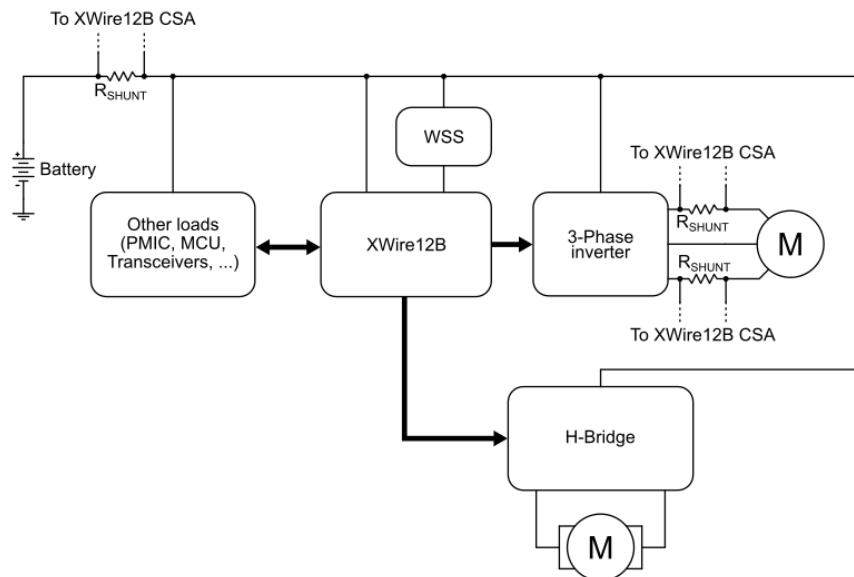


Figure 8 shows a typical current sensing architecture implementation that uses two CSAs with in-phase shunt connection to sense the current flowing in two of the 3 phases of the Service Brake inverter, while the third CSA is used to sense the overall current from the battery. In this architecture the shunt on the battery line can be used to sense the overall current to the 3-phase motor during the Service Brake actuation, to measure the EPB current during parking brake actuation and to measure also the current when no actuation is applied to monitor the ECU current consumption.

As specified in Section 4, the CSAs are supplied by the actuation stages power supply, and the three CSAs are enabled if at least one of the CPs output voltages is above VCPn_UV (n=2, 3).

5.1 Current sense amplifiers (CSAs) filters selection

5.1.1 Output filter

Each current sense amplifier output CSOn requires an RC filter to stabilize the output and to reject the noise that may affect the current sense chain accuracy. The filter bandwidth must be selected to be smaller than the CSA bandwidth to be effective, but given that it also impacts the CSA input common-mode recovery time (T_{CM_REC}) and the output settling time (T_{SET}) its lower boundary must be limited to guarantee a response fast enough to allow a correct signal sampling in every PWM conditions, particularly when CSA is used to sense in-phase shunt resistor.

Typical 3-phase PMSM Field-Oriented Control are based on a SVPWM center-aligned technique that requires to sample the inverter currents simultaneously at the center of specific PWM periods when all the three High Side (or Low Side) are on at the same time (zero vector state), therefore the maximum $T_{CM_REC} + T_{SET}$ time is limited by:

$$T_{CM_REC} + T_{SET} < \frac{T_{PWM} * D_{min}}{2} \quad (1)$$

Where:

- T_{CM_REC} is the CSA common-mode transient recovery time
- T_{SET} is the CSA output settling time
- T_{PWM} is the PWM period
- D_{min} is the minimum PWM duty cycle

The equation must be satisfied only in applications where the CSA inputs are exposed to common-mode voltage transients (in-phase current sensing); if CSA inputs are not exposed to such variations (low-side current sensing, DC-Link current sensing) the T_{CM_REC} can be neglected.

The reference application circuit includes a $R_{CSO} = 1 \text{ k}\Omega$ and a $C_{CSO} = 220 \text{ pF}$, and the overall CSA response is:

$$T_{CM_REC} + T_{SET} \leq 1.5 \text{ } \mu\text{s} + 1 \text{ } \mu\text{s} = 2.5 \text{ } \mu\text{s} \quad (2)$$

At a first approximation, the T_{CM_REC} is independent of the RC output filter value, while the T_{SET} can be considered as the time constant of a 2-poles system, where a pole is given by the CSA frequency response, and the second is the pole of the CSO RC filter.

In the reference circuit the CSO RC filter and the CSA have similar but different frequencies, allowing to approximate the output filter pole as the dominant one (see calculation example 1). The resistance and/or capacitance of the CSO RC filter can be reduced to improve CSA chain dynamic response; in this case the system must be evaluated as a dual coincident poles system (see calculation example 2).

Further increment of CSO filter bandwidth is in principle allowed but it must be evaluated case by case to ensure output signal stability and avoid oscillations.

Calculation example 1:

Data:

$BW_{CSA} \geq 1.5 \text{ MHz} \rightarrow T_{CSA} \leq 110 \text{ ns}$
 $F_{PWM} = 20 \text{ kHz} \rightarrow T_{PWM} = 50 \text{ } \mu\text{s}$
 $R_{CSO} = 1 \text{ k}\Omega$, $C_{CSO} = 220 \text{ pF} \rightarrow T_{RC} \approx 220 \text{ ns}$
 In-phase current sensing

Calculation:

$T_{CSA} > T_{RC} \approx 110 \text{ ns} \rightarrow T_{CSA}$ dominant pole
 $T_{SET} \approx 5 * R_{CSO} * C_{CSO} \approx 1 \text{ } \mu\text{s}$
 $T_{CM_REC} + T_{SET} < \frac{T_{PWM} * D_{min}}{2} = 2.5 \text{ } \mu\text{s} \rightarrow D_{min} = 10 \%$

Calculation example 2:

Data:

$BW_{CSA} \geq 1.5 \text{ MHz} \rightarrow T_{CSA} \leq 110 \text{ ns}$

$F_{PWM}=20\text{ kHz} \rightarrow T_{PWM}=50\text{ }\mu\text{s}$
 $R_{CSO}=500\Omega, C_{CSO}=220\text{ pF} \rightarrow \tau_{RC}\approx 110\text{ ns}$

In-phase current sensing

Calculation:

$\tau_{CSA}\approx\tau_{RC}\approx 110\text{ ns} \rightarrow$ coincident poles

$T_{SET}\approx 7.4*\tau_{CSA}=7.4*\tau_{RC}\approx 0.8\text{ }\mu\text{s}$

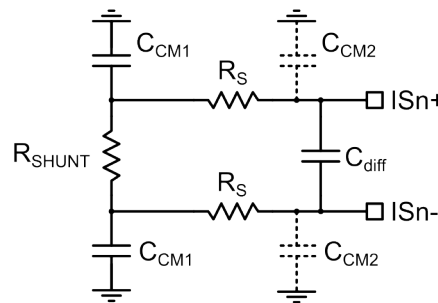
$T_{CM_REC} + T_{SET} < \frac{T_{PWM} * D_{min}}{2} = 2.3\text{ }\mu\text{s} \rightarrow D_{min} \approx 9\%$

If the control algorithm requires to support lower duty cycles the center-aligned sampling strategy must be discarded for a more sophisticated method (for example, earlier sampling with error compensation).

5.1.2 Input filter

The introduction of a low-pass filter on the CSA inputs is recommended to remove the input noise and improve the signal-to-noise ratio at the output. Components selection must be carried out by the user as they are familiar with their system and should determine the minimum frequency above which noise must be filtered. Components for this filter must have the lowest tolerance; a mismatch between I_{Sn+} and I_{Sn-} may result in a systematic error in current measurement. The filter is composed of two filtering stages: the common-mode filter, which stabilizes the common-mode input voltage, and the differential filter, which reduces the differential noise. A typical CSA input filter architecture is shown in Figure 9, where the C_{CMn} capacitors are used to filter common-mode noise, while C_{diff} to filter the differential noise.

Figure 9. CSA input filter typical implementation example



The R_S resistors and the C_{diff} capacitor must be placed as close as possible to the device input pins to ensure maximum differential noise filtering efficacy. Given the circuit depicted in Figure 9 the differential low pass filter cutoff frequency follows the relationship below:

$$f_{p_diff} \approx \frac{1}{2\pi C_{diff}(R_{SHUNT} + 2R_S)} \approx \frac{1}{4\pi C_{diff}R_S} \quad (3)$$

Where the shunt resistor value is considered negligible compared to R_S resistance.

When the CSA is used to sense LS FET current, the bandwidth of the sensing chain must be sized to be able to amplify correctly also current pulses of very small duration. A generally applicable rule is to have the cutoff frequency 10 to 100 times higher than the PWM frequency.

When the CSA is used to sense the phase current, the minimum value for sensing chain bandwidth is given by the dynamic response of the amplifier to the common-mode transient: the low pass filter bandwidth must be large enough to ensure a proper $T_{CM_REC}+T_{SET}$ duration (see Section 5.1.1 for details).

The R_S resistance must be in the order of a few tens of ohms maximum to avoid an impact on accuracy due to CSA input bias current.

The C_{CM1} capacitors must be placed as close as possible to the shunt resistor terminals to avoid a common mode-to-differential conversion that may happen along the path due to parasitics and components tolerances. Typical value for C_{CM1} capacitors are in the range of tens of nF.

C_{CM2} capacitors are optional and must be added close to device pins only when PCB layout cannot guarantee a proper shielding against common-mode disturbances to the CSA input traces.

Given the circuit depicted in Figure 9 and assuming $C_{CM2} \ll C_{diff}$ and $(R_{SHUNT} \cdot C_{CM1}) \ll R_S \cdot C_{CM2}$ the common-mode low pass filter cut frequency will be equal to:

$$f_{p_CM} \approx \frac{1}{2\pi C_{CM2} R_S} \quad (4)$$

The common-mode filter cutoff frequency should be selected to be at least 10 times the differential filter cutoff frequency.

Calculation example:

Data:

$$f_{PWM} = 20 \text{ kHz} \rightarrow T_{PWM} = 50 \text{ } \mu\text{s}$$

$$D = 5\% \div 95\% \rightarrow T_{ON_LS_min} = 2.5 \text{ } \mu\text{s}$$

Low side current sensing

To ensure correct current reading, the selected differential cutoff frequency is 50 times the PWM frequency.

Calculation:

$$f_{p_diff} \approx \frac{1}{4\pi C_{diff} R_S} = 50 * f_{PWM} = 1 \text{ MHz}$$

Selected $R_S = 10 \text{ } \Omega$

$$C_{diff} \approx \frac{1}{4\pi f_{p_diff} R_S} \approx 8 \text{ nF}$$

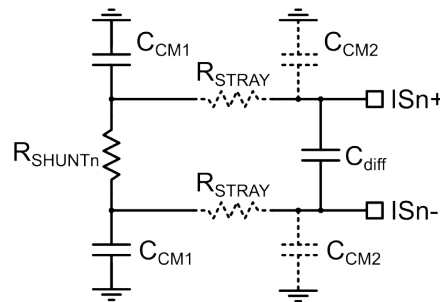
To ensure correct filter sizing, the selected common-mode cutoff frequency is 20 times the differential cutoff frequency.

$$C_{CM2} \approx \frac{1}{2\pi f_{p_CM} R_S} = 800 \text{ pF}$$

As suggested above, the selected value of the CCM1 capacitor is 10 nF.

When system constraints (e.g. layout) requires to avoid placing external components as much as possible, the R_S resistors can be avoided and replaced by R_{STRAY} , as depicted in Figure 10:

Figure 10. CSA input filter without series resistors



Where R_{STRAY} is the PCB trace stray resistance that must be estimated to properly select the components' value. The cutoff frequencies of the two filters can be estimated using the following relationships:

$$f_{p_diff} \approx \frac{1}{2\pi C_{diff} (R_{SHUNTn} + 2R_{STRAY})} \quad (5)$$

$$f_{p_CM} \approx \frac{1}{2\pi C_{CM2} R_{STRAY}} \quad (6)$$

5.2 CSA residual offset compensation algorithm

In Section 5 current sense amplifier (CSA) has been described, including its usage and the sizing of input and output filters.

This section describes a suggested calibration procedure for the entire acquisition chain to be performed at ECU level to improve the accuracy of the CSA. The aim of the calibration is to reduce the contribution of CSA offset error.

The suggested compensation algorithm follows these steps:

1. Measure the offset as:

$$\begin{aligned}\Delta V[V] &= Offset_{real} - Offset_{ideal} = \\ &= V_{CSO_{measured}}(Vin = 0) - V_{CSO_{ideal}}(Vin = 0)\end{aligned}\quad (7)$$

2. Save data in memory

3. Subtract ΔV from each measurement as:

$$Vin_{compensated}[V] = Vin - \Delta V \quad (8)$$

4. Calculate the current as:

$$I[A] = \frac{Vin_{compensated} - Offset_{ideal}}{G * R_{shunt}} \quad (9)$$

Where:

- G is the setted gain
- Rshunt is the shunt resistor

5.2.1 Evaluation of CSA accuracy improvement

To show improvement of CSA accuracy, a set of measures have been implemented.

The algorithm that calculates the error offset compensated [%] requires the following steps:

1. Calculate the offset: Offset [V]
2. Calculate the error before offset compensation: Error [%]
3. Calculate the compensated error: Error_offset_compensated [%]

Steps 2 and 3 must be repeated for the entire input range of the current sense amplifier (CSO), considering the nonsaturation region, which depends on the configured gain value (G).

The formulas are shown below:

$$Offset[V] = V_{CSO_{measured}}(Vin = 0) - V_{CSO_{ideal}}(Vin = 0) \quad (10)$$

Where:

- $V_{CSO_{measured}}(Vin=0)$ is the current sense amplifier-measured output (CSO) when the input voltage applied is 0 V.
- $V_{CSO_{ideal}}(Vin=0)$ is the current sense amplifier ideal output (CSO) when the input voltage applied is 0 V, which basically means:

$$V_{CSO_{ideal}}(Vin = 0)[V] = \frac{V_{CSP_{measured}}}{2} \quad (11)$$

Where $V_{CSP_{measured}}$ is the CSA supply input measured.

$$Error[V] = V_{CSO_{measured}} - V_{CSO_{ideal}} \quad (12)$$

Where:

- $V_{CSO_measured}$ is the current sense amplifier-measured output (CSO).
- V_{CSO_ideal} is the current sense amplifier ideal output (CSO), which basically means:

$$V_{CSO_ideal}[V] = G * V_{in} + \frac{V_{CSP_measured}}{2} \quad (13)$$

Where G is the current sense amplifier gain set.

$$Error\left[\%\right] = \frac{Error[V]}{V_{CSO_ideal} - \frac{V_{CSP_measured}}{2}} * 100 \quad (14)$$

$$Error_{offset\,compensated}[V] = Error[V] - Offset[V] \quad (15)$$

$$Error_{offset\,compensated}\left[\%\right] = \frac{Error_{offset\,compensated}[V]}{V_{CSO_ideal} - \frac{V_{CSP_measured}}{2}} * 100 \quad (16)$$

Table 5 shows examples of the algorithm results for different CSA power supply settings and configured gain values, where the pink lines show the XWire12B total input/output error, while the green lines show the residual input/output error after residual offset compensation algorithm application.

Table 5. Evaluation of CSA accuracy improvement

Residual offset compensation algorithm results	
	The settings are: • Current sense amplifier supply $V_{csp}=5\text{ V}$ • $G=20\text{ V/V}$ • Ambient temperature • Nonsaturation zone: $\pm 130\text{ mV}$
	The settings are: • Current sense amplifier supply $V_{csp}=3.3\text{ V}$ • $G=50\text{ V/V}$ • Ambient temperature • Nonsaturation zone: $\pm 60\text{ mV}$
	The settings are: • Current sense amplifier supply $V_{csp}=5\text{ V}$ • $G=10\text{ V/V}$ • Ambient temperature • Nonsaturation zone: $\pm 175\text{ mV}$

6 Failsafe driving

XWire12B enables the control of a dedicated external failsafe MOSFET for each actuator stage, aiming to disconnect the specific load from the battery in case of failure. Each failsafe MOSFET can be directly controlled by the charge pump that provides the supply to the relevant actuation stage, eliminating the need for a dedicated failsafe switch driver. Each charge pump is independently deactivated when the related actuation stage enters a safe state upon a fault detection (as described in the device datasheet) thus ensuring the load disconnection when a malfunction is detected.

To ensure compliance with safety requirements for the Fault Tolerant Time Interval (FTTI) allotted to the device, it is recommended to drive the failsafe MOSFET gate from the CPn+ pins (n=2, 3) instead of CPn_OUT (n=2, 3) pins which voltage may take significantly longer to decay due to the bulk capacitors connected to these pins, whereas the CPn+ voltage decays more quickly once the charge pump stops.

Figure 11. Example of independent failsafe switches driving

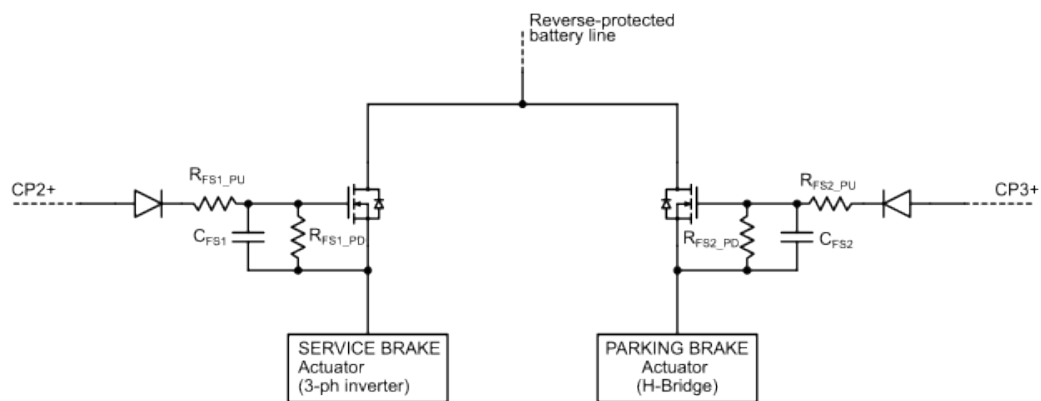


Figure 11 shows an example of failsafe switches driving circuit. R_{FSn_PU} must be selected to avoid excessive inrush current from CPn+ pins that may trigger the undervoltage protection at startup, a typical value is 100 Ω . R_{FSn_PD} must be selected to turn off the failsafe MOSFET within the FTTI while maintaining low the DC current consumption. A recommended value for the current consumption is a maximum of one-tenth of the total charge pump current capability. C_{FSn} is needed to help stabilize the gate voltage, given that CPn+ voltage is continuously switching; typical values are between 1 nF and 10 nF.

Calculation example:

Data:

$$C_{FS}=4.7 \text{ nF}$$

$$R_{FS_PU}=100 \text{ } \Omega$$

$$Q_{g_FET}=115 \text{ nC@12 V; approximately equivalent to a 10 nF capacitor}$$

$$V_{GSth}=2 \text{ V}$$

$$V_{GS_ON}=7 \text{ V}$$

$$V_{final_min}=V_{CP2_OUTmin}-V_{F_DIODE}-V_{VDH}=V_{CP3_OUTmin}-V_{F_DIODE}-V_{VHBR}=7.3 \text{ V}$$

$$V_{final_max}=V_{CP2_OUTmax}-V_{F_DIODE}-V_{VDH}=V_{CP3_OUTmax}-V_{F_DIODE}-V_{VHBR}=12.3 \text{ V}$$

$$FTTI=1 \text{ ms}$$

$$I_{CP2+_MAX}=2 \text{ mA}$$

$$I_{CP3+_MAX}=1 \text{ mA}$$

Concerning the calculation, the MOSFETs are considered fully on when $V_{GS} \geq V_{GS_ON}$ and are considered fully off when $V_{GS} \leq V_{GSth}$.

Calculation:

Time needed to turn on the failsafes:

$$\begin{aligned}
 T_{FSn_on} &= (C_{eq} + C_{FS}) * R_{FSn_PU} * \ln\left(\frac{V_{final_min}}{V_{final_min} - V_{GS_{ON}}}\right) = \\
 &= 14.7 \text{ nF} * 100 \text{ } \Omega * \ln\left(\frac{7.3 \text{ V}}{7.3 \text{ V} - 7 \text{ V}}\right) = 4.7 \text{ } \mu\text{s}
 \end{aligned}
 \tag{17}$$

Pull-down resistor sizing:

$$\begin{cases}
 R_{FSn_PD} \leq \frac{FTTI}{(C_{eq} + C_{FS}) * \ln\left(\frac{V_{final_max}}{V_{GSth}}\right)} = \frac{1 \text{ ms}}{14.7 \text{ nF} * \ln\left(\frac{12.3 \text{ V}}{2 \text{ V}}\right)} = 37.45 \text{ k}\Omega \\
 R_{FS1_PD} \geq \frac{V_{final_max}}{I_{CP2_max}} = \frac{12.3 \text{ V}}{2 \text{ mA}} = 6.15 \text{ k}\Omega \\
 R_{FS2_PD} \geq \frac{V_{final_max}}{I_{CP3_max}} = \frac{12.3 \text{ V}}{1 \text{ mA}} = 12.3 \text{ k}\Omega
 \end{cases}
 \tag{18}$$

Selected $R_{FS1_PD}=R_{FS2_PD}=20 \text{ k}\Omega$

Time needed to turn off the failsafe switches:

$$\begin{aligned}
 T_{FSn_OFF} &= R_{FSn_PD} * (C_{eq} + C_{FS}) * \ln\left(\frac{V_{final_max}}{V_{GSth}}\right) = \\
 &= 20 \text{ k}\Omega * 14.7 \text{ nF} * \ln\left(\frac{12.3 \text{ V}}{2 \text{ V}}\right) = 0.53 \text{ ms}
 \end{aligned}
 \tag{19}$$

Maximum DC current consumption from each charge pump:

$$I_{CPn+} = \frac{V_{final_max}}{R_{FSn_PU} + R_{FSn_PD}} \approx \frac{V_{final_max}}{R_{FSn_PD}} = \frac{12.3 \text{ V}}{20 \text{ k}\Omega} = 615 \text{ } \mu\text{A}
 \tag{20}$$

7 Layout suggestions

Board layout includes several aspects, such as track dimensions (length and width), circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements and power sources in the PCB area. Reasons to pay particular attention to the PCB layout include:

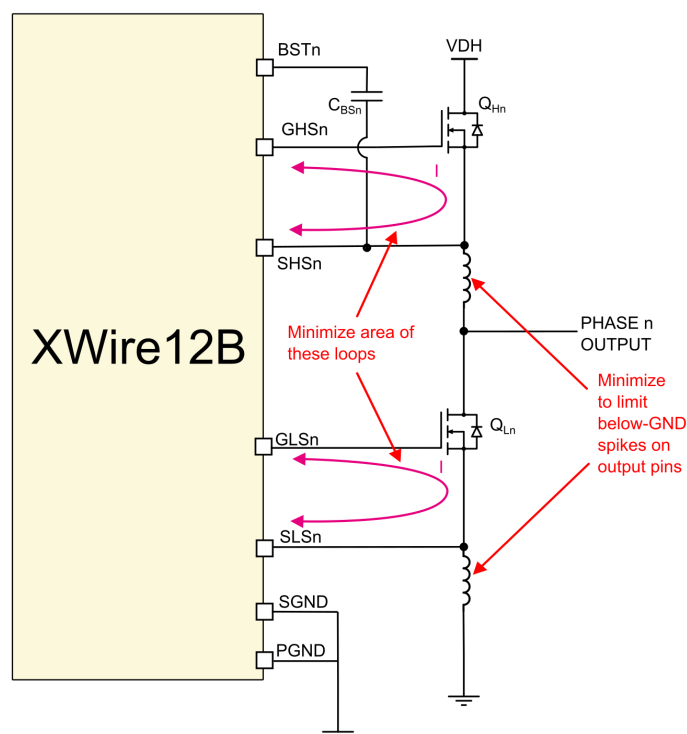
- EMI issues (both induced and perceived by the application);
- Overvoltage spikes due to parasitic inductances along the PCB traces;
- Proper connections of sense blocks, logic inputs and analog outputs of the device;
- Power dissipation and thermal management.

Gate driving PCB traces should be designed to be as short as possible, and the area of the loop formed by the gate line and its return line should be minimized to avoid the sensitivity of such structures to the surrounding noise. Typically, a good power system layout keeps the power MOSFETs of each half-bridge as close as possible to the related gate driver.

In Figure 12 is depicted the service brake portion schematic, highlighting the sensitive paths and the main parasitic inductances contributions.

The various groups of inductances may have undesired effects which should be limited as much as possible. Moreover, note that Figure 12 emphasizes parasitic inductances located on the lines usually managing high voltages and fast current transitions, which are very noisy analog signals. In fact, each phase of the bridge causes high currents (with high dI/dt) to flow on these paths, resulting in voltage noise which drops between the gate driver ground and the controller ground. This noise is directly added to all logic and analog voltage signals between the gate driver and the microcontroller, included the input logic signals and the analog output of the related gate driver. It is recommended to minimize this noise by reducing the distance between the signal ground and the driver ground (for each gate driver in the system) as much as possible. Generally, it is recommended to connect the signal ground to the power ground in a single point to avoid switching current noise recirculation into low voltage signal ground.

Figure 12. Layout suggestion for 3-phase system



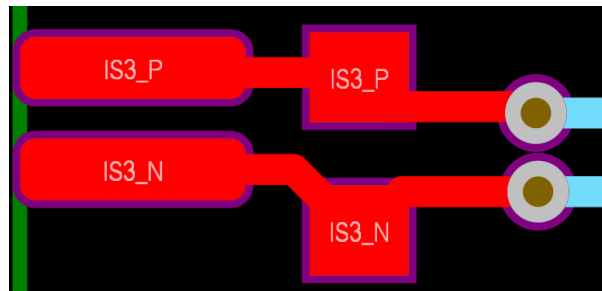
Note: it is very important to avoid any ground loop: only a single path must connect two different ground nodes.

Another useful suggestion is to ensure some distance between the lines switching with high-voltage transitions, and the signal lines are sensitive to electrical noise. Specifically, the tracks of each motor phase bringing significant currents and high voltages should be separated from the logic lines and analog sensing circuits.

For the layout section related to the current sense amplifier (CSA), it is recommended to:

- Route the CSP net on the internal layer of the PCB to ensure adequate electromagnetic shielding.
- Route the input lines (ISn+ and ISn-) on an internal layer of the PCB, keeping them coupled and symmetrical. Route with short traces on the top layer and use closely spaced vias to transition to the same inner layer as in Figure 13. Place the differential capacitor as close as possible to the device pins.

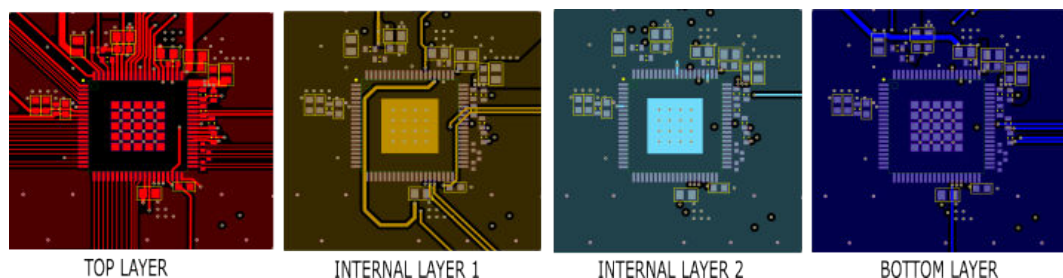
Figure 13. Suggested layout of CSA input lines



In Figure 14 there is a layout suggestion of a 4 layers board. Observing the four-layer structure, it is evident that the ground reference is managed in a distributed and consistent manner throughout the entire stack-up of the PCB. On the top layer, the exposed pad must be connected to ground planes in internal and bottom layers through a dense network of thermal vias (for details regarding the device footprint, see Section 7.2). This solution is optimal for thermal relief. Additionally, the traces routed around the component are kept organized and radially routed, which is essential to avoid crossings and discontinuities.

On internal layers 1 and 2, the area under the exposed pad is filled with copper connected to GND to improve the thermal performance. The bottom layer is almost completely covered by the GND plane, thus further improving the ability to reduce overall thermal resistance. Finally, it is suggested to place the decoupling and filter capacitors as close as possible to the device. Their placement will be discussed in the paragraph below.

Figure 14. Layout suggested board



7.1 Capacitors' placement

Figure 15 shows a recommended placement of capacitors around the device.

Table 6 lists the capacitors used and their corresponding packages.

It is suggested to use the smallest capacitor package size available to ensure their placement to be as close as possible to the XWire12B package. Particular attention must be given to capacitors C_{diff1} , C_{diff2} and C_{diff3} , for which the recommended package is 0402. These capacitors must be placed as close as possible to the device pins (note that ISn+ and ISn- are adjacent pins).

From a layout perspective, minimizing the distance between the pins and the capacitor reduces the trace length, and therefore the series inductance and parasitic capacitance. As a result, overshoot and ringing at the CSA input pins are reduced, and it is more stable, especially in case of fast transients on the measurement line.

Proximity to the pins and a symmetrical connection between ISn+ and ISn- further improve common-mode rejection. High frequency noise coupled onto the lines is locally bypassed by the capacitor, forming a very small loop. This reduces both the noise seen by the CSA and EMI emissions. Consequently, the current measurement is cleaner and more accurate, with less error due to switching noise.

Using a 0402 package for C_{diffn} ($n=1,2,3$) further reduces inductance and occupied area:

- The component is physically small, so the connections to the device pins can be extremely short;
- The self-inductance of the capacitor and its connections is lower than that of the larger package (0603, 0805), making it more effective at high frequencies.

Figure 15. Suggested components placement

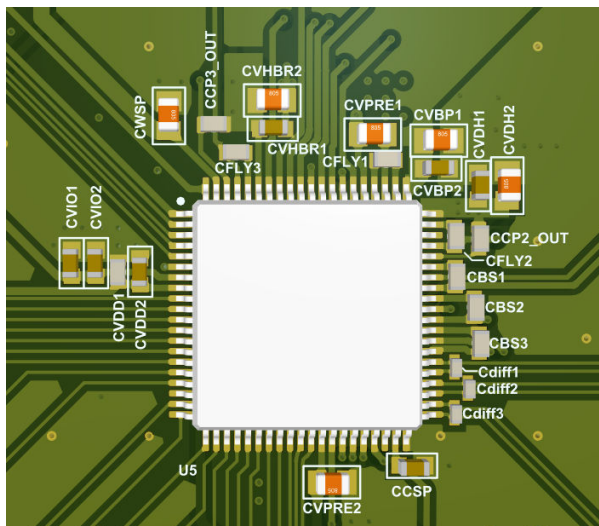


Table 6. Capacitors vs package

Capacitor name	Package
CWSP, CVHBR2, CVPRE1, CVBP1, CVDH2, CVPRE2	0805
CCP3_OUT, CFLY3, CFLY1, CCP2_OUT, CFLY2, CBS1, CBS2, CBS3, CVDD1, CVIO1, CVIO2, CVDD2, CCSP, CVHBR1, CVDH1	0603
Cdiff1, Cdiff2, Cdiff3	0402

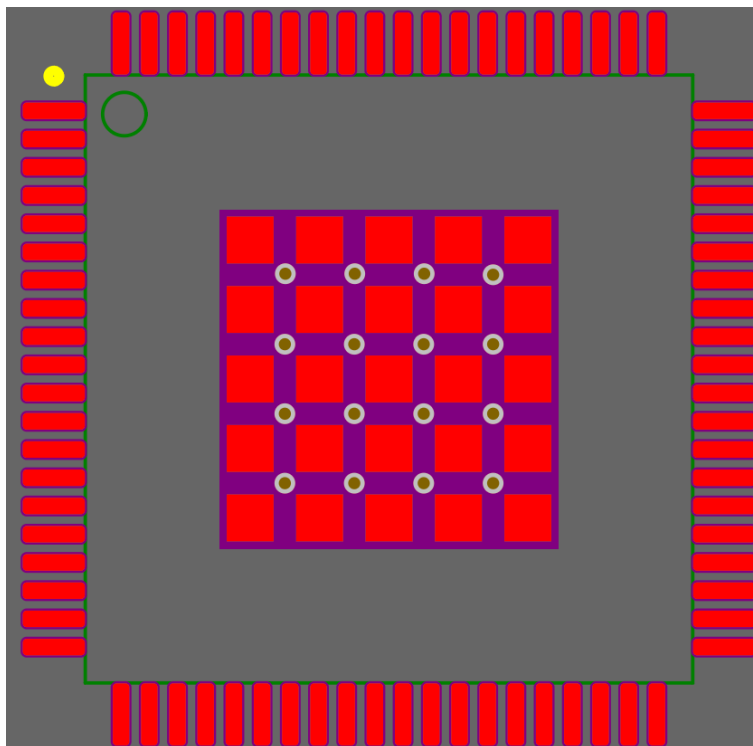
7.2 Suggested device footprint

In Figure 16 is reported a suggested device footprint.

The central area below the exposed pad is composed of a matrix of smaller copper areas connected to GND. This design avoid excessive solder paste deposition during PCB assembly process and provides effective thermal dissipation of the device through the underlying ground plane.

For details of the dimensions of the thermal vias and thermal pads, refer to the suggested land pattern in the datasheet dedicated chapter.

Figure 16. Suggested device footprint



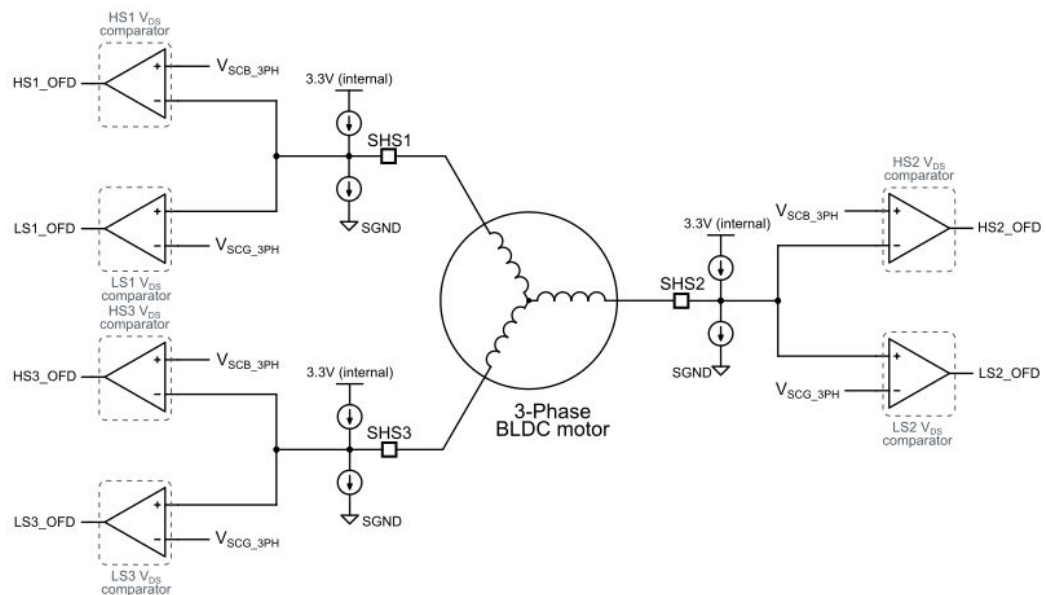
8 Off state diagnosis (OFD)

8.1 3-Phase OFD

XWire12B implements a monitoring unit to detect failure condition affecting the 3-phase load during the half bridges tristate condition ($V_{GHSn}-V_{SHSn}=0V$ and $V_{GLSn}-V_{SLSn}=0V$). Load failure mode detection:

- Open load at one of the SHSn terminals;
- Short-circuit to ground at one or multiple SHSn terminals;
- Short-circuit to battery at one or multiple SHSn terminals.

Figure 17. 3PH-OFD simplified block diagram



The off-state diagnosis unit is composed by a multiple forcing stages and a multiple monitor stages.

The forcing stage has the purpose of driving the state of each SHSn terminal into a predetermined voltage condition, any deviation from this condition is then detected by the monitor stage and interpreted as a faulty condition.

Forcing stage is composed by a protected controlled pull-up/pull-down current source for each phase respectively towards internal supply and SGND.

The monitor stage is composed by LS VDS and the HS VDS comparators which compare the n-th phase voltage respectively with V_{SCB_3PH} and V_{SCG_3PH} fixed thresholds, and each comparator output status is echoed in internal SPI register (HSn_OFD and LSn_OFD , with $n=1, 2, 3$). In case of fault at least one VDS comparator's output is set low, and the OFD_SERV_FAIL fault flag is set and latched until the failure condition is removed and the flag is cleared by SPI command.

By default, the diagnosis is disabled. To activate the diagnosis, user can choose the configuration as summarized in Table 7 and it is important to have $INLn/INHn=0$ [$n=1, 2, 3$], $HSn_OFF_FAIL=LSn_OFF_FAIL=0$ and ASC pin low.

To work properly, the correct configuration is one pull-up and two pull-downs are enabled. If this enabling condition is violated the $OFD_CFG_SERV_ERR$ flag is set until the diagnosis is disabled or correctly configured.

Once enabled, the OFD circuit is stopped as soon as a 0→1 transition of $INHn/INLn$ is detected.

Once the OFD_SERV_FAIL fault flag is set, the microcontroller shall read the HSn_OFD and LSn_OFD while the diagnosis is still active to evaluate the actual fault according to the example in Table 8:

Table 7. 3PH-OFD configuration bits

SERV_BRK-OFDn_EN1	SERV_BRK-OFDn_EN0	Description
0	0	Off State diagnosis disabled (Default)
0	1	Pull-up current enabled, pull-down current disabled
1	0	Pull-down current enabled, pull-up current disabled
1	1	Off-State Diagnosis disabled

Table 8. 3PH-OFD fault evaluation example

SERV_BRK-OFD_EN[1:0]	Comparator flag	Fault description
OFD1=10 (pull-down) OFD2=01 (pull-up) OFD3=10 (pull-down)	HS1_OFD=1 HS2_OFD=1 HS3_OFD=1 LS1_OFD=1 LS2_OFD=1 LS3_OFD=1	No fault
	HS1_OFD=1 HS2_OFD=1 HS3_OFD=1 LS1_OFD=0 LS2_OFD=0 LS3_OFD=0	Short to ground on one or multiple motor phase
	HS1_OFD=0 HS2_OFD=0 HS3_OFD=0 LS1_OFD=1 LS2_OFD=1 LS3_OFD=1	Short to battery on one or multiple motor phase
	HS1_OFD=1 HS2_OFD=1 HS3_OFD=1 LS1_OFD=0 LS2_OFD=1 LS3_OFD=1	Open connection on motor phase 1 (SHS1)
	HS1_OFD=1 HS2_OFD=0 HS3_OFD=1 LS1_OFD=0 LS2_OFD=1 LS3_OFD=0	Open connection on motor phase 2 (SHS2)
	HS1_OFD=1 HS2_OFD=1 HS3_OFD=1 LS1_OFD=1	Open connection on motor phase 3 (SHS3)

SERV_BRK-OFD_EN[1:0]	Comparator flag	Fault description
OFD1=10 (pull-down)	LS2_OFD=1	Multiple faults
OFD2=01 (pull-up)	LS3_OFD=0	
OFD3=10 (pull-down)	Other combinations	

Table 9 provides an example of OFD register configurations with the following configuration: pull up current enabled on phase 1, pull down current enabled on phase 2 and phase 3.

Table 9. 3PH-OFD register configuration (example)

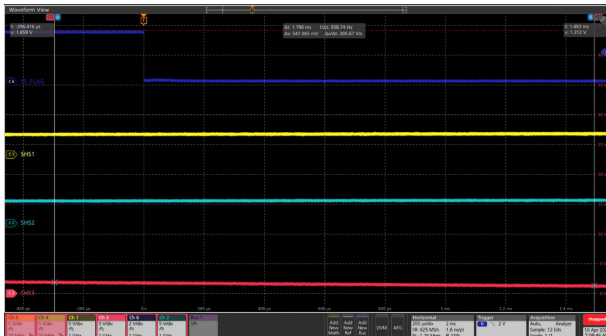
# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
1	Enter Normal mode			Refer to Section 9.
2	CONFIG mode access (first unlock frame)	0x31	0x55	Enter in configuration mode by writing two SPI frames.
3	CONFIG mode access (second unlock frame)	0x31	0x33	
4	Enable 3 ph actuation	0x0A	0x00	
5	OFD configuration	0x13	0x9A	Pull up current enabled on phase 1, pull-down current enabled on phase 2 and phase3.
6	CONFIG mode exit	0x31	0xAA	
7	Clear all faults			Refer to Section 9.
8	Pull EN_3PH=1			Pin driving
9	Read STATUS8	0x3F		Read STATUS8 to verify the presence/absence of OFD configuration error and/or faults.

Table 10 contains some snapshots from the oscilloscope with the previously mentioned register configuration.

Table 10. 3PH-OFD oscilloscope results

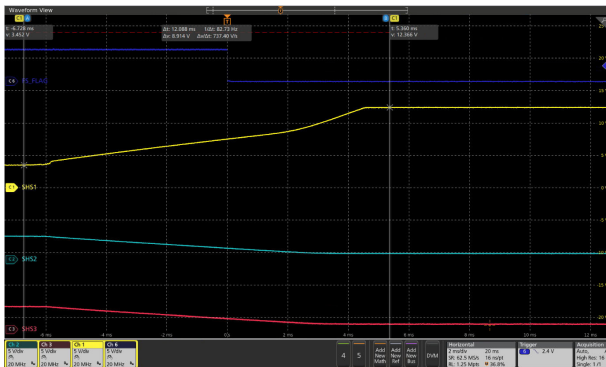
Ch1 SHS1, Ch2 SHS2, Ch3 SHS3, Ch6 FS_FLAG																
	This is the right configuration: 1 pull up current and 2 pull-down currents is the correct one. Voltage levels of all three phases are: 3.3 V no faults detected.															
	<table> <tr> <td>OFD_CFG_SERV_ERR</td><td>0</td></tr> <tr> <td>OFD_SERV_FAIL</td><td>0</td></tr> <tr> <td>HS1_OFD</td><td>1</td></tr> <tr> <td>HS2_OFD</td><td>1</td></tr> <tr> <td>HS3_OFD</td><td>1</td></tr> <tr> <td>LS1_OFD</td><td>1</td></tr> <tr> <td>LS2_OFD</td><td>1</td></tr> <tr> <td>LS3_OFD</td><td>1</td></tr> </table>	OFD_CFG_SERV_ERR	0	OFD_SERV_FAIL	0	HS1_OFD	1	HS2_OFD	1	HS3_OFD	1	LS1_OFD	1	LS2_OFD	1	LS3_OFD
OFD_CFG_SERV_ERR	0															
OFD_SERV_FAIL	0															
HS1_OFD	1															
HS2_OFD	1															
HS3_OFD	1															
LS1_OFD	1															
LS2_OFD	1															
LS3_OFD	1															

Ch1 SHS1, Ch2 SHS2, Ch3 SHS3, Ch6 FS_FLAG



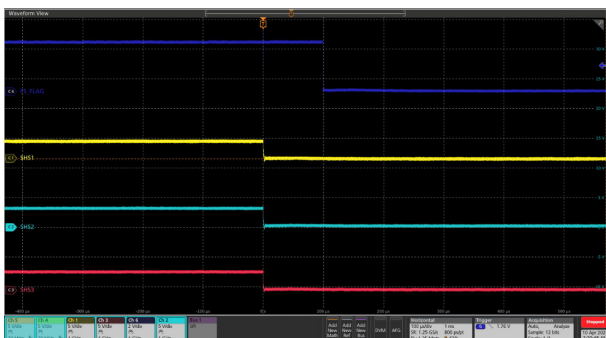
Open connection in phase 3 has been detected.
The voltage level of phase 3 goes from 3.3 V to 0.8 V.

OFD_CFG_SERV_ERR	0
OFD_SERV_FAIL	1
HS1_OFD	1
HS2_OFD	1
HS3_OFD	1
LS1_OFD	1
LS2_OFD	1
LS3_OFD	0



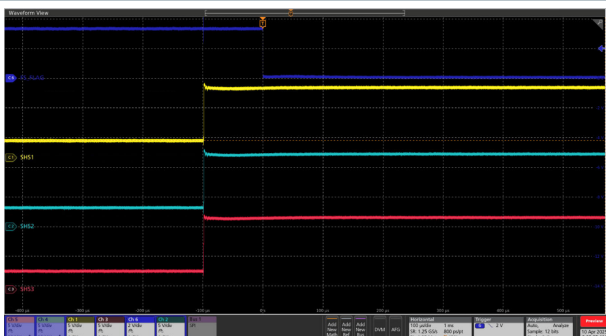
Open connection in phase 1 has been detected.
The voltage level of phase 1 goes from 3.3 V to around 12 V. This is due to the configuration (PU current enabled on phase 1, PD currents enabled on phases 2 and 3).

OFD_CFG_SERV_ERR	0
OFD_SERV_FAIL	1
HS1_OFD	0
HS2_OFD	1
HS3_OFD	1
LS1_OFD	1
LS2_OFD	0
LS3_OFD	0



A short to ground on all three phases has been detected.
Voltage levels of all three phases go from 3.3 V to a few mV.

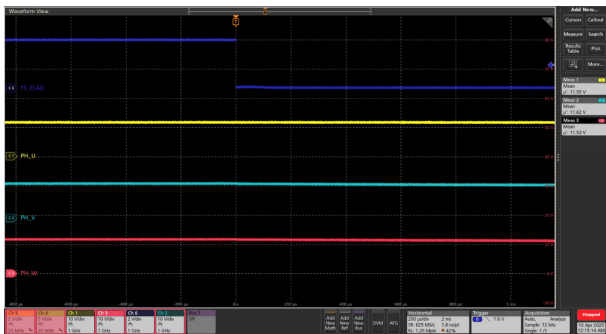
OFD_CFG_SERV_ERR	0
OFD_SERV_FAIL	1
HS1_OFD	1
HS2_OFD	1
HS3_OFD	1
LS1_OFD	0
LS2_OFD	0
LS3_OFD	0



A short to battery on all three phases has been detected.
Voltage levels of all three phases go from 3.3 V to 12 V (VBP).

Ch1 SHS1, Ch2 SHS2, Ch3 SHS3, Ch6 FS_FLAG

OFD_CFG_SERV_ERR	0
OFD_SERV_FAIL	1
HS1_OFD	0
HS2_OFD	0
HS3_OFD	0
LS1_OFD	1
LS2_OFD	1
LS3_OFD	1

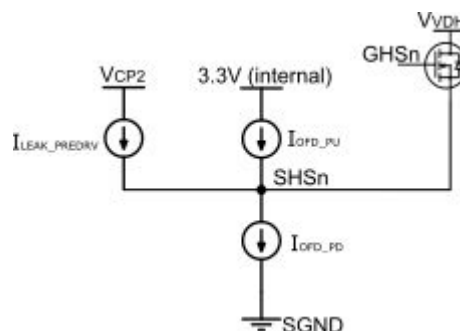


Here, a wrong configuration has been set.

OFD_CFG_SERV_ERR	1
OFD_SERV_FAIL	0
HS1_OFD	1
HS2_OFD	1
HS3_OFD	1
LS1_OFD	1
LS2_OFD	1
LS3_OFD	1

When there is an open condition in the branch where the pull-up has been enabled (see Image 2 of the previous table) it is correct that the final value is almost equal to the battery voltage, this is due to the leakage/bias current of the HS predriver which will pull up the SHS voltage above 3.3 V since it is referred to CP2, and the voltage keeps rising until the body diode of the ext. FET is switched on, clamping the voltage to $V_{BP} + V_F$, where V_F is the diode forward voltage.

Figure 18. 3PH-OFD schematic detail



8.1.1 Minimum resistance value connected on phase nodes

Correct functionality of OFD is based on a current mismatch between pull-up and pull-down current.

To measure the voltage on each motor phase, it is possible to insert a voltage divider on each phase. However, it's important that the equivalent resistance is properly balanced; for example, if the resistance is too low, the node may not charge correctly.

To size the equivalent resistance, use the following formula to be sure that in the worst case no faults appear:

$$Req * I_{OFD PD 3PH max} \geq V_{OFD 3PH NORM MIN} \quad (21)$$

$$Req \geq \frac{2.6 V}{0.9 mA} \approx 2.9 k \Omega \quad (22)$$

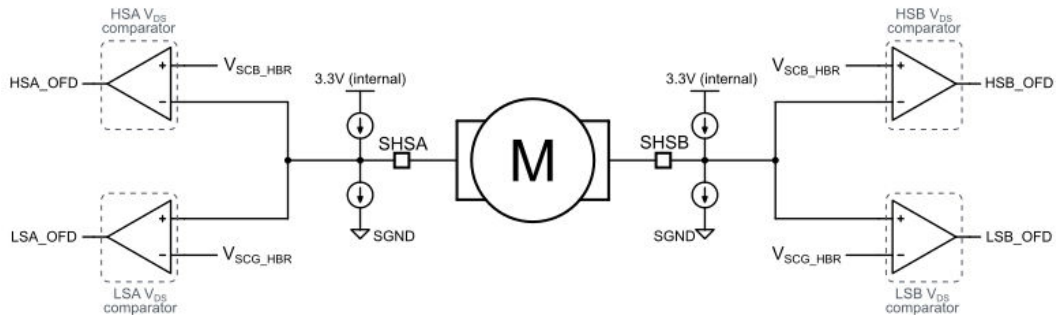
8.2

H-Bridge OFD

XWire12B implements a monitoring unit to detect failure condition affecting the load during the H-Bridge tristate condition ($V_{GHSn}-V_{SHSn}=0V$ and $V_{GLSn}-V_{SLSn}=0V$) when the driver is used for DC-Motor driving. Load failure mode detection:

- Open load at one of the SHSn terminals;
- Short-circuit to ground at one SHSn terminals;
- Short-circuit to battery at one SHSn terminals.

Figure 19. HBR-OFD simplified block diagram



The off-state diagnosis unit is composed by a multiple forcing stages and a multiple monitor stages.

By default, the diagnosis is disabled. To activate the diagnosis, user can choose the configuration as summarized in Table 11 and it is important to have $INLn/INHn=0$ [$n=A, B$] and $HSn_OFF_FAIL=LSn_OFF_FAIL=0$.

To work properly, the diagnosis shall be configured as one pull-up and one ull-down enabled. If this enabling condition is violated the `OFD_CFG_PARK_ERR` flag is set until the diagnosis is disabled or correctly configured.

Once enabled, the HBR-OFD circuit is stopped as soon as a $0 \rightarrow 1$ transition of $INHn/INLn$ is detected.

Once the `OFD_SERV_FAIL` fault flag is set, the microcontroller shall read the `HSn_OFD` and `LSn_OFD` while the diagnosis is still active to evaluate the actual fault according to the example in Table 12:

Table 11. HBR-OFD configuration bits

PARK_BRK-OFDn_EN1	PARK_BRK-OFDn_EN0	Description
0	0	Off State diagnosis disabled (Default)
0	1	Pull-up current enabled, pull-down current disabled
1	0	Pull-down current enabled, pull-up current disabled
1	1	Off-State Diagnosis disabled

Table 12. 3PH-OFD fault evaluation example

PARK_BRK-OFD_EN[1:0]	Error flag	Description
OFDA=10 (pull-down) OFDB=01 (pull-up)	HSA_OFD=1 HSB_OFD=1 LSA_OFD=1 LSB_OFD=1	No fault
	HSA_OFD=1 HSB_OFD=1 LSA_OFD=0 LSB_OFD=0	Short to ground on one or both motor phases
	HSA_OFD=0 HSB_OFD=0 LSA_OFD=1	Short to battery on one or both motor phases

PARK_BRK-OFD_EN[1:0]	Error flag	Description
OFDA=10 (pull-down) OFDB=01 (pull-up)	LSB_OFD=1	Open connection on one or more motor phase
	HSA_OFD=1	
	HSB_OFD=1	
	LSA_OFD=0	
	LSB_OFD=1	
	Other combinations	Multiple faults

Table 13 provides an example of OFD register configurations with the following configuration: pull up current enabled on phase B, pull-down current enabled on phase A.

Table 13. HBR-OFD register configuration (example)

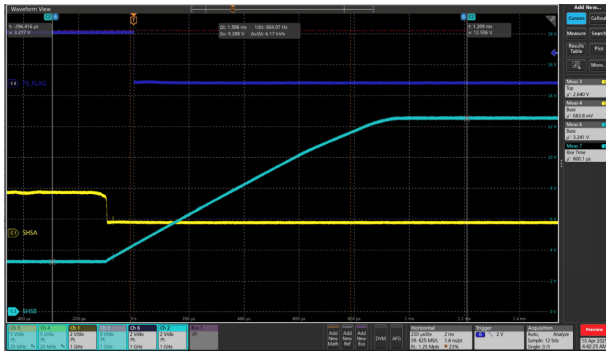
# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
1	Enter Normal mode			Refer to Section 9 .
2	CONFIG mode access (first unlock frame)	0x31	0x55	Enter in configuration mode by writing two SPI frames.
3	CONFIG mode access (second unlock frame)	0x31	0x33	
4	Enable HBR actuation	0x0E	0x00	
5	OFD configuration	0x17	0x29	Pull up current enabled on phase B, pull-down current enabled on phase A
6	CONFIG mode exit	0x31	0xAA	
7	Clear all faults			Refer to Section 9 .
8	Pull EN_HBR=1			Pin driving
9	Read STATUS8	0x3F		Read STATUS8 to verify the presence/absence of OFD configuration error and/or faults.

Table 14 contains some snapshots from the oscilloscope with the previously mentioned register configuration.

Table 14. HBR-OFD oscilloscope results

Ch1 SHSA, Ch2 SHSB, Ch6 FS_FLAG												
	This is the right configuration: 1 pull up current and 1 pull-down currents is the correct one. Voltage levels of SHSA and SHSB are: 3.3 V. No faults detected.											
	<table> <tr> <td>OFD_CFG_PARK_ERR</td><td>0</td></tr> <tr> <td>OFD_PARK_FAIL</td><td>0</td></tr> <tr> <td>HSA_OFD</td><td>1</td></tr> <tr> <td>HSB_OFD</td><td>1</td></tr> <tr> <td>LSA_OFD</td><td>1</td></tr> <tr> <td>LSB_OFD</td><td>1</td></tr> </table>	OFD_CFG_PARK_ERR	0	OFD_PARK_FAIL	0	HSA_OFD	1	HSB_OFD	1	LSA_OFD	1	LSB_OFD
OFD_CFG_PARK_ERR	0											
OFD_PARK_FAIL	0											
HSA_OFD	1											
HSB_OFD	1											
LSA_OFD	1											
LSB_OFD	1											

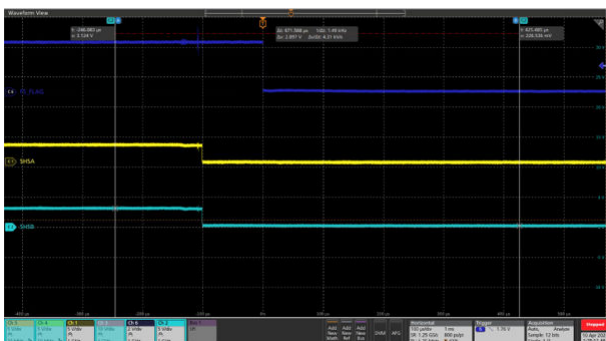
Ch1 SHSA, Ch2 SHSB, Ch6 FS_FLAG



Open connection has been detected.
Voltage on SHSA goes to few mV (0.68 V), while on SHSB goes to around 12 V. This is due to the configuration (PU current enabled on phase B, PD current enabled on phase A).

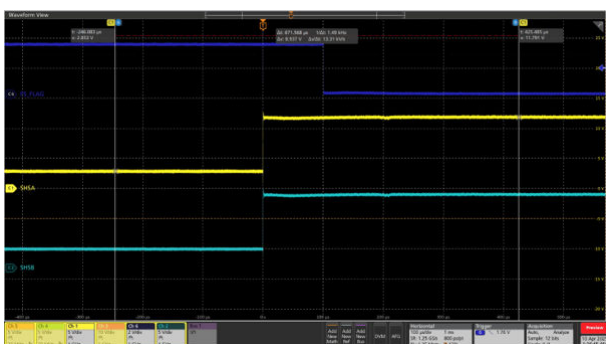
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{OFD_HBR_OPEN}$	OFD open load voltage in pd mode	PARK_BRK-OFDn-EN=10. SHSn= No load			0.9	V

OFD_CFG_PARK_ERR	0
OFD_PARK_FAIL	1
HSA_OFD	1
HSB_OFD	1
LSA_OFD	0
LSB_OFD	1



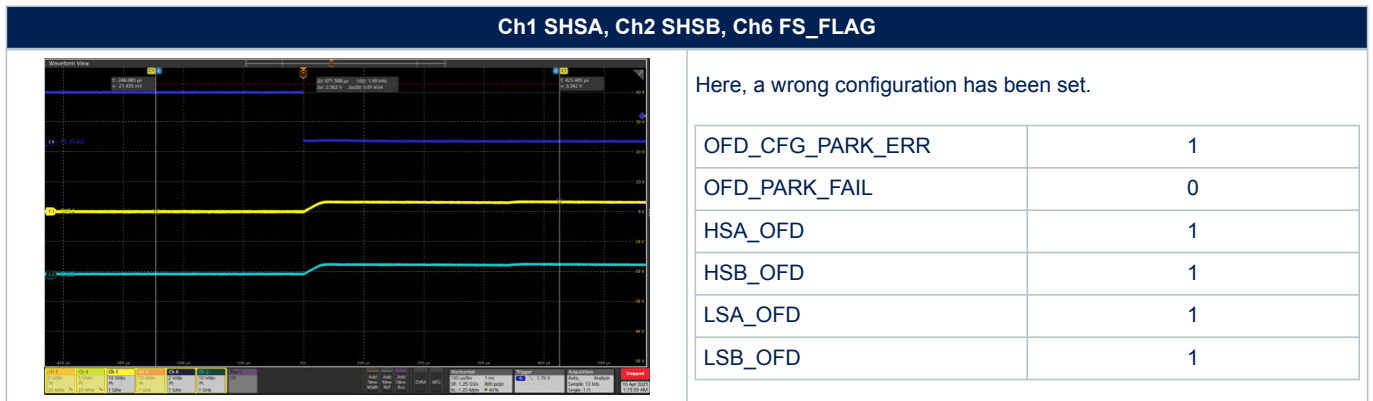
A short to ground on phase A and B has been detected.
Voltage levels of all two phases go from 3.3 V to few mV.

OFD_CFG_PARK_ERR	0
OFD_PARK_FAIL	1
HSA_OFD	1
HSB_OFD	1
LSA_OFD	0
LSB_OFD	0



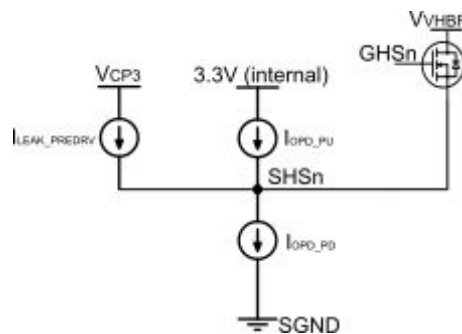
A short to battery on phase A and B has been detected.
Voltage levels of phase A and B go from 3.3 V to 12 V (VBP).

OFD_CFG_PARK_ERR	0
OFD_PARK_FAIL	0
HSA_OFD	0
HSB_OFD	0
LSA_OFD	1
LSB_OFD	1



When there is an open condition in the branch where the pull-up has been enabled (see image 2 of the previous table) it is correct that the final value is almost equal to the battery voltage, this is due to the leakage/bias current of the HS predriver which will pull up the SHS voltage above 3.3 V since it is referred to CP3, and the voltage keeps rising until the body diode of the ext. FET is switched on, clamping the voltage to $V_{BP} + V_F$, where V_F is the diode forward voltage.

Figure 20. HBR-OFD schematic detail



8.2.1 Minimum resistance value connected on phase nodes

Correct functionality of OFD is based on a current mismatch between pull-up and pull-down current.

To measure the voltage on each motor phase, it is possible to insert a voltage divider on each phase. However, it's important that the equivalent resistance is properly balanced; for example, if the resistance is too low, the node may not charge correctly.

To size the equivalent resistance, use the following formula to be sure that in the worst case no faults appear:

$$Req * I_{OFD PD HBR max} \geq V_{OFD HBR NORM min} \quad (22)$$

$$Req \geq \frac{2.6 V}{0.9 mA} \approx 2.9 k\Omega \quad (23)$$

9 Startup guidelines

The following table contains the typical steps for the XWire12B initial configuration.

Table 15. Startup procedure

# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
1	Pull NDIS=1			Pin driving
2	Read STATUS1	0x38		Read all status registers: from STATUS1 to STATUS9 and WSI_HS_STATUS (1 to 4), WSI_LS_STATUS (1 to 2).
3	Read STATUS2	0x39		
4	Read STATUS3	0x3A		
5	Read STATUS4	0x3B		
6	Read STATUS5	0x3C		
7	Read STATUS6	0x3D		
8	Read STATUS7	0x3E		
9	Read STATUS8	0x3F		
10	Read STATUS9	0x40		
11	Read WSI_LS_STATUS2	0x2E		
12	Read WSI_LS_STATUS1	0x2D		
13	Read WSI_HS_STATUS1	0x26		
14	Read WSI_HS_STATUS2	0x27		
15	Read WSI_HS_STATUS3	0x28		
16	Read WSI_HS_STATUS4	0x29		
17	CONFIG mode access (first unlock frame)	0x31	0x55	Enter in configuration mode by writing two SPI frames.
18	CONFIG mode access (second unlock frame)	0x31	0x33	
19	Enable 3 ph actuation	0x0A	0x00	
20	Enable HBR actuation	0x0E	0x00	
21	CONFIG mode exit	0x31	0xAA	
22	Pull EN_3PH=1			Pin driving
23	Pull EN_HBR=1			Pin driving
24	Wait 5 ms			
25	Clear status register			
24	CONFIG mode ⁽¹⁾ access (first unlock frame)	0x31	0x55	Enter in configuration mode by writing two SPI frames.
25	CONFIG mode access (second unlock frame)	0x31	0x33	

# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
26	BST_PRECHARGE=1	0x0A	0x10	To activate the bootstrap precharge routine, see paragraph 5.10.6.2 in the datasheet.
27	CONFIG mode exit	0x31	0xAA	

1. The configuration shall be ended within 100 ms from the unlock procedure.

In case of failsafe switches driven by CP2 and CP3 as described in [Section 6](#), the following configuration must be added between step 18 and step 19 to allow the device to enter Normal mode even if VHBR and VDH undervoltage are detected.

Table 16. VDH_UV and VHBR_UV configuration for startup

# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
1	VHBR_UV_REACT_CFG=11	0x01	0x19AD	
2	VDH_UV_REACT_CFG=11	0x02	0x6AB7	

Then, after step 26, the two registers must be reconfigured to the desired value for the application.

Table 17. VDH_UV and VHBR_UV configuration for the application

# step	Description	SPI frame		Comment
		Reg [hex]	Data [hex]	
1	VHBR_UV_REACT_CFG=00	0x01	0x183F	Reverted to default value (0b00)
2	VDH_UV_REACT_CFG=00	0x02	0xAA9	Reverted to default value (0b00)

Revision history

Table 18. Document revision history

Date	Version	Changes
16-Oct-2026	1	Initial release.

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