# Motor control Discovery kit with STM32G564QE MCU

## Introduction

The B-G564E-MC1S Discovery kit is part of the motor control development platform supporting ZeST and HSO algorithms. The B-G564E-MC1S is a control board with the STM32G564QET3 microcontroller in the ZeST Discovery pack and works together with a power board such as STEVAL-LVLP01, an optional adaptor board such as B-ZEST-ADAPT1, and an accessory package such as B-MOTOR-PMSMA1. The B-G564E-MC1S Discovery kit integrates two terminal block connectors for easy evaluation of the POSENC feature.

The B-G564E-MC1S Discovery kit is connected to the power or adaptor board through an embedded motor control V2 connector. It can also support motor driver expansion boards such as X-NUCLEO-IHM07M1, X-NUCLEO-IHM08M1, X-NUCLEO-IHM09M1, X-NUCLEO-IHM09M2, and X-NUCLEO-IHM16M1 via the ST morpho connector.

The B-G564E-MC1S Discovery kit enables two POSENC functions that interface with EnDat 3 and HIPERFACE DSL® protocols in 2-wire and 4-wire modes, with onboard RS-485 transceivers, and associated circuitry.

STLINK-V3EC is integrated into the board, as an embedded in-circuit debugger and programmer for the STM32 MCU and the USB Virtual COM port bridge.

The STM32 ZeST algorithm is available for selected users only.

**Figure 1. B-G564E-MC1S top view**

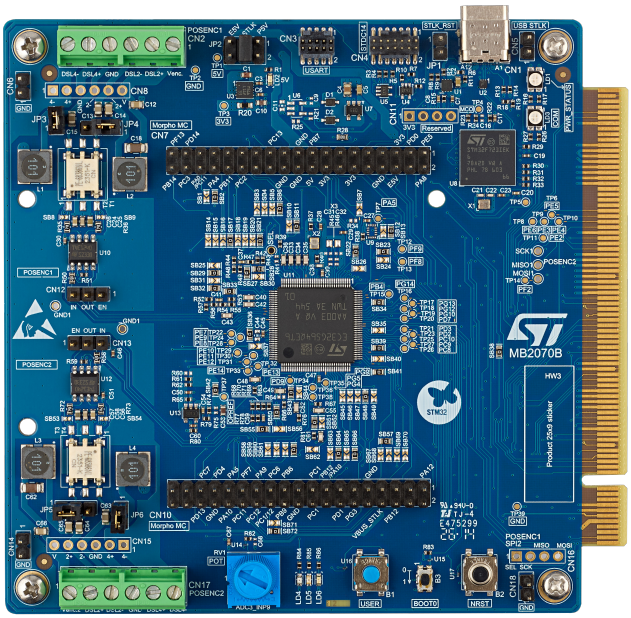
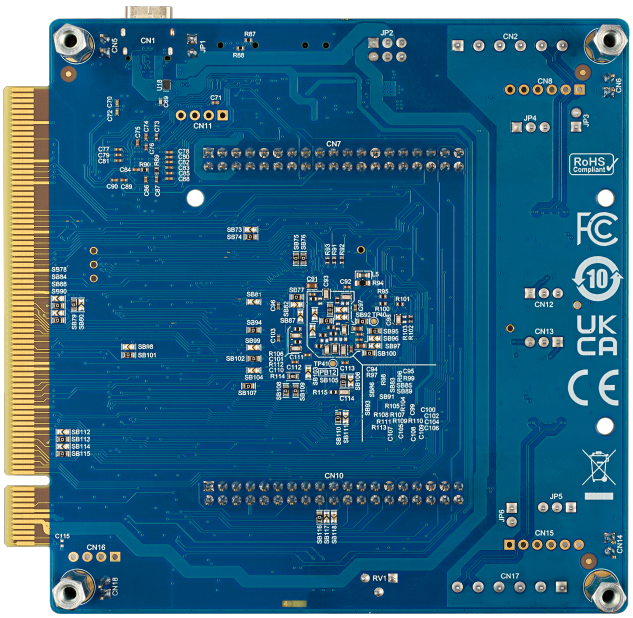


**Figure 2. B-G564E-MC1S bottom view**



*Picture is not contractual.*

# 1 Features

- STM32G564QET3 microcontroller based on the Arm® Cortex®-M33 core, featuring 512 Kbytes of flash memory and 112 Kbytes of SRAM, in an LQFP128 package
- Three user LEDs
- Three push-buttons (user/tamper, reset, and boot mode)
- Potentiometer for ADC
- Board connectors:
  - STLINK-V3EC USB Type-C® connector
  - Motor control V2 connector
  - Position encoder interface with two POSENC terminal blocks for EnDat 3 and HIPERFACE DSL® protocols
  - STDC14 and USART debug port
  - ST morpho motor control
- Flexible power-supply options: 5 V from motor control V2 connector, STLINK-V3EC USB Type-C® $V_{BUS}$, or 5 V external source from ST morpho connector
- On-board STLINK-V3EC debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeG5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE
- Part of STM32 motor control ecosystem with X-CUBE-MCSDK motor project configuration tool
- STM32 ZeST algorithm available for selected users only

arm

*Note: Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere.*

*The Arm word and logo are trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All rights reserved.*

# 2 Ordering information

To order the B-G564E-MC1S Discovery kit, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

**Table 1. Ordering information**

| Order code | Board reference | Target STM32 |
|---|---|---|
| B-G564E-MC1S | MB2070 | STM32G564QET3 |

## 2.1 Codification

The meaning of the codification is explained in Table 2.

**Table 2. Codification explanation**

| B-XXYY-Z-MC1S | Description | Example: B-G564E-MC1S |
|---|---|---|
| B | Discovery kit | Discovery kit |
| XX | MCU series in STM32 32-bit Arm Cortex MCUs | STM32G5 series |
| YY | MCU product line in the series | STM32G5x4 product line |
| Z | STM32 flash memory size:<br>• E for 512 Kbytes | 512 Kbytes |
| -MC1S | Application type | Motor control |

# 3 Development environment

## 3.1 System requirements

- Multi-OS support: Windows® 10 or 11, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to USB Type-C® cable

*Note:* *macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.*

*Linux® is a registered trademark of Linus Torvalds.*

*Windows is a trademark of the Microsoft group of companies.*

## 3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

## 3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

## 3.4 EDA resources

All board design resources, including schematics, EDA databases, manufacturing files, and the bill of materials, are available from the B-G564E-MC1S product page at *www.st.com*.

# 4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

**Table 3. ON/OFF convention**

| Convention | Definition |
|---|---|
| Jumper JPx ON | Jumper fitted |
| Jumper JPx OFF | Jumper not fitted |
| Jumper JPx [1-2] | Jumper fitted between pin 1 and pin 2 |
| Solder bridge SBx ON | SBx connections closed by 0 Ω resistor |
| Solder bridge SBx OFF | SBx connections left open |
| Resistor Rx ON | Resistor soldered |
| Resistor Rx OFF | Resistor not soldered |
| Capacitor Cx ON | Capacitor soldered |
| Capacitor Cx OFF | Capacitor not soldered |

# 5 Safety recommendations

## 5.1 Targeted audience

This product targets users with at least basic electronics or embedded software development knowledge like engineers, technicians, or students.

This board is not a toy and is not suited for use by children.

## 5.2 Handling the board

This product contains a bare printed circuit board and like all products of this type, the user must be careful about the following points:

- The connection pins on the board might be sharp. Be careful when handling the board to avoid injury.
- This board contains static sensitive devices. To avoid damaging it, handle the board in an ESD-proof environment.
- While powered, do not touch the electric connections on the board with your fingers or anything conductive. The board operates at a voltage level that is not dangerous, but components might be damaged when shorted.
- Do not put any liquid on the board and avoid operating it close to water or at a high humidity level.
- Do not operate the board if it is dirty or dusty.
- The pins of the board are exposed and must not come into contact with a metal surface, as this can produce a short circuit and damage the board.

## 5.3 Delivery recommendations

Before the first use, inspect the board for any damage that may have occurred during shipment. Ensure that all socketed components are securely fixed in their sockets and that nothing is loose in the plastic bag.

## 5.4 Power supply

This equipment must be powered by a power supply unit or auxiliary equipment that complies with EN 62368-1:2014+A11:2017, or a replacement standard, and that provides safety extra-low voltage (SELV/ES1) with limited power capability (LPS/PS2).

# 6 Quick start

Before installing and using the product, accept the evaluation product license agreement from the *www.st.com/epla* webpage. For more information on the B-G564E-MC1S Discovery kit and for the demonstration software example, visit the *www.st.com/B-G564E-MC1S* webpage.

## 6.1 Getting started

Follow the sequence below to configure the B-G564E-MC1S Discovery kit and explore different applications (refer to Figure 3 and Figure 4 for component location).

1. For the correct identification of all the device interfaces from the host PC and before connecting the kit, install the STLINK-V3EC USB driver available as described in the technical note *Overview of ST-LINK derivatives* (TN1235).
2. Check the jumper position on the board: JP1 is OFF, JP2 is set on STLK, JP3 and JP4 are ON, JP4 and JP5 are ON (pins 1-2).
3. Connect the B-G564E-MC1S Discovery kit to a PC with a USB cable (USB Type-C® to USB Type-C®) through the STLINK-V3EC USB connector (CN1) to power the board.
4. The 5 V LED (LD2), the COM LED (LD3), and the PWR_STATUS LED (LD1) lights up.
5. The green LED (LD6), red LED (LD5), and yellow LED (LD4) are scrolling, indicating the default software demo application has started. The application software and its user manual, as well as other software examples for exploring STM32G5 features are available at B-G564E-MC1S.
6. Develop a custom application using the available examples.

## 6.2 Default board configuration

**Table 4. Default jumper configuration**

| Jumper | Function | Default setting | Comment |
|---|---|---|---|
| JP1 | STLINK reset | **OFF** | STLINK-V3EC MCU not under RESET mode |
| JP2 | 5 V power source selection | **[3-4]** | 5 V power supply from ST-LINK USB |
| JP3 | POSENC1 EnDat 3 configuration | **ON** | 470 nF capacitor bypassed |
| JP4 | POSENC1 EnDat 3 configuration | **[1-2]** | Capacitor choice (100 nF connected) |
| JP5 | POSENC2 EnDat 3 configuration | **[1-2]** | Capacitor choice (100 nF connected) |
| JP6 | POSENC2 EnDat 3 configuration | **ON** | 470 nF capacitor bypassed |

# 7 Hardware layout and configuration

## 7.1 Hardware layout

B-G564E-MC1S Discovery kit is designed around the STM32G564QET3 microcontroller. The hardware block diagram in Figure 3 illustrates the connections between the microcontroller and the peripherals. Figure 4 shows where these peripherals are located on the board.

**Figure 3. B-G564E-MC1S block diagram**

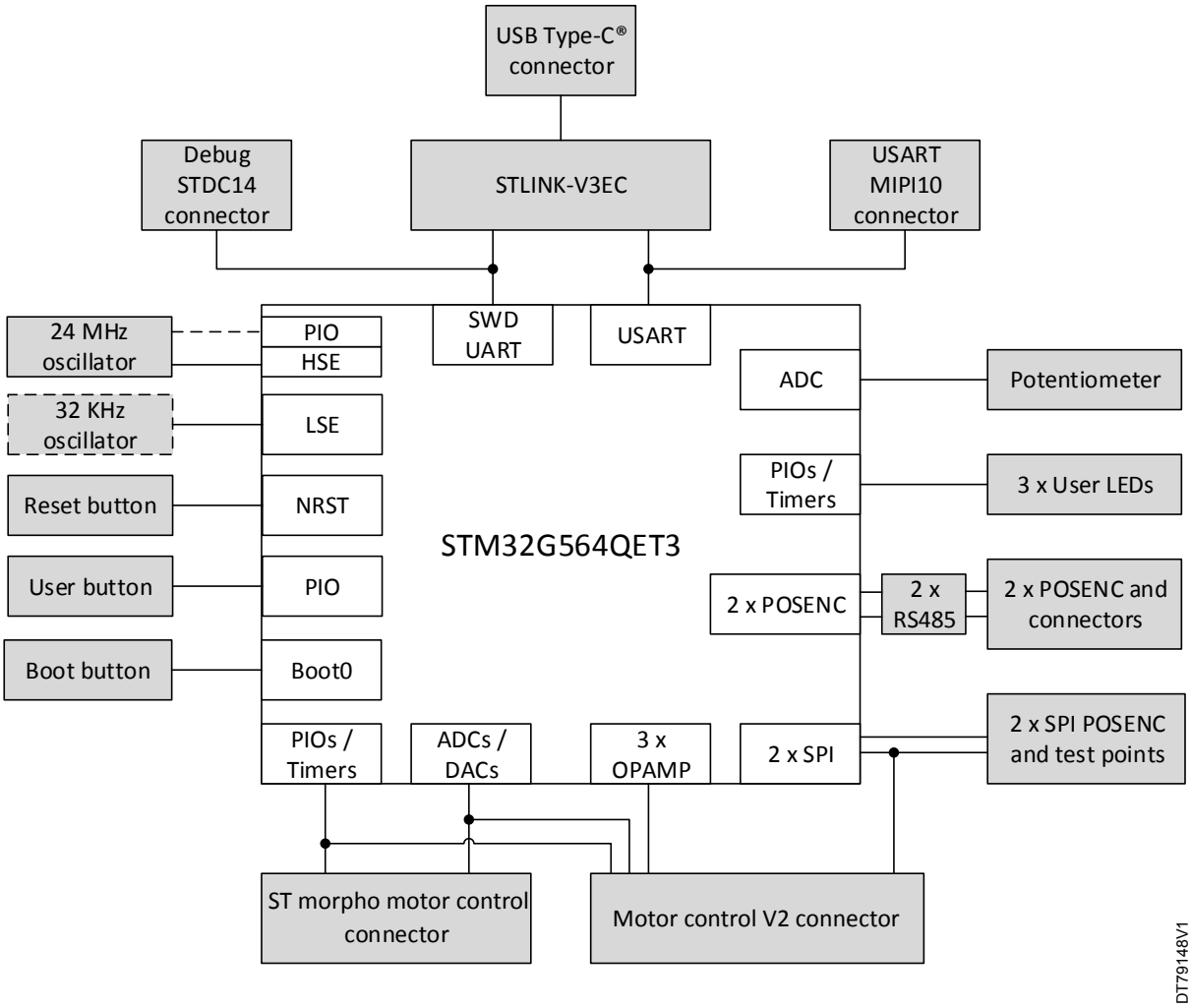
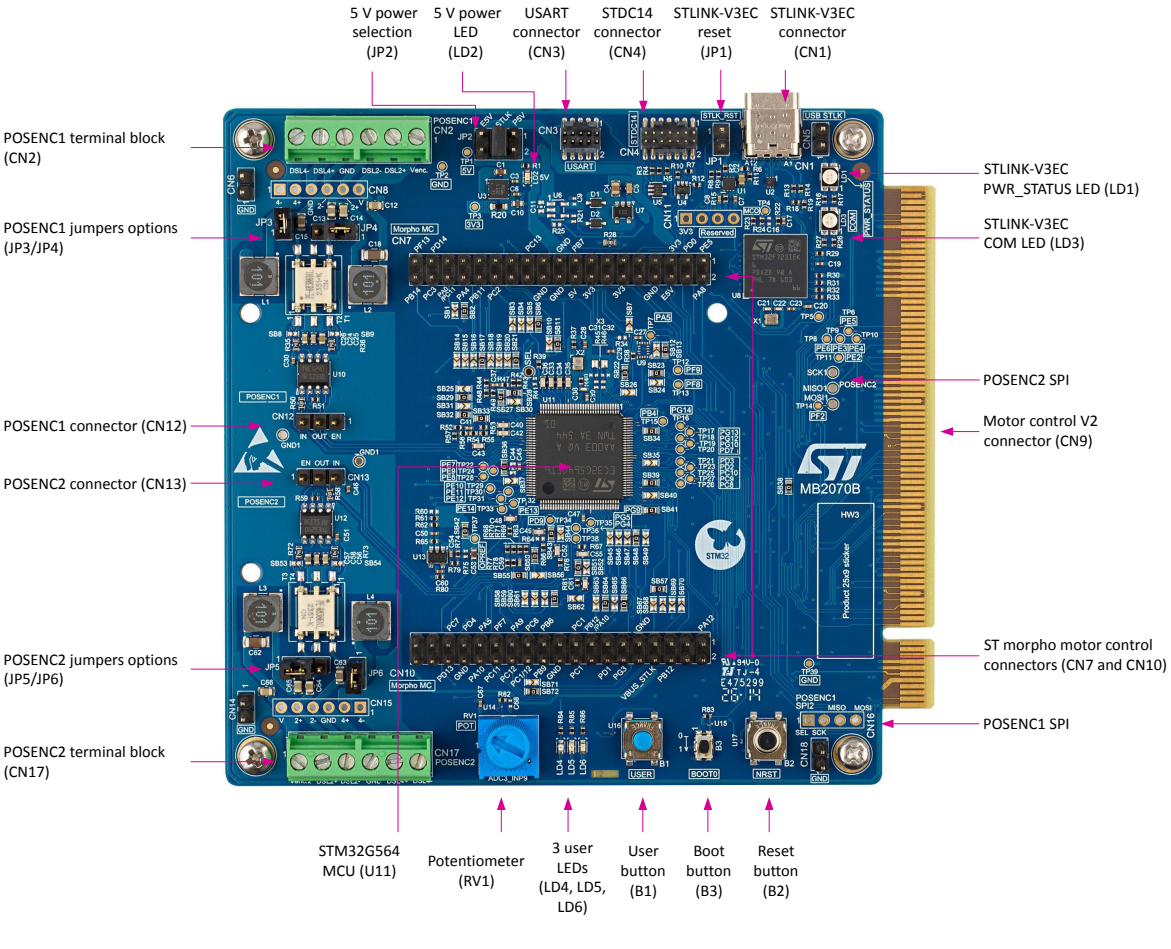


**Figure 4. B-G564E-MC1S board layout (top view)**



## 7.2 Mechanical dimensions

Figure 5. **B-G564E-MC1S mechanical drawing top layout**

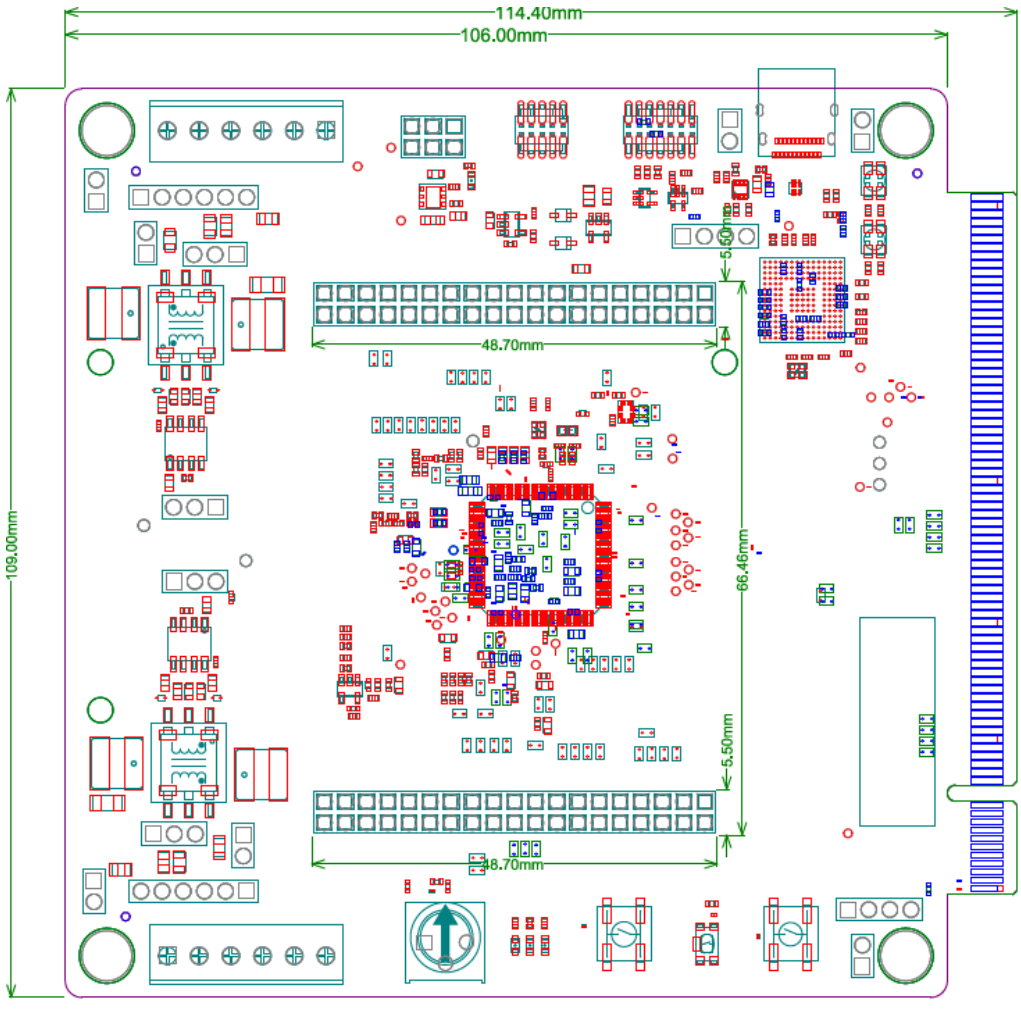
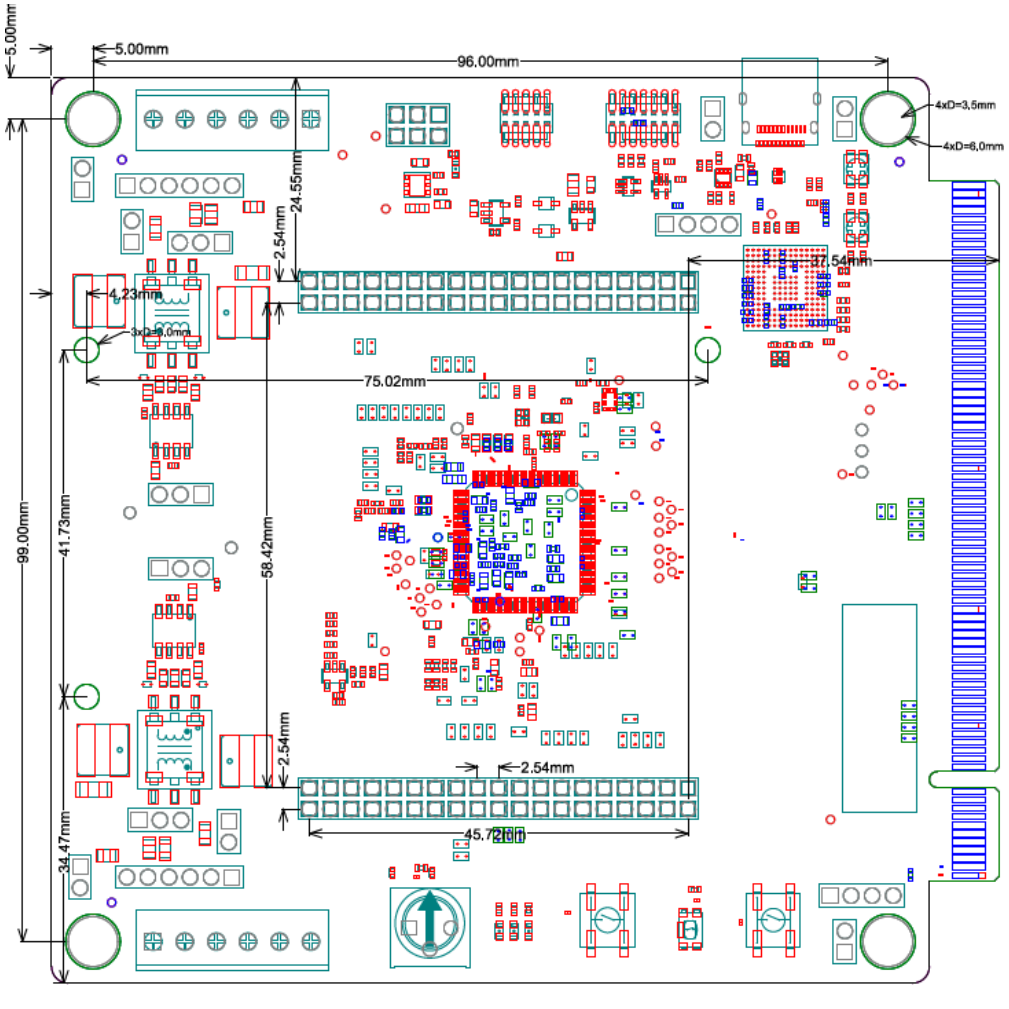


Figure 6. **B-G564E-MC1S mechanical drawing bottom layout**




## 7.3 Embedded STLINK-V3EC

This section provides information about the implementation of the embedded STLINK-V3EC on the B-G564E-MC1S Discovery kit.

For further details on ST-LINK capabilities, LED management, and driver and firmware for STLINK-V3EC, refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

For more information about the debugging and programming features of STLINK-V3EC, refer to the user manual *STLINK-V3SET debugger/programmer for STM8 and STM32* (UM2448).

### 7.3.1 Description

There are three different ways to program and debug the onboard STM32G564QET3 MCU:

1. Using the embedded STLINK-V3EC (CN1)
2. Using an external probe connected to the STDC14 connector (CN4)
3. Using an external probe connected to the USART connector (CN3) for the second USART Virtual COM port (VCP)

The STLINK-V3EC facility STDC14 for debugging and programming is integrated in this B-G564E-MC1S Discovery kit.

The embedded STLINK-V3EC supports only SWD and VCP for STM32 devices.

Features supported in STLINK-V3EC:

- 5 V power supplied by the USB Type-C® connector (CN1), with 1.5 A budget limit
- USB 2.0 high-speed compatible interface
- Serial Wire Debug (SWD) and VCP (UART) interfaces, 3.3 V
- Second USART connector (CN3) for external connection
- STDC14 debug connector (CN4)
- Tricolor (green, orange, and red) COM status LED (LD3) that provides information about communication status with the PC
- Tricolor (green, orange, and red) power status LED (LD1) that provides information about the STLINK-V3EC target power

*Note: For a summary of all debug/program/trace or other interface capabilities, refer to Section 8.3.*

Table 5 describes the STLINK-V3EC interface with STM32G564QE:

**Table 5. STLINK-V3EC interface with STM32G564QE**

| STLINK-V3EC signal name | STM32G564QE pin | Function |
|---|---|---|
| T_SWCLK | PA14 | SWCLK / JTCK |
| T_SWDIO | PA13 | SWDIO / JTMS |
| T_SWO | PB3 | SWO / JTDO, as option |
| T.JTDI | - | JTDI (not used by default), on TP5 |
| STLK_VCP_RX | PC15 | UART5_TX bootloader (480 kBaud max.) |
| STLK_VCP_TX | PC14 | UART5_RX bootloader (480 kBaud max.) |
| Bridge_USART_RX | PD5 | USART2_TX (no boot) |
| Bridge_USART_TX | PD6 | USART2_RX (no boot) |
| MCO | - | MCO (not used by default), on TP4 |
| T_NRST/PA6 | NRST | Board reset |

**Table 6. Solder bridge configuration for STLINK-V3EC**

| I/O | Bridge | Setting(1) | Comment |
|---|---|---|---|
| PC15 – OSC32_OUT | SB76 | **ON** | **PC15 is used as UART5_TX, it is connected to DBG_VCP1_TX (bootloader support).** |
| | | OFF | PC15 is NOT connected to DBG_VCP1_TX.<br>PC15 may be used to connect to an external 32.768 kHz oscillator (not populated by default, connect R46) |
| PC14 – OSC32_IN | SB75 | **ON** | **PC14 is used as UART5_RX, it is connected to DBG_VCP1_RX (bootloader support).** |
| | | OFF | PC14 is NOT connected to DBG_VCP1_RX.<br>PC14 may be used to connect to an external 32.768 kHz oscillator (not populated by default, connect R47) |
| PB3 | SB81 | **OFF** / ON | **PB3 is not connected to SWO** / contrary |
| | SB34 | **ON** / OFF | **PB3 is used as a timer on motor control V2 connector** / contrary |

1. *The default configuration is in bold.*

### 7.3.2 STLINK-V3EC drivers

The installation of drivers is not mandatory since Windows 10® but allocates an ST-specific name to the ST-LINK COM port in the system device manager.

### 7.3.3 STLINK-V3EC firmware upgrade

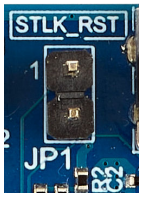
STLINK-V3EC includes a firmware upgrade mechanism (STSW-LINK007) through the USB port. The firmware can change during the STLINK-V3EC lifetime, to add new features, correct errors, or support new microcontrollers. Visit the www.st.com website regularly and before using this board to stay up to date with the latest firmware version.

### 7.3.4 STLINK-V3EC deactivation (reset mode)

**Attention:** *Attention: The reset mode of STLINK-V3EC is useful to connect an external probe to the debug (CN4) or the USART (CN3) connectors for embedded STM32 debug. In this reset mode, the 5 V selection JP2 STLK is not functional. Check Section 8.3.2 for more details.*

It is simple to deactivate the STLINK-V3EC function, by adding a jumper on JP5 to connect STLK NRST to GND, as shown in Figure 7 and Table 6. Programming, debugging, and monitoring through ST-LINK are impossible in this reset state, where most STLINK-V3EC PIOs are in high impedance.

**Figure 7. STLK NRST default configuration (JP1)**




DT79167V1

**Table 7. STLK NRST configuration (JP1)**

| Reference | Jumper[1] | Function | Comment |
|---|---|---|---|
| JP1 | ON | STLINK-V3EC reset | STLINK RESET is active (STLINK-V3EC inactive) |
| | **OFF** | | STLINK RESET is inactive (STLINK-V3EC active) |

1. *The default setting is in bold.*

## 7.4 Power supply

### 7.4.1 Power supply architecture

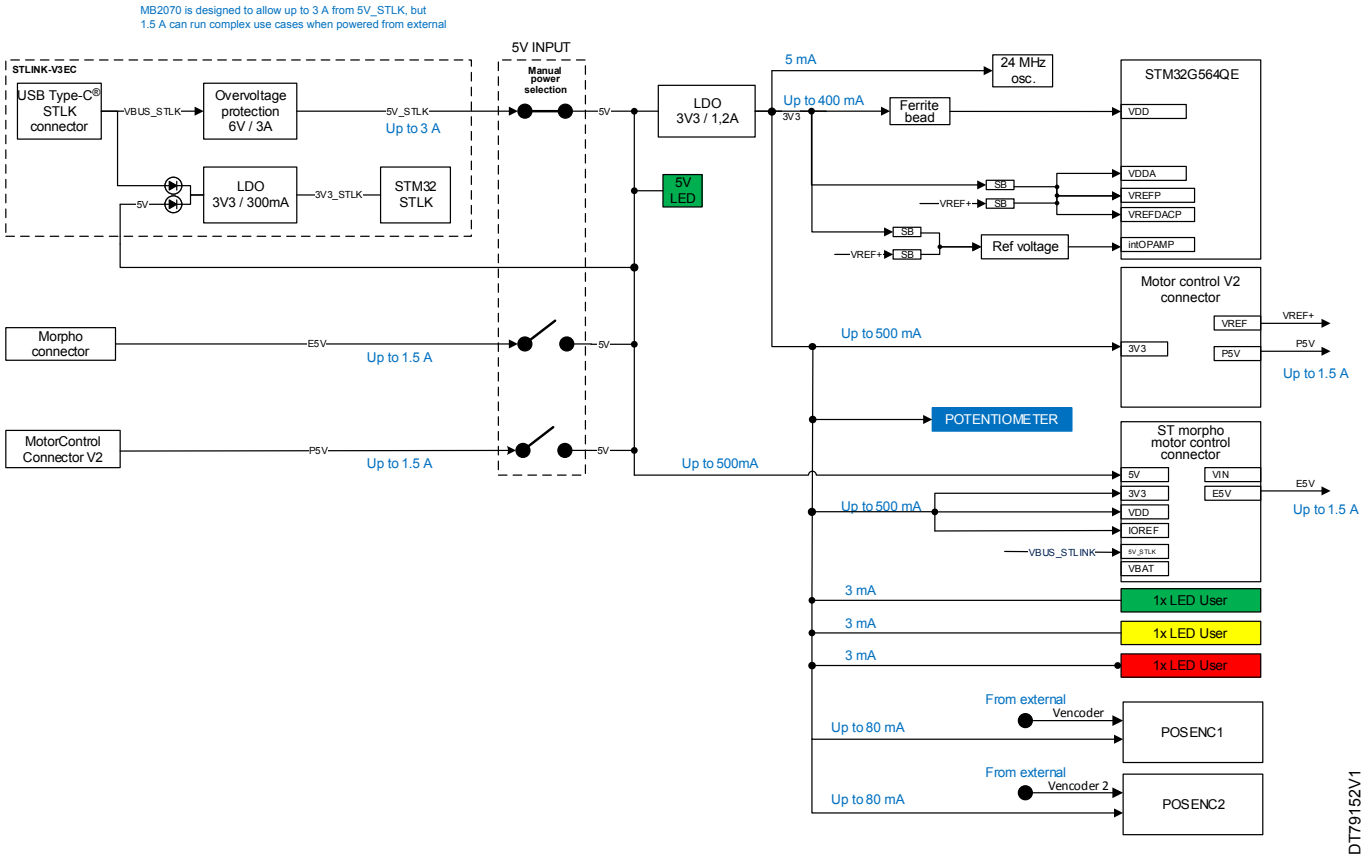
*Note: This B-G564E-MC1S Discovery kit uses a microcontroller power scheme that might be different from standard application notes. Refer to the relevant application notes for design.*

The following B-G564E-MC1S power diagram describes the power architecture and the maximum voltage and current limits under which functions can be safely used on the B-G564E-MC1S product. In any case, ensure the total power budget of the application always conforms to the selected 5 V power source mode, if not, malfunction can occur. For detailed configuration, refer to the relevant function description and technical application notes.

*Note: 1.5 A total current is the typical power budget considered on a 5 V power supply. In case this budget is not sufficient to support a specific use case, some additional boards on Motor control V2 and on ST morpho motor control connectors may be self-powered externally.*

Figure 8 shows the power diagram of the B-G564E-MC1Sboard:

**Figure 8. Power diagram**




### 7.4.2 5 V power source selection

B-G564E-MC1S Discovery kit is designed to be powered from the 5 V power rail. By selecting the jumper position on the JP2 header, it is possible to select any of the three following power sources as the input for the 5 V power rail (all of them are 5 V DC power supplies sources):

- P5V from motor control V2 connector V2 (CN9) for power board
- 5V_ STLK from the USB Type-C® receptacle (CN4) of STLINK-V3EC (default)
- E5V from ST morpho motor control connector (CN7) for custom daughterboard

Table 8 describes the different 5 V DC power source selection characteristics.

When the 5 V is present onboard, the 5 V green LED (LD2) lights up.

**Table 8. 5 V power source selection**

| Reference | Jumper position (1) | Function | Comment |
|---|---|---|---|
| JP2 | P5V<br>(pin [1-2]) | 5 V is supplied by MC V2 (CN9) | • 5 V (±5%)<br>• up to 1.5 A capable<br>• no embedded overcurrent protection |
| | **STLK**<br>(pin [3-4]) | 5 V is supplied by USB STLK<br>(CN1) | • 5 V (+10%/- 5% at current < 500 mA, ±10% at current < 1.5 A)<br>• USB legacy host supported<br>• Up to 3 A capable<br>• 3.2 A embedded overcurrent protection |

| Reference | Jumper position (1) | Function | Comment |
|---|---|---|---|
| JP2 | E5V<br>(pin [5-6]) | 5 V is supplied by ST morpho motor control (CN7) | • 5 V (±5%)<br>• up to 1.5 A capable<br>• no embedded overcurrent protection |

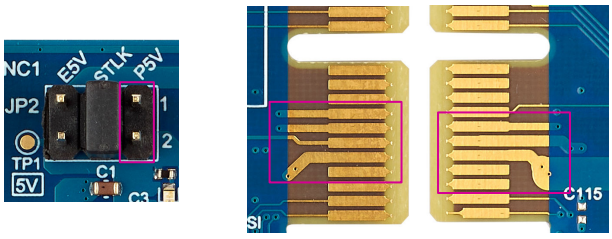
1. *The default setting is in bold.*

*Note: MB2070 is designed to allow up to 3 A from STLK, but 1.5 A can run complex use cases when powered from external power supplies (E5V, P5V).*

#### 7.4.2.1 *P5V power source*

P5V is the DC power coming from a power board connected through motor control V2 connector (CN9) from P5V pins (A05 and B05) and GND pins (A07 and B07). P5V can be supplied by boards like STEVAL-LVLP01. Figure 9 below shows the P5V selection on JP2 [1-2], with a power source connected to motor control V2 connector (CN9).

**Figure 9. P5V (JP2) from motor control V2 connector (CN9)**




DT79153V1

#### 7.4.2.2 *STLK power source (for compatibility with legacy USB host port)*

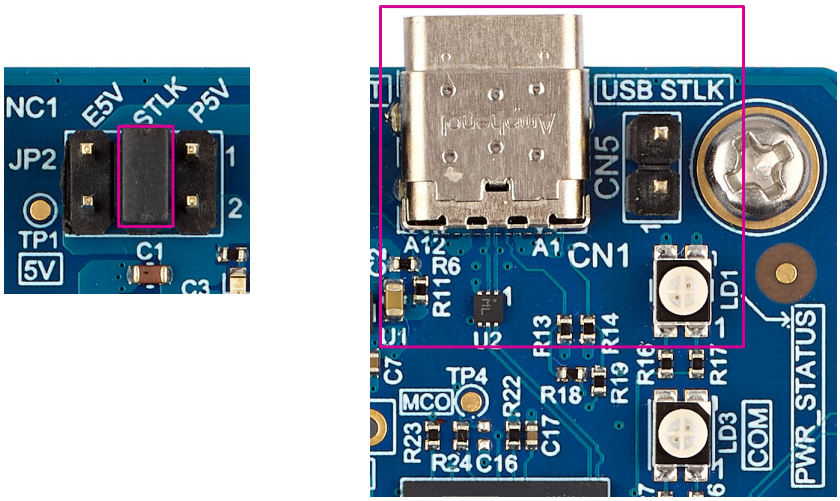
On the B-G564E-MC1S Discovery kit, the STLINK-V3EC is programmed with a power budget of 1.5 A, so the following behavior is expected:

- If the host port is only 100 mA capable, the PWR_STATUS LED (LD1) remains OFF, and the board is not powered (5 V LED LD2 remains OFF).
- If the USB host port is only 500 mA or 900 mA capable, STLINK-V3EC activates a 550 mA overcurrent protection and lights the PWR_STATUS LED (LD1) in orange to indicate users a possible limitation depending on the application. The board is powered and the 5V LED (LD2) lights green.
- If the USB host port is 1.5 A capable or more, the STLINK-V3EC lights the PWR_STATUS LED (LD1) in green (this ensures that the current is sufficient for any intended application) and sets the overcurrent protection depending on host capability. The board is powered and the 5V LED (LD2) lights green.

*Note: Using a 1.5 A USB Type A host charging port (usually marked with ϟ ) activates the 550 mA overcurrent protection and lights the PWR_STATUS LED (LD1) in orange.*

Figure 10 shows the selection of 5 V from USB STLK on JP2 [3-4], with a power source connected to the USB STLK connector (CN1). It is the default setting.

Figure 10. **STLK (JP2) from USB STLK (CN1)**

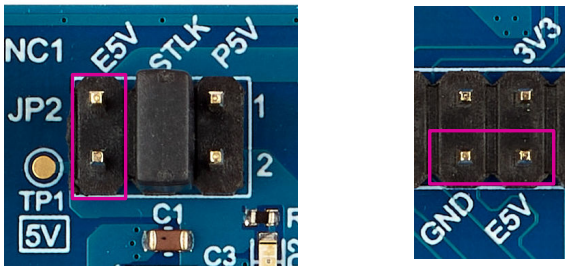



#### 7.4.2.3 *E5V power source*

E5V is the 5 V DC power coming from the ST morpho motor control connector (CN7, pin 6, and GND pins). Figure 11 shows the JP2 jumper be set on pin [5-6] to select the E5V power source and use of CN7 relevant pins.

In this configuration, a power supply unit or auxiliary equipment complying with standard EN 60950-1: 2006+A11/2009+A12/2011+A2/2013 or EN 62368-1 (2014+A11/2017) may also power the discovery board

Figure 11. **E5V (JP2) from ST morpho motor control connector (CN7)**




### 7.4.3 STM32 microcontroller power

The STM32G564QET3 microcontroller power is supplied from a 3.3 V/1.2 A LDO regulator: digital (VDD)/analog (VDDA/VREFP/VREFDACP) power inputs are all connected to 3V3 by default.

By default, a ferrite bead in parallel with a 5 mΩ low ohmic resistor shunt are present on digital (VDD) input power paths of the STM32G564QET3 microcontroller. The user can select any preferred configuration depending on its application and unsolder the undesired component.

As an option, all analog power supplies (VDDA/VREFP/VREFDACP) can be independently connected to VREF+ (coming from motor control V2 connector) thanks to dedicated solder bridges, refer to Table 9:

Table 9. **VDDA, VREFP, and VREFDACP configuration options**

| Power supply | Setting(1) | Configuration |
|---|---|---|
| VDDA | **SB95 ON, SB96 OFF** | VDDA is supplied from 3V3 |
| | SB95 OFF, SB96 ON | VDDA is supplied from VREF+ (coming from motor control V2 connector) |
| VREFP | **SB100 ON,** | VREFP is supplied from 3V3 |

| Power supply | Setting[1] | Configuration |
|---|---|---|
| VREFP | **SB97 OFF** | |
| | SB100 OFF, SB97 ON | VREFP is supplied from VREF+ (coming from a motor control V2 connector) |
| VREFDACP[2] | **SB36 ON, SB37 OFF** | VREFDACP is supplied from 3V3 |
| | SB36 OFF, SB37 ON | VREFDACP is supplied from VREF+ (coming from motor control V2 connector) |

1. *The default configuration is in bold.*
2. *If VREFDACP and VREFP are not powered by the same power supply, fit C44 for VREFDACP.*

A dedicated OPREF reference voltage is used for OPAMPs inputs of STM32G564QET3: this OPREF can be supplied from 3V3 or from VREF+ (coming from motor control V2 connector), depending on R60 and R61 connection.

OPREF can also be optionally generated and filtered through an external operational amplifier (U13). The following Table 10 summarizes the different possibilities regarding OPREF:

**Table 10. OPREF configuration options**

| Function | Hardware | Setting[1] | Configuration |
|---|---|---|---|
| OPREF input power choice | R60, R61 | **R61 ON, R60 OFF** | OPREF is supplied from 3V3 |
| | | R61 OFF, R60 ON | OPREF is supplied from VREF+ |
| OPREF external OPAMP (U13) | SB42, R75 | **SB42 ON R75 OFF** | External operational amplifier U13 is not used to generate OPREF |
| | | SB42 OFF R75 ON | External operational amplifier U13 used to generate OPREF |

1. *The default configuration is in bold.*

The analog ground (AGND) is connected to general ground (GND) through SB92.

## 7.5 Clock sources

Two clock references are available on B-G564E-MC1S for the STM32G564QET3 target microcontroller:

- 32.768 kHz crystal X3 for embedded RTC, not populated by default
- 24 MHz oscillator X2 for HSE clock

*Note: The HSE external oscillator can optionally be disabled:*

- *By hardware: move R114 on the SB103, and use internal HSI*
- *By software: use PG9 (HSE_DISABLE_N) in output mode to control the external oscillator (PG9 is inactive by default)*

## 7.6 Boot options

By default, the B-G564E-MC1S boots on internal flash memory. Other settings are possible.

### 7.6.1 BOOT0 pin

The BOOT0 value may come from the BOOT0 pin (active) or may come from an option bit depending on the value of a user option bit.

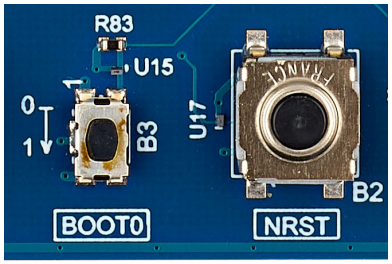
On the B-G564E-MC1S Discovery kit, the BOOT0 pin is:

- Set as active by default (the nSWBOOT0 option bit has been programmed to 1)
- LOW level by default (with an external pull-down)

Thus, the B-G564E-MC1S boots from internal flash memory by default.

To change the memory boot location to internal SRAM, the user can set the BOOT0 pin at HIGH level by pressing B3 BOOT0 button while releasing NRST signal (thanks to B2 NRST button release for example).

**Figure 12. BOOT0 (B3) and NRST (B2) push-buttons**




DT79156V1

### 7.6.2 Other memory boot location

Depending on many other option bits settings and/or BOOT0 pin status, other boot mechanisms are also offered (RSS, TrustZone®, bootloader, etc.). The user can choose any appropriate boot procedure according to his needs Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

## 7.7 LEDs

### 7.7.1 Description

Three general-purpose color LEDs (LD4, LD5, and LD6) are available as light indicators. Each LED is on when a low level is applied to the corresponding I/O ports. PWM control function is available for each LED

Table 11 describes the hardware IO configuration for the LEDs.

**Table 11. Hardware IO configuration for the LEDs**

| Signal name | STM32 pin | Function |
|---|---|---|
| PH5-YELL_LED | PH5 | Yellow LED (LD4) activation, TIM17_CH1 |
| PG11-RED_LED | PG11 | Red LED (LD5) activation, TIM12_CH2 |
| PA11-GREEN_LED | PA11 | Green LED (LD6) activation, TIM13_CH1 |

## 7.8 Push-buttons

### 7.8.1 Description

B-G564E-MC1S Discovery kit provides three push-buttons that are:

- An NRST reset button NRST (B2)
- A tamper/user button (B1)
- A boot0 button (B3), refer to Section 7.6

**Caution:** *The MB2070 user push-button shall not be used if PC13 to be used as wake-up input for the ST morpho motor control push-button function, adapt SB7, and SB22 accordingly.*

The reset signal of the STM32G564QET3 on the B-G564E-MC1S Discovery kit is active LOW. Sources of reset are:

- B2 NRST reset button (black button)
- STDC14 connector (CN4), reset from debug tools
- Embedded STLINK-V3EC microcontroller (U12)

### 7.8.2 Push-buttons input I/O interface

Table 12 describes the hardware IO configuration for the buttons.

**Table 12. Hardware IO configuration for the push-buttons**

| Reference | STM32 pin | Configuration |
|---|---|---|
| B1 | PC13 | User button B2 (active HIGH), use internal pull-down |
| B2 | NRST | Button for RESET source (active LOW) |
| B3 | BOOT0 | Button for BOOT0 configuration: BOOT0 is LOW by default (not pressed).<br>Button is active HIGH (maintain pressed during NRST release) |

## 7.9 Position encoder (POSENC1 and POSENC2)

**Warning:** *The POSENC feature available on this B-G564E-MC1S Discovery kit is not a reference design for direct use in a final product.*

The purpose of B-G564E-MC1S Discovery kit is to give access to relevant STM32G564 interfaces and help to develop software in an application context of EnDat 3 or HIPERFACE DSL® protocol, with controller role, and in a simple point-to-point RS-485 connection (bus mode not supported).

As an example, the B-G564E-MC1S Discovery kit design does not intend to be used for an official certification, as it may not be compliant with the most severe constraints in this domain.

Nevertheless, the B-G564E-MC1S Discovery kit supports functional testing of encoders to evaluate STM32G564 features.

The following references of encoders have been used to check this functional status:

- HIPERFACE DSL®: EDM35-2KF0A024A, EDM35-2KF0A024A | SICK(1)
- EnDat 3: EQN1337, ordering E30-R2, ID 1296523-01, Infobase-Detail | HEIDENHAIN(1)

1. *The URL belongs to a third party. It is active at document publication however STMicroelectronics shall not be liable for any change, move, or inactivation of the URL or the referenced material.*

Refer to the application note *Getting started with the POSENC on STM32 MCUs* (AN6601), for more details on related application examples.

### 7.9.1 Overview description

The B-G564E-MC1S Discovery kit provides access to a new position encoder (POSENC) feature. Two POSENC functions are integrated on MB2070, to be able to access independently and at the same time to the two interfaces integrated in the STM32G564QET3.

Both POSENC1 / two function can be configured to support either EnDat 3 or either HIPERFACE DSL® protocols, in the 2-wire or in the 4-wire configuration (not tested yet). The user has the possibility to select the desired configuration thanks to jumpers and thanks to different values/footprints integrated onboard.

Both POSENC1 / two functions rely on an RS-485 40 Mbps transceiver, a transformer and a 6-pin 3.81 mm pitch terminal block to allow easy connection with dedicated cables (not provided). HIPERFACE DSL® has a typical transfer rate of 9.375 MBaud. EnDat 3 has a data transmission rate of 12.5 Mbit/s (and up to 25 Mbit/s depending on transceiver peripheral choice).

Both POSENC1 and POSENC2 functions offer access to dedicated probing and debug capabilities such as: POSENC digital interface 3-pin header, SPI POSENC test points, and terminal block signals test points.

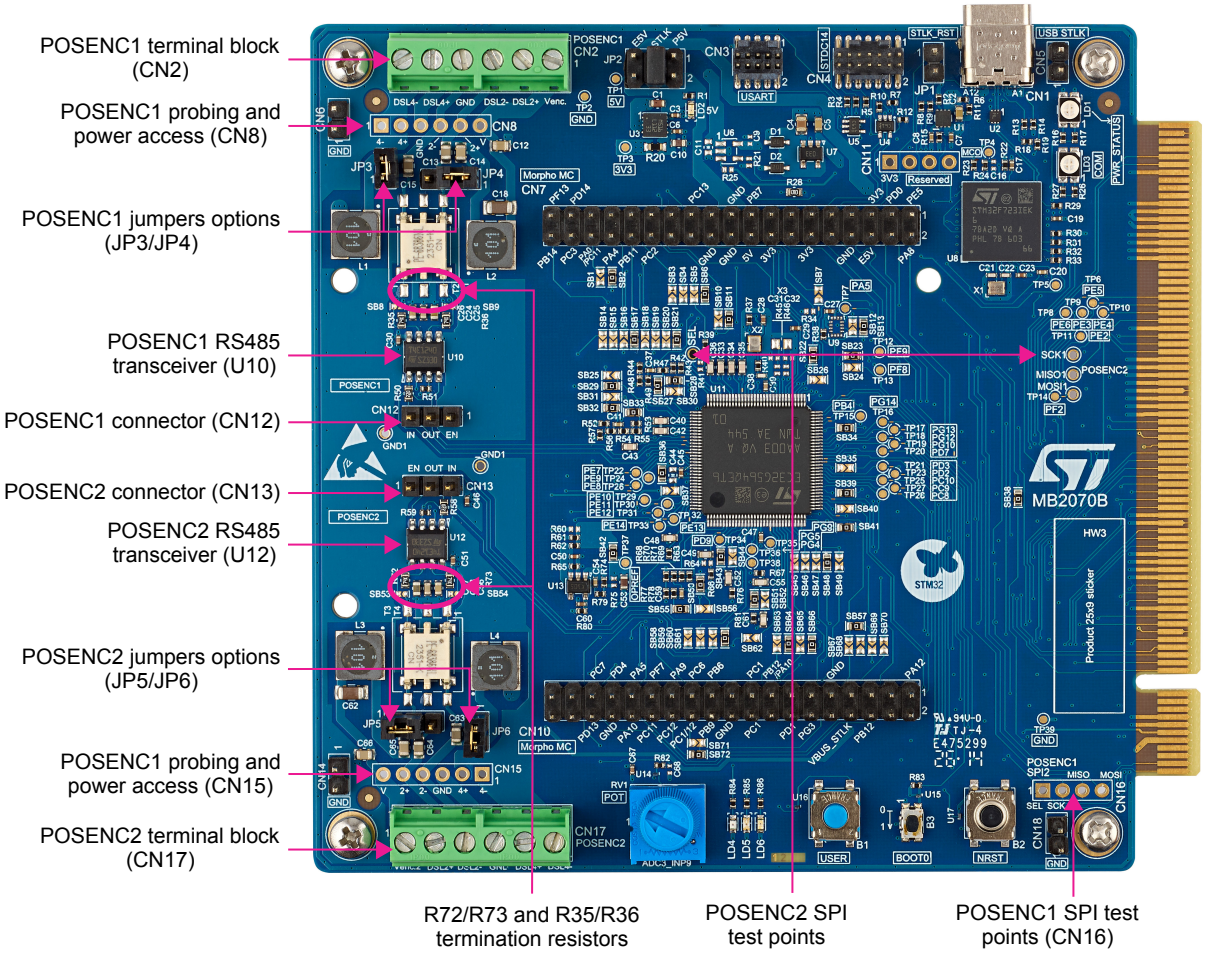
The encoder power supply must come from an external power supply (check encoder for voltage/current constraints, a 12 V typical voltage may be necessary in 2-wire mode), which should be connected through onboard test points. A power supply unit or auxiliary equipment complying with standard EN 60950-1: 2006+A11/2009+A12/2011+A2/2013 or EN 62368-1 (2014+A11/2017) must be used.

*Note:*

1. *The termination resistors R35/R36 and R73/R74 can have their temperature increased if RS-485 transceivers on the motor encoder side are powered by a 5 V supply.*
2. *The RS-485 transceivers are not protected against EFT > 4 kV (neither to EFT pulse train or surge transients)*
3. *Before using any POSENC function, read section Section 7.9.2 and Section 7.9.3:*
   - *Section 7.9.2 describes the modes/configuration of POSENC functions and their terminal block connection description.*
   - *Section 7.9.3 describes solder bridge configuration and shared interfaces (digital POSENC and SPI POSENC interfaces).*

Figure 13 shows the positions linked to the POSENC1 and POSENC2 functions on B-G564E-MC1S.

**Figure 13. POSENC1 and POSENC2 overview**




## 7.9.2 POSENC functions mode and configuration

Each POSENC feature can be configured to support EnDat 3 or HIPERFACE DSL® protocol mode, in 2-wire or 4-wire configuration. B-G564E-MC1S integrated POSENC functions have only the controller role.

Table 13 shows the POSENC1 different options selection in a simple matrix:

**Table 13. POSENC1 function mode and configuration description**

| POSENC1[1] | 2-wire configuration[2] | 4-wire configuration[3] |
|---|---|---|
| **EnDat 3 protocol mode** | **DSL2+/DSL2- are the data wires with short and uncontrolled impedance (DSL4+/DSL4- are not used, SB8 and SB9 are OFF).[4]**<br>**External power is supplied from Vencoder / GND pins (on CN8 pins V and GND): it feeds the data cable through L1/L2 choke coils directly on the 2-data wires.**<br>**Requires JP3 ON (bypass C15) and JP4 ON (connect pins 1-2)**<br>**EnDat 3 requires C26 (220 nF), C24 can be kept for EMC reasons, C25 may be removed.**<br>**EnDat 3 uses typical termination resistors of 60 Ω, but 57.6 Ω resistors are integrated onboard. EnDat 3 is using 2-core cables with 120 Ω ±10% impedance.** | DSL4+/DSL4- are the data wires designed with 114 Ω typical impedance (DSL2+/DSL2- are not used). Set SB8 and SB9 to ON.<br>External power can be supplied from Vencoder / GND pins (connect on CN8 pins V and GND) to feed dedicated cable wires plugged in CN2.<br>Set JP3 / JP4 jumpers OFF to avoid configuration confusion and to disconnect DSL2 from transformer.<br>EnDat 3 requires C26 (220 nF), C24 can be kept for EMC reasons, C25 may be removed.<br>EnDat 3 uses typical termination resistors of 60 Ω, but 57.6 Ω resistors are integrated onboard. EnDat 3 is using 4-core cables with 120 Ω ±10% impedance. |
| HIPERFACE DSL® protocol mode | DSL2+/DSL2- are the data wires with short and uncontrolled impedance (DSL4+/DSL4- are not used, SB8 and SB9 set to OFF).[4]<br>External power is supplied from Vencoder / GND pins (on CN8 pins V and GND): it feeds the data cable through L1/L2 choke coils directly on the 2-data wires.<br>Requires JP3 OFF and JP4 ON (connect pins 2-3)<br>HIPERFACE DSL® requires C25 (2.2 µF), C24 to be kept for EMC reasons, C26 may be removed.<br>HIPERFACE DSL® uses typical termination resistors of 56 Ω, but 57.6 Ω resistors are integrated onboard.<br>HIPERFACE DSL® is using 2-core cables with 110 Ω ±10 Ω impedance. | DSL4+/DSL4- are the data wires designed with 114 Ω typical impedance (DSL2+/DSL2- are not used). Set SB8 and SB9 to ON.<br>External power can be supplied from Vencoder / GND pins (connect on CN8 pins V and GND) to feed dedicated cable wires plugged in CN2.<br>Set JP3 / JP4 jumpers OFF to avoid configuration confusion and to disconnect DSL2 from transformer.<br>HIPERFACE DSL® requires C25 (2.2 µF), C24 can be kept for EMC reasons, C26 may be removed.<br>HIPERFACE DSL® uses typical termination resistors of 56 Ω, but 57.6 Ω resistors are integrated onboard.<br>HIPERFACE DSL® is using 4-core cables with 110 Ω ±10 Ω impedance. |

1. *The default configuration is in bold.*
2. *The 2-wire configuration stands for using data wires to transmit data and feed the power on same wires (2-core cable).*
3. *The 4-wire configuration stands for using data wires to transmit data and power wires to feed the power (four core cable).*
4. *Optionally, the transformer can be changed into 78601/1C. A double footprint is integrated on board.*

Table 14 is showing the POSENC1 connectors pinout (terminal block and probing access):

**Table 14. POSENC1 connectors pinout (CN2 terminal block and CN8 probing/power access)**

| Pin number | Terminal block marking (CN2) | Signal name | Probing access marking (CN8) | Pin number |
|---|---|---|---|---|
| 1 | 4- | DSL4_N | DSL4- | 6 |
| 2 | 4+ | DSL4_P | DSL4+ | 5 |
| 3 | GND | GND | GND | 4 |
| 4 | 2- | DSL2- | DSL2- | 3 |
| 5 | 2+ | DSL2+ | DSL2+ | 2 |
| 6 | V | Vencoder | VENC | 1 |

Table 15 shows the POSENC2 different options selection in a simple matrix:

**Table 15. POSENC2 function mode and configuration description**

| POSENC2 (1) | 2-wire configuration (2) | 4-wire configuration (3) |
|---|---|---|
| EnDat 3 protocol mode | **2_DSL2+/DSL2- are the data wires with short and uncontrolled impedance (2_DSL4+/ - are not used, SB53 and SB54 are OFF).(4)**<br>**External power is supplied from Vencoder2 / GND pins (on CN15 pins V and GND): it feeds the power to the cable through L3/L4 choke coils directly on the 2-data wires.**<br>**Requires JP6 ON (bypass C63) and JP5 ON (connect pins 1-2).**<br>**EnDat 3 requires C56 (220 nF), C58 can be kept for EMC reasons, C57 may be removed.**<br>**EnDat 3 uses typical termination resistors of 60 Ω, but 57.6 Ω resistors are integrated onboard. EnDat 3 is using 2-core cables with 120 Ω ±10% impedance.** | DSL4+/DSL4- are the data wires designed with 114 Ω typical impedance (DSL2+/DSL2- are not used). Set SB53 and SB54 to ON.<br>External power is supplied from Vencoder2 / GND pins (connect on CN15 pins V and GND) to feed dedicated cable wires plugged in CN17.<br>Set JP5 / JP6 jumpers OFF to avoid configuration confusion and to disconnect DSL2 from the transformer.<br>EnDat 3 requires C56 (220 nF), C58 can be kept for EMC reasons, C57 may be removed.<br>EnDat 3 uses typical termination resistors of 60 Ω, but 57.6 Ω resistors are integrated onboard. EnDat 3 is using 4-core cables with 120 Ω ±10% impedance. |
| HIPERFACE DSL® protocol mode | 2_DSL2+/ - are the data wires with short and uncontrolled impedance (2_DSL4+/ - are not used, SB53 and SB54 set to OFF).(4)<br>External power is supplied from Vencoder2 / GND pins (on CN15 pins V and GND): it feeds the power to the cable through L3/L4 choke coils directly on the 2-data wires.<br>Requires JP6 OFF and JP5 ON (connect pins 2-3).<br>HIPERFACE DSL® requires C57 (2.2 µF), C58 can be kept for EMC reasons, C56 may be removed.<br>HIPERFACE DSL® uses typical termination resistors of 56 Ω, but 57.6 Ω resistors are integrated onboard.<br>HIPERFACE DSL® is using 2-core cables with 110 Ω ±10 Ω impedance. | DSL4+/DSL4- are the data wires designed with 114 Ω typical impedance (DSL2+/DSL2- are not used). Set SB53 and SB54 to ON.<br>External power is supplied from Vencoder2 / GND pins (on CN15 pin V and GND) to feed dedicated cable wires plugged in CN17.<br>Set JP5 / JP6 jumpers OFF to avoid configuration confusion and to disconnect DSL2 from the transformer.<br>HIPERFACE DSL® requires C57 (2.2 µF), C58 can be kept for EMC reasons, C56 may be removed.<br>HIPERFACE DSL® uses typical termination resistors of 56 Ω, but 57.6 Ω resistors are integrated onboard.<br>HIPERFACE DSL® is using 4-core cables with 110 Ω ±10 Ω impedance. |

1. *Using POSENC2 and SPI POSENC2 is exclusive with other functions. Take take care to configure the board according to table 29 and table 30 before configuring the jumpers. The default configuration is in bold.*
2. *The 2-wire configuration stands for using data wires to transmit data and feed the power on same wires (2-core cable).*
3. *The 4-wire configuration stands for using data wires to transmit data and power wires to feed the power (four core-cables).*
4. *Optionally, the transformer can be changed into 78601/1C. A double footprint is integrated on board.*

Table 16 shows the POSENC2 connectors pinout (terminal block and probing access):

**Table 16. POSENC2 connectors pinout (CN17 terminal block and CN15 probing/power access)**

| Pin number | Terminal block marking (CN17) | Signal name | Probing access marking (CN15) | Pin number |
|---|---|---|---|---|
| 1 | 4- | 2_DSL4_N | DSL4- | 6 |
| 2 | 4+ | 2_DSL4_P | DSL4+ | 5 |
| 3 | GND | GND | GND | 4 |
| 4 | 2- | 2_DSL2- | DSL2- | 3 |
| 5 | 2+ | 2_DSL2+ | DSL2+ | 2 |
| 6 | V | Vencoder2 | VENC2 | 1 |

### 7.9.3 Microcontroller physical input I/O interface

All the digital signals of POSENC1 and POSENC2 are available on dedicated 2.54 mm pitch headers or on through hole test points for probing.

Table 17, Table 18, Table 19, and Table 20 describe the hardware IO description and connector pinout for the digital interface of POSENC1 and POSENC2 and for their corresponding SPI POSENC monitoring interface.

SPI POSENC interface related schematics are present on STM32 microcontroller IOs schematics page.

#### 7.9.3.1 *POSENC1 digital interfaces*

**Table 17. CN12 pinout description for POSENC1 digital interface**

| Pin number | Pin name | STM32 signal | Comment |
|---|---|---|---|
| 1 | PF14 | POSENC1.EN | POSENC1 enable |
| 2 | PF11 | POSENC1.OUT | POSENC1 data output |
| 3 | PF12 | POSENC1.IN | POSENC1 data input |

The SPI interface of POSENC1 is sharing the same pins than the SPI2 interface available on the motor control V2 connector. Both can be accessed on CN16. Refer to Table 18:

**Table 18. CN16 pinout description for POSENC1 SPI interface (also SPI2 of MC V2)**

| Pin number | Pin name | STM32 signal | Comment |
|---|---|---|---|
| 1 | PF10 | SPI.nSS | SPI POSENC1 select (also SPI2_NSS or PFC.PWM2 of motor control V2 connector) |
| 2 | PF3 | SPI.SCK | SPI POSENC1 clock (and SPI2_SCK for motor control V2 connector) |
| 3 | PF0 | SPI.MISO | SPI POSENC1 controller in completer out data (and SPI2_MISO for motor control V2 connector) |
| 4 | PF4 | SPI.MOSI | SPI POSENC1 controller out completer in data (and SPI2_MOSI for motor control V2 connector) |

#### 7.9.3.2 *POSENC2 digital interfaces*

POSENC2 digital interface is available on CN13, but it is exclusive with some other functions. Take care to adapt solder bridge configuration before using POSENC2 (refer to Table 19):

**Table 19. CN13 pinout description for POSENC2 digital interface**

| Pin number | Pin name | STM32 signal | Comment |
|---|---|---|---|
| 1 | PD15 | POSENC2.EN | POSENC2 enable |
| 2 | PD14 | POSENC2.OUT | POSENC2 data output |
| 3 | PD13 | POSENC2.IN | POSENC2 data input |

The SPI interface of POSENC2 can be accessed on some through hole test points. This SPI POSENC2 interface is sharing same pins than other functions available on motor control V2 connector (refer to Table 20 and Table 21). Figure 14 shows the position of the SPI POSENC2 interface test points on board.

**Figure 14. SPI POSENC2 test points position**

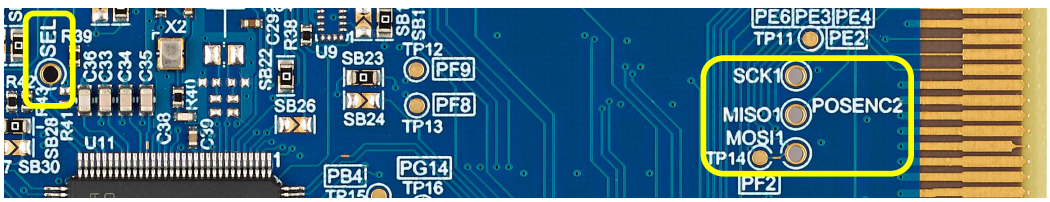


**Table 20. Description of SPI POSENC2 interface (on through hole test points)**

| Pin marking | Pin name | STM32 signal | Comment |
|---|---|---|---|
| SEL | PC3 | M2.Resolver_Cos | SPI POSENC2 select (it is necessary to unconnect C36 and all PC3 solder bridges described in Table 36) |
| SCK | PF7 | M3.Emergency(BKIN) | SPI POSENC2 clock |
| MISO | PF8 | M3.Emergency(BKIN2) | SPI POSENC2 controller in completer out data |
| MOSI | PF2 | M3.PWM_WH | SPI POSENC2 controller out completer in data |

### 7.9.4 POSENC functions solder bridge and jumper configuration

Table 21 and Table 22 show the different solder bridge configuration for POSENC functions:

**Table 21. Solder bridge configuration for POSENC functions**

| Solder bridge | Function | STM32 I/O | Setting[1] | Description |
|---|---|---|---|---|
| SB38, SB98 | POSENC1 | PF10 | **SB38 ON, SB98 OFF** | **PF10 is connected to POSENC1 SPI SEL function and to SPI.nSS on motor control V2 connector**<br>**PF10 is not connected to PFC.PWM2 of motor control V2 connector** |
| | | | SB38 OFF, SB98 ON | PF10 is not connected to POSENC1 SPI SEL function and to SPI.nSS on motor control V2 connector<br>PF10 can be connected to PFC.PWM2 of motor control V2 connector |
| SB60, SB61 | POSENC2 | PD15 | **SB60 OFF, SB61 ON** | **PD15 is not connected to POSENC2.EN**<br>**PD15 is connected to PFC.BKIN_OC of motor control V2 connector** |
| | | | SB60 ON, SB61 OFF | PD15 is connected to POSENC2.EN<br>PD15 is not connected to PFC.BKIN_OC of motor control V2 connector |
| SB59, SB58 | | PD14 | **SB59 OFF, SB58 OFF** | **PD14 is not connected to POSENC2.OUT**<br>**PD14 is not connected to ST morpho CN7 pin 35** |
| | | | SB59 ON, SB58 OFF | PD14 is connected to POSENC2.OUT<br>PD14 is not connected to ST morpho CN7 pin 35 |
| SB44, SB43 | | PD13 | **SB44 OFF, SB43 ON, SB110 ON SB111 OFF** | **PD13 is not connected to POSENC2.IN**<br>**PD13 is connected to the motor control V2 connector**<br>**PD13 is not connected to ST morpho CN10 pin 34** |
| | | | SB44 ON, SB43 OFF, SB110 ON SB111 OFF | PD13 is connected to POSENC2.IN and not connected elsewhere |

1. *The default configuration is in bold.*

**Table 22. POSENC jumpers configuration**

| Jumper | Function | Setting[1] | Description |
|---|---|---|---|
| JP3 | POSENC1 | **ON** | **EnDat 3 mode in 2-wire configuration (connects DSL2- directly to transformer)** |
| | | OFF | HIPERFACE DSL® mode in 2-wire configuration (connects DSL2- to transformer through serial 470 nF)<br>or<br>EnDat 3 / HIPERFACE DSL® in 4-wire configuration |

| Jumper | Function | Setting(1) | Description |
|---|---|---|---|
| JP4 | POSENC1 | **ON Pin [1-2]** | **EnDat 3 mode in 2-wire configuration (connects DSL2+ to transformer through serial 100 nF)** |
| | | ON Pin [2-3] | HIPERFACE DSL® mode in 2-wire configuration (connects DSL2+ to transformer through serial 470 nF) |
| | | OFF | EnDat 3 or HIPERFACE DSL® in 4-wire configuration |
| JP6 | POSENC2 | **ON** | **EnDat 3 mode in 2-wire configuration (connects 2_DSL2- directly to transformer)** |
| | | OFF | HIPERFACE DSL® mode in 2-wire configuration (connects 2_DSL2- to transformer through serial 470 nF) or EnDat 3 / HIPERFACE DSL® in 4-wire configuration |
| JP5 | | **ON Pin [1-2]** | **EnDat 3 mode in 2-wire configuration (connects 2_DSL2+ to transformer through serial 100 nF)** |
| | | ON Pin [2-3] | HIPERFACE DSL® mode in 2-wire configuration (connects 2_DSL2+ to transformer through serial 470 nF) |
| | | OFF | EnDat 3 or HIPERFACE DSL® in 4-wire configuration |

1. *The default configuration is in bold.*

## 7.10 Operational amplifier

### 7.10.1 Description

The B-G564E-MC1S Discovery board offers the possibility to test the internal operational amplifier for Motor1 shunt signals. Shunt signals can pass through the internal operational amplifier or enter the ADC input of STM32G564QET3 directly by setting solder bridges.

### 7.10.2 Operational amplifier interface

Table 23 describes the hardware I/O configuration for the OPAMP interface.

**Table 23. Hardware I/O configuration for the OPAMP interface**

| Solder bridge | Amplifier | Setting(1) | Description |
|---|---|---|---|
| SB27, SB28, and SB30 | OPAMP1 | **SB27 and SB28 ON SB30 OFF** | Shunt1 uses OPAMP1 INP is PA1, INM is PA3, OUT is PA2 |
| | | SB27 and SB28 OFF SB30 ON | Shunt1 does not use OPAMP1 and is measured on ADC input ADC_2_IN5 (PC4) directly. |
| SB31, SB32, and SB33 | OPAMP2 | **SB33 and SB32 ON SB31 OFF** | Shunt2 uses OPAMP2 INP is PA7, INM is PC5, OUT is PA6 |
| | | SB33 and SB32 OFF SB31 ON | Shunt2 does not use OPAMP2 and is measured on ADC input ADC_12_IN6 (PC0) directly. |
| SB50, SB55, and SB56 | OPAMP3 | **SB50 and SB55 ON SB56 OFF** | Shunt3 uses OPAMP3 INP is PB13, INM is PB10, OUT is PB1 |
| | | SB50 and SB55 OFF SB56 ON | Shunt3 does not use OPAMP3 and is measured on ADC input ADC_1_IN15 / ADC_3_IN12 (PB0) directly. |

1. *The default configuration is in bold.*

## 7.11 Analog input potentiometer

### 7.11.1 Description

The B-G564E-MC1S Discovery kit provides an onboard analog-to-digital converter ADC. The onboard potentiometer is connected to PD12 (ADC_3_IN9).

**Caution:** *The potentiometer cannot be used if PD12 is used for the Motor2 Resolver_Sin function of motor control V2 connector, adapt SB51, and SB52 accordingly.*

### 7.11.2 Potentiometer solder bridge

Table 24 describes the hardware I/O configuration for the potentiometer.

**Table 24. Hardware I/O configuration for the potentiometer**

| I/O | Hardware | Setting(1) | Configuration |
|---|---|---|---|
| PB11 | SB51 and SB52 | **SB51 ON**<br>**SB52 OFF** | **PD12 is used as a potentiometer input (ADC_3_IN9)** |
| | | SB51 OFF<br>SB52 ON | PD12 is used for motor2 Resolver_Sin on motor control V2 connector |

1. *The default configuration is in bold.*

## 7.12 Jumpers and solder bridges

### 7.12.1 Jumpers

The jumper functions and their default status are described in Table 25:

**Table 25. Jumper configuration**

| Jumper | Setting(1) | Function | Comment |
|---|---|---|---|
| JP1 | ON | STLINK-V3EC reset | • STLINK RESET is active (STLINK-V3EC inactive) |
| | **OFF** | | • **STLINK RESET is inactive (STLINK-V3EC active)** |
| JP2 | P5V<br>Pin [1-2] | 5 V is supplied by the motor control V2 connector (CN9) | • 5 V (±5%)<br>• Up to 1.5 A<br>• No embedded overcurrent protection |
| | **STLK**<br>**Pin [3-4]** | 5 V is supplied by USB STLK (CN1) | • **5 V (+10%/- 5% at current < 500 mA, ±10% at current < 1.5 A)**<br>• **USB legacy host supported**<br>• **Up to 3 A capable**<br>• **Up to 3.2 A embedded overcurrent protection** |
| | E5V<br>Pin [5-6] | 5 V is supplied by ST morpho motor control (CN7) | • 5 V (±5%)<br>• Up to 1.5 A capable<br>• No embedded overcurrent protection |
| JP3 | **ON** | POSENC1 DSL2-connection to transformer | • **Connects DSL2- directly to transformer** |
| | OFF | | • Connects DSL2- to transformer through serial 470 nF |
| JP4 | **ON**<br>**Pin [1-2]** | POSENC1 DSL2+ connection to transformer | • **Connects DSL2+ to transformer through serial 100 nF** |
| | ON<br>Pin [2-3] | | • Connects DSL2+ to transformer through serial 470 nF |
| | OFF | | • DSL2+ not connected to transformer |

| Jumper | Setting[1] | Function | Comment |
|---|---|---|---|
| JP5 | **ON Pin [1-2]** | POSENC2 2_DSL2+ connection to transformer | • **Connects 2_DSL2+ to transformer through serial 100 nF** |
| | ON Pin [2-3] | | • Connects 2_DSL2+ to transformer through serial 470 nF |
| | OFF | | • 2_DSL2+ not connected to transformer |
| JP6 | **ON** | POSENC2 2_DSL2- connection to transformer | • **Connects 2_DSL2- directly to transformer** |
| | OFF | | • Connects 2_DSL2- to transformer through serial 470 nF |

1. *The default setting is in bold.*

### 7.12.2 Solder bridges

The solder bridge functions and their default status are described in Table 26.

**Table 26. Solder bridge configuration**

| Solder bridge | Setting[1] | Function[2] | Comment |
|---|---|---|---|
| SB3, SB12, SB16, SB18, SB24, SB25, SB26, SB35, SB40, SB45, SB46, SB47, SB49, SB58, SB63, SB65, SB67, SB99, SB104, SB106 | ON | ST morpho motor control 2 function connection to MCU GPIOs or motor control V2 connector function connection to MCU GPIOs (M1 to M3) | ST morpho motor control 2 function is connected to MCU GPIOs |
| | **OFF** | | **ST morpho motor control 2 function is not connected to MCU** |
| SB13, SB23, SB29, SB34, SB39, SB41, SB43, SB48, SB57, SB64, SB66, SB94, SB102, SB105, SB107, SB108, SB109 | **ON** | | **Motor control V2 connector function (M1 to M3) is connected to MCU GPIOs** |
| | OFF | | Motor control V2 connector M2 function (M1 to M3) is not connected to MCU |
| SB2, SB72, SB116 | **ON** | ST morpho motor control additional solder bridges configuration to support X-NUCLEO-IHM16 (for other X-NUCLEO, refer to Section 8.5) | **To configure some signals necessary for X-NUCLEO-IHM16** |
| SB1, SB7, SB68, SB69, SB70, SB71, SB117, SB118 | **OFF** | | **To disconnect some signals not necessary for X-NUCLEO-IHM16** |
| SB27, SB28, SB32, SB33, SB50, SB55 | **ON** | MCU OPAMP1, 2 and 3 connection to motor 1 motor control V2 connector current ADC or Motor 1 motor control V2 connector current ADC connection to MCU (no OPAMP) | **MCU OPAMP1, 2 and 3 connected to motor control V2 connector** |
| | OFF | | MCU OPAMP1, 2 and 3 not connected to motor control V2 connector |
| SB30, SB31, SB56 | ON | | Connected to MCU (no MCU OPAMP possible) |
| | **OFF** | | **Not connected to MCU (using MCU OPAMP is possible, see above)** |
| SB36, SB95, SB100 | **ON** | VDDA, VREFDACP, and VREFP connection to 3V3 or VDDA, VREFDACP, and VREFP connection to VREF+ | **MCU analog supplies connected to 3V3** |
| | OFF | | MCU analog supplies not connected to 3V3 |

| Solder bridge | Setting[1] | Function[2] | Comment |
|---|---|---|---|
| SB37, SB96, SB97 | ON | VDDA, VREFDACP, and VREFP connection to 3V3 or VDDA, VREFDACP, and VREFP connection to VREF+ | MCU analog supplies connected to VREF+ |
| | **OFF** | | **MCU analog supplies not connected to VREF+** |
| SB77, SB83, SB91 | **ON** | Motor control V2 connector motor 2 current ADC filters connected to MCU or Motor control V2 connector motor 1 voltage connected to motor 2 current ADC filters or ST morpho motor control connected to motor 2 current ADC filters | **MCU ADC filter connected to motor 2 shunt** |
| | OFF | | MCU ADC filter not connected to motor 2 shunt |
| SB86, SB87, SB93 | ON | | MCU ADC filter connected to motor 1 voltage |
| | **OFF** | | **MCU ADC filter not connected to motor 1 voltage** |
| SB82, SB85, SB89 | ON | | MCU ADC filter connected to ST morpho motor control2 |
| | **OFF** | | **MCU ADC filter not connected to ST morpho motor control2** |
| SB5, SB14, SB20 | ON | [3] M1 and M2 resolver filters connected to resolvers or M1 and M2 resolver filters connected to M2 voltage or M1 and M2 resolver filters connected to M3 current shunt | Resolver filters connected to resolvers |
| | **OFF** | | **Resolver filters not connected to resolvers** |
| SB6, SB17, SB21 | **ON** | | **Resolver filters connected to M2 voltage** |
| | OFF | | Resolver filters not connected to M2 voltage |
| SB4, SB15, SB19 | ON | | Resolver filters connected to M3 current shunt |
| | **OFF** | | **Resolver filters not connected to M3 current shunt** |
| SB113, SB115, SB34 | **ON** | M1 encoder signals connection | **PB4/PC9/PB3 connected to encoder** |
| | OFF | | PB4/PC9/PB3 not connected to encoder |
| SB112, SB114 | ON | M1 Hall signals connection | PB4/PC9 connected to HALL, and PB3 to SWO |
| | **OFF** | | **PB4/PC9 not connected to HALL** |
| SB79, SB84, SB90 | **ON** | M2 encoder signals[4] connection | **PB7/PD4/PA9 connected to encoder** |
| | OFF | | PB7/PD4/PA9 not connected to encoder |
| SB78, SB80, SB88 | ON | M2 hall signals[4] connection | PB7/PD4/PA9 connected to HALL |
| | **OFF** | | **PB7/PD4/PA9 not connected to HALL** |
| SB75, SB76 | **ON** | PC14 and PC15 connection to VCP1 | **PC14/PC15 connected to VCP1_RX/TX (exclusive with external 32 kHz crystal function)** |
| | OFF | | PC14/PC15 not connected to VCP1_RX/TX |
| SB22 | **ON** | PC13 connection | **PC13 connected to user button** |
| | OFF | | PC13 not connected to user button |
| SB7 | ON | | PC13 connected to ST morpho motor control |
| | **OFF** | | **PC13 not connected to ST morpho motor control** |
| SB51 | **ON** | PD12 connection | **PD12 connected to onboard potentiometer** |

| Solder bridge | Setting[1] | Function[2] | Comment |
|---|---|---|---|
| SB51 | OFF | PD12 connection | PD12 not connected to onboard potentiometer |
| SB52 | ON | | PD12 connected to motor control V2 connector |
| | **OFF** | | **PD12 not connected to motor control V2 connector** |
| SB74 | **ON** | PA5 connection | **PA5 connected to motor control V2 connector DAC_PWM** |
| | OFF | | PA5 not connected to motor control V2 connector DAC_PWM |
| SB73 | ON | | PA5 connected to motor control V2 connector ADC |
| | **OFF** | | **PA5 not connected to motor control V2 connector ADC** |
| SB44, SB59, SB60 | ON | POSENC2 connection to MCU | POSENC2 is connected to the MCU |
| | **OFF** | | **POSENC2 is not connected to MCU** |
| SB61 | **ON** | PFC.BKIN_OC connection | **PD15 (TIM16_BKIN) connected to PFC.BKIN_OC (exclusive with POSENC2, see SB59)** |
| | OFF | | PD15 not connected to PFC.BKIN_OC |
| SB62 | ON | | PG2 (TIM15_BKIN) connected to PFC.BKIN_OC |
| | **OFF** | | **PG2 (TIM15_BKIN) not connected to PFC.BKIN_OC** |
| SB38 | **ON** | PF10 connection | **PF10 connected to SPI2.NSS** |
| | OFF | | PF10 is not connected to SPI2.NSS |
| SB98 | ON | | PF10 (TIM15_CH2) connected to PFC.PWM2 |
| | **OFF** | | **PF10 not connected to PFC.PWM2** |
| SB101 | **ON** | PB5 connection | **PB5 (TIM16_CH1) connected to PFC.PWM2** |
| | OFF | | PB5 is not connected to PFC.PWM2 (see SB94 to connect PFC.PWM2) |
| SB42 | **ON** | OPREF connection | **OPREF connected to 3V3 (R76 OFF)** |
| | OFF | | OPREF not connected to 3V3 (R76 can be ON) |
| SB92 | **ON** | AGND connection | **AGND connected to GND** |
| | OFF | | AGND is not connected to GND |
| SB103 | ON | 24 MHz external oscillator hardware deactivation | 24 MHz external oscillator disabled |
| | **OFF** | | **24 MHz external oscillator not disabled (depends also on HSE_DISABLE_N)** |
| SB81 | ON | PB3 connection | PB3 is connected to SWO |
| | **OFF** | | **PB3 is not connected to SWO** |
| SB34 | **ON** | | **PB3 is connected to M1.encoder_Z** |
| | OFF | | PB3 is not connected to M1.encoder_Z |

1. *The default setting is in bold.*
2. *When a function is describing multiple solder bridge groups, only one group of solder bridge can be ON at the same time: the user can choose the relevant configuration among the offered possibilities.*

3. *Using ST morpho motor control on resolver filters (SB3, SB18 and SB16 ON) implies these three solder bridge groups are OFF.*
4. *Using these MC-V2 functions implies SB39, SB41, SB94 solder bridges are ON (ST morpho motor control not used).*

# 8 Board connectors

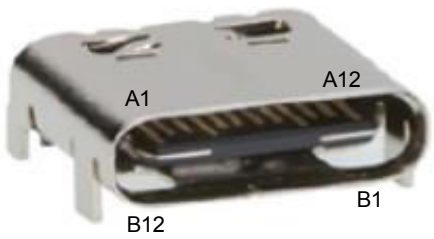
Twelve connectors are implemented on the B-G564E-MC1S Discovery kit:

- CN1: USB Type-C® (USB STLK)
- CN2 and CN17: terminal block connectors (POSENC1 and POSENC2)
- CN3: MIPI10 USART connector
- CN4: STDC14 debug connector
- CN7 and CN10 ST morpho motor control connectors
- CN9 Motor control V2 connector
- CN5, CN6, CN14, and CN18: GND connector headers

## 8.1 USB Type-C® receptacle connector (CN1)

CN1 is a 24-pin double-row USB Type-C® hybrid right-angle receptacle compatible with USB Type-C® specifications and is shown in Figure 15.

**Figure 15. USB Type-C® receptacle connector front view (CN1)**




DT79161V1

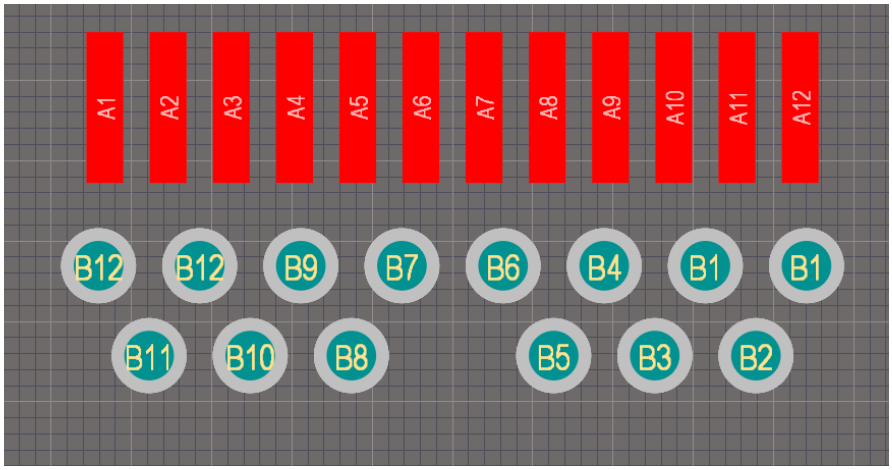
The CN1 pinout and top layer footprint are described in Figure 16 and Figure 17.

**Figure 16. USB Type-C® connector pinout (CN1)**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | TX1+ | TX1- | $V_{BUS}$ | CC1 | D+ | D- | SBU1 | $V_{BUS}$ | RX2- | RX2+ | GND |
| | | | | | | | | | | | |
| GND | RX1+ | RX1- | $V_{BUS}$ | SBU2 | D- | D+ | CC2 | $V_{BUS}$ | TX2- | TX2+ | GND |
| B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 |

DT79162V1

Figure 17. **USB Type-C® top layer footprint pinout (CN1)**




The CN1 signal assignment is described in Table 27.

Table 27. **USB STLK connector signal assignment (CN1)**

| Pin number | Description | Signal assignment | Pin number | Description | Signal assignment |
|---|---|---|---|---|---|
| B12 | GND | GND | A1 | GND | GND |
| B11 | RX1_P | - | A2 | TX1_P | - |
| B10 | RX1_N | - | A3 | TX1_N | - |
| B9 | VBUS | VBUS_STLK | A4 | VBUS | VBUS_STLK |
| B8 | SBU2 | - | A5 | CC1 | STLK_CC1_CN |
| B7 | DM2 | STLK_USB_CN_N | A6 | DP1 | STLK_USB_CN_P |
| B6 | DP2 | STLK_USB_CN_P | A7 | DM1 | STLK_USB_CN_N |
| B5 | CC2 | STLK_CC2_CN | A8 | SBU1 | - |
| B4 | VBUS | VBUS_STLK | A9 | VBUS | VBUS_STLK |
| B3 | TX2_N | - | A10 | RX2_N | - |
| B2 | TX2_P | - | A11 | RX2_P | - |
| B1 | GND | GND | A12 | GND | GND |

## 8.2 MIPI10 USART connector (CN3)

The USART 5x2-pin header 1.27 mm pitch connector (CN3) can interface with USART2 signals used for the second VCP port of STM32G564QET3. This VCP2 is also connected to STLINK Bridge_USART.

Before using the MIPI10 connector, refer to Section 8.3

Table 28 describes the USART connector I/O connection:

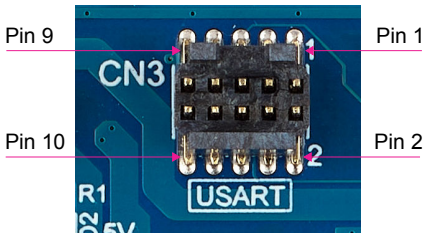
Table 28. **MIPI10 USART connector pinout (CN3)**

| Connector pin number | STM32 pin | Board function |
|---|---|---|
| 1 | - | NC |
| 2 | - | NC |
| 3 | PD6 | DBG_VCP2_RX: target Rx used for VCP2 and also connected to Bridge_USART_TX of STLINK |
| 4 | - | NC |

| Connector pin number | STM32 pin | Board function |
|---|---|---|
| 5 | PD5 | DBG_VCP2_TX: Target TX used for VCP2 and also connected to Bridge_USART_RX of STLINK |
| 6 | - | NC |
| 7 | - | NC |
| 8 | - | NC |
| 9 | GND | Ground |
| 10 | - | NC |

Figure 18 shows the USART connector (CN3) pinout.

**Figure 18. MIPI10 USART connector pinout (CN3)**




DT79165V1

## 8.3 STDC14 and USART connectors

### 8.3.1 SWD debug/program/trace and JTAG/UART/USART

**Attention:** *Before using CN3 or CN4, also check the specific constraints detailed in Section 8.3.2.*

The SWD debug/program/trace interface is accessible through the STLINK-V3EC USB connector (CN1) by default, and the STDC14 debug connector (CN4) or USART connector (CN3) are other options.

By default, access to SWO trace and JTAG bus are not available.

The UART5 bootloader is accessible through STLINK-V3EC by default, and the USART2 bridge is also accessible.

To debug/program/trace, first, choose any of the exclusive following connectors and consider Table 29 to summarize B-G564E-MC1S Discovery kit capabilities:

**Table 29. Debug/program/trace and JTAG/UART/USART interface overview**

| Connector | SWD debug/program | SWO trace (1) | JTAG(1)(2) | UART5 bootloader(3) | USART2 |
|---|---|---|---|---|---|
| USB STLINK-V3EC CN1 | Yes | Yes, as an option | Yes, 3-wire only | Yes | Yes |
| STDC14 debug CN4 | Yes | Yes, as an option | Yes, 3-wire only | Yes | No |
| USART CN3 | No | No | No | No | Yes |

1. *SWO/JTDO can be used by setting SB81 ON and SB34 OFF (exclusive with M1.Encoder_Z function on CN9)*
2. *JTDI has only TP5 access to STLINK-V3EC. NJTRST is not used but accessible on PB4 GPIO.*
3. *The UART5 bootloader interface is limited to 480 kBauds.*

When using STLINK-V3EC USB CN1 by default, refer to the software tool description for any specific constraints or capabilities. Here are the interface signals between STM32G564QE MCU and STLINK-V3EC or the external probes:

**Table 30. Default STM32G564QE MCU interface to external debug tools**

| Signal name | STM32G564QE pin | Function |
|---|---|---|
| DBG.SWCLK | PA14 | SWCLK/JTCK |
| DBG.SWDIO | PA13 | SWDIO/JTMS |
| DBG.SWO | PB3 | SWO/JTDO (as option, not connected by default) |
| *DBG.JTDI* | *PA15* | *JTDI (not used by default)* |
| *JNTRST* | *PB4* | *JNTRST (not used by default)* |
| DBG.VCP1_TX | PC15 | UART5_TX bootloader (only on CN4) |
| DBG.VCP1_RX | PC14 | UART5_RX bootloader (only on CN4) |
| DBG.VCP2_TX | PD5 | USART2_TX bootloader (only on CN3) |
| DBG.VCP2_RX | PD6 | USART2_RX bootloader (only on CN3) |

For details about CN3 and CN4 connector pinout, refer to Section 8 and Section 8.4.

### 8.3.2 Using an external debug tool to program and debug the onboard STM32

**Warning:**
1. *Take care STDC14 debug and USART connectors are 3.3 V signaling interface by default. Use only adequate/compatible tools to connect.*
2. *The CN1 is exclusive with CN3 and with CN4. CN3 and CN4 can be used at the same time.*

Before using any external debug tool/probe on CN3 or CN4, read carefully its user manual, to check if specific constraints apply. Then, follow the step by step actions below:

1. Put the embedded STLINK-V3EC in reset mode: add a jumper on the STLK_RST header (JP1), no data transfer is possible from USB ST-LINK. This allows the use of either CN3 or CN4 without the risk of signal conflict with STLINK-V3EC on any interface.
2. Because STLINK-V3EC is in reset mode, remove the jumper (JP2) from the STLK position and put it in any other position according to the user-required configuration (refer to Section 7.4.2 and Section 7.4.1).
3. If the SWD interface is used in 2-wire mode (without SWO), no further modifications are required.
4. To use SWO, set SB81 to ON and SB34 to OFF. SWO is exclusive with the M1.Encoder_Z function on the CN9.
5. To use the JTAG interface, only the 3-wire mode is available on CN4 (JTMS/JTCK/JTDO). JTDO is exclusive with M1.Encoder_Z function on CN9). JTDI and NJTRST are not connected, but are accessible on TP5 or PB4 GPIO.

*Note:*
1. *SWCLK is connected on CN4 pin 9 for compatibility with some debug probes (JRTCK).*
2. *Only the CN4 connector provides access to the NRST pin of the STM32G564QE microcontroller.*

6. Power up the board: connect the power source to the board.
   To use the UART5 bootloader (set 480 kBauds or lower) or SWD interface, connect to CN4.
   To use the USART2 interface, connect to CN3.
7. Use the STDC14 cable/probe to connect to the debug connector (CN4) or use a MIPI-10 compatible cable/probe to connect to the USART connector (CN3). Reminder: The board is 3.3 V by default, so use only adequate/compatible tools to connect.

## 8.4 STDC14 debug connector (CN4)

The STDC14 7x2-pin header 1.27 mm pitch connector (CN4) allows connection to SWD interface, SWO trace, and VCP1 UART of STM32G564QET3.

The STDC14 has a common footprint with MIPI10: Table 31 describes the STDC14 connector pinout compatibility with both interfaces: STDC14 and MIPI10.

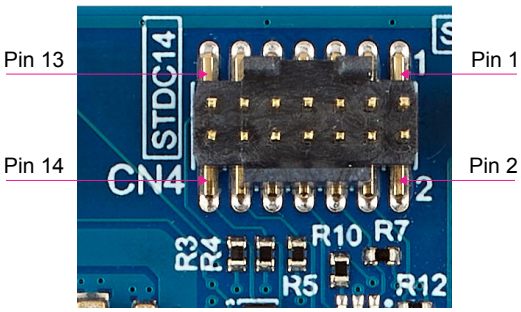
Before using the STDC14 debug connector, refer to Section 8.3: STDC14 and USART connectors.

Table 31. **STDC14 debug connector pinout (CN4)**

| MIPI10 connector pin number | STDC14 connector pin number | STM32 pin | Board function |
|---|---|---|---|
| - | 1 | - | Reserved |
| - | 2 | - | Reserved |
| 1 | 3 | - | STM32 VDD (3V3) |
| 2 | 4 | PA13 | STM32 Serial Wire Data input/output |
| 3 | 5 | GND | Ground |
| 4 | 6 | PA14 | STM32 Serial Wire clock |
| 5 | 7 | GND | Ground |
| 6 | 8 | PB3 | STM32 Serial Wire Output |
| 7 | 9 | - | NC |
| 8 | 10 | - | NC |
| 9 | 11 | - | GNDdetect: GND detection for plug indicator |
| 10 | 12 | NRST | STM32 reset (active low) |
| - | 13 | PC14 | Virtual COM port UART serial interface connected to STM32 UART Rx |
| - | 14 | PC15 | Virtual COM port UART serial interface connected to STM32 UART Tx |

Figure 19 shows the STDC14 CN4 connector pinout.

Figure 19. **STDC14 connector pinout (CN4)**




DT79166V1

## 8.5 ST morpho motor control connectors (CN7 and CN10)

The two 38-pins double-row 2.54 mm pitch header connectors (CN7 and CN10) can interface with some X-NUCLEO IHM boards (plugged on top side or on bottom side depending on the X-NUCLEO reference).

### 8.5.1 Description

The ST morpho motor control connectors (CN7 and CN10) are implemented on B-G564E-MC1S to be compatible with the X-NUCLEO-IHM16M1 (default configuration), X-NUCLEO-IHM07M1, X-NUCLEO-IHM08M1, X-NUCLEO-IHM09M1, and X-NUCLEO-IHM09M2 motor-driver expansion boards. Other ST morpho motor control shields may be compatible with this B-G564E-MC1S kit in the future. Refer to related document/tools from the motor control ecosystem.

**Warning:** *ST morpho motor control is exclusive with motor control V2 connector on many functions: this is managed through solder bridges for shared PIOs. Because the motor control V2 connector is the interface used by default, many changes are necessary before being able to interface with X-NUCLEO add-on boards. Refer to microcontroller I/Os Table 41 and configure solder bridges accordingly.*

- *In addition, before using any ST morpho motor control shield, refer to its relevant user manual, to check if hardware specific configurations are needed depending on the user application.*
- *In addition, before using ST morpho motor control connectors on B-G564E-MC1S, follow actions and rules detailed in Figure 20 to help configuring MB2070 according to the user application.*
- *To use 34-pin motor control connector J7 of IHM09, a socket elevator should be used such as ESQ-119-24-x-D on the connectors CN7/CN10.*

Figure 20 shows the MB2070 configuration for the ST morpho motor control connectors on B-G564E-MC1S.

**Figure 20. ST morpho motor control configuration on MB2070**

First, populate all the relevant ST Morpho Motor Control 2 Solder Bridge positions on page 3 (by moving the ones fitted on MC-V2 for each shared PIO)
Check SB59 and SB44 are not fitted (POSENC2 SPI)
using PE5 implies to connect SB26
using PB14 also implies to move SB17 on SB16
using PF13 also implies to move SB21 on SB18
using PC3 also implies to move SB6 on SB3
using PB11 also implies to move SB91 on SB89
using PC1 also implies to move SB77 on SB82
using PA0 also implies to move SB83 on SB85
using PD13 also implies to move SB110 on SB111
using PC2 also implies to move SB11 on SB10

Chose any of SB2, SB1 (by moving SB2)
Chose any of SB116, SB117 or SB118 (by moving SB116)
Use SB72 or SB71 or none
Use SB70 or SB69 or none
Use SB71 or SB118 or none
Use SB68 or SB69 or none

using SB1 also implies to move SB66 on SB65
using SB2 also implies to move SB83 on SB85
using SB68 also implies to move SB57 on SB67
using SB69 also implies to move SB105 on SB106
using SB70 also implies to move SB105 on SB106
using SB71 also implies to move SB109 on SB45
using SB72 also implies to move SB109 on SB45
using SB116 also implies to move SB77 on SB82
using SB117 also implies to move SB77 on SB82
using SB118 also implies to move SB77 on SB82

| SBxx | IHM16 (default) | IHM07 | IHM08 | IHM09 | Connector pin |
|---|---|---|---|---|---|
| SB1 | OPEN | OPEN | CLOSED | CLOSED | CN7-34 |
| SB2 | CLOSED | CLOSED | OPEN | OPEN | CN7-34 |
| SB68 | OPEN | OPEN | CLOSED | CLOSED | CN10-15 |
| SB69 | OPEN | CLOSED | OPEN | OPEN | CN10-15 |
| SB70 | OPEN | OPEN | CLOSED | OPEN | CN10-6 |
| SB71 | OPEN | OPEN | CLOSED | CLOSED | CN10-24 |
| SB72 | CLOSED | OPEN | OPEN | OPEN | CN10-26 |
| SB116 | CLOSED | OPEN | CLOSED | OPEN | CN10-18 |
| SB117 | OPEN | OPEN | OPEN | OPEN | CN10-17 |
| SB118 | OPEN | CLOSED | OPEN | OPEN | CN10-24 |

DT79168V1

**Caution:** *Due to the sharing of some I/Os of STM32G564QET3 by multiple peripherals, the following limitations apply in using the ST morpho motor control connectors:*

1. *PD13 and PD14 cannot be used at the same time as POSENC2 function (check SB59 and SB44 status)*
2. *PC13 must not be used together with MB2070 user push-button (chose any of SB7 or SB22)*

### 8.5.2 ST morpho motor control pinout

Figure 21 shows the position of the ST morpho motor control connectors on B-G564E-MC1S Discovery kit.

Figure 21. **CN7 and CN10 connector pinout**

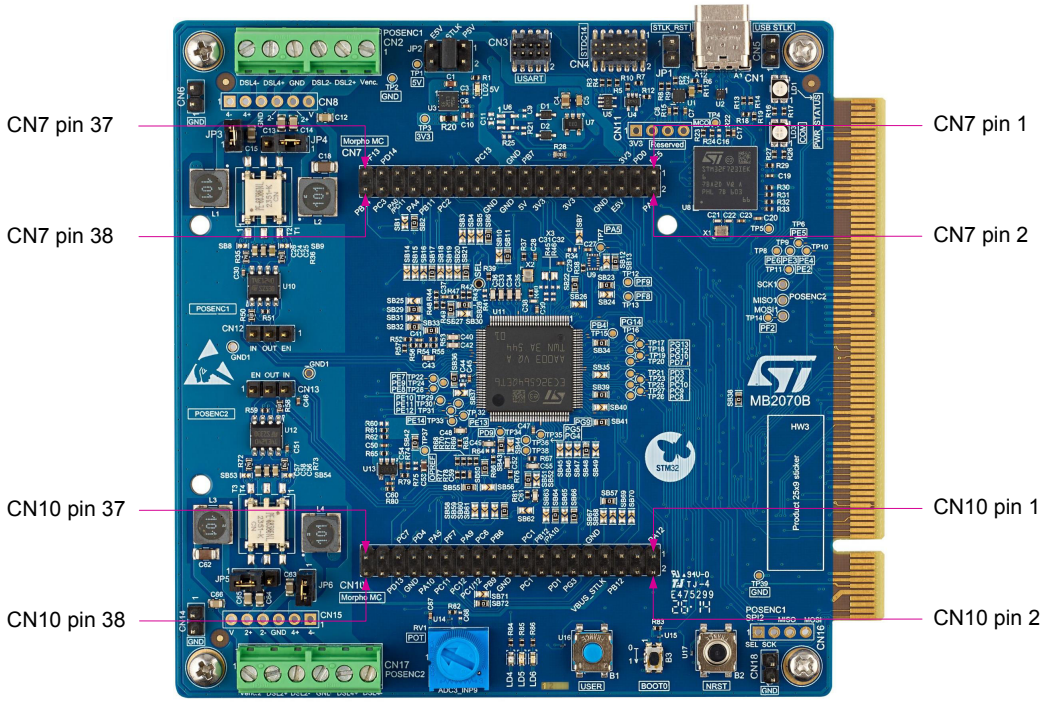



Table 32 and Table 33 describe the pinout of the ST morpho motor control connectors and associated functions available for each X-NUCLEO shield.

Table 32 and Table 33 describe also some specific comments linked to the use of *X-NUCLEO-IHM16M1*, as it is the X-NUCLEO shield supported by default. Specific configuration of any other X-NUCLEO is not described in Table 32 and Table 33, refer to each relevant X-NUCLEO user manual.

Table 32. **ST morpho motor control connector (CN7)**

| Connector pin number | Category(1) | Pin name(1) | STM32 pin(1) | Function of X-NUCLEO-IHM16M1 | Function of X-NUCLEO-IHM08M1 | Function of X-NUCLEO-IHM07M1 | Function of X-NUCLEO-IHM09M1 |
|---|---|---|---|---|---|---|---|
| 1 | GPIO | GPIO | PE5 | - | - | Enable_CH1 | NTC bypass |
| 2 | GPIO | GPIO | PA8 | - | - | Enable_CH2 | Dissipative brake/OCP disable |
| 3 | GPIO | GPIO | PD0 | - | - | Enable_CH3 | - |
| 4 | - | - | - | - | - | - | - |
| 5 | - | - | - | - | - | - | - |
| 6 | E5V | - | - | - | E5V | E5V | E5V |
| 7 | - | - | - | - | - | - | - |
| 8 | - | - | - | - | - | - | - |
| 9 | - | - | - | - | - | - | - |
| 10 | - | - | - | - | - | - | - |
| 11 | - | - | - | - | - | - | - |
| 12 | VDD | - | - | VDD | VDD | VDD | VDD |
| 13 | - | - | - | - | - | - | - |

| Connector pin number | Category[1] | Pin name[1] | STM32 pin[1] | Function of X-NUCLEO-IHM16M1 | Function of X-NUCLEO-IHM08M1 | Function of X-NUCLEO-IHM07M1 | Function of X-NUCLEO-IHM09M1 |
|---|---|---|---|---|---|---|---|
| 14 | - | - | - | - | - | - | - |
| 15 | - | - | - | - | - | - | - |
| 16 | - | - | - | - | - | - | - |
| 17 | TIMy_CH1 | TIM2_CH1 | PB7 | Encoder A/Hall H1 | Encoder A/Hall H1 | Encoder A/Hall H1 | Encoder A/Hall H1 |
| 18 | +5 V | - | - | +5 V | +5 V | +5 V | +5 V |
| 19 | - | - | - | - | - | - | - |
| 20 | GND | - | - | GND | GND | GND | GND |
| 21 | - | - | - | - | - | - | - |
| 22 | GND | - | - | GND | GND | GND | GND |
| 23[2] | GPIO | PC13-USER_BUTTON | PC13 | - | Button | Button | - |
| 24 | - | - | - | - | - | - | - |
| 25 | - | - | - | - | - | - | - |
| 26 | - | - | - | - | - | - | - |
| 27 | - | - | - | - | - | - | - |
| 28 | ADC | ADC_12_IN8 | PC2[3] | VBUS | Current_A | Current_A | Current_A |
| 29 | - | - | - | - | - | - | - |
| 30 | ADC | ADC_12_IN14 | PB11[3] [4] | Current_U | VBUS | VBUS | VBUS |
| 31 | - | - | - | - | - | - | - |
| 32 | DAC | DAC_1_OUT1/ ADC2_IN17 | PA4 | CURRENT_REFDAC[5] | CURRENT_REFDAC/ Speed | CURRENT_REFDAC | CURRENT_REFDAC |
| 33 | - | - | - | - | - | - | - |
| 34 | TIMx_CH2N | TIM_8_CH2N | PC11[6] | - | VL | - | VL |
| | **ADC** | **ADC_12_IN1** | **PA0** [3] [4] | **Current_W** | - | BEMF2 | - |
| 35 | ADC | ADC_3_IN11 | PD14 | Speed | Temp | Temp | Temp |
| 36 | ADC | ADC_12_IN9 | PC3[3] | BEMF3 | Current_B | Current_B | Current_B |
| 37 | ADC | ADC_2_IN0 | PF13[3] | BEMF2 | BEMF1 | BEMF1 | Speed |
| 38 | ADC | ADC_1_IN5 | PB14[3] | BEMF1 | Current_C | Current_C | Current_C |

1. *For multiple choice, the default configuration is in bold.*
2. *This pin is not connected by default, but it can be optionally connected depending on the user application. To use pin 23, it is highly recommended to move SB22 on SB7 to avoid an inadvertent short circuit with MB2070 user push-button.*
3. *Some STM32 signals are sharing filters with other connector pins refer to Table 36 for details.*
4. *Check other configuration when using these PIOs, refer to Table 37 for details.*
5. *Optional configuration of the X-NUCLEO-IHM16M1, refer to the related user manual.*
6. *Check other configuration when using these PIOs, refer to Table 34 for details.*

Table 33. **ST morpho motor control connector (CN10)**

| Pin number | Category[1] | Pin name[1] | STM32 signal[1] | Function of X-NUCLEO-IHM16M1 | Function of X-NUCLEO-IHM08M1 | Function of X-NUCLEO-IHM07M1 | Function of X-NUCLEO-IHM09M1 |
|---|---|---|---|---|---|---|---|
| 1 | GPIO | BEMF_GPIO | PA12 | GPIO_BEMF | GPIO_BEMF | GPIO_BEMF | - |
| 2 | - | - | - | - | - | - | - |
| 3 | - | - | - | - | - | - | - |
| 4 | - | - | - | - | - | - | - |
| 5 | - | - | - | - | - | - | - |
| 6 | ADC | ADC_1_IN11 | PB12[2] | VBUS[3] | BEMF3 | - | - |
| 7 | - | - | - | - | - | - | - |
| 8 | U5V | - | - | - | - | - | - |
| 9 | - | - | - | - | - | - | - |
| 10 | - | - | - | - | - | - | - |
| 11 | - | - | - | - | - | - | - |
| 12 | TIMx_ETR | TIM_8_ETR | PG3 | - | CPOUT | CPOUT | - |
| 13 | - | - | - | - | - | - | - |
| 14 | TIMx_BKIN | TIM_8_BKIN2 | PD1 | BKIN2 | BKIN | BKIN | BKIN |
| 15 | TIMx_CH1N | TIM_8_CH1N | PA10[2] | UL[3]/ Current_W[3] | UL | - | UL |
| | ADC | ADC_1_IN11 | PB12[2] | - | - | BEMF3 | - |
| 16 | - | - | - | - | - | - | - |
| 17 | ADC | ADC_12_IN7 | PC1[4][5] | - | - | - | - |
| 18 | ADC | ADC_12_IN7 | PC1[2][4][5] | Current_V | BEMF2 | - | - |
| 19 | - | - | - | - | - | - | - |
| 20 | - | - | - | - | - | - | - |
| 21 | TIMx_CH2 | TIM_8_CH2 | PB6 | VH | VH | VH | VH |
| 22 | GPIO (PWM) | TIMx_CHy | PB9 | - | LED_RED | LED_RED | LED_RED |
| 23 | TIMx_CH1 | TIM_8_CH1 | PC6 | UH | UH | UH | UH |
| 24 | TIMx_CH3N | TIM_8_CH3N | PC12[2] | - | WL | - | WL |
| | ADC | ADC_12_IN7 | PC1[2][4][5] | Current_V [3] | - | Speed | - |
| 25 | TIMy_CH3 | TIM_2_ETR/ 2_CH3 | PA9 | Encoder Z/Hall H3 | Encoder Z/Hall H3 | Encoder Z/Hall H3 | Encoder Z/Hall H3 |
| 26 | TIMx_CH3N | TIM_8_CH3N | PC12[2] | WL | - | - | - |
| 27 | TIMz | TIM_5_CH2 | PF7 | CURRENT_REF PWM[3] | CURRENT_REF PWM | CURRENT_REF PWM | CURRENT_REF PWM |
| 28 | TIMx_CH2N[4] | TIM_8_CH2N | PC11[2] | VL | - | - | - |
| 29 | DAC/TIMw | DAC_2_OUT1/ TIM9_CH1 | PA5 | STBY | DAC/PWM | DAC/PWM | DAC/PWM |
| 30 | TIMx_CH1N[4] | TIM_8_CH1N | PA10[2] | UL | - | - | - |
| 31 | TIMy_CH2 | TIM_2_CH2 | PD4 | Encoder B/Hall H2 | Encoder B/Hall H2 | Encoder B/Hall H2 | Encoder B/Hall H2 |
| 32 | GND | AGND | - | - | - | - | - |
| 33 | TIMx_CH3 | TIM_8_CH3 | PC7 | WH | WH | WH | WH |
| 34 | ADC | ADC_3_IN10 | PD13[2][5] | NTC/temp | - | - | - |

| Pin number | Category(1) | Pin name(1) | STM32 signal(1) | Function of X-NUCLEO-IHM16M1 | Function of X-NUCLEO-IHM08M1 | Function of X-NUCLEO-IHM07M1 | Function of X-NUCLEO-IHM09M1 |
|---|---|---|---|---|---|---|---|
| 35 | - | - | - | - | - | - | - |
| 36 | - | - | - | - | - | - | - |
| 37 | - | - | - | - | - | - | - |
| 38 | - | - | - | - | - | - | - |

1. *For multiple choice, the default configuration is in bold.*
2. *Check other configuration when using these PIOs, refer to Table 34 for details.*
3. *Optional configuration for the X-NUCLEO-IHM16M1, refer to the related user manual.*
4. *Check other configuration when using this PIO, refer to Table 37 for details.*
5. *Some STM32 signals are sharing filters with other connector pins refer to Table 36 for details.*

### 8.5.3 Hardware configuration description of the ST morpho motor control page

Table 34 describes the configuration of solder bridges, which are present on the ST morpho motor control page.

**Table 34. Hardware configuration description of the ST morpho motor control page**

| Pin | Hardware | Setting(1) | Configuration |
|---|---|---|---|
| CN7 pin 23 | SB7 | **OFF** | **PC13 is not connected to CN7 pin 23** |
| | | ON | PC13 is connected to CN7 pin 23 (it is highly recommended to move SB22 on SB7 to avoid any inadvertent short circuit with MB2070 user push-button) |
| CN7 pin 34 | SB1 | **OFF** | **PC11 is not connected to CN7 pin 34** |
| | | ON | PC11 is connected to CN7 pin 34 (PC11 is also connected on CN10 pin 28) |
| | SB2 | OFF | PA0 is not connected to CN7 pin 34 |
| | | **ON** | **PA0 is connected to CN7 pin 34** |
| CN10 pin 6 | SB70 | **OFF** | **PB12 is not connected to CN10 pin 6** |
| | | ON | PB12 is connected to CN10 pin 6 (check also SB69) |
| CN10 pin 15 | SB68 | **OFF** | **PA10 is not connected to CN10 pin 15** |
| | | ON | PA10 is connected to CN10 pin 15 (PA10 is also connected on CN10 pin 30) |
| | SB69 | **OFF** | **PB12 is not connected to CN10 pin 15** |
| | | ON | PB12 is connected to CN10 pin 15 (check also SB70) |
| CN10 pin 24 | SB118 | **OFF** | **PC1 is not connected to CN10 pin 24** |
| | | ON | PC1 is connected to CN10 pin 24 (check also SB116, SB117, and SB71) |
| | SB71 | **OFF** | **PC12 is not connected to CN10 pin 24** |
| | | ON | PC12 is connected to CN10 pin 24 (check also SB72 and SB118) |
| CN10 pin 26 | SB72 | OFF | PC12 is not connected to CN10 pin 26 |
| | | **ON** | **PC12 is connected to CN10 pin 26 (see also SB71)** |
| CN10 pin 18 | SB116 | OFF | PC1 is not connected to CN10 pin 17 |
| | | **ON** | **PC1 is connected to CN10 pin 18 (check also SB117 and SB118)** |
| CN10 pin 17 | SB117 | **OFF** | **PC1 is not connected to CN10 pin 17** |
| | | ON | PC1 is connected to CN10 pin 17 (check also SB116 and SB118) |

1. *The default configuration is in bold.*

## 8.6 GND connector (CN5, CN6, CN14, CN18)

Four 2.54 mm pitch two-pin headers are present to ease the GND connection for probes in each corner of the board (top/bottom).

## 8.7 Motor control V2 connector (CN9)

### 8.7.1 Description

The Motor control V2 connector top/bottom footprint is based on the standard PCIe® x16 gold edge-finger design and can interface with some dedicated application boards. A total of 164 pins are available, 82 on top (CN9B) and 82 on bottom (CN9A). Refer to Figure 22.

The motor control V2 connector (CN9) is an interface between the control board and the power board (or adaptor board). It is a PCI Express® format connector.

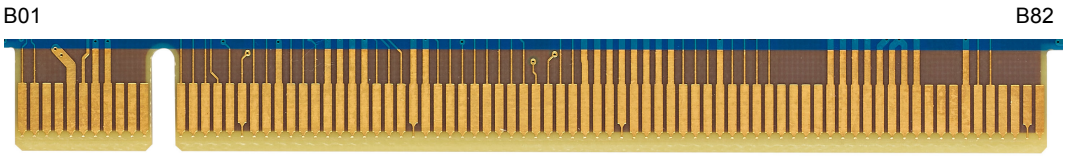
Three motors, PFC, SPI , ADCs and control signals are implemented on the Motor control V2 connector.

*Note:*

1. *Many signals from the motor control V2 connector are exclusive with other functions. Refer to Section 8.7.3 to Section 8.7.6 for more details.*
2. *Some pins are supporting different functions. Refer to the connected board user manual for specific configuration.*
3. *The motor control V2 connector is configured to use internal operational amplifiers by default. Refer to Section 7.10 for other setting.*

**Caution:** *Before using motor control V2 connector check Section 8.7.2, Section 8.7.3, and Section 8.7.4 for board configuration, and refer to Section 7.11 before using M2_Resolver_Sin.*

**Figure 22. PCIEx16 gold finger pinout (top side, CN9B)**




DT79157V1

The opposite pins on the bottom side (CN9A) follow exactly the same pinout: from A01 (left) to A82 (right).

### 8.7.2 Pinout

Table 35 describes the pinout of the motor control V2 connector (CN9).

**Table 35. Motor control V2 connector**

| Connector pin number | Category | Pin name | STM32 signal(1) | Function(1) | Comment |
|---|---|---|---|---|---|
| A side (bottom) | | | | | |
| 1 | SPI | SPI_nSS | PF10 | M_SPI_2_NSS | PF10 shared with pin B-36 and POSENC1 function(2) |
| 2 | | SPI_SCK | PF3 | M_SPI_2_SCK | - |
| 3 | | SPI_nSS | - | - | - |
| 4 | | SPI_SCK | - | - | - |
| 5 | | 5V_to_CTRLB | - | P5V | - |
| 6 | | 3.3V_to_PWRB | - | 3V3 | - |
| 7 | | DGND | - | GND | - |

| Connector pin number | Category | Pin name | STM32 signal[1] | Function[1] | Comment |
|---|---|---|---|---|---|
| 8 | SPI | ID_Enable | PG14 | GPIO | - |
| 9 | ADC | ADC | - | - | - |
| 10 | | ADC | - | - | - |
| 11 | | ADC | - | - | - |
| 12 | Motor1 | Emergency(BKIN) | PB12 | M1_EmergencySTOP_TIM_1_BKIN | - |
| 13 | | INH/PWM | PE9 | M1_PWM_UH_TIM_1_CH1 | - |
| 14 | | INH/PWM | PE11 | M1_PWM_VH_TIM_1_CH2 | - |
| 15 | | INH/PWM | PE13 | M1_PWM_WH_TIM_1_CH3 | - |
| 16 | | Master_EN | PG13 | M1_Master_EN(GPIO) | - |
| 17 | | Timer_ETR | PE7 | M1_TIM_1_ETR | - |
| 18 | | Hall_sensors_H1 | PB4 | M1_Hall_1_TIM_3_CH1 | PB4 shared with other[6] |
| 19 | | Hall_sensors_H2 | PC9 | M1_Hall_2_TIM_3_CH2 | PC9 shared with other[6] |
| 20 | - | DGND | - | GND | - |
| 21 | Motor1 | Shunt1+ | PA1 | M1_SHUNT1_OPAMP_1_VIN0P | Refer to Table 23 for SB setting |
| | | ADC input | PC4 | M1_CURR_U_ADC_2_IN5 | |
| 22 | | Shunt2+ | PA7 | M1_SHUNT2_OPAMP_2_VIN0P | |
| | | ADC input | PC0 | M1_CURR_V_ADC_12_IN6 | |
| 23 | | Shunt3+ | PB13 | M1_SHUNT3_OPAMP_3_VIN1P | |
| | | ADC input | PB0 | M1_CURR_W_ADC_1_IN15 (ADC_3_IN12) | |
| 24 | - | AGND | - | GND | - |
| 25 | Motor1 | Ph_Voltage+/ BEMF_zc[5] | PB15 | M1_VOL+_U_ADC_2_IN15 | |
| 26 | | Ph_Voltage+/ BEMF_zc[5] | PF15 | M1_VOL+_V_ADC_1_IN0 | |
| 27 | | Ph_Voltage+/ BEMF_zc[5] | PD8 | M1_VOL+_W_ADC_3_IN6 | - |
| 28 | | Temperature/Board ID | PB2 | M1_TEMP_ADC_2_IN12 | - |
| 29 | | VBUS | PH1 | M1_VBUS_ADC_2_IN10 | - |
| 30 | | Dissipative_brake | PD7 | M1_DissipativeBrake(GPIO) or M1_DissipativeBrake_TIM9_CH1 | - |
| 31 | - | DGND | - | GND | - |
| 32 | - | AGND | - | GND | - |
| 33 | PFC | AC_voltage | PD9 | M_AC voltage_ADC_3_IN15 | - |
| 34 | | PFC_Current1 | PD11 | M_PFC current 1_ADC_3_IN8 | - |
| 35 | | PFC_BKIN_OC | **PD15 /** PG2 | **M_PFC_BKIN_OC_TIM_16_BKIN** M_PFC_BKIN_OC_TIM_15_BKIN | PD15 shared with POSENC2 function[2] |
| 36 | | PFC_PWM1 | PF9 | M_PFC_PWM1_TIM_15_CH1 | - |
| 37 | Motor2 | Emergency(BKIN) | PD2 | M2_EmergencySTOP_TIM_8_BKIN | - |
| 38 | | INH/PWM | PC6 | M2_PWM_UH_TIM_8_CH1 | - |
| 39 | | INH/PWM | PB6 | M2_PWM_VH_TIM_8_CH2 | - |

| Connector pin number | Category | Pin name | STM32 signal(1) | Function(1) | Comment |
|---|---|---|---|---|---|
| 40 | Motor2 | INH/PWM | PC7 | M2_PWM_WH_TIM_8_CH3 | - |
| 41 | | Master_EN | PA8 | M2_Master_EN(GPIO) | - |
| 42 | | Timer_ETR | PG3 | M2_TIM_8_ETR | - |
| 43 | | Hall_sensors_H1 | PB7 | M2_Hall_1_TIM_2_CH1 | PB7 shared with other(6) |
| 44 | | Hall_sensors_H2 | PD4 | M2_Hall_2_TIM_2_CH2 | PD4 shared with other(6) |
| 45 | - | DGND | - | GND | - |
| 46 | Motor2 | Shunt1+ | PB11 | M2_SHUNT1_ADC_12_IN14 | PB11 shared with other(3) |
| 47 | | Shunt2+ | PC1 | M2_SHUNT2_ADC_12_IN7 | PC1 shared with other(3) |
| 48 | | Shunt3+ | PA0 | M2_SHUNT3_ADC_12_IN1 | PA0 shared with other(3) |
| 49 | - | AGND | - | GND | - |
| 50 | Motor2 | Ph_Voltage+/BEMF_zc | PB14 | M2_VOL+_U_ADC_1_IN5 | PB14 shared with other(3) |
| 51 | | Ph_Voltage+/BEMF_zc | PF13 | M2_VOL+_U_ADC_2_IN0 | PF13 shared with other(3) |
| 52 | | Ph_Voltage+/BEMF_zc | PC3 | M2_VOL+_U_ADC_12_IN9 | PC3 shared with other(3) |
| 53 | | Temperature/Board ID | PD13 | M2_TEMP_ADC_3_IN10 | PD13 shared with POSENC2 and ST morpho motor control functions(2) |
| 54 | | VBUS | PC2 | M2_VBUS_ADC_12_IN8 | PC2 shared with ST morpho motor control functions(2) |
| 55 | | Dissipative_brake | PG10 | M2_DissipativeBrake(GPIO) or M2_DissipativeBrake_TIM9_CH2 | - |
| 56 | - | DGND | - | GND | - |
| 57 | Motor3 | Emergency(BKIN) | PF7 | M3_EmergencySTOP_TIM_20_BKIN | - |
| 58 | | INH/PWM | PE2 | M3_PWM_UH_TIM_20_CH1 | - |
| 59 | | INH/PWM | PE3 | M3_PWM_VH_TIM_20_CH2 | - |
| 60 | | INH/PWM | PF2 | M3_PWM_WH_TIM_20_CH3 | - |
| 61 | | Master_EN | - | - | - |
| 62 | | Timer_ETR | - | - | - |
| 63 | | Hall_sensors_H1 | - | - | - |
| 64 | | Hall_sensors_H2 | - | - | - |
| 65 | - | DGND | - | GND | - |
| 66 | Motor3 | Shunt1+ | PB14 | M3_SHUNT1_ADC_1_IN5 | PB14 shared with other pins(3) |
| 67 | | Shunt2+ | PC3 | M3_SHUNT2_ADC_12_IN9 | PC3 shared with other pins(3) |

| Connector pin number | Category | Pin name | STM32 signal(1) | Function(1) | Comment |
|---|---|---|---|---|---|
| 68 | Motor3 | Shunt3+ | PF13 | M3_SHUNT3_ADC_2_IN0 | PF13 shared with other pins(3) |
| 69 | - | AGND | - | GND | - |
| 70 | Motor3 | Ph_Voltage+/BEMF_zc | - | - | - |
| 71 | | Ph_Voltage+/BEMF_zc | - | - | - |
| 72 | | Ph_Voltage+/BEMF_zc | - | - | - |
| 73 | | Temperature/Board ID | PA5 | M3_BoardID_ADC2_IN13 | PA5 shared with pin B-53 |
| 74 | | VBUS | - | - | - |
| 75 | | Dissipative_brake | - | - | - |
| 76 | - | DGND | - | GND | - |
| 77 | Motor1 | SD_CLKO/SPI_nSS | - | - | - |
| 78 | | SD_DIN/Enable | - | - | - |
| 79 | Motor2 | SD_CLKO/SPI_nSS | - | - | - |
| 80 | | SD_DIN/Enable | - | - | - |
| 81 | Motor3 | SD_CLKO/SPI_nSS | - | - | - |
| 82 | | SD_DIN/Enable | - | - | - |
| B side (top) | | | | | |
| 1 | SPI | SPI_MISO | PF0 | M_SPI_2_MISO | - |
| 2 | | SPI_MOSI | PF4 | M_SPI_2_MOSI | - |
| 3 | | SPI_MISO | - | - | - |
| 4 | | SPI_MOSI | - | - | - |
| 5 | - | 5V_to_CTRLB | - | P5V | - |
| 6 | - | VREF+ | - | 3V3 | - |
| 7 | - | DGND | - | GND | - |
| 8 | - | AGND | - | GND | - |
| 9 | ADC | ADC | - | - | - |
| 10 | | ADC | - | - | - |
| 11 | | ADC | - | - | - |
| 12 | Motor1 | Emergency(BKIN2) | PE14 | M1_EmergencySTOP_TIM_1_BKIN2 | - |
| 13 | | INL/EN | PE8 | M1_PWM_UL_TIM_1_CH1N | - |
| 14 | | INL/EN | PE10 | M1_PWM_VL_TIM_1_CH2N | - |
| 15 | | INL/EN | PE12 | M1_PWM_WL_TIM_1_CH3N | - |
| 16 | | Encoder_A | PB4 | M1_Encoder_A_TIM_3_CH1 | PB4 shared with other(6) |
| 17 | | Encoder_B | PC9 | M1_Encoder_B_TIM_3_CH2 | PC9 shared with other(6) |
| 18 | | Encoder_Z | PB3 | M1_Encoder_Z_TIM_3_ETR | PB3 shared with other(6) |
| 19 | | Hall_sensors_H3 | PC8 | M1_Hall_3_TIM_3_CH3 | - |
| 20 | - | DGND | - | GND | - |
| 21 | Motor1 | Shunt1- | PA3 | M1_SHUNT1_OPAMP_1_VIN0M | - |

| Connector pin number | Category | Pin name | STM32 signal(1) | Function(1) | Comment |
|---|---|---|---|---|---|
| 22 | Motor1 | Shunt2- | PC5 | M1_SHUNT2_OPAMP_2_VIN1M | - |
| 23 | | Shunt3- | PB10 | M1_SHUNT3_OPAMP_3_VIN1M | - |
| 24 | - | AGND | - | GND | - |
| 25 | Motor1 | Ph_Voltage-/BEMF_ref | - | GND | - |
| 26 | | Ph_Voltage-/BEMF_ref | - | GND | - |
| 27 | | Ph_Voltage-/BEMF_ref | - | GND | - |
| 28 | | Res.Ex/Curr.REF | PA4 | M1_DAC_1_OUT1 | - |
| 29 | | Resolver_Sin/ GPIO_BEMF | PB14 | M1_Resolver_Sin/ADC_1_IN5 | PB14 shared with other pins(3) |
| 30 | | Resolver_Cos | PF13 | M1_Resolver_Cos/ADC_2_IN0 | PF13 shared with other pins(3) |
| 31 | - | DGND | - | GND | - |
| 32 | - | AGND | - | GND | - |
| 33 | PFC | AC_zero_crossing | PE15 | M_AC zero crossing_ADC_3_IN2 | - |
| 34 | | PFC_Current2 | PD10 | M_PFC current 2_ADC_3_IN7 | - |
| 35 | | Inrush_lim. | PC10 | Inrush lim(GPIO) | - |
| 36 | | PFC_PWM2 | **PB5**/PF10 | **M_PFC_PWM2_TIM_16_CH1 or** M_PFC_PWM2_TIM_15_CH2 | PF10 shared with pin A-1 |
| 37 | Motor2 | Emergency(BKIN2) | PD1 | M2_EmergencySTOP_TIM_8_BKIN2 | - |
| 38 | | INL/EN | PA10 | M2_PWM_UL_TIM_8_CH1N | - |
| 39 | | INL/EN | PC11 | M2_PWM_VL_TIM_8_CH2N | - |
| 40 | | INL/EN | PC12 | M2_PWM_WL_TIM_8_CH3N | - |
| 41 | | Encoder_A | PB7 | M2_Encoder_A_TIM_2_CH1 | PB7 shared with other(6) |
| 42 | | Encoder_B | PD4 | M2_Encoder_B_TIM_2_CH2 | PD4 shared with other(6) |
| 43 | | Encoder_Z | PA9 | M2_Encoder_Z_TIM_2_ETR | PA9 shared together(6) |
| 44 | | Hall_sensors_H3 | PA9 | M2_Hall_3_TIM_2_CH3 | |
| 45 | - | DGND | - | GND | - |
| 46 | Motor2 | Shunt- | - | GND | - |
| 47 | | Shunt- | - | GND | - |
| 48 | | Shunt- | - | GND | - |
| 49 | - | AGND | - | GND | - |
| 50 | Motor2 | Ph_Voltage-/BEMF_ref | - | GND | - |
| 51 | | Ph_Voltage-/BEMF_ref | - | GND | - |
| 52 | | Ph_Voltage-/BEMF_ref | - | GND | - |
| 53 | | Res.Ex/Curr.REF | PA5 | M2_Res_Ex/DAC_2_OUT1 | PA5 shared with pin A-73 |
| 54 | | Resolver_Sin/ GPIO_BEMF | PD12 | M2_Resolver_Sin/ADC_3_IN9 | PD12 shared with POT(4) |
| 55 | | Resolver_Cos | PC3 | M2_Resolver_Cos/ADC_12_IN9 | PC3 shared with other pins(3) |
| 56 | - | AGND | - | GND | - |

| Connector pin number | Category | Pin name | STM32 signal(1) | Function(1) | Comment |
|---|---|---|---|---|---|
| 57 | Motor3 | Emergency(BKIN2) | PF8 | M3_EmergencySTOP_TIM_20_BKIN 2 | - |
| 58 | | INL/EN | PE4 | M3_PWM_UL_TIM_20_CH1N | - |
| 59 | | INL/EN | PE5 | M3_PWM_VL_TIM_20_CH2N | - |
| 60 | | INL/EN | PE6 | M3_PWM_WL_TIM_20_CH3N | - |
| 61 | | Encoder_A | - | - | - |
| 62 | | Encoder_B | - | - | - |
| 63 | | Encoder_Z | - | - | - |
| 64 | | Hall_sensor_H3 | - | - | - |
| 65 | - | DGND | - | GND | - |
| 66 | Motor3 | Shunt- | - | GND | - |
| 67 | | Shunt- | - | GND | - |
| 68 | | Shunt- | - | GND | - |
| 69 | - | AGND | - | GND | - |
| 70 | Motor3 | Ph_Voltage-/BEMF_ref | - | GND | - |
| 71 | | Ph_Voltage-/BEMF_ref | - | GND | - |
| 72 | | Ph_Voltage-/BEMF_ref | - | GND | - |
| 73 | | Res.Ex/Curr.REF | - | - | - |
| 74 | | Resolver_Sin/ GPIO_BEMF | - | - | - |
| 75 | | Resolver_Cos | - | - | - |
| 76 | - | AGND | - | GND | - |
| 77 | Motor1 | SD_DIN/Enable | PD3 | M1_ENABLE1(GPIO) | - |
| 78 | | SD_DIN/Enable | PG12 | M1_ENABLE2(GPIO) | - |
| 79 | Motor2 | SD_DIN/Enable | - | - | No enable for motor 2/3 |
| 80 | | SD_DIN/Enable | - | - | |
| 81 | Motor3 | SD_DIN/Enable | - | - | |
| 82 | | SD_DIN/Enable | - | - | |

1. *For multiple choice, the default configuration is in bold.*
2. *Refer to Section 7.9.4 for details.*
3. *Refer to Section 8.7.3, Section 8.7.4, Section 8.7.5, and Section 8.7.6 for details.*
4. *Before using motor control V2 connector pin 54 (as Resolver_Sin function), it is mandatory to move SB51 on SB52. Refer to Section 7.11.2 for details.*
5. *Ph_Voltage+/BEMF_zc of motor 1 can also be used in two ADCs mode, refer to Table 37.*
6. *Refer to Table 39.*

### 8.7.3 Hardware configuration for motor control V2 connector filters

Before using external resolver filters on a motor control V2 connector, check the required solder bridges configuration according to Table 36.

**Table 36. Hardware I/O configuration for resolver filters**

| I/O | Hardware | Setting(1) | Configuration |
|---|---|---|---|
| PB14 (ADC1_IN5) | SB14, SB15, SB16, SB17 | **SB17 ON, SB14/15/16 OFF** | **PB14 is used as the motor2 voltage phase 1** |

| I/O | Hardware | Setting[1] | Configuration |
|---|---|---|---|
| PB14 (ADC1_IN5) | SB14, SB15, SB16, SB17 | SB15 ON, SB14/16/17 OFF | PB14 is used as the motor3 current input 1 |
| | | SB14 ON, SB15/16/17 OFF | PB14 is used as the motor1 Resolver_Sin signal |
| | | SB16 ON, SB14/15/17 OFF | PB14 is used as the motor2 voltage phase 1 (from ST morpho motor control) |
| PF13 (ADC2_IN0) | SB18, SB19, SB20, SB21 | **SB21 ON, SB18/19/20 OFF** | **PF13 is used as the motor2 voltage phase 2** |
| | | SB19 ON, SB18/20/21 OFF | PF13 is used as the motor3 current input 3 |
| | | SB20 ON, SB18/19/21 OFF | PF13 is used as the motor1 Resolver_Cos signal |
| | | SB18 ON, SB19/20/21 OFF | PF13 is used as the motor2 voltage phase 2 (from ST morpho motor control) |
| PC3 (ADC12_IN9) | SB3, SB4, SB5, SB6 | **SB6 ON, SB3/4/5 OFF** | **PC3 is used as the motor2 voltage phase 3** |
| | | SB4 ON, SB3/5/6 OFF | PC3 is used as the motor3 current input 2 |
| | | SB5 ON, SB3/4/6 OFF | PC3 is used as the motor2 Resolver_Cos signal |
| | | SB3 ON, SB4/5/6 OFF | PC3 is used as the motor2 voltage phase 3 (from ST morpho motor control) |
| | | ALL OFF | PC3 may be used for the POSENC2 SPI selection function, refer to Table 20 |

1. *The default configuration is in bold.*

Before using external motor2 current input filters on motor control V2 connector, check the required solder bridges configuration according to Table 37:

**Table 37. Hardware I/O configuration for motor2 current input filters**

| I/O | Hardware | Setting [1] | Configuration |
|---|---|---|---|
| PB11 (ADC12_IN14) | SB89, SB91, SB93 | **SB91 ON, SB89/93 OFF** | **PB11 is used as the motor2 current input 1 signal** |
| | | SB93 ON, SB89/91 OFF | PB11 is used as the motor1 voltage phase 1 (2 ADCs mode) |
| | | SB89 ON, SB91/93 OFF | PB11 is used as the motor2 current input 1 (from ST morpho motor control) |
| PC1 (ADC12_IN7) | SB77, SB82, SB87 | **SB77 ON, SB82/87 OFF** | **PC1 is used as the motor2 current input 2 signal** |
| | | SB87 ON, SB77/82 OFF | PC1 is used as the motor1 voltage phase 2 (2 ADCs mode) |
| | | SB82 ON, SB77/87 OFF | PC1 is used as the motor2 current input 2 (from ST morpho motor control) |
| PA0 (ADC12_IN1) | SB83, SB85, SB86 | **SB83 ON, SB85/86 OFF** | **PA0 is used as the motor2 current input 3 signal** |
| | | SB86 ON, SB83/85 OFF | PA0 is used as the motor1 voltage phase 3 (2 ADCs mode) |
| | | SB85 ON, SB83/86 OFF | PA0 is used as the motor2 current input 3 (from ST morpho motor control) |

| I/O | Hardware | Setting (1) | Configuration |
|---|---|---|---|
| PD13 (ADC3_IN10) | SB110, SB111 | **SB110 ON, SB111 OFF** | **PD13 is used as M2_TEMP_ID from MC V2 connector** |
| | | SB111 ON, SB110 OFF | PD13 is used for ST morpho motor control connector function |
| PC2 (ADC2_IN8) | SB11, SB10 | **SB11 ON, SB10 OFF** | **PC2 is used as M2_VBUS from MC V2 connector** |
| | | SB10 ON, SB11 OFF | PC2 is used for ST morpho motor control connector function |

1. *The default configuration is in bold.*

### 8.7.4 Hardware configuration for motor control V2 connector PFC and SPI

Before using PFC and SPI on motor control V2 connector, check the required solder bridges configuration according to Table 38

**Table 38. Hardware I/O configuration for PFC and SPI**

| Function | Hardware | Setting(1) | Configuration |
|---|---|---|---|
| **PFC BKIN_OC** / POSENC2.EN (PD15 / PG2) | SB60, SB61, SB62, | **SB61 ON, SB60/62 OFF** | **PD15 is used for the PFC BKIN_OC: POSENC2.EN function cannot be used. Only one PFC PWM2 can be used, PFC PWM1 cannot be used (TIM15)** |
| | | SB61 OFF, SB60/62 ON | PG2 is used for the PFC BKIN_OC: POSENC2.EN can be used and both PFC PWM may be used on TIM15, SPI POSENC1 SEL cannot be used in that case on PF10. |
| PFC PWM2 / **SPI_NSS / SPI POSENC1 SEL** (PF10/PB5) | SB38, SB98, SB101 | **SB38/101 ON SB98 OFF** | **PF10 is used for SPI_NSS or for SPI POSENC1 SEL: only one PFC PWM can be used with PFC BKIN_OC (PFC PWM2 on PB5 TIM16)** |
| | | SB38/101 OFF SB98 ON | PF10 is used for PFC PWM2: SPI_NSS / SPI POSENC1 SEL cannot be used and PFC can use both PWM on TIM15. POSENC2.EN may be used (see above) |

1. *The default configuration is in bold.*

### 8.7.5 Encoder/Hall sensors motor control V2 connector solder bridges

Some solder bridges are present to allow isolation of M1 and M2 encoder and hall sensor signals coming from the motor control V2 connector. Refer to Table 39 for configuration details

**Table 39. M1 and M2 encoder/hall sensors solder bridges(2)**

| I/O | Hardware | Setting(1) | Configuration |
|---|---|---|---|
| PB4 (TIM3_CH1) | SB115, SB114 | **SB115 ON, SB114 OFF** | **PB4 is used as M1 Encoder_A from motor control V2 connector** |
| | | SB114 ON, SB115 OFF | PB4 is used as M1 Hall_H1 sensor from motor control V2 connector |
| PC9 (TIM3_CH2) | SB113, SB112 | **SB113 ON, SB112 OFF** | **PC9 is used as M1 Encoder_B from motor control V2 connector** |
| | | SB112 ON, SB113 OFF | PC9 is used for M1 Hall_H2 sensor from motor control V2 connector |
| PB3 (TIM3_ETR) | SB34, SB81 | **SB34 ON, SB81 OFF** | **PB3 is used as M1 Encoder_7 from motor control V2 connector** |
| | | SB81 ON, SB34 OFF | PB3 is used as a SWO debug signal |

| I/O | Hardware | Setting[1] | Configuration |
|---|---|---|---|
| PB7 (TIM2_CH1) | SB90, SB88 | **SB90 ON, SB88 OFF** | **PB7 is used as M2 Encoder_A from motor control V2 connector** |
| | | SB88 ON, SB90 OFF | PB7 is used for M2 Hall_H1 sensor from motor control V2 connector |
| PD4 (TIM2_CH2) | SB84, SB78 | **SB84 ON, SB78 OFF** | **PD4 is used as M2 Encoder_B from motor control V2 connector** |
| | | SB78 ON, SB84 OFF | PD4 is used for M2 Hall_H2 sensor from motor control V2 connector |
| PA9 (TIM2_CH2/TER) | SB79, SB80 | **SB79 ON, SB80 OFF** | **PA9 is used as M2 Encoder_Z from motor control V2 connector** |
| | | SB80 ON, SB79 OFF | PA9 is used for M2 Hall_H3 sensor from motor control V2 connector |

1. *The default configuration is in bold.*
2. *SB41/SB94/SB39 allows to connect motor control V2 connector M2 signals. To connect ST morpho motor control M2 signals on the same PIOs, connect SB35/SB99/SB104 instead. Refer to Table 26.*

### 8.7.6 I/O restriction on the features

**Warning:** *Due to the sharing of some I/Os of STM32G564QET3 by multiple peripherals, the following limitations apply in using the motor control V2 connector:*

- *The Motor2 (M2) cannot be operated simultaneously with the ST morpho motor control connectors (Motor2 also).*
- *The M2_Resolver sin (PD12) cannot be operated simultaneously with the potentiometer (refer to Table 24).*
- *The M2 Res_EX/Curr_REF cannot be operated simultaneously with the M3 temperature / Board ID*
- *The M2 temperature / Board ID cannot be operated simultaneously with the POSENC2 function*
- *TIM15 can be used on PFC with both PWM if POSENC2 is not used*
- *SPI interface can be used only if POSENC1 SPI is not used*
- *The M2 and M3 have no assigned enable GPIOs*

## 8.8 Terminal block connectors (CN2 and CN17)

CN2 and CN17 are 6-pin through-hole 3.81 mm pitch terminal blocks, shown in Figure 23. They can be connected to standard connection depending on the user application.

**Figure 23. Terminal block connector upper front view (CN2 and CN17)**

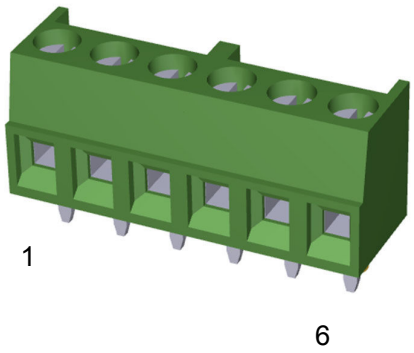



**Table 40. Terminal block pinout (CN2 and CN17)**

| Pin number | CN2 board function | CN17 board function |
|---|---|---|
| 1 | Vencoder | Vencoder2 |
| 2 | DSL2+ 2-wire with power or power line in 4-wire mode | 2_DSL2+ 2-wire with power or power line in 4-wire mode |
| 3 | DSL2- 2-wire with GND or GND line in 4-wire mode | 2_DSL2- 2-wire with GND or GND line in 4-wire mode |
| 4 | Ground | Ground |
| 5 | DSL4_P 4-wire mode positive differential signal | 2_DSL4_P 4-wire mode positive differential signal |
| 6 | DSL4_N 4-wire mode negative differential signal | 2_DSL4_N 4-wire mode negative differential signal |

# 9 STM32G564QET3 pin and GPIO assignment

Table 41 describes the STM32G564QET3 pins and GPIOs assignment according to three categories: Motor control V2 connector function, ST morpho motor control2 connection, and function and other board function.

*Note: The ADC input names are simplified as ADCx_INyy (they all refer to the ADCx_INPyy inputs).*

**Table 41. STM32G564QET3 GPIO and pin assignment(1)**

| STM32G564QET3 pin name | Pin function assignment | Other board function | Motor control V2 connector function | ST morpho motor control2 connection(2) (function) |
|---|---|---|---|---|
| PA0 | **ADC1_IN1 / ADC2_IN1** COMP3_IN1 | - | **M2.SHUNT3+** | Morpho-MC.L-34 (ADC1/2_IN1) |
| PA1 | **OPAMP1_VINP0** / COMP1_IN1 | - | **M1.SHUNT1+** | - |
| PA2 | **OPAMP1_VOUT** | - | **M1 Shunt1 out OPAMP1(3) to PC4** | - |
| PA3 | **OPAMP1_VINM0** / COMP2_IN2 | - | **M1.SHUNT1-** | - |
| PA4 | DAC1_OUT1 / **ADC2_IN17** | - | **M1.Res.Ex** | Morpho-MC.L-32 (CUR_REF) |
| PA5 | DAC2_OUT1 / **ADC2_IN13 /** TIM9_CH1 | - | **M2.Res.Ex / M3.Board_ID** | Morpho-MC.R-29 (STDBY / DAC / PWM) |
| PA6 | **OPAMP2_VOUT** | - | **M1 Shunt2 out OPAMP2 (3) to PC0** | - |
| PA7 | **OPAMP2_VINP0** / COMP2_IN1 | - | **M1.SHUNT2+** | - |
| PA8 | GPIO | - | **M2.Master_EN** | Morpho-MC.L-2 (GPIO) |
| PA9 | **TIM2_CH3 /** TIM2_ETR | - | **M2.Encoder_Z /** M2.Hall_H3 | Morpho-MC.R-25 (TIM2_CH3 / ETR) |
| PA10 | **TIM8_CH1N** | - | **M2.PWM_UL** | Morpho-MC.R-30 for CN10 pin 30 or 15 (TIM_UL) |
| PA11 | GPIO / **TIM13_CH1** | **User green LED** | - | - |
| PA12 | GPIO | - | - | Morpho-MC.R-1 (BEMF GPIO) |
| PA13 | **SWDIO** / JTMS | **SWDIO debug** | - | - |
| PA14 | **SWCLK** / JTCK | **SWCLK debug** | - | - |
| PA15 | GPIO | Analog switch control | - | - |
| PB0 | ADC1_IN15 / ADC3_IN12 | - | M1.SHUNT3+ option | - |
| PB1 | **OPAMP3_VOUT** | - | **M1 Shunt3 out OPAMP3 (3) to PB0** | - |
| PB2 | ADC2_IN12 | - | **M1.TEMP_ID** | - |
| PB3 | SWO / JTDO / **TIM3_ETR** | SWO trace | **M1.Encoder_Z** | - |
| PB4 | TIM3_CH1 | - | **M1.Encoder_A /** M1.Hall_H1 | - |
| PB5 | TIM16_CH1 | - | **PFC.PWM2** | - |
| PB6 | TIM8_CH2 | - | **M2.PWM_VH** | Morpho-MC.R-21 (TIM_VH) |

| STM32G564QET3 pin name | Pin function assignment | Other board function | Motor control V2 connector function | ST morpho motor control2 connection(2) (function) |
|---|---|---|---|---|
| PB7 | TIM2_CH1 | - | **M2.Encoder_A** / M2.Hall_H1 | Morpho-MC.L-17 (TIM2_CH1) |
| PB9 | TIM4_CH4 | - | - | Morpho-MC.R-22 (LED) |
| PB10 | OPAMP3_VINM1 | - | **M1.SHUNT3-** | - |
| PB11 | **ADC1_IN14** / **ADC2_IN14** / COMP6_IN1 | - | **M2.SHUNT1+** | Morpho-MC.L-30 (ADC1/2_IN14) |
| PB12 | **TIM1_BKIN** / ADC1_IN11 | - | **M1.Emergency** | Morpho-MC.R-6 for CN10 pin 6 or 15 (ADC1_IN11) |
| PB13 | **OPAMP3_VINP1** / COMP5_IN1 | - | **M1.SHUNT3+** | - |
| PB14 | ADC1_IN5 | - | M1.Resolver_Sin / **M2_VOL+_U** / M3_SHUNT1+ | Morpho-MC.L-38 (ADC1_IN5) |
| PB15 | ADC2_IN15 | - | **M1.VOL+_U** | - |
| PC0 | ADC1_IN6 / ADC2_IN6 | - | M1.SHUNT2+ option | - |
| PC1 | **ADC1_IN7** / **ADC2_IN7** / COMP3_IN2 | - | **M2.SHUNT2+** | Morpho-MC.R-18 for CN10 pin 18 or 24 or 17 (ADC1/2_IN7) |
| PC2 | **ADC1_IN8** / **ADC2_IN8** | - | **M2.VBUS** | Morpho-MC.L-28 (ADC1/2_IN8) |
| PC3 | **ADC1_IN9** / ADC2_IN9 / POSENC2_SEL | POSENC2 SPI | M2.Resolver_Cos / **M2_VOL+_W** / M3_SHUNT2+ | Morpho-MC.L-36 (ADC1/2_IN9) |
| PC4 | ADC2_IN5 | - | M1.SHUNT1+ option | - |
| PC5 | OPAMP2_VINM1 | - | **M1.SHUNT2-** | - |
| PC6 | TIM8_CH1 | - | **M2.PWM_UH** | Morpho-MC.R-23 (TIM_UH) |
| PC7 | TIM8_CH3 | - | **M2.PWM_WH** | Morpho-MC.R-33 (TIM_WH) |
| PC8 | TIM3_CH3 | - | M1.Hall_H3 | - |
| PC9 | TIM3_CH2 | - | **M1.Encoder_B** / M1.Hall_H2 | - |
| PC10 | GPIO | - | **PFC.Inrush_lim.** | - |
| PC11 | TIM8_CH2N | - | **M2.PWM_VL** | Morpho-MC.R-28 for CN10 pin 28 or CN7 pin 34 (TIM_VL) |
| PC12 | TIM8_CH3N | - | **M2.PWM_WL** | Morpho-MC.R-24 for CN10 pin 24 or 26 (TIM_WL) |
| PC13 | GPIO-WKUP4 | **User button** | - | Morpho-MC.L-23 (GPIO – WKUP4) |
| PC14 - OSC32_IN | **UART5_RX** / OSC32_IN | **VCP1_RX debug and bootloader** / LSE crystal IN | - | - |
| PC15 - OSC32_OUT | **UART5_TX** / OSC32_OUT | **VCP1_TX debug and bootloader** / LSE crystal OUT | - | - |

| STM32G564QET3 pin name | Pin function assignment | Other board function | Motor control V2 connector function | ST morpho motor control2 connection(2) (function) |
|---|---|---|---|---|
| PD0 | GPIO | - | - | Morpho-MC.L-3 (GPIO) |
| PD1 | TIM8_BKIN2 | - | **M2.Emergency(BKIN2)** | Morpho-MC.R-14 (TIM8_BKIN2) |
| PD2 | TIM8_BKIN | - | **M2.Emergency(BKIN)** | - |
| PD3 | GPIO | - | **M1.Enable1** | - |
| PD4 | TIM2_CH2 | - | **M2.Encoder_B /** M2.Hall_H2 | Morpho-MC.R-31 (TIM2_CH2) |
| PD5 | USART2_TX | **VCP2_TX bridge** | - | - |
| PD6 | USART2_RX | **VCP2_RX bridge** | - | - |
| PD7 | **TIM9_CH1** / GPIO | - | **M1.DissipativeBrake** | - |
| PD8 | ADC3_IN6 | - | **M1.VOL+_W** | - |
| PD9 | ADC3_IN15 | - | **PFC.AC_voltage** | - |
| PD10 | ADC3_IN7 | - | **PFC.Current2** | - |
| PD11 | ADC3_IN8 | - | **PFC.Current1** | - |
| PD12 | ADC3_IN9 | **User potentiometer** | M2.Resolver_Sin | - |
| PD13 | **ADC3_IN10 /** POSENC2_IN | POSENC2 | **M2.TEMP_ID** | Morpho-MC.R-34 (ADC3_IN10) |
| PD14 | ADC3_IN11 / POSENC2_OUT | POSENC2 | - | Morpho-MC.L-35 (ADC3_IN11) |
| PD15 | **TIM16_BKIN /** POSENC2_EN | POSENC2 | **PFC.BKIN_OC** | - |
| PE2 | TIM20_CH1 | - | **M3.PWM_UH** | - |
| PE3 | **TIM20_CH2** | - | **M3.PWM_VH** | - |
| PE4 | TIM20_CH1N | - | **M3.PWM_UL** | - |
| PE5 | **TIM20_CH2N** / GPIO | - | **M3.PWM_VL** | Morpho-MC.L-1 (GPIO) |
| PE6 | TIM20_CH3N | - | **M3.PWM_WL** | - |
| PE7 | TIM1_ETR | - | **M1.Timer_ETR** | - |
| PE8 | TIM1_CH1N | - | **M1.PWM_UL** | - |
| PE9 | TIM1_CH1 | - | **M1.PWM_UH** | - |
| PE10 | TIM1_CH2N | - | **M1.PWM_VL** | - |
| PE11 | TIM1_CH2 | - | **M1.PWM_VH** | - |
| PE12 | TIM1_CH3N | - | **M1.PWM_WL** | - |
| PE13 | TIM1_CH3 | - | **M1.PWM_WH** | - |
| PE14 | TIM1_BKIN2 | - | **M1.Emergency(BKIN2)** | - |
| PE15 | ADC3_IN2 | - | **PFC.AC_zero_crossing** | - |
| PF0 | SPI2_MISO / **POSENC1_MISO** | **POSENC1 SPI** | SPI.MISO | - |
| PF2 | **TIM20_CH3 /** POSENC2_MOSI | POSENC2 SPI | **M3.PWM_WH** | - |
| PF3 | SPI2_SCK / **POSENC1_SCK** | **POSENC1 SPI** | SPI.SCK | - |

| STM32G564QET3 pin name | Pin function assignment | Other board function | Motor control V2 connector function | ST morpho motor control2 connection(2) (function) |
|---|---|---|---|---|
| PF4 | SPI2_MOSI / **POSENC1_MOSI** | **POSENC1 SPI** | SPI.MOSI | - |
| PF7 | **TIM20_BKIN /** TIM5_CH2 / POSENC2_SCK | POSENC2 SPI | **M3.Emergency(BKIN)** | Morpho-MC.R-27 (CURR_REF) |
| PF8 | **TIM20_BKIN2 /** POSENC2_MISO | POSENC2 SPI | **M3.Emergency(BKIN2)** | - |
| PF9 | TIM15_CH1 | - | **PFC.PWM1** | - |
| PF10 | SPI2_NSS / **POSENC1_SEL** / TIM15_CH2 | **POSENC1 SPI** | SPI.NSS / PFC.PWM2 | - |
| PF11 | POSENC1_OUT | **POSENC1** | - | - |
| PF12 | POSENC1_IN | **POSENC1** | - | - |
| PF13 | ADC2_IN0 | - | M1.Resolver_Cos / **M2_VOL+_V** / M3_SHUNT3+ | Morpho-MC.L-37 (ADC2_IN0) |
| PF14 | POSENC1_EN | **POSENC1** | - | - |
| PF15 | ADC1_IN0 | - | **M1.VOL+_V** | - |
| PG2 | TIM15_BKIN | - | PFC.BKIN_OC | |
| PG3 | TIM8_ETR | - | **M2.Timer_ETR** | Morpho-MC.R-12 (CPOUT Stop_PWM) |
| PG4 | - | - | **-** | - |
| PG5 | - | - | **-** | - |
| PG9 | GPIO | HSE DISABLE_N | **-** | - |
| PG10 | **TIM9_CH2 /** GPIO | - | **M2.DissipativeBrake** | - |
| PG11 | TIM12_CH2 | **User red LED** | - | - |
| PG12 | GPIO | - | **M1.Enable2** | - |
| PG13 | GPIO | - | **M1.Master_EN** | - |
| PG14 | GPIO | - | **ID_Enable** | - |
| PH0-OSC_IN | OSC_IN | **24 MHz external oscillator** | - | - |
| PH1-OSC_OUT | ADC2_IN10 | - | **M1.VBUS** | - |
| PH5 | TIM17_CH1 | **User yellow LED** | - | - |
| NRST | NRST | **System reset** | - | - |
| BOOT0 | BOOT0 | **BOOT0 button** | - | - |
| VDD | VDD | **VDD_MCU** | - | - |
| VDDA | VDDA | **3V3** | - | - |
| VREFDAC+ | VREFDACP | **3V3** | - | - |
| VREF+ | VREFP | **3V3** | - | - |
| VCAP | VCAP | **Internal LDO** | - | - |
| VSS | VSS | **GND** | - | - |
| VSSA | AGND | **GND** | - | - |
| VREFDAC- | AGND | **GND** | - | - |

| STM32G564QET3 pin name | Pin function assignment | Other board function | Motor control V2 connector function | ST morpho motor control2 connection(2) (function) |
|---|---|---|---|---|
| VREF- | AGND | **GND** | - | - |

1. *The default setting is in bold. If multiple settings are bold in the same cell, it means that the user has multiple choices depending on his application*
2. *ST morpho motor control2 column gives the indication of pinout (L-34 stands for CN7 left connector pin 34, R-1 stands for CN10 right connector pin 1), and the indication of the assigned function (it can be multiple pin functions options or ST morpho motor control2 function name corresponding to a unique configuration).*
3. *Function description, which has no specific signal name in design (signal name is MCU pin name).*

# 10 B-G564E-MC1S product information

## 10.1 Product marking

The product and each board composing the product are identified with one or several stickers. The stickers, located on the top or bottom side of each PCB, provide product information:

- Main board featuring the target device: product order code, product identification, serial number, and board reference with revision.

  Single-sticker example:

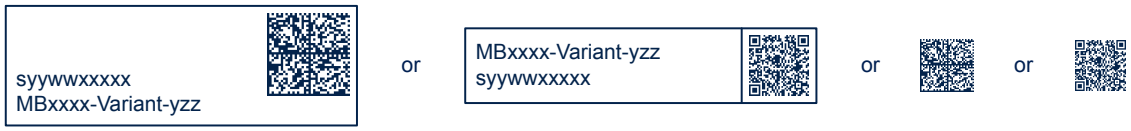
  
  

  Dual-sticker example:

- Other boards if any: board reference with revision and serial number.

  Examples:

On the main board sticker, the first line provides the product order code, and the second line the product identification.

On all board stickers, the line formatted as *"MBxxxx-Variant-yzz"* shows the board reference *"MBxxxx"*, the mounting variant *"Variant"* when several exist (optional), the PCB revision *"y"*, and the assembly revision *"zz"*, for example B01. The other line shows the board serial number used for traceability.

Products and parts labeled as *"ES"* or *"E"* are not yet qualified or feature devices that are not yet qualified. STMicroelectronics disclaims any responsibility for consequences arising from their use. Under no circumstances will STMicroelectronics be liable for the customer's use of these engineering samples. Before deciding to use these engineering samples for qualification activities, contact STMicroelectronics' quality department.

*"ES"* or *"E"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the ordering part number of the evaluation tool that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

## 10.2 B-G564E-MC1S product history

Table 42. **Product history**

| Order code | Product identification | Product details | Product change description | Product limitations |
|---|---|---|---|---|
| B-G564E-MC1S | BG564EMC1S$CR1 | MCU:<br>STM32G564QET3 silicon revision "A" | Initial revision | No limitation |
| | | MCU errata sheet:<br>*STM32G564xx, STM32G554xx, and STM32G553xx device errata* (ES0656) | | |
| | | Board:<br>• MB2070-G564QE-B02 (main board) | | |

## 10.3 Board revision history

Table 43. **Board revision history**

| Board reference | Board variant and revision | Board change description | Board limitations |
|---|---|---|---|
| MB2070 (main board) | G564QE-B02 | Initial revision | No limitation |

# 11 Compliance statements and conformity declarations

## 11.1 Federal Communications Commission (FCC) compliance statement

**Part 15.19**

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

**Part 15.21**

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

**Part 15.105**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

*Note: Use only shielded cables.*

**Responsible Party - U.S. Contact Information:**

Francesco Doddo
STMicroelectronics, Inc.
200 Summit Drive | Suite 405 | Burlington, MA 01803
USA
Telephone: +1 781-472-9634

## 11.2 Innovation, Science and Economic Development Canada (ISED) compliance statement

**This product complies with the ICES-003 standard class B of the ISED regulation.**

ISED Canada ICES-003 Compliance Label: CAN ICES (B)/NMB (B).

*Note: Use only shielded cables.*

**Ce produit est conforme à la norme NMB-003 classe B de la ISDE.**

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES (B) / NMB (B).

*Note: Utiliser uniquement des câbles blindés.*

## 11.3 UKCA conformity

**Simplified UK declaration of conformity**

Hereby, the manufacturer STMicroelectronics, declares that the equipment type B-G564E-MC1S is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK SI 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK SI 2012 No. 3032).

*Note: Use only shielded cables.*

## 11.4 CE conformity

### 11.4.1 Simplified EU declaration of conformity

Hereby, STMicroelectronics declares that the equipment type B-G564E-MC1S is in compliance with directives 2011/53/EU and 2015/863/EU (RoHS), and 2014/30/EU (EMC).

*Note:*
- *RoHS: Restriction of hazardous substances*
- *EMC: Electromagnetic compatibility*

*Note: Use only shielded cables.*

### 11.4.2 Déclaration de conformité UE simplifiée

STMicroelectronics déclare que l'équipement électrique du type B-G564E-MC1S est conforme aux directives 2011/53/UE et 2015/863/UE (LdSD), et à la directive 2014/30/UE (CEM).

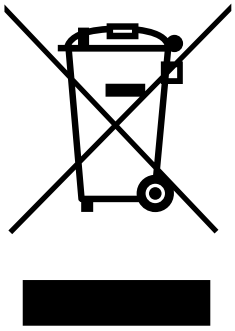
*Note:*
- *LdSD : directive sur la limitation de l'utilisation des substances dangereuses*
- *CEM : compatibilité électromagnétique*

*Note: Utiliser uniquement des câbles blindés.*

# 12 Product disposal

**Disposal of this product: WEEE (Waste Electrical and Electronic Equipment)**

(Applicable in Europe)



This symbol on the product, accessories, or accompanying documents indicates that the product and its electronic accessories must not be disposed of with household waste at the end of their working life.

To prevent possible harm to the environment and human health from uncontrolled waste disposal, separate these items from other types of waste and recycle them responsibly at a designated collection point to promote the sustainable reuse of material resources.

Household users:

Contact the retailer that you purchased the product from or your local authority for details of your nearest designated collection point.

Business users:

Contact your dealer or supplier for further information.

# Revision history

Table 44. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 26-Oct-2026 | 1 | Initial release. |

# Contents

1 **Features** . . . . . 2
2 **Ordering information** . . . . . 3
2.1 Codification . . . . . 3
3 **Development environment** . . . . . 4
3.1 System requirements . . . . . 4
3.2 Development toolchains . . . . . 4
3.3 Demonstration software . . . . . 4
3.4 EDA resources . . . . . 4
4 **Conventions** . . . . . 5
5 **Safety recommendations** . . . . . 6
5.1 Targeted audience . . . . . 6
5.2 Handling the board . . . . . 6
5.3 Delivery recommendations . . . . . 6
5.4 Power supply . . . . . 6
6 **Quick start** . . . . . 7
6.1 Getting started . . . . . 7
6.2 Default board configuration . . . . . 7
7 **Hardware layout and configuration** . . . . . 8
7.1 Hardware layout . . . . . 8
7.2 Mechanical dimensions . . . . . 10
7.3 Embedded STLINK-V3EC . . . . . 11
7.3.1 Description . . . . . 11
7.3.2 STLINK-V3EC drivers . . . . . 12
7.3.3 STLINK-V3EC firmware upgrade . . . . . 13
7.3.4 STLINK-V3EC deactivation (reset mode) . . . . . 13
7.4 Power supply . . . . . 13
7.4.1 Power supply architecture . . . . . 13
7.4.2 5 V power source selection . . . . . 14
7.4.3 STM32 microcontroller power . . . . . 16
7.5 Clock sources . . . . . 17
7.6 Boot options . . . . . 17
7.6.1 BOOT0 pin . . . . . 17
7.6.2 Other memory boot location . . . . . 18
7.7 LEDs . . . . . 18

7.7.1 Description . . . 18
7.8 Push-buttons . . . 18
7.8.1 Description . . . 18
7.8.2 Push-buttons input I/O interface . . . 19
7.9 Position encoder (POSENC1 and POSENC2) . . . 19
7.9.1 Overview description . . . 19
7.9.2 POSENC functions mode and configuration . . . 20
7.9.3 Microcontroller physical input I/O interface . . . 22
7.9.4 POSENC functions solder bridge and jumper configuration . . . 24
7.10 Operational amplifier . . . 25
7.10.1 Description . . . 25
7.10.2 Operational amplifier interface . . . 25
7.11 Analog input potentiometer . . . 26
7.11.1 Description . . . 26
7.11.2 Potentiometer solder bridge . . . 26
7.12 Jumpers and solder bridges . . . 26
7.12.1 Jumpers . . . 26
7.12.2 Solder bridges . . . 27
**8 Board connectors . . . 31**
8.1 USB Type-C® receptacle connector (CN1) . . . 31
8.2 MIPI10 USART connector (CN3) . . . 32
8.3 STDC14 and USART connectors . . . 33
8.3.1 SWD debug/program/trace and JTAG/UART/USART . . . 33
8.3.2 Using an external debug tool to program and debug the onboard STM32 . . . 34
8.4 STDC14 debug connector (CN4) . . . 34
8.5 ST morpho motor control connectors (CN7 and CN10) . . . 35
8.5.1 Description . . . 35
8.5.2 ST morpho motor control pinout . . . 36
8.5.3 Hardware configuration description of the ST morpho motor control page . . . 40
8.6 GND connector (CN5, CN6, CN14, CN18) . . . 41
8.7 Motor control V2 connector (CN9) . . . 41
8.7.1 Description . . . 41
8.7.2 Pinout . . . 41
8.7.3 Hardware configuration for motor control V2 connector filters . . . 46
8.7.4 Hardware configuration for motor control V2 connector PFC and SPI . . . 48
8.7.5 Encoder/Hall sensors motor control V2 connector solder bridges . . . 48
8.7.6 I/O restriction on the features . . . 49

8.8 Terminal block connectors (CN2 and CN17) . . . 50
**9 STM32G564QET3 pin and GPIO assignment . . . 51**
**10 B-G564E-MC1S product information . . . 56**
10.1 Product marking . . . 56
10.2 B-G564E-MC1S product history . . . 57
10.3 Board revision history . . . 57
**11 Compliance statements and conformity declarations . . . 58**
11.1 Federal Communications Commission (FCC) compliance statement . . . 58
11.2 Innovation, Science and Economic Development Canada (ISED) compliance statement . . . 58
11.3 UKCA conformity . . . 58
11.4 CE conformity . . . 59
11.4.1 Simplified EU declaration of conformity . . . 59
11.4.2 Déclaration de conformité UE simplifiée . . . 59
**12 Product disposal . . . 60**
**Revision history . . . 61**
**List of tables . . . 65**
**List of figures . . . 66**

# List of tables

Table 1. Ordering information . . . 3
Table 2. Codification explanation . . . 3
Table 3. ON/OFF convention . . . 5
Table 4. Default jumper configuration . . . 7
Table 5. STLINK-V3EC interface with STM32G564QE . . . 12
Table 6. Solder bridge configuration for STLINK-V3EC . . . 12
Table 7. STLK NRST configuration (JP1) . . . 13
Table 8. 5 V power source selection . . . 14
Table 9. VDDA, VREFP, and VREFDACP configuration options . . . 16
Table 10. OPREF configuration options . . . 17
Table 11. Hardware IO configuration for the LEDs . . . 18
Table 12. Hardware IO configuration for the push-buttons . . . 19
Table 13. POSENC1 function mode and configuration description . . . 21
Table 14. POSENC1 connectors pinout (CN2 terminal block and CN8 probing/power access) . . . 21
Table 15. POSENC2 function mode and configuration description . . . 22
Table 16. POSENC2 connectors pinout (CN17 terminal block and CN15 probing/power access) . . . 22
Table 17. CN12 pinout description for POSENC1 digital interface . . . 23
Table 18. CN16 pinout description for POSENC1 SPI interface (also SPI2 of MC V2) . . . 23
Table 19. CN13 pinout description for POSENC2 digital interface . . . 23
Table 20. Description of SPI POSENC2 interface (on through hole test points) . . . 24
Table 21. Solder bridge configuration for POSENC functions . . . 24
Table 22. POSENC jumpers configuration . . . 24
Table 23. Hardware I/O configuration for the OPAMP interface . . . 25
Table 24. Hardware I/O configuration for the potentiometer . . . 26
Table 25. Jumper configuration . . . 26
Table 26. Solder bridge configuration . . . 27
Table 27. USB STLK connector signal assignment (CN1) . . . 32
Table 28. MIPI10 USART connector pinout (CN3) . . . 32
Table 29. Debug/program/trace and JTAG/UART/USART interface overview . . . 33
Table 30. Default STM32G564QE MCU interface to external debug tools . . . 34
Table 31. STDC14 debug connector pinout (CN4) . . . 35
Table 32. ST morpho motor control connector (CN7) . . . 37
Table 33. ST morpho motor control connector (CN10) . . . 39
Table 34. Hardware configuration description of the ST morpho motor control page . . . 40
Table 35. Motor control V2 connector . . . 41
Table 36. Hardware I/O configuration for resolver filters . . . 46
Table 37. Hardware I/O configuration for motor2 current input filters . . . 47
Table 38. Hardware I/O configuration for PFC and SPI . . . 48
Table 39. M1 and M2 encoder/hall sensors solder bridges(2) . . . 48
Table 40. Terminal block pinout (CN2 and CN17) . . . 50
Table 41. STM32G564QET3 GPIO and pin assignment(1) . . . 51
Table 42. Product history . . . 57
Table 43. Board revision history . . . 57
Table 44. Document revision history . . . 61

# List of figures

Figure 1. B-G564E-MC1S top view . . . 1
Figure 2. B-G564E-MC1S bottom view . . . 1
Figure 3. B-G564E-MC1S block diagram . . . 8
Figure 4. B-G564E-MC1S board layout (top view) . . . 9
Figure 5. B-G564E-MC1S mechanical drawing top layout . . . 10
Figure 6. B-G564E-MC1S mechanical drawing bottom layout . . . 11
Figure 7. STLK NRST default configuration (JP1) . . . 13
Figure 8. Power diagram . . . 14
Figure 9. P5V (JP2) from motor control V2 connector (CN9) . . . 15
Figure 10. STLK (JP2) from USB STLK (CN1) . . . 16
Figure 11. E5V (JP2) from ST morpho motor control connector (CN7) . . . 16
Figure 12. BOOT0 (B3) and NRST (B2) push-buttons . . . 18
Figure 13. POSENC1 and POSENC2 overview . . . 20
Figure 14. SPI POSENC2 test points position . . . 23
Figure 15. USB Type-C® receptacle connector front view (CN1) . . . 31
Figure 16. USB Type-C® connector pinout (CN1) . . . 31
Figure 17. USB Type-C® top layer footprint pinout (CN1) . . . 32
Figure 18. MIPI10 USART connector pinout (CN3) . . . 33
Figure 19. STDC14 connector pinout (CN4) . . . 35
Figure 20. ST morpho motor control configuration on MB2070 . . . 36
Figure 21. CN7 and CN10 connector pinout . . . 37
Figure 22. PCIEx16 gold finger pinout (top side, CN9B) . . . 41
Figure 23. Terminal block connector upper front view (CN2 and CN17) . . . 50

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved