AN4407
Application note

Advantage of the use of an added driver source lead in discrete Power MOSFETs

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Introduction

In modern power supply design, more and more attention is given to the electrical efficiency of an overall system and to the junction temperature of semiconductor devices handling all the power to be converted into a usable form.

Among all the semiconductor devices, transistors are by far the most important category; almost all of them are three pin devices (MOSFET, BJT, IGBT) and, as opposed to diodes, they have a driving section which makes them more sensitive to issues related to the interaction between power to handle and input signal. Even if this document focuses on Power MOSFETs, in some cases the results could be extended to other power transistors depending on the current level to be switched and on the switching speed. The aim of this document is to illustrate the limitation related to a 3-pin device and detail the advantages of using a fourth driving source pin, also known as Kelvin source, besides the traditional power source.

In a 3-pin device, during every switching (turn-on or turn-off) cycle, the stray inductance of the source wire bonding coupled with the slope of the current being interrupted always generates a voltage signal opposite to the driving signal (V_{GS}) of a MOSFET, in our case. The effect of this opposing signal is to slow down the switching cycle, which in turn increases the cycle by cycle switching loss. The introduction of the Kelvin source pin allows separating the path of the power from that of the driving signal and to refer the driving network to the Kelvin source, where no current is supposed to flow. In this situation, it is possible to obtain a driving signal which is immune to any disturbance deriving from the verylarge and fast current variation flowing though the power path. This results in the reduction of the overall power loss in the transistor, and consequently a lower operating temperature and potentially more reliable and longer lasting power systems.

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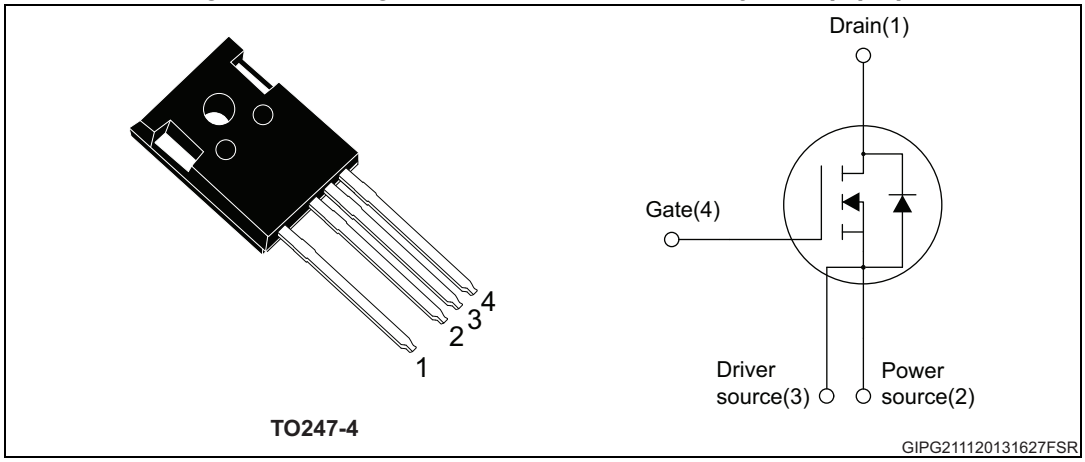
1 Description

The aim of the following paper is to illustrate the analysis evaluating the performance of the STMicroelectronics MDmeshM5 super-junction MOSFET housed in a TO247-4 package with an additional driving pin.

The new electrical symbol and package are shown in *Figure 1*. Note the repositioned drain, source and gate pins to allow the introduction of the Kelvin pin (pin 3), always ensuring the right creepage distance.

Figure 1. Package silhouette and electrical symbol (4 pin)



A demonstration power board (*Figure 2*) was created for test purposes, which implements a 2 kW PFC designed for industrial applications, using a FOT (Fixed-Off-Time) control patented by ST. The PFC stage functions mainly in CCM and can be supplied directly from AC mains between 185 and 265 V_{RMS} to provide a 400 V stable and regulated DC bus. This system was chosen because it allows investigation of the parasitic effect on the switching system. Furthermore, the working CCM properties allow investigation of both the on and off switching operations. *Table 1*shows the principal electrical specifications.

Table 1. Electrical characteristics

Parameter	Value
V_{in}	from 185 V_{ac} to 265 V_{ac}
Line frequency	50 Hz
Output voltage	400 V_{dc}
Max output voltage	2000 W
Output voltage ripple	5%
Max switching frequency	55 kHz
Ripple (Kr) inductor current	0.25
IC in used	L6563

Figure 2. Demo board of PFC 2 kW using MOSFETs in TO247-4 (4 pin)

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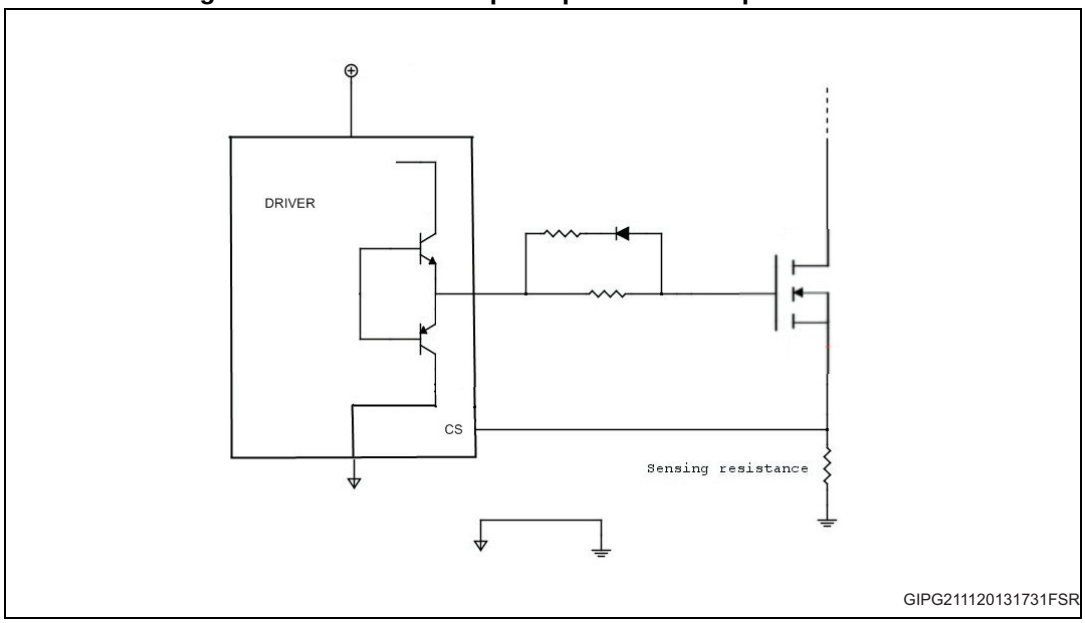
1.1 Approach to the study

Usually, in electronic power systems, a feedback network is implemented to create a control of the electrical parameters (for the DC/DC converter, this can involve both the output voltage and output current or only one of these). In order to control the current on the system, a resistor is often connected in series to the line under control, forming a common path between the input and output network. The information coming from this element, (voltage across the sensing resistor) is used as the control signal and sent to the pin of the driver. This pin is connected to an input of the internal comparator inside the driver; it's output signal is used to regulate the conduction time of the power switch.

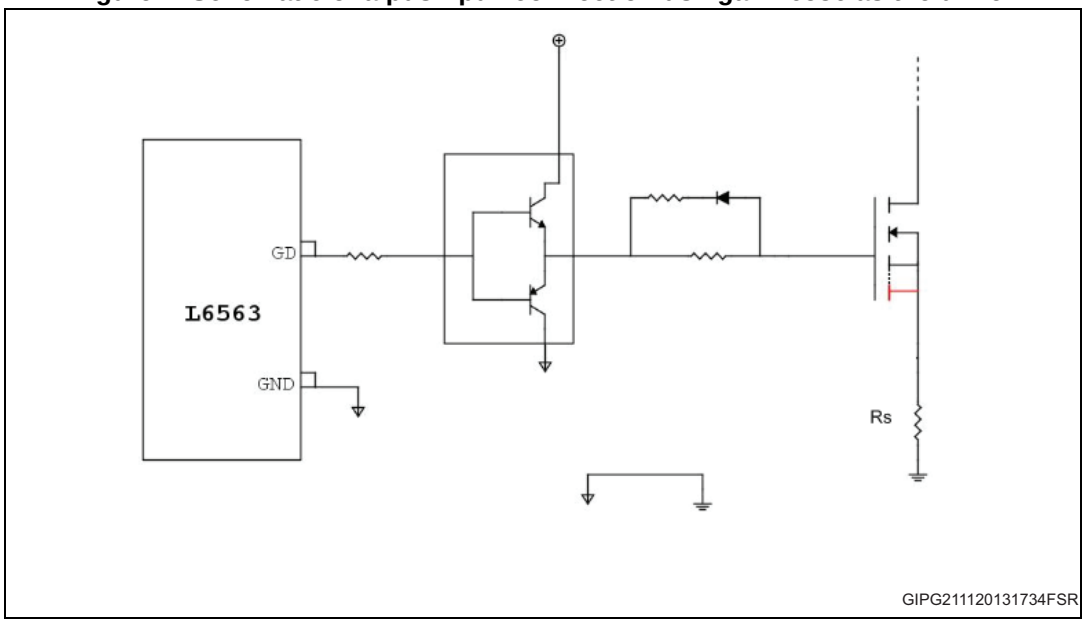
When the power switch requires particular source/sink current values, the drivers are created with a push-pull on the output (*Figure 3*). The feedback type is known as current sampling series-mixing, which offers the main benefit of increasing the input impedance, while the drawback lies in the impact of the output net on the driving circuitry. A possible way to reduce the latter phenomenon is to separate the input circuit from the output one, which is along the lines of the solution proposed by STMicroelectronics.

Figure 3. Schematic of a push-pull driver for power device



A current amplifier solution can be integrated directly inside the driver or put in series with the output driver externally. This solution is used on the demo board made by STMicroelectronics. Since the L6563 driver used on the demo needs a sensing signal for current control, a resistor is put in series with the source of the power device (*Figure 4*).

Figure 4. Schematic of a push-pull connection usingan L6536 as the driver



This solution necessitates a slight modification on the driving network to correctly use the new device with the added sensing pin. In fact, if we directly replace the standard 3-pin TO-247 MOSFET with the 4-pin version (TO247-4), we risk short-circuiting the sensing resistor and losing any information coming from it (*Figure 5*).

Figure 5. Risk of short-circuiting the sensing resistor

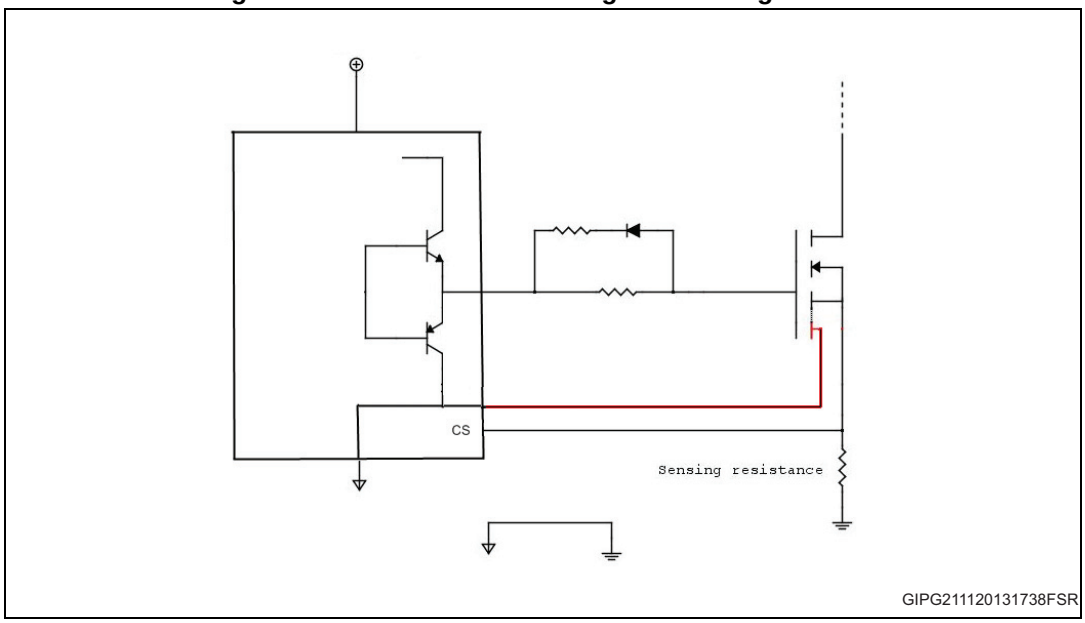
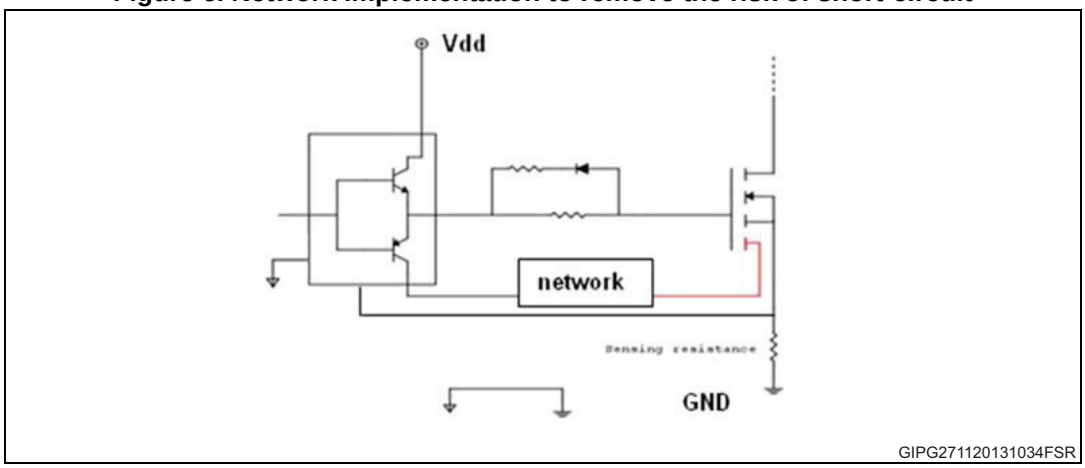


Figure 6 shows that, as the connection to the ground of the push-pull buffer circuit grounds the sensing source pin, and since the power source pin is shorted internally with it, the connection creates a short circuit for the sensing resistor.

So, when a 4-pin package is used, special precautions must be applied in order to preserve system functionality (*Figure 6*).

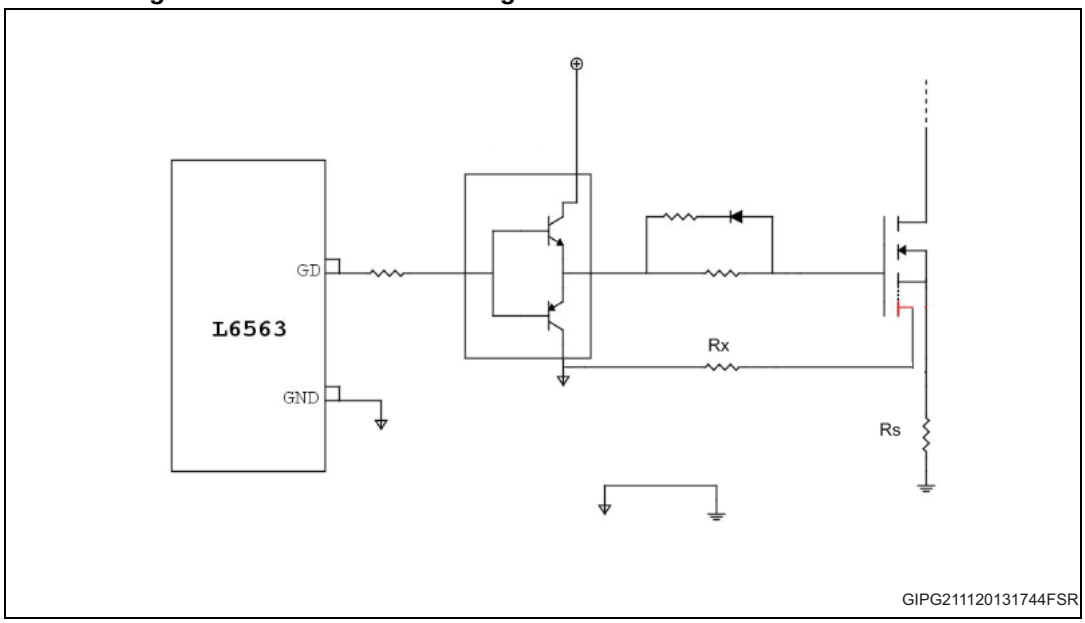
Figure 6. Network implementation to remove the risk of short-circuit



The following solution is implemented on the ST demo board:

- In the system, the value of the sensing resistor Rs is 18 mΩ (*Figure 4*).
- When using a 4-pin MOSFET, the connection shown in *Figure 7* is applied to remove the possibility of creating a short-circuit on Rs.

Figure 7. Section of the driving network related to the demo board



It is important to ensure that the current flowing through Rx is negligible compared to the current flowing through the sensing resistor Rs.

Hence, a 1Ω resistor was chosen.

1.2 Parasitic inductance effects

Usually, to drive the fast switching super-junction MOSFET, it is necessary to reduce the impact of the package and the parasitic effects introduced by the layout. This aspect is well known for low voltage MOSFETs where high current values are commonly detected. But what happens when a high voltage device is used on an application where clearance and creepage distance requirements must be considered?

This section demonstrates the impact of the parasitic inductance of the single source lead deriving from the connection of the lead with the die (*Figure 8* and *Figure 9*).

The impact of the package is limited by the internal wire bonding. There are several ways to calculate the magnitude of this effect, the first being to analyze the parasitic inductance due to a wire.

Figure 8. Picture of the wires bonding used on power device

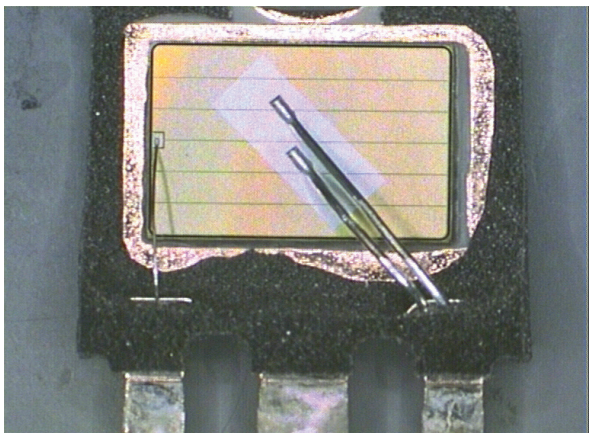


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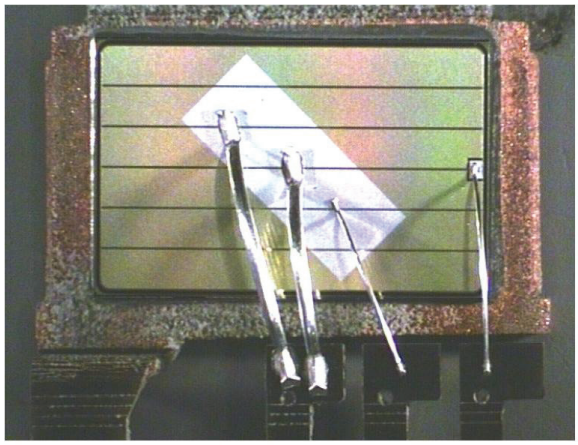
Figure 9. Picture of the wires bonding used on power device with 4 pin



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If we use the relationship below:

Equation 1

$$L = l(\ln\frac{4l}{d} \quad 1) \times 200 \times 10^{\ 9}$$

where l is the length and d the diameter of a wire, we can estimate the stray inductance of the source wire bonding linked to a single connection as:

Equation 2

$$l \approx 12 \quad 10^{\ 3} m$$

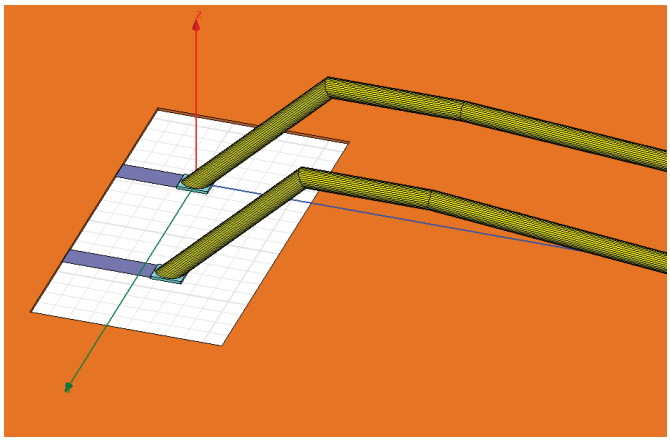
$$d = 15mls = 0.381 \quad 10^{\ 3} m$$

Equation 3

$$L = l(\ln\frac{4l}{d} \quad 1) \times 200 \times 10^{\ 9} \approx 9{,}2nH$$

The second method involves estimating the value of Ls using a simulation tool. A HFSS Electromagnetic simulator tool gave the following results after factoring in the data regarding the length and section of a wire bonding:

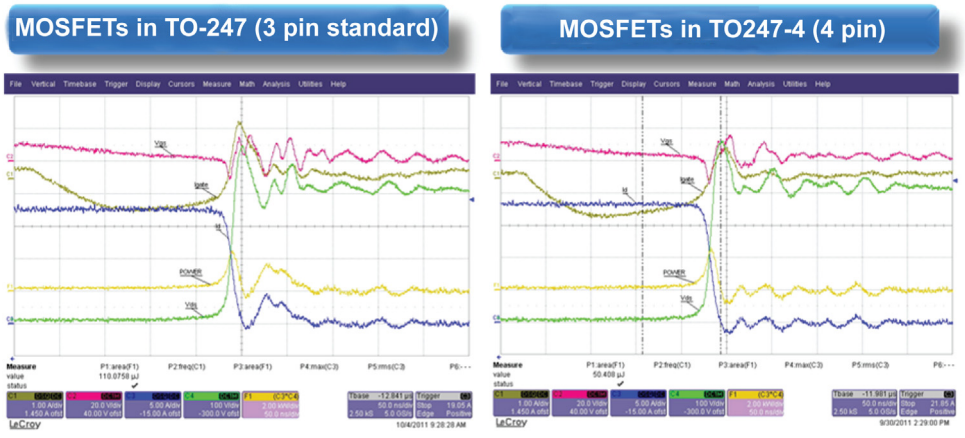
Figure 10. Wires bonding for the HFSS tool



In this case, the simulations return a value of 8.9 nH.

This data is confirmed by the measurements performed on the bench. *Figure 11* shows the computation of the parasitic inductance at around 4 nH because, in this case, the source path is realized using two wires in parallel.

Figure 11. Wires bonding for the HFSS tool

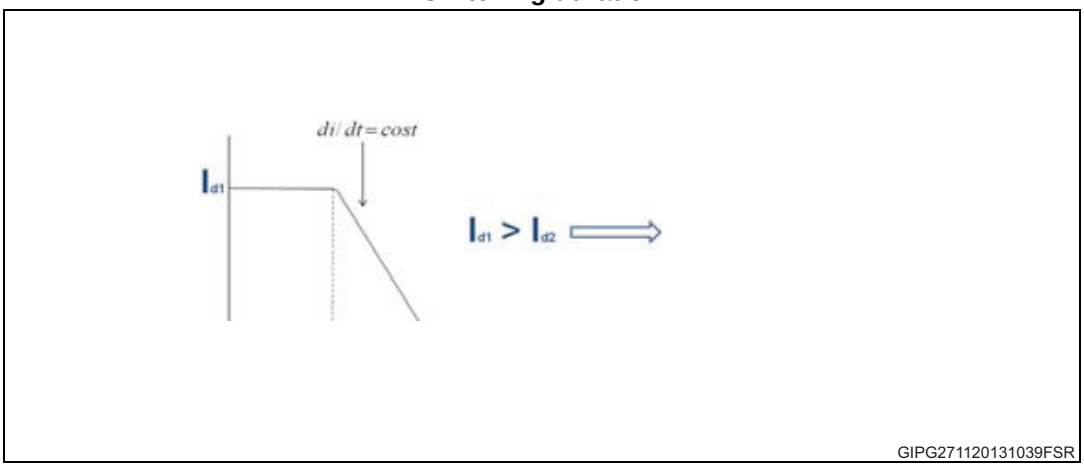


Given this data, we can proceed with the study of its impact on the system.

Before looking at the influence of the parasitic inductance on the switching commutations, consider a commutation on the inductive load: the influence of the inductive parasitic effect is associated with the slope of the current during the switching phase as well as the time of the commutation.

In others words, for a fixed value of Ld, (when di/dt is constant), the delay time is more and more evident when the output power increases and the switching current level also increases (*Figure 12*).

Figure 12. Relationship between stray inductance parasitic effect and current switching duration

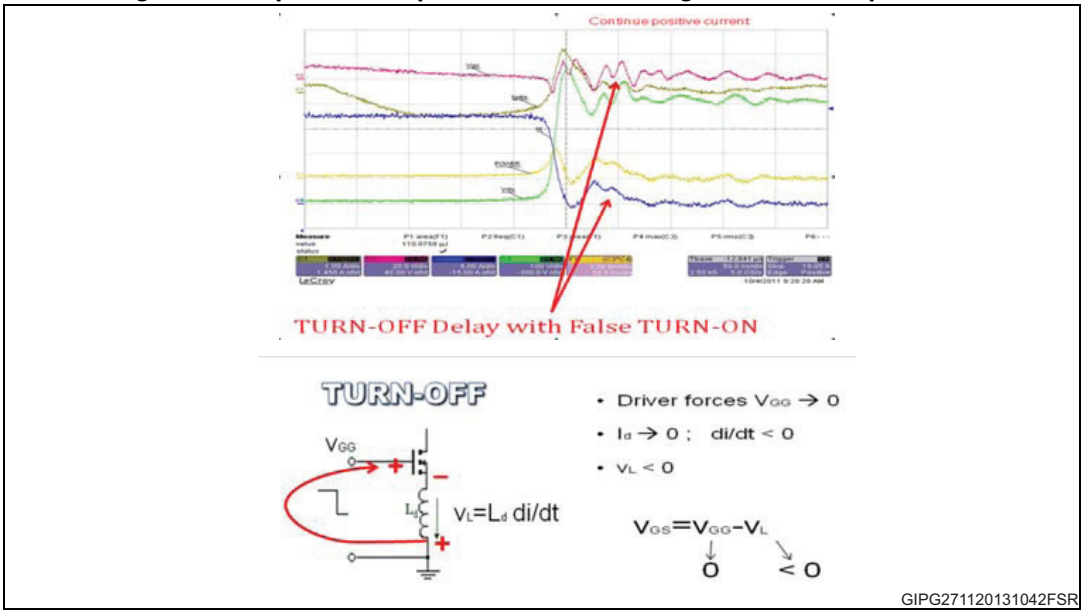


This theoretical situation is confirmed by experimental data during the switching instants for both turn-off and turn-on.

1.2.1 Turn-off

If we refer to *Figure 13*, which shows a turn-off at high power levels, when the driver forces V_{GG}=0 V, the MOSFET is forced to turn off, but the negative extra-voltage generated over the stray inductance introduces a turn-off delay and consequently higher turn-off switching losses. This can even lead to false turn-on phenomena, which can further increase the turn-off switching power dissipation.

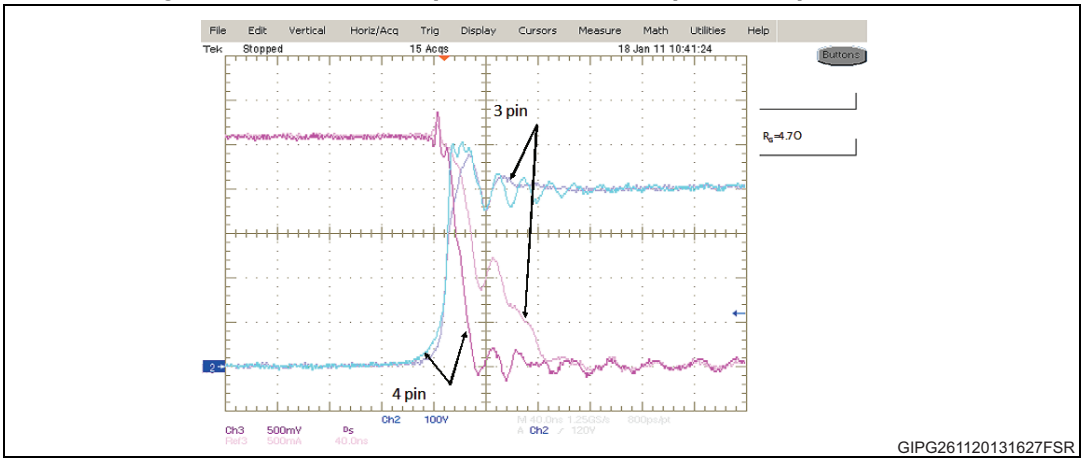
Figure 13. Impact of the parasitic effect during the turn-off operation



In fact, the real voltage across the gate and source pin, equal to the difference between the driving voltage and the parasitic overvoltage, becomes positive and fully equivalent to the extra voltage generated.

This aspect is confirmed by the waveform comparisons between the tests with a standard 3-pin solution and the 4-pin alternative. In *Figure 14*, this specific aspect is shown.

Figure 14. Turn-off comparison between 3 pin and 4 pin solution



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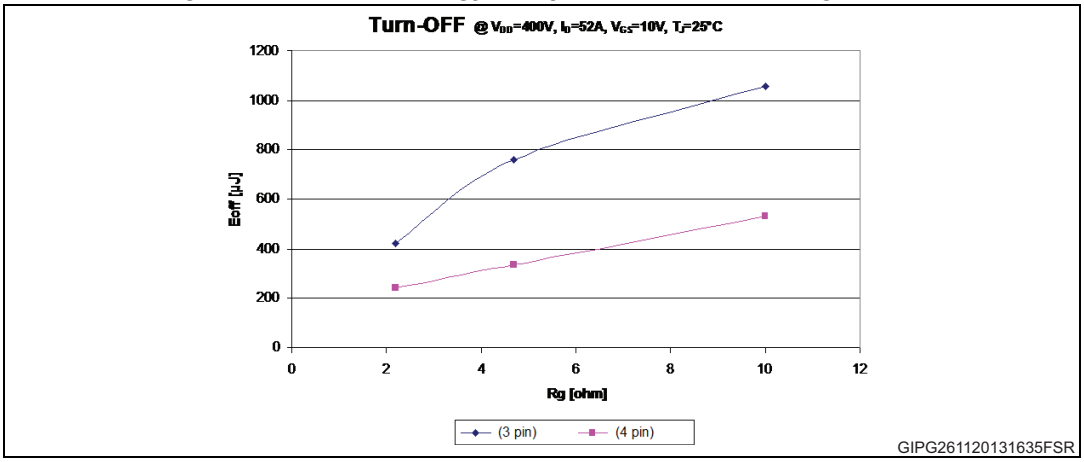
The improvement in terms of reduction of power loss is also present when the value of R_{GATE} is changed, accelerating or delaying the switching operations.

Figure 15. Turn-off energy comparison @ different Rg values



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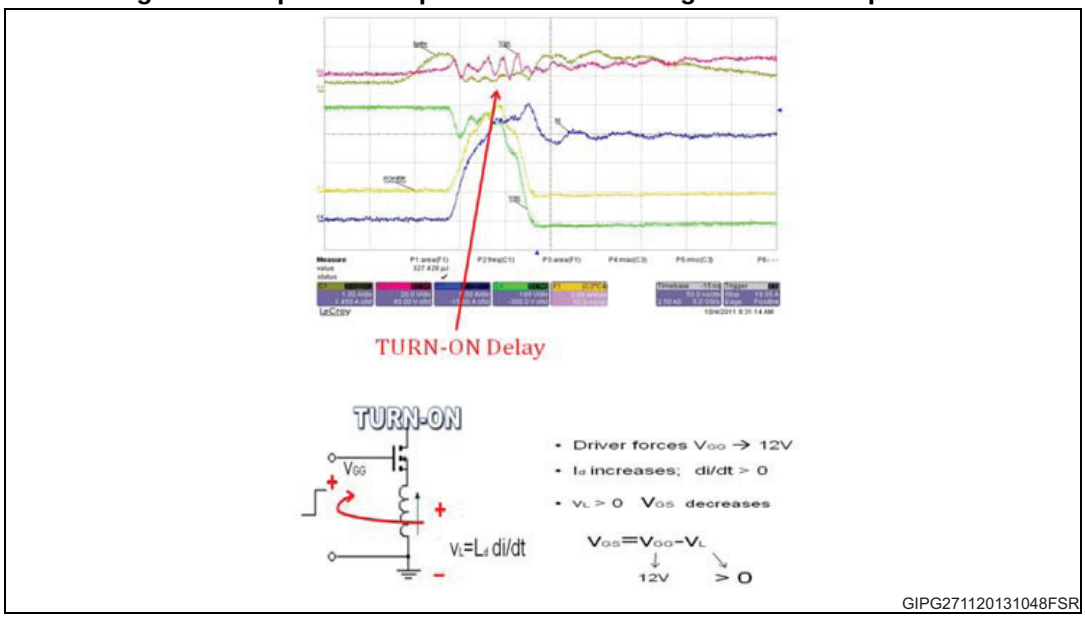
1.2.2 Turn-on

Also for the turn-on situation, when the driver forces V_{GG}=12 V and the MOSFET turns on, the positive extra-voltage generated over the stray inductance introduces a turn-on delay, reducing the effective value of V_{GS} with consequently higher turn-on switching losses and increased total switching power dissipation (*Figure 16*).

Figure 16. Impact of the parasitic effect during the turn-on operation



In this case, the real voltage across the gate and source pin becomes lower than the set positive threshold necessary to fully turn-on the device because the extravoltage generates a negative contribution. This aspect is confirmed by the waveform comparisons between the standard 3-pin solution and the 4-pin alternative in *Figure 17* and *Figure 18*.

1.3 Comparison analysis between 3-pin and 4-pin devices in efficiency and temperature; turn-on and turn-off energy at different output powers

The effect of the analyzed solution is the reduction of the overall power loss in the transistor, which translates into lower operating temperatures and potentially more reliable and longer lasting power systems. In the previous sections, we have seen the effects of the parasitic inductance on the single switching instant. In order to understand the total effect on the whole system, a deeper analysis has been performed on the system at different output power levels for thermal and energy saving aspects.

The following graphs give the comparative switching energy data for different power levels, using both the 3-pin and 4-pin solutions.

Figure 17. Switching energy comparison @ 500 W and 1 kW(a)

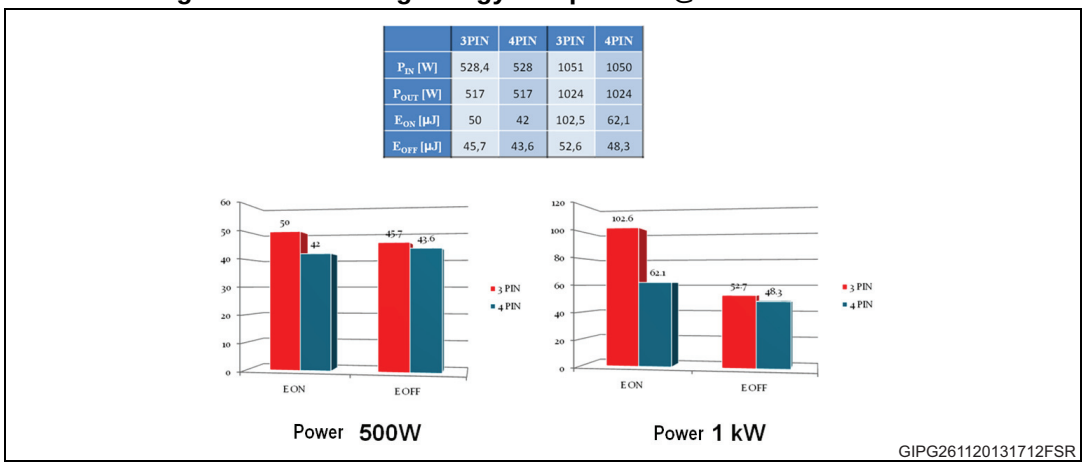


Figure 18. Switching energy comparison @ 1.5 kW and 2kW(a)

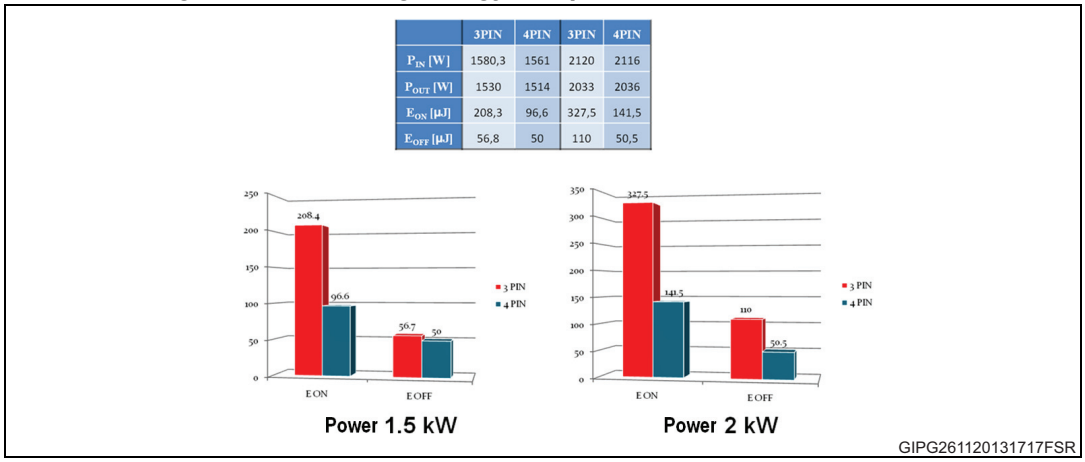
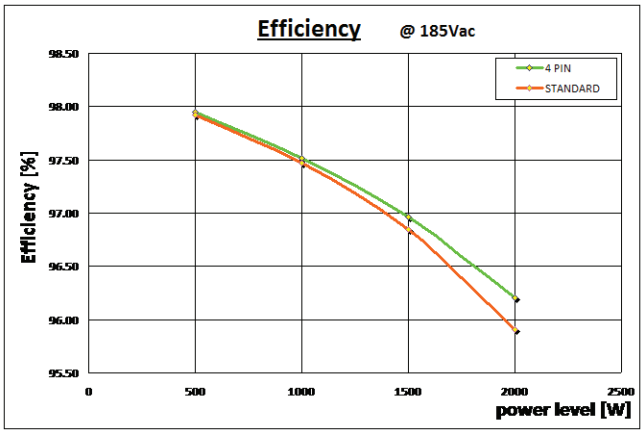


Figure 17 and *Figure 18* demonstrate that the new solution has more impact when the power level, and hence the current, are very high. In particular, the reduction of the on-switching loss is always present and increases with the power level, while the drop in the off-switching loss becomes more evident when the power level increases.

The new solution is therefore always advantageous across the entire power spectrum and, in a market which is always seeking energy saving solutions, it allows the attainment of new thermal and efficiency targets.

a. For MDmesh M5 MOSFETs in TO-247 (3 pin) and MDmesh M5 MOSFETs in TO247-4 (4 pin)

Figure 19. Efficiency comparison at different power level



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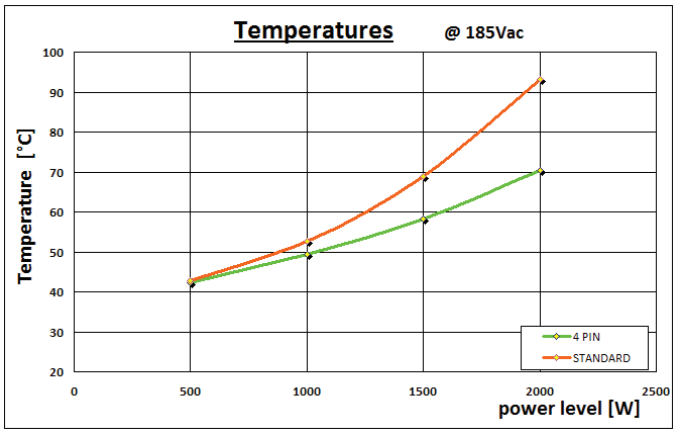
The improvement in terms of efficiency is negligible at lower power levels, but it becomes significant when the power level increases. The efficiency improvement in the demo board at maximum power level (2 kW) achieves a highly significant value of 0.32%.

Figure 20. Efficiency comparison at different power level



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From a thermal point of view, the temperature gap is already significant at low power levels and reaches 20°C at the maximum load.

2 Eon / Eoff energy: experimental waveforms

Figure 21. Waveforms and power losses during the turn-on commutation @ 1.5 kW for MDmesh M5 MOSFETs in TO247-4 (4 pin)

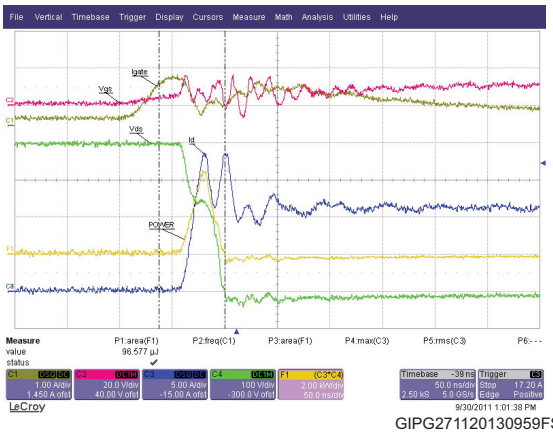

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Figure 22. Waveforms and power losses during the turn-on commutation @ 1.5 kW for MDmesh M5 MOSFETs in TO-247 (3 pin)

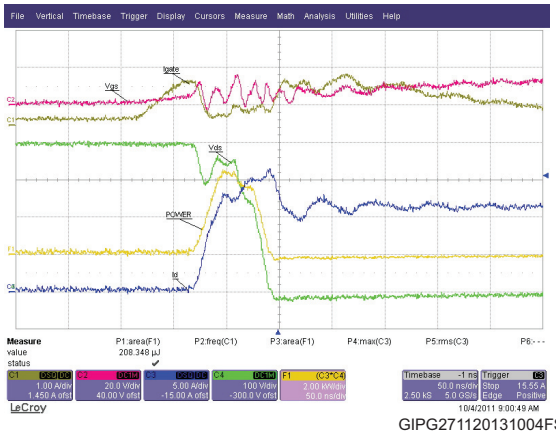

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Figure 23. Waveforms and power losses during the turn-off commutation @ 1.5 kW for MDmesh M5 MOSFETs in TO247-4 (4 pin)

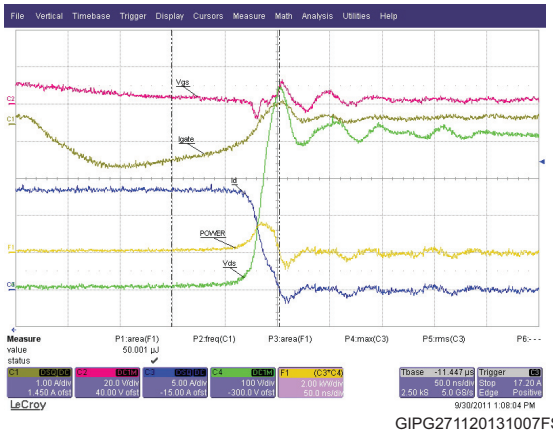

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Figure 24. Waveforms and power losses during the turn-off commutation @ 1.5 kW for MDmesh M5 MOSFETs in TO-247 (3 pin)

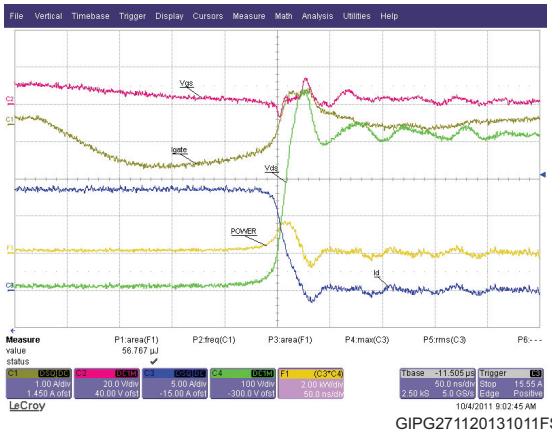

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Figure 25. Turn-on details @ 2 kW for MDmesh M5 MOSFETs in TO247-4 (4 pin)

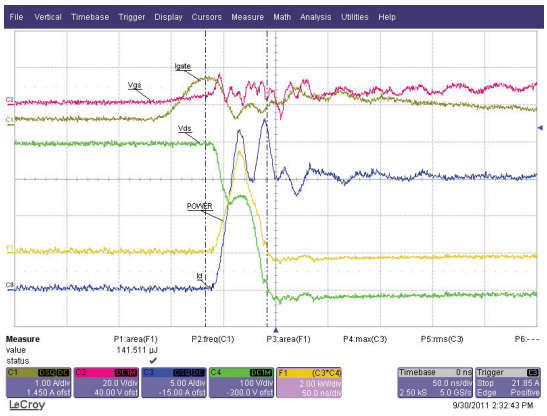

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Figure 26. Turn-on details @ 2 kW for MDmesh M5 MOSFETs in TO-247 (3 pin)

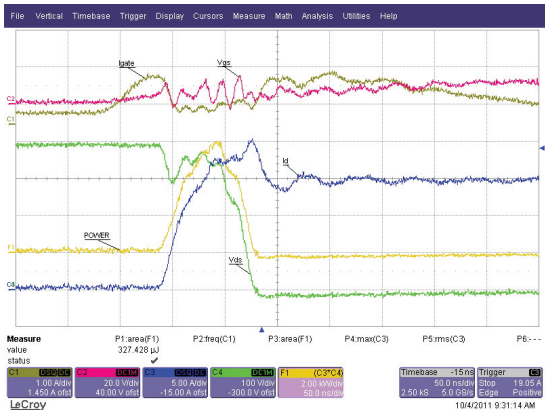

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Figure 27. Turn-off details @ 2 kW for MDmesh M5 MOSFETs in TO247-4 (4 pin)

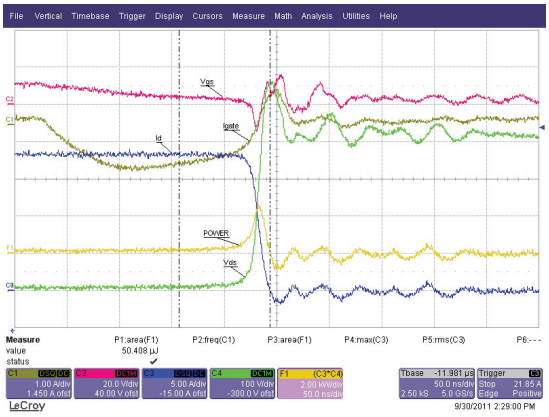

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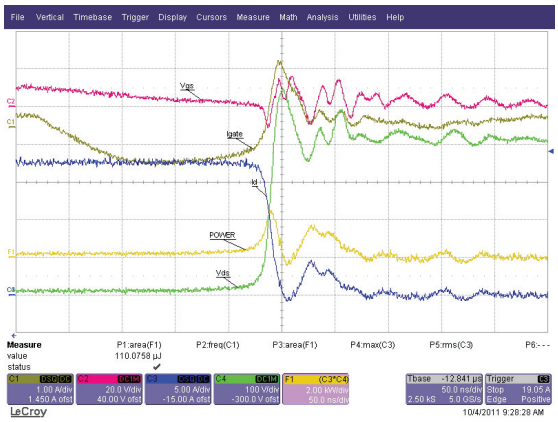
Figure 28. Turn-off details @ 2 kW for MDmesh M5 MOSFETs in TO-247 (3 pin)



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3 Conclusions

The introduction of the fourth (driving) pin strongly improves the dynamic performance of Power MOSFET devices, which is even more evident when the switching current levels and the output power levels are higher during both device turn-off and turn-on. The test results show that the MDmesh™ M5 technology device assembled with the driving source pin provides significant benefits when the switching current is higher than approximately 10 A at turn-off, but the advantages are present at all power levels. Different increments in efficiency were measured for different power levels, and in a market where power levels are always increasing, each small efficiency improvement represents a large advantage for energy saving systems demanded in today's very competitive market.

For our demo board, the energy saving was almost 7 W at maximum output power (2 kW). The most important benefit, however, lies in the thermal behavior: in fact, a small magnitude of power loss is translated into a difference of many degrees (around 20°C) on case temperatures for the power device. Lower working temperatures allow the use of smaller heat sinks which occupy less area on board or, more importantly, can increase the reliability of the entire system.

4 References

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5 Revision history

Table 2. Document revision history

Date	Revision	Changes
29-Jan-2015	1	Initial release.
07-May-2015	2	Minor text changes.

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