Application note

Designing with the L99H02

Introduction

The L99H02 is a sophisticated H-bridge MOSFET controller IC designed to control up to 5 N-Channel MOSFETs in a full H-bridge configuration with reverse battery protection. It has a SPI configurable current sense amplifier able to mux in two separate current sense resistors. The L99H02 incorporates SPI control for functional programming and high-level diagnostics. There is also a provision to include external thermal sensors to protect the MOSFET switches.

The L99H02 is optimally intended to drive higher current motor control systems in an automotive environment. This document will walk the engineer through the design decision process for developing a higher current motor control application.

This application note also applies to the L99H01. Any references to the L99H02 also apply to the L99H01. The L99H02 is an improved version of the L99H01.

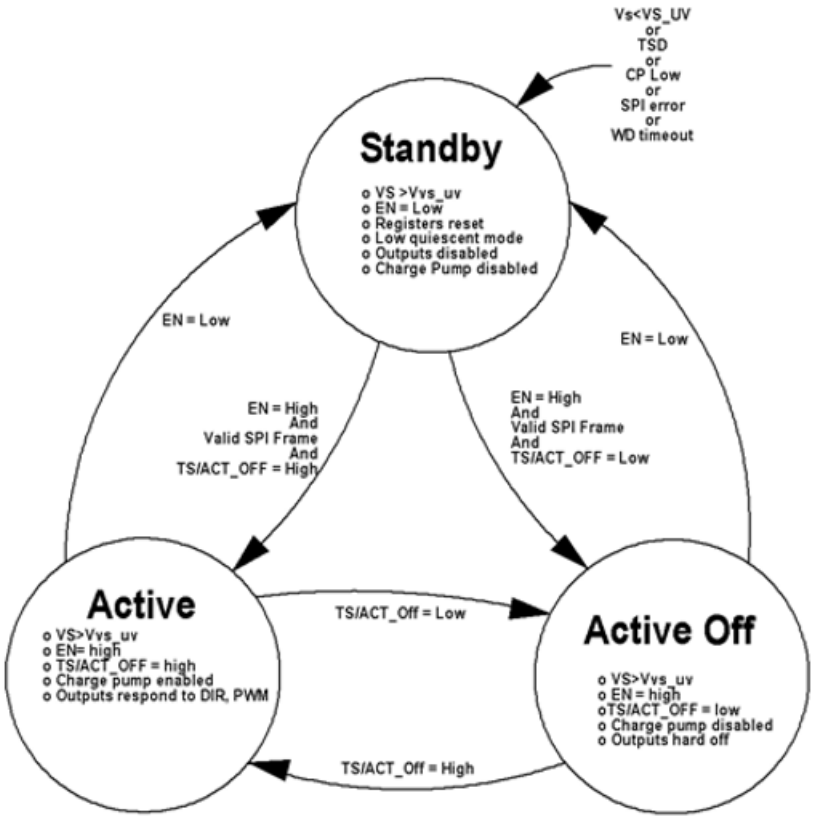
1 Functionality

The L99H02 is an H-bridge MOSFET controller IC that uses both direct inputs and a SPI bus to manage the H-bridge functionality. The following is a brief synopsis of the L99H02 basic operation. More details can be found in the datasheet (see Section 14 Reference documents).

1.1 Functional states

The L99H02 does not contain a state machine. It does, however, function in three regions, standby, active, and active off. It is described using the following diagram.

Figure 1. L99H02 regions of operation



1.2 Direct Input Control

What is managed by direct inputs are:

- Enable
  - When this pin is low all registers are reset to the default setting and the MOSFET drivers are set to passive off mode.
  - When enable goes high the L99H02 enters an interim state that still does not allow activation of the outputs. A valid SPI command must occur to fully wake the device from standby. This is a safety feature that requires both a hardware event (EN going high) and a valid microcontroller interaction (valid SPI frame) to activate outputs.
- Direction (DIR pin)
  - This pin controls which high-side / low-side pair are active.
  - When high, HS1 and LS2 are active when driving
  - When low, HS2 and LS1 are active when driving

- PWM control (PWM pin)
  - When this pin is high the H-bridge is in driving mode.
  - When this pin is low the H-bridge is in freewheeling mode.
- Failsafe/thermal override (TS/ACT_OFF pin)
  - When programmed as a Thermal sensor (EXT_TS = 1) this pin has a bias current to properly bias thermal sensing diodes. The threshold is programmable according to a formula (see Section 9 Thermal sensor operation).
  - When programmed as a failsafe off function (EXT_TS = 0) there is no bias current and the threshold is fixed.
  - In both cases the threshold is low going (i.e. the device disables the outputs when the voltage is below the threshold).
  - In the thermal sensor mode there is a 64 µs delay after the threshold is crossed. There is no delay when in Failsafe mode.
  - When in failsafe/thermal override the following occurs:
    - The charge pump is disabled
    - The gate drivers actively drive the Gates to their respective sources, forcing all H-bridge MOSFETs off.
    - In thermal sensor mode (EXT_TS = 1) the OT_EXT status bit must be cleared to resume operation.

1.3 SPI Control

The SPI uses an in-frame response protocol. Each command byte requires an op-code, address, and command bits. Each command has an associated op-code and address. Refer to Section 13 Programmer's guide or in the L99H01 and L99H02 datasheets (see Section 14 Reference documents).

1.3.1 SPI commands

What is managed by SPI command is:

- Freewheeling control
  - High side or low side PWM
  - Active or passive freewheeling
- VDS monitoring
  - Voltage thresholds
  - Delay timing
- The thermal sensor / failsafe input
  - Thresholds
  - Bias current enable
- Over/undervoltage recovery actions
  - Latch off or auto recover
- Current sense amplifier
  - Gain settings
  - Input offset calibration mode
  - Input MUX selection (CSI1 or CSI2)
- Watchdog control

1.3.2 SPI diagnostics

The in-frame response SPI protocol provides the general health and well-being of the H-Bridge in a Global Status Byte on the DO pin every time the host micro provides the op-code and address during a command SPI frame. This information is general. More detailed diagnostics are available in the status registers. The contents of the address given is returned when the data bits are clocked in. The diagnostics available in total are:

- Global error
- SPI Frame error

- Reset event
- Thermal events
- Under/overvoltage event
- Watchdog timeout
- VDS fault
- Charge pump low event
- TS/ACT_OFF low event

More details regarding device diagnostics can be found in Section 13 Programmer's guide or in the L99H01 or L99H02 datasheets (see Section 14 Reference documents).

1.4 Watchdog function

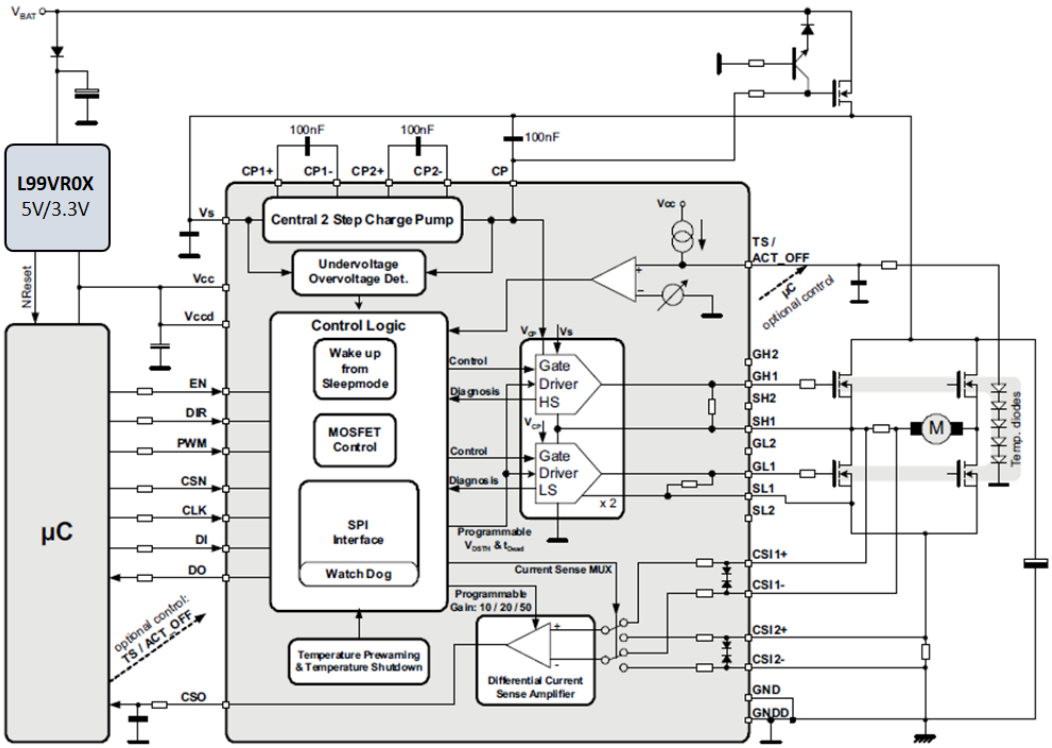
The function of the watchdog is to monitor the microcontroller during normal operation within a nominal trigger cycle of 60 ms. The microcontroller must restart the watchdog timer by sending a watchdog restart bit via SPI repeatedly within the watchdog time T_{WDTO}. If no correct watchdog service is sent from the microcontroller, all gate drivers switch to a sink condition and the watchdog time out bit (WDTO) is set. Once the watchdog times out, the gate drivers can only be reactivated by sending a valid SPI command clearing the WDTO bit.

2 The L99H01 or L99H02 application circuit

There are a few external components that are required to fully utilize the features of the L99H02. These include charge pump capacitors, gate resistors, sense resistors, MOSFETs for the H-bridge and an additional MOSFET for reverse battery protection if needed.

It is assumed that the application is high current or other less complex solutions would be pursued. When considering high current H-bridge applications, active recirculation is preferred to minimize the power dissipation in the H-bridge. Most H-bridge applications are driving bi-directional motors. As a result, this design guide will cover driving higher current motors.

Figure 2. Application and block diagram



This application note will break down each individual aspect of the design starting with the hardware selection including circuit board layout guidelines and software considerations.

3 Determining the proper MOSFET for the H-bridge

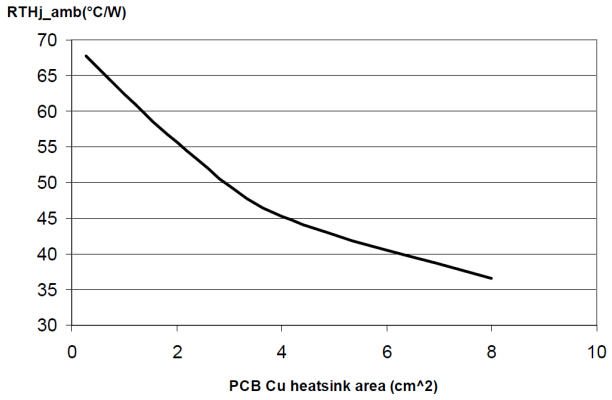
MOSFET selection requires knowing several parameters such as, maximum voltage, maximum current, maximum ambient temperature, and the switching speed required. With that you can narrow your search for the proper MOSFET.

The limiting factor in any surface mounted power device is the capability of the circuit board to dissipate heat. That capability is dependent on several parameters. Circuit boards come in many different flavors. From single sided to multilayer boards, from ½ Oz copper to 10 Oz copper or more.

A two-sided board with 2 Ounce copper (70 µm) and thermal vias will provide a reasonable amount of heat sinking for a given amount copper area. A four-layer board will provide better thermal conductivity.

For a DPAK sized MOSFET on a two sided board a general rule of thumb would be approximately 35 C°/W with a total of 8 cm^2 of copper area under the part. Figure 3. Typical thermal resistance for a DPAK vs. Cu area applies to a typical DPAK MOSFET on a two sided FR4 board : most of the thermal impedance in this system is in the circuit board.

Figure 3. Typical thermal resistance for a DPAK vs. Cu area



Note: layout condition of Rth measurements (double sided PCB FR4 area = 58 mm x 58 mm, PCB thickness = 1.8 mm, Cu thickness = 2 Oz, Copper areas: from minimum pad lay-out to 8 cm^2 on the back side).

When using a DPAK, adding two more (inner) layers improves the thermal impedance of 25°C/W (for 8 cm^2 CU area) with an optimized layout.

There are two ways of considering the maximum allowable $R_{ds(on)}$. The first method is using the maximum allowable junction temperature to have the upper limit in power dissipation. Junction temperature can be calculated by the equation:

$$T_{Junction} = P_{Diss} \times R_{\theta(J-A)} + T_{Amb} \quad (1)$$

Power dissipation comes from two things: conduction losses and switching losses. Conduction losses are a function of the square of the current times the $R_{DS(on)}$ of the switch. Rds(on) changes with temperature. For a typical MOSFET, the $R_{DS(on)}$ doubles between 25 °C and 175 °C. A reasonable equation for $R_{DS(on)}$ over temperature then looks like:

$$R_{DS(on)}(T_J) = R_{DS(on)}@25C\left(1 + \frac{T_J - 25C}{150C}\right) \quad (2)$$

We insert this into Eq. (1) above and add switching losses then solve for $R_{DS(on)}$:

$$R_{DS(on)max} = \frac{150C\left(T_{Jmax} + T_{Amb\_max} - P_{SW}R_{\theta(j-a)}\right)}{I_{load}^2 R_{\theta(j-a)}\left(125C + T_{Jmax}\right)} \quad (3)$$

Where:

- T_{Jmax}= the maximum rated temperature of the FR4 circuit board
- T_{Amb_max}= the maximum ambient temperature for the application
- $R_{th(j-a)}$= the estimated thermal resistance from junction to ambient
- P_{SW}= switching losses (refer to Eq. (10))

Just using this equation alone can get you in trouble. The concern with higher power in surface mounted power devices is the temperature of the circuit board itself. A typical DPAK MOSFET has a thermal resistance junction to case ($R_{th(j-c)}$) around 2 °C/W. The circuit board is then the next 33 °C/W (using the 2-sided board example). Simple resistor division indicates that the circuit board under the part will not be much different in temperature than the Junction. MOSFET junction temperatures can safely reach 175 °C. Even at 4 W, that drops the temperature down to 167 °C at best on the TAB. Most FR4 cannot handle that heat. As a result we start with the max circuit board temperature as the limiting parameter and work backwards.

$$T_{PCB} = T_{Junction} - P_{DISS} \times R_{TH(j-c)} \quad (4)$$

Combining Eq. (1) with Eq. (4) provides for the maximum power each MOSFET can dissipate using the circuit board as the limiting factor:

$$P_{diss\_max} = \frac{T_{PCB\_max} - T_{Amb\_max}}{R_{th(j-a)} - R_{th(j-c)}} \quad (5)$$

Where:

- T_{PCB_max} = the maximum rated temperature of the FR4 circuit board
- T_{Amb_max} = the maximum ambient temperature for the application
- $R_{th(j-a)}$ = the estimated thermal resistance from junction to ambient
- $R_{th(j-c)}$ = the published thermal resistance from junction to case

We are looking for the maximum allowable $R_{DS(on)}$ for a given system. Given the thermal resistances and circuit board limitations the maximum 25 °C $R_{DS(on)}$ that can be safely used in a system is calculated by:

$$R_{DS(on)\_max} = \frac{150C \times \left(T_{PCB\_max} - T_{Amb\_max} - P_{SW} \times R_{th(j-c)}\right)}{I_{load}^2 \times \left[R_{th(j-a)} \times (T_{PCB} + 125C) - R_{th(j-c)} \times \left(125C + T_{Amb\_max}\right)\right]} \quad (6)$$

Where:

- I_{load} is the maximum expected motor current atT_{Amb_max}.
- $R_{DS(on)\_max}$ is the highest the MOSFET 25 °C $R_{DS(on)}$ cannot dissipate too much heat to hurt the circuit board.
- P_{SW} is the loss due to switching. Refer to Eq. (10).

Note: Eq. (6) ignores any benefits due to duty cycle while including switching losses. As a result, this is an absolute worst-case condition.

It is important to note that motor run/stall currents change with temperature. The hotter the motor the lower typically the current becomes, as the winding resistance goes up with heat.

3.1 Layout guidelines

Power dissipation capability in the copper is reduced as you get further away from the device.

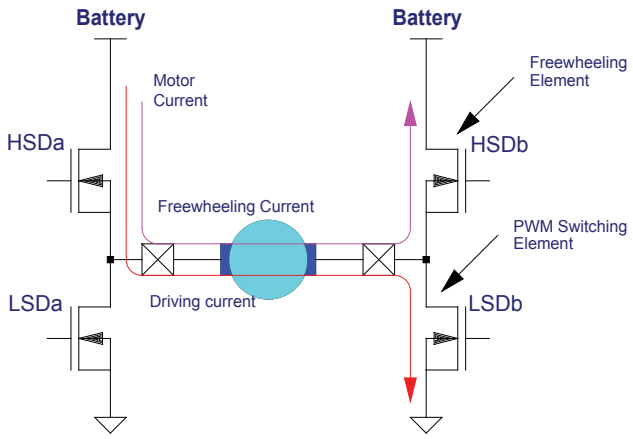
3.2 MOSFET power dissipation calculations

With a general idea of the thermal impedance of the application, MOSFET selection turns to power generation. There are two components to MOSFET power dissipation; conduction losses and switching losses. Conduction losses are only present when the switch is active. Switching losses only contribute when PWMming and then only on the switching component.

3.2.1 Conduction losses

Conduction losses are simply I^2R losses. In an H-bridge configuration there are two elements that are on at the same time. While driving the load the high side of one leg and the low side of the other leg (or vice versa) are active and conducting load current. If PWMming, then the conduction losses in the switching element are reduced by the duty cycle as the freewheeling element shares in the conduction losses at 1 – % *Duty cycle*.

Figure 4. Currents in an H-bridge (low side PWM)



The MOSFET switch power equations when low side PWMming would look like:

$$P_{Cond\_HSDa} = I^2 \times R_{ON(HSDa)} \quad (7)$$

$$P_{Cond\_LSDb} = I^2 \times R_{ON(LSDb)} \times Duty \quad (8)$$

$$P_{Cond\_HSDb} = I^2 \times R_{ON(HSDb)}\left(1 - Duty\right) \quad (9)$$

Where:

- P_{Cond_XSDx} = the conduction losses in each of the H-bridge elements. When driving an inductive (motor) load P_{Cond_HSDb} is included
- I = load current
- R_{ON_HSDa} = the $R_{DS(on)}$ of the conducting high side switch
- R_{ON_LSDb} = the $R_{DS(on)}$ of the conducting (PWMmed) low side switch
- R_{ON_HSDb} = the $R_{DS(on)}$ of the freewheeling high side switch
- *Duty* = the % PWM duty cycle of the low side switch

If there is no PWMming then the third equation (Eq. (9)) disappears. When calculating conduction losses in the freewheeling element it is assumed that the load is inductive and that the system is turning on the freewheeling element during recirculation.

3.2.2 Switching losses

Switching losses are a result of the driver behaving as a linear output for very short periods of time. The MOSFET is neither on nor off. It is effectively being driven linearly from one rail to the other.

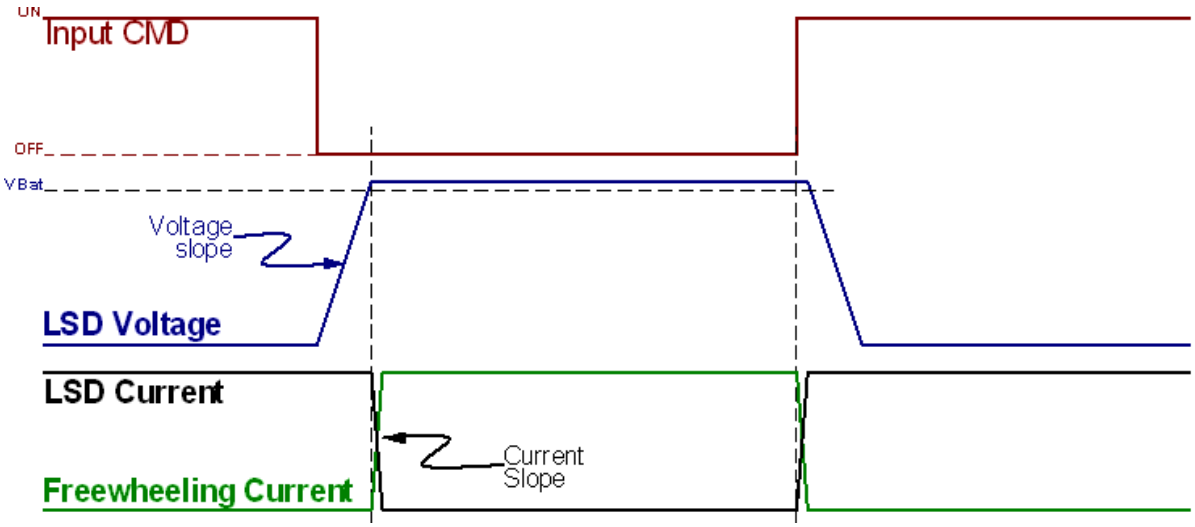
In a PWMmed H-bridge application there are two elements that are switching. In the example shown in Figure 4. Currents in an H-bridge (low side PWM) the low side switch, LSDb, is the driving element and the high side switch, HSDb, is the freewheeling element. However, only the driving element experiences switching losses.

In our example (see Figure 4. Currents in an H-bridge (low side PWM)) when LSDb turns off, the current slope becomes negative. A negative current slope in the motor inductance causes the voltage at the motor to invert (becomes negative with respect to what it was originally). The voltage climbs until the diode in the freewheeling MOSFET starts to conduct current. That is, there is no current flow in the freewheeling element (high side switch in our example) until the forward voltage of the MOSFET's body diode is satisfied (~0.7 V).

This works in both directions. The current starts or stops flowing in the freewheeling element when the voltage across it is low (see Figure 5. Low side PWM switching curves for an inductive load). As a result, there is no linear control occurring at the freewheeling element. Thus, no switching losses.

There is only one switch in the system that experiences switching losses, the PWM switching element (LSDb in our example). Switching losses are different for inductive or motor type loads than they are for resistive loads. For resistive loads, the current is proportional to the voltage across the load (Ohm's law). In an inductive load, the current is constant during the entire switching time and only changes once the freewheeling or driving element starts conducting. As a result, the equations that describe the losses during switching are different.

Figure 5. Low side PWM switching curves for an inductive load



A reasonable first order estimation on switching losses is to assume a trapezoidal waveform while ignoring the losses due to the current switching. The current switching losses are typically an order of magnitude less than the losses due to the voltage slope. Inductive switching losses can be estimated in the following equation.

$$P_{Switch} = V_{Bat} I_{Ave} \frac{t_{rise} + t_{fall}}{2} f_{PWM} \quad (10)$$

Where:

- V_{bat} = the supply voltage
- I_{AVE} = is the avarage current due to PWMming
- t_{rise}+ t_{fall} = these are the rise and fall times during switching
- f_{PWM} = switching frequency

  This power equation works for either the high side PWMming or the low side PWMming.

3.2.3 Total losses

The total losses calculated are the sum of the conduction and switching losses from equationsEq. (7) , Eq. (8) , Eq. (9), and Eq. (10), where the driving (PWMmed) element losses include both conduction and switching. In our example that would be Eq. (8) and Eq. (10).

$$P_{MOSFET} = I^2 R_{ON(LSDb)} Duty + V_{Bat} I_{Ave} \frac{t_{rise} + t_{fall}}{2} f_{PWM} \quad (11)$$

It is understood that the $R_{DS(on)}$ is a function of junction temperature. Using Eq. (2) for $R_{DS(on)}$ in Eq. (11) will obtain a more accurate power dissipation equation in the MOSFET.

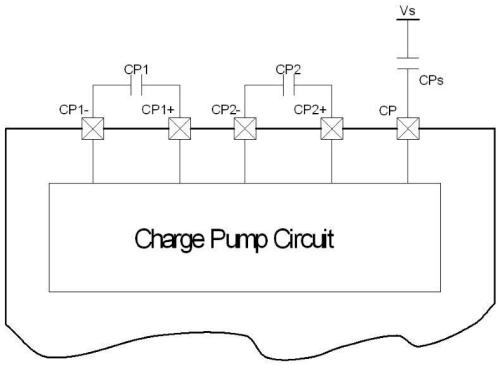
$$P_{MOSFET}\left(T_J\right) = I^2 R_{DS(on)@25C}\left(1 + \frac{T_J - 25C}{150C}\right) Duty + V_{Bat} I_{Ave} \frac{t_{rise} + t_{fall}}{2} f_{PWM} \quad (12)$$

4 Calculating charge pump capacitor values.

The L99H02 uses a 2-stage charge pump. This configuration can maintain fairly good gate drive voltages during low voltage operation. There are three charge pump capacitors. Two are for generating the boost and one for storage. The charge pump supplies both the high side and low side MOSFET gate drive circuits.

The datasheet recommends that all three charge pump caps be 100 nF ceramic, 50 V capacitors. Most applications can use these suggested values. It is only in the most extreme cases where there is a large number of very low Ohmic MOSFETs in parallel that consideration must be made for the charge pump capacitors.

Figure 6. Charge pump



The charge pump storage (CPs) capacitor should be connected to supply and not ground. As the supply changes the charge pump storage voltage will “float” with it. This is not possible if the cap is tied to ground.

The charge pump frequency is based on the internal clock frequency (divided by 32). That frequency can change depending on the V_{cc} value chosen. At 5 V the range is 93.7 kHz to 141 kHz. At 3 V the range is from 75 kHz to 109 kHz.

4.1 Average charge pump current draw

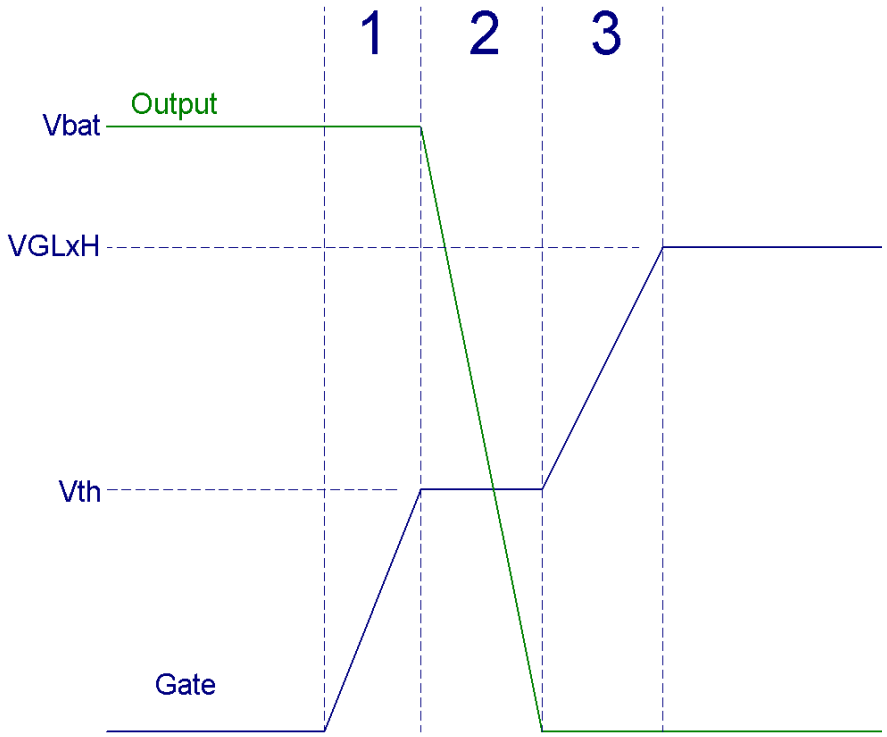
The charge pump supplies current to both the high and low side MOSFETs. This guarantees a fully enhanced MOSFET even at very low battery voltages. The only time there is meaningful current draw from the charge pump is during PWMming. That means that only one low side element and one high side element are PWMming. This occurs when using active freewheeling while driving an inductive load. It should be noted that if you are not driving an inductive type load then active freewheeling is not recommended.

For the example shown in Figure 4. Currents in an H-bridge (low side PWM), the switching elements are the LSDb and HSDb MOSFETS. The high side current draw is simple, the drain and source voltage do not change. Only the charging of the input capacitance due to the gate voltage is rising.

$$I_{CP\_HS\,(ave)} = \quad C_{iss} \times (V_{GHxH} - V_{Bat}) f_{PWM} \tag{13}$$

When considering the low side there are three regions of interest.

Figure 7. **Low side MOSFET gate charge regions**



The equations for these three regions are as follows:

$$\begin{matrix} Region\ 1 & C_{iss} \times V_{GSth} \\ Region\ 2 & C_{rss} \times V_{Bat} \\ Region3 & C_{iss} \times (V_{GLxH} - V_{GSth}\ \ ) \end{matrix} \quad (14)$$

Adding these three together and inserting Eq. (13) then multiplying them by the PWM frequency provides the total average current draw from PWMming.

$$I_{CP\_ave} = \left[C_{iss\_HS}(V_{GHxH} - V_{Bat}) + C_{iss\_LS}V_{GLxH} + C_{rss\_LS}V_{Bat}\right]f_{PWM} \quad (15)$$

Note: adding the equations from region 1 and region 3 removes the threshold voltage from the equation. We can simplify this further in that C_{rss} is typically orders of magnitude lower than C_{iss}. Therefore, its contribution is not significant.

The charge pump is specified to be able to supply at least 26 mA ($I_{CP(min)}$) at 14 V.

Table 1. STD65N55F3 dynamic parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_m	Forward transconductance	V_{DS} = 25 V, I_D = 32 A	-	50		S
Ciss	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2200		pF
Coss	Output capacitance		-	500		pF
Crss	Reverse transfer capacitance		-	25		pF
Q_g	Total gate charge	V_{DD} = 27 V, I_D = 65 A	-	33.5	45	nC
Qgs	Gate-source charge	V_{GS} = 10 V	-	12.5		nC
Qgd	Gate-drain charge		-	9.5		nC

Using an STD65N55F3 (a 6.5 mΩ MOSFET) as an example of a low Ohmic device we have a C_{iss} of 2200 pF. If we bump that up to 50% for absolute worst case the total C_{iss} is 3300 pF. The average DC current from Eq. (16) is 1.52 mA at V_{Bat} = 12 V :

$$I_{CP\_ave} = (3300pF \times (26V - 12V) + 3300pF \times 12V + 25pF \times 12V) \times 20kHz \quad (16)$$

As you can see this is much lower than the minimum specified charge pump capability of 26 mA. This tells us that the device is well able to handle the MOSFET in question. There is still instantaneous current draw when the gate is being charged. The instantaneous current draw can cause the charge pump voltage to droop and slow the rise time on the MOSFET.

4.2 Instantaneous gate drive current

Instantaneously, the gate drive circuits are able to drive as much as 800 mA according to the specification ($I_{GHx(ON)}$, $I_{GLx(ON)}$). Each gate is driven separately and out of phase with each other. When one is being charged the other is being discharged and vice versa. Discharging does not tax the charge pump. The 800 mA limit can be reached depending on the C*iss* and the rise time by the equation:

$$I_{Gate_{rise}} = C_{iss} \times \frac{V_{Gate}}{t_{rise}} \quad (17)$$

Going one step further and calculating the potential instantaneous gate charge current using a 100 ns rise time we obtain:

$$I_{Gate\_rise} = 3300pF \times \frac{12V}{100ns} = 396mA \quad (18)$$

This current is well within the gate drive capability but outside the charge pump capability. The worst case difference is used to determine the maximum expected voltage drop across the charge pump storage capacitor, C_{CP}.

$$\Delta V_{CP\_cap} = \frac{\left(I_{CP(min)} - I_{ave} - I_{Gate\_rise}\right) \times t_{rise}}{C_{CP}} \quad (19)$$

Using the standard 100 nF cap mentioned above we find a charge pump voltage dip of:

$$\frac{(26mA - 1.52mA - 396mA) \times 100ns}{100nF} = -372mV \quad (20)$$

Using these calculations, the total dip in the charge pump supply in the worst case would be 372 mV. So even with a 6.5 mΩ MOSFET and a fast rise time the standard 100 nF solution is more than adequate. In conclusion, the L99H02 will handle most MOSFETs with a simple selection of 100 nF capacitors.

If you should ever have the need to increase the charge pump capacitors there is a limit to the size of capacitor. This limit is based on the frequency of the charge pump and the resistance of the switches in the charge pump.

Assuming a 50% duty cycle and a maximum charge pump frequency of 141 kHz, the largest capacitor that can be safely used is 510 nF.

5 Calculating gate resistance

The gate resistors are used in this application to control the rise and the fall times on the MOSFET switching elements. As discussed earlier the rise and fall times influence the power dissipation in the system in terms of switching losses. Rise and fall times also contribute to radio frequency interference or RFI. The faster the switching speeds the lower the power dissipation due to switching losses. However, faster switching speeds also generate more RFI.

The engineering has to find the range where both power dissipation and RFI are manageable. In short the goal is typically to drive the MOSFETs as slow as the thermal limitations allow.

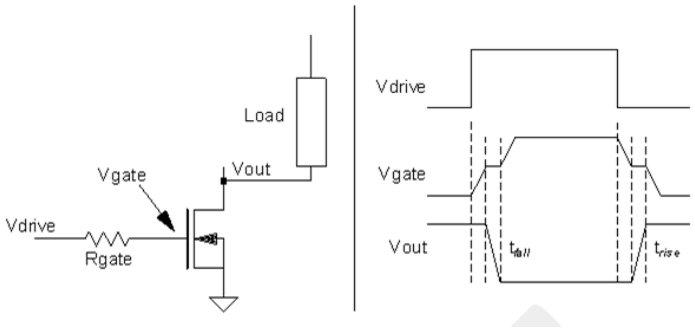
The rise and fall time calculations change between the low side drivers and the high side drivers. Since the bridge is driving inductive loads the choice of which MOSFET is PWMming has a great effect on how switching speed is calculated. Mainly because the drain - source voltages are doing different things with respect to the gate voltage for each of these elements.

5.1 Low side PWMming

5.1.1 Low side driver gate resistance calculations

Using the example in Figure 4. Currents in an H-bridge (low side PWM), the H-bridge is PWMming an inductive load using the high side element as the freewheeling component. The low side driver (LSDb) is taking all of the switching losses. As a result, the rise and the fall times on the low side MOSFET are critical to the design.

Figure 8. Low side gate drive and simplified waveforms



Looking at the waveform in figure above, the drain voltage fall and the rise times have two considerations; the initial delay and the actual fall time. These two times are governed by two different parameters in the MOSFET along with the gate threshold voltage. The input capacitance, C_{iss} governs the initial delay (Region 1 Figure 7. Low side MOSFET gate charge regions) as that capacitance must be charged to the gate threshold before the MOSFET begins to turn on. Then the gate to drain charge, Q_{gd}, determines the transition times. Typically, C_{iss} and Q_{gd} can be found in the MOSFET datasheet.

These next four equations describe the time from the initial gate drive rise at the L99H02 pin to the end of the drain voltage transition. Both equations have a delay component followed by the transition time component.

Delay times:

$$t_{fall\_delay} = R_{Gate} C_{iss} ln\left(\frac{V_{GLxH}}{V_{GS(th)}}\right) \quad (21)$$

$$t_{rise\_delay} = R_{Gate} C_{iss} ln\left(\frac{V_{GLxH}}{V_{GLxH} - V_{GS(th)}}\right) \quad (22)$$

The rise and fall times are best calculated using the gate charge parameter Q_{gd}:

$$t_{fall} = \frac{Q_{gd} \times R_{Gate}}{V_{GLxH} - V_{GS(th)}} \quad (23)$$

$$t_{rise} = \frac{Q_{gd} \times R_{Gate}}{V_{GS(th)}} \quad (24)$$

Where:

- R_{Gate} = total gate resistance (RGLx + R_{gate})
- C_{iss} = MOSFET input capacitance
- Q_{gd} = MOSFET gate to drain capacitance
- V_{GLxH} = low side gate driver voltage from L99H01 or L99H02
- $V_{GS(th)}$ = MOSFET gate threshold voltage

Both the delay and the transition times are important for dead time calculations. That is discussed in more details in Section 5.5 Dead time considerations.

Solving equations Eq. (23) and Eq. (24) for R_{Gate} (and subtracting the internal gate resistance for turn off only) provides:

$$R_{Gate(on)} = \frac{t_{fall}\left(V_{GLxH} - V_{GS(th)}\right)}{Q_{gd}} \quad (25)$$

$$R_{Gate(off)} = \frac{t_{rise} V_{GS(th)}}{Q_{gd}} - R_{GLx} \quad (26)$$

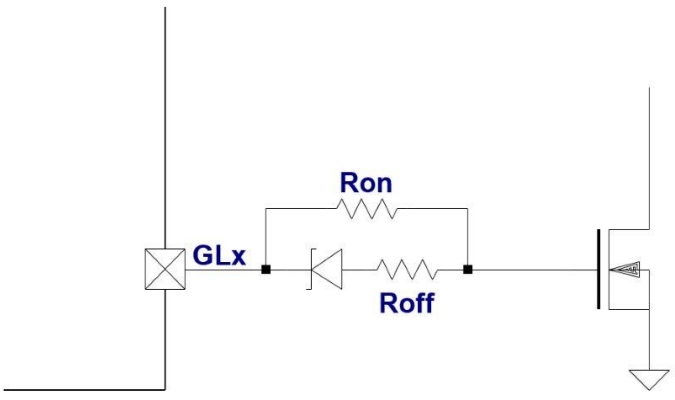
Using our example from Figure 4. Currents in an H-bridge (low side PWM) with a transition time of 100 ns and a gate threshold of 3 V the R_{Gate} value can be calculated as:

$$R_{Gate(on)} = \frac{100ns(12V - 3V)}{9.5nC} = 95\ \Omega \quad (27)$$

$$R_{gate(off)} = \frac{100ns \times 3V}{9.5nC} - 5.3\ \Omega = 26.3\ \Omega \quad (28)$$

As you can see, there is a difference between rise time and fall time resistor sizes due to the different driving voltages across the gate resistor. A difference in rise and fall times may not be too much of an issue. However, if this is critical to your application there is a solution. To obtain similar rise and fall times the gate resistor will need to be different when turning on versus when turning off. This can be achived by using a parallel diode and resistor as shown in the figure below.

Figure 9. Low side PWM gate drive option



Where the R_{on} and R_{off} resistors can be calculated as:

$$R_{on} = R_{Gate(on)} \quad (29)$$

from equation 24 above

$$R_{off} = \frac{R_{Gate(on)} \times R_{Gate(off)}}{R_{Gate(on)} - R_{Gate(off)}} \quad (30)$$

from equation 24 and 25 above

5.1.2 Freewheeling MOSFET gate resistor calculations

If the L99H02 is using active recirculation or active freewheeling, then the high side switches are only turned on when the body diode in the MOSFET is already conducting. That means that output will get no transition as a result of the gate voltage slew rate. With that, it is understood that there are no voltage rise and fall times associated with the freewheeling MOSFET gate voltage. However, there are two concerns: the first is the decay time of the gate voltage at turn-off. The second is the high side switch turning back when the low side switch turns on due to the fall time of the low side switch. The second one is unlikely to be an issue. However, it is always good to double check. As a result, we consider the high side MOSFET gate resistor accordingly.

5.1.3 Cross conduction protection

Cross conduction occurs when the upper and lower MOSFETs in a single leg are on at the same time. Some call it shoot-through current. There are two places this is considered. First, the duration between when the low side MOSFET is commanded off and when the high side MOSFET is commanded on. And vice versa, when the high side MOSFET is turned off to when the low side MOSFET is commanded on.

The first one is the dead time between commanding off the low side MOSFET to when it is safe to turn on the high side MOSFET. This includes two parameters: the delay time and the rise time. This is a simple addition of two previously calculated equations:

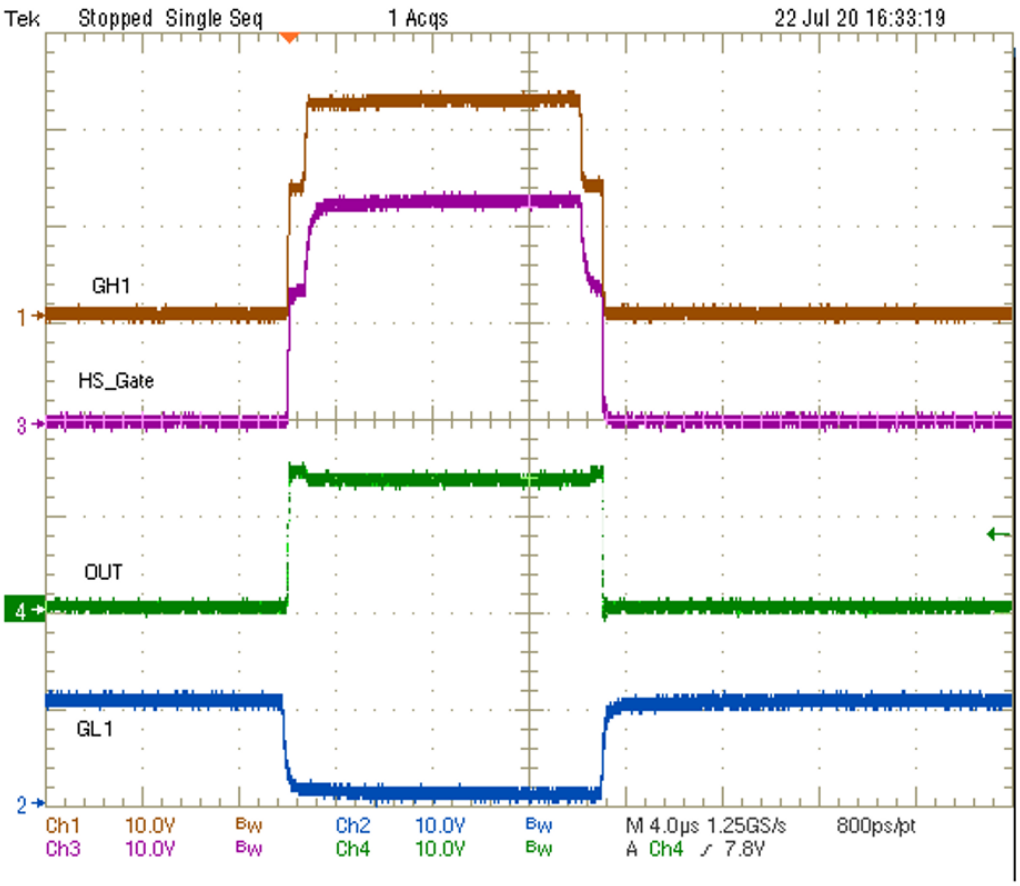
$$t_{dead\_ls} = R_{Gate} C_{iss} ln\left(\frac{V_{GLxH}}{V_{GLxH} - V_{GS(th)}}\right) + \frac{Q_{gd} \times R_{Gate}}{V_{GS(th)}} \quad (31)$$

Considering the dead time when the upper transistor turns off is less complex as the only time that is needed to be calculated is the time it takes to discharge the gate. Being the freewheeling component, the high side switch drain-source voltage does not change when this switch is

$$t_{dead\_hs} = R_{Gate} C_{iss} ln\left(\frac{2V_{GHxH}}{V_{GS(th)}}\right) \quad (32)$$

That requires the high side gate resistor to be considerably smaller than the low side gate resistor to keep the dead time within reason. Figure 10. Scope plot of LSD switching (high side freewheeling) using 47 Ω gate resistor illustrates the long decay on the high side MOSFET gate with just a 47 Ω resistor.

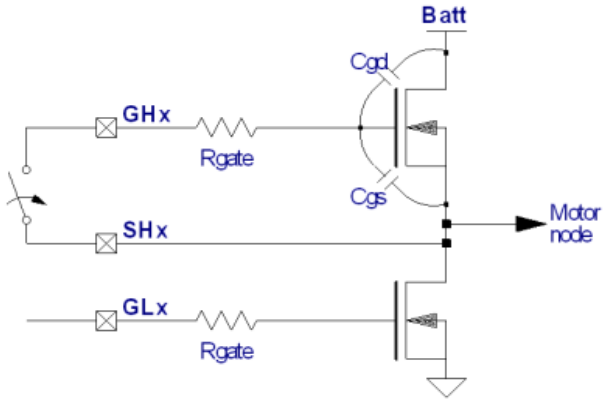
Figure 10. **Scope plot of LSD switching (high side freewheeling) using 47 Ω gate resistor**



5.1.4 Slew rate and shoot through

The gate drive circuit does more than turn on and off a transistor. It also keeps the transistor off when the other is switching on or off. There is a significant amount of capacitance between the gate terminal and the motor node terminal (the Source of the high side MOSFET). When the motor terminal node is falling quickly the gate voltage has to fall with it to keep the upper MOSFET off. This requires the gate-drain capacitance, *Cgd*, to charge at the slew rate of the motor node.

Figure 11. **Cross conduction due to gate capacitance**



As a result, there is current pulled from the high side MOSFET gate-drain capacitance through *Cgs* and the gate resistor when the low side switch is turning on. The speed at which the low side switch is turning on dictates the amount of current that is drawn from the supply through the charging *Cgd* capacitor. The high side MOSFET gate resistor will need to be proportioned to ensure that the MOSFET Vgs(th) is not exceeded during switching. In most cases the ratio between *Crss* and *Ciss* is such that the gate threshold will never be reached, even with an instantaneous voltage change on the source and a very high Ohmic gate resistor. To be sure, the following equations can be used.

For a high side recirculating MOSFET the worst-case gate voltage can be calculated using capacitor division:

$$V_{Gate} = V_{Bat}\frac{C_{rss}}{C_{iss}} \tag{33}$$

Where:

- V_{Gate} = Expected worst case gate voltage when the low side MOSFET is turning on
- V_{Bat} = The supply voltage
- C_{rss} = C_{gd}, the Gate to Drain capacitance
- C_{iss} = C_{gd} + C_{gs}, the total Gate capacitance

If V_{Gate} in this equation is less than $V_{GS(th)}/2$ then there is no concern with the high side MOSFET turning on when the low side MOSFET turns on and the gate resistance governed by Eq. (32) stands. If, on the other hand, V_{Gate} is greater than $V_{GS(th)}/2$ then the following equation may apply:

$$R_{Gate} < \frac{t_{fall}}{C_{iss} ln\left(\frac{C_{iss}V_{GS(th)}}{2C_{rss}V_{Bat}}\right)} \tag{34}$$

If Eq. (34) applies, then the lesser of the two equations (Eq. (32) and Eq. (34)) is selected. These equations apply for both high side and low side freewheeling (for low side freewheeling V_{GLxH} is used in place of V_{GHxH} in Eq. (32)).

5.2 High side PWMming

5.2.1 High side driver gate resistance calculations

High side PWMming has a different set of equations that govern the rise and fall times as the voltage transition is occurring as a source-follower to the gate voltage. There are six regions to the gate voltage rise and fall. We will consider four of them: the turn-on delay (A), the rise time (B), the turn-off delay (D) and the fall time (E).

Figure 12. High side driver voltages

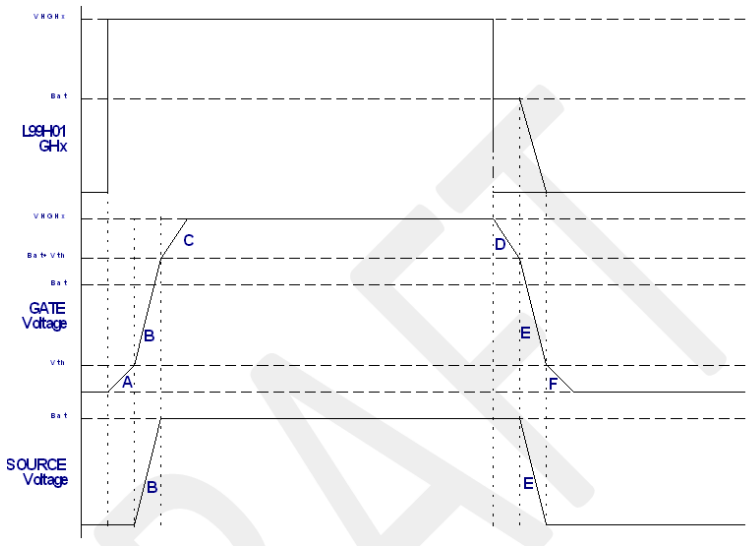
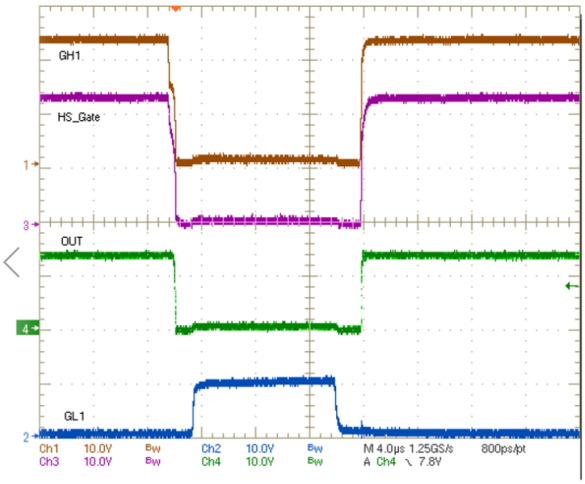


Figure 13. Scope plot of HSD switching (Low side freewheeling) using 47 Ω gate resistor



As in the low side drive timing calculations, the rise and fall conditions have very different driving parameters. The nature of this switch (high side, source follower) makes it difficult to use gate charge as the controlling MOSFET parameter for the rise time. When considering the rise time calculation, we use the specified gate-drain capacitance, C_{rss} in the classic RC time constant exponential equation. During the fall time, however, the voltage across the gate resistor is fixed at the gate threshold voltage, $V_{GS(th)}$. This creates a constant current in our first order estimation of fall times and allows us to use the gate charge parameter, Q_{gd}.

Delay times:

$$t_{rise\_delay} = R_{Gate}C_{iss}ln\left(\frac{V_{GHxH}}{V_{GHxH} - V_{GS(th)}}\right) \quad (35)$$

$$t_{fall\_delay} = R_{Gate}C_{iss}ln\left(\frac{V_{GHxH} - V_{Bat} - V_{GS(th)}}{V_{GS(th)}}\right) \quad (36)$$

Using these equations for a given set of parameters the rise delay is about 1/3rd the length of the fall time delay. In fact, Figure 13. Scope plot of HSD switching (Low side freewheeling) using 47 Ω gate resistor shows no appreciable rise time delay.

Rise and fall times:

$$t_{rise} = C_{rss}R_{Gate}ln\left(\frac{V_{GS(th)} - V_{GHxH}}{V_{Bat} - V_{GHxH} + V_{GS(th)}}\right) \quad (37)$$

$$t_{fall} = \frac{R_{Gate}Q_{gd}}{V_{GS(th)}} \quad (38)$$

Where:

- V_{GHxH}-V_{Bat} = voltage seen from source to gate of the high side MOSFET
- R_{Gate} = gate resistance
- Q_{gd} = MOSFET gate to source defined by the MOSFET spec (see Table 1. STD65N55F3 dynamic parameters)
- V_{Bat} = battery voltage
- $V_{GS(th)}$ = MOSFET gate threshold voltage

From Eq. (37) and Eq. (38) we can calculate the high side gate resistances needed to achieve the rise and fall times required. Again, the diode resistor circuit shown in Figure 9. Low side PWM gate drive option is only needed if having similar rise and fall times are required.

One thing to note, the delay times are much larger than one would expect with these calculations. This is because the total gate capacitance (C_{iss}, Table 1. STD65N55F3 dynamic parameters) is much larger than the gate-drain capacitance (C_{rss}, Table 1. STD65N55F3 dynamic parameters). The difference can be orders of magnitude. The delay time is charging both the gate-source capacitance and the gate-drain capacitance. In contrast, the rise times (both low and high side switching) are only involving the gate-drain capacitance.

Solving Eq. (37) and Eq. (38) for R_{Gate} provides:

$$R_{Gate(on)} = \frac{t_{rise}}{C_{rss} ln\left(\frac{V_{GS(th)} - V_{GHxH}}{V_{Bat} - V_{GHxH} + V_{GS(th)}}\right)} \quad (39)$$

$R_{Gate(off)}$ subtracts the internal resistance found in the datasheet.

$$R_{gate(off)} = \frac{t_{fall} V_{GS(th)}}{Q_{gd}} - R_{GHx} \quad (40)$$

Using our example from Figure 4. Currents in an H-bridge (low side PWM) with a transition time of 100 ns and a gate threshold of 3 V the R_{Gate} value can be calculated as:

$$R_{Gate(on)} = \frac{100ns}{25pF * ln\left(\frac{3V - 24V}{12V - 24V + 3V}\right)} = 4.7k\Omega \quad (41)$$

$$R_{Gate(off)} = \frac{100ns \times 3V}{9.5nC} - 5.3\Omega = 26.3\Omega \quad (42)$$

As you can see, there is a difference between rise time and fall time resistor sizes due to the different driving voltages across the gate resistor. A difference in rise and fall times may not be too much of an issue. However, if this is critical to your application there is a solution. To obtain similar rise and fall times the gate resistor will need to be different when turning on versus when turning off. This can be done by using the same parallel diode and resistor as shown in Figure 9. Low side PWM gate drive option along with equations Eq. (29) and Eq. (30).

5.3 High side vs. low side PWMming considerations

Because of how the high side MOSFET gate is driven, the size of the turn on gate resistor, $R_{Gate(on)}$, is relatively large. This causes the turn-on delay times to get very large in comparison to the rise time. When considering the large on-time gate resistor of 4.7 Ω (plugging in $R_{Gate(on)}$ in Eq. (35)) gives a turn on delay of almost 2 µs. That may introduce up to 4% error in a 20 kHz PWM cycle.

However, when considering the relative size of the low side MOSFET gate resistors the delay times are not nearly as onerous. Plugging in the results of Eq. (27) into Eq. (21) gives a turn on delay time of less than 300 ns. This would indicate that using low side PWMming would be more favorable than high side PWMming as it would introduce less PWM error due to turn on delays.

Another consideration to help in determining whether to use high side or low side PWMming is the current sense amplifier reaction to PWMmed voltages. See Section 7.3 Load current sensing with PWM control for details.

5.4 Accuracy considerations

These equations will get you close to the actual rise and fall times. Because the MOSFET parameters are typically defined outside the range where they are used (e.g. gate charge is defined at 27 V, 65 A in this case – see Table 1. STD65N55F3 dynamic parameters), the rise/fall and delay times are at best an estimate. One may want to build and test a circuit to determine the optimum component values.

5.5 Dead time considerations

Dead time is required to prevent cross conduction when PWMming using active recirculation. Dead time is needed for both driving and recirculating phases. The needs can be different but the programmability for the dead time is universal. It applies to both sets of switches. There is not one dead time parameter for the high side switches and another for the low side switches. As a result we can consider the slowest transition time to determine how much dead time is needed.

Looking at Figure 13. Scope plot of HSD switching (Low side freewheeling) using 47 Ω gate resistor it provides a good indication on which side of the transition is slower. In Figure 13. Scope plot of HSD switching (Low side freewheeling) using 47 Ω gate resistor the H-bridge is PWMming on the high side using the low side MOSFETs as the freewheeling component. The transition from driving to freewheeling has the longest transition time. In this figure the dead time is programmed to be 2 us.

Note: it takes about a microsecond for the gate voltage to fall from V_{GHxH} to V_{Bat}. The C_{iss} of that MOSFET is about the same as the example MOSFET we have been using.

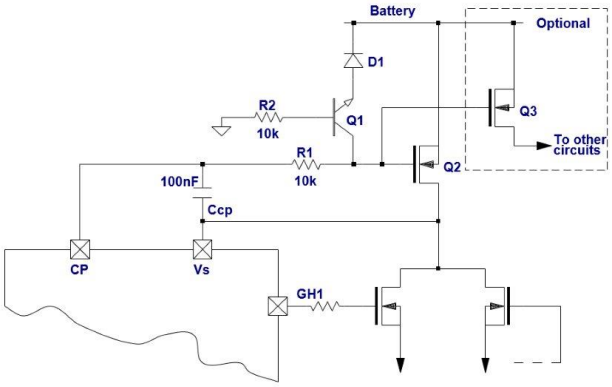
The dead time has to be longer than the delay time plus the transition (rise or fall) time of the slowest switch. Use the above equations for whichever method of PWMming you choose.

6 Reverse battery component selection

The fifth MOSFET and associated circuitry blocks current when the module is exposed to a negative voltage. This circuit is not intended to stop negative transients. This only provides an accidental reversal of the battery terminals during battery installation. The circuit is simple. We take advantage of the charge pump storage voltage and add an N-Channel MOSFET with the source tied to battery and the drain connected to the upper H-bridge MOSFET drains.

There are five components to select (R1, R2, D1, Q1 and Q2). They are all necessary for proper and safe operation.

Figure 14. Reverse battery circuit



During a reverse battery condition this circuit turns on Q1 thereby limiting the voltage at the Gate-Source terminals of Q2 to just over 0.7 V, keeping Q2 (and Q3) off. The resistors are there to limit the current in Q1 during the reverse battery condition. R2 limits the base current in Q1 during reverse battery. R1 limits the Q1 collector current thus allowing a voltage drop between the charge pump output, CP, and the Gate of Q2.

D1 is required to block battery voltage during normal operation. The typical reverse voltage capability of a standard small signal NPN transistor is around 7 V. This is not enough to survive normal operating voltages. D1 must have a high enough breakdown voltage to sustain any positive transients this circuit might experience. In automotive, this is typically 100 V (ISO 7637-2).

Q1 must safely drive the current in R1 with the base current created by R2. With a 10 kΩ resistor, the base current is approximately 1 mA. The collector current is similar. This makes for a fairly inexpensive transistor. Due to the charge pump, the collector voltage will reach approximately 13.5 V above battery. The NPN bipolar transistor collector to emitter breakdown voltage (BVCEO) will need to be sufficient to sustain that voltage.

This circuit can be used to protect not only the H-bridge but also the rest of the module as well from reverse battery. In some cases, the noise at Vs can be a concern to other more sensitive circuitry. With that, a second inverted MOSFET (Q3) can be installed in parallel with Q2. This is done by tying the gate and the source to the same nodes of Q2 and allowing the drain to drive the rest of the module. Q3 can be scaled to accommodate the type of loads that it supports. There would be no need, for instance, to have a very low Ohmic MOSFET for a simple 1 A or less load.

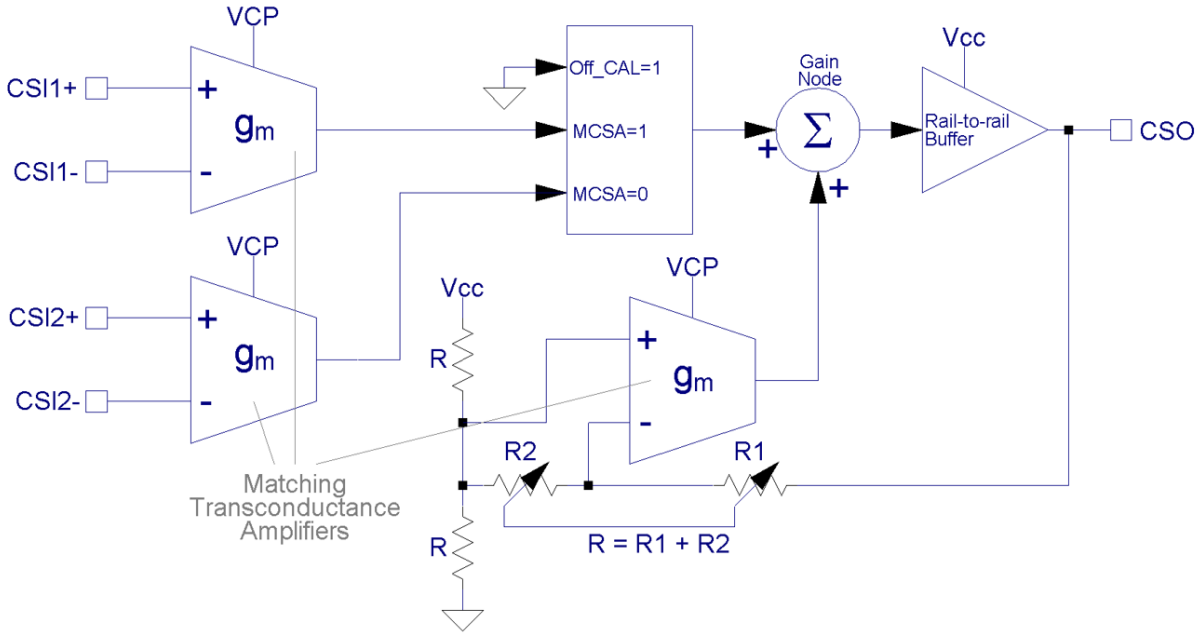
7 Current sense design

The current sense amplifier (CSA) is specially designed for current shunt automotive applications. It is a bidirectional, single-supply difference amplifier for amplifying small differential voltages in a wide common mode voltage range (-4 V to V_{CP} - 8V). It supports the current measurement at two shunts. The result of a respective shunt can be multiplexed to the microcontroller compatible output voltage by a SPI command (Section 13.2.2.2 Application register 02). It has a gain of 10, 20 or 50 that is SPI programmable (see Table 16. Current sense amplifier programmable gain table).

The inputs (CSI1+ / CSI1- and CSI2+ / CSI2-) are constructed as a transconductance stage. Therefore, a series resistor (for filtering etc.) should not exceed 50 Ω to keep the additional gain error below 1%.

The output works at half scale. That means that when there is no voltage difference between the CSI+ and CSI- terminals the output voltage is ½Vcc (V_{CSO0} = (½V_{CC}) V for $V_{(IDIFF)}$ = 0 V).

Figure 15. L99H02 current sense amplifier circuit



An internal offset measurement is available during normal operation with the "OFF_CAL" SPI-bit set to logic "1". When set to a logic “1”, the input transconductance amplifiers are disconnected and a virtual zero input is selected. With that, the software can safely determine and record the zero current CSO value even when there is current in the system (see Section 8 Calibration).

If any the current sense amplifiers are not being used, the inputs (CSA+, CSA-) should be tied together and then grounded. It is good design practice not to leave high impedance inputs floating. This is done to limit noise from being injected into the IC. Noise injected into a floating CSA input can interfere with the measurement of the other current sense amplifier. If neither current sense amplifiers are being used all inputs should be grounded.

7.1 Placing the sense resistor(s)

The L99H02 has the option of placing two sense resistors. This option is there to fully mitigate all possible fault conditions. Placing one sense resistor in the leg of the H-bridge and one in the ground (see Figure 1. L99H02 regions of operation) provides confirmation that the currents are flowing where they should. With this configuration a short of any kind can be detected.

Table 2. Fault detection methods

Fault		Description
Short to ground at either leg	1	VDS fault on high side switch Ground sense resistor reports zero current Leg sense resistor reports zero current
	2	VDS fault on high side switch Ground sense resistor reports zero current Leg sense resistor reports high current prior to VDS fault
	3	No VDS fault Ground sense resistor reports zero current Leg sense resistor reports normal current
Short across the load	1	Possible VDS fault on either active elements Ground and leg sense resistors report high current (prior to VDS fault)
Short to supply at either leg	1	VDS fault on low side switch No current in leg sense resistor prior to VDS fault Ground sense resistor reports high current (prior to VDS fault)
	2	VDS fault on ground sided elements Leg sense resistor reports high current prior to VDS fault Ground sense resistor reports high current (prior to VDS fault)
Shorted MOSFET	1	VDS fault on opposite switch in same leg High current in ground sense resistor prior to VDS fault No current in leg sense resistor
	2	Normal operation. Not detectable in one direction only

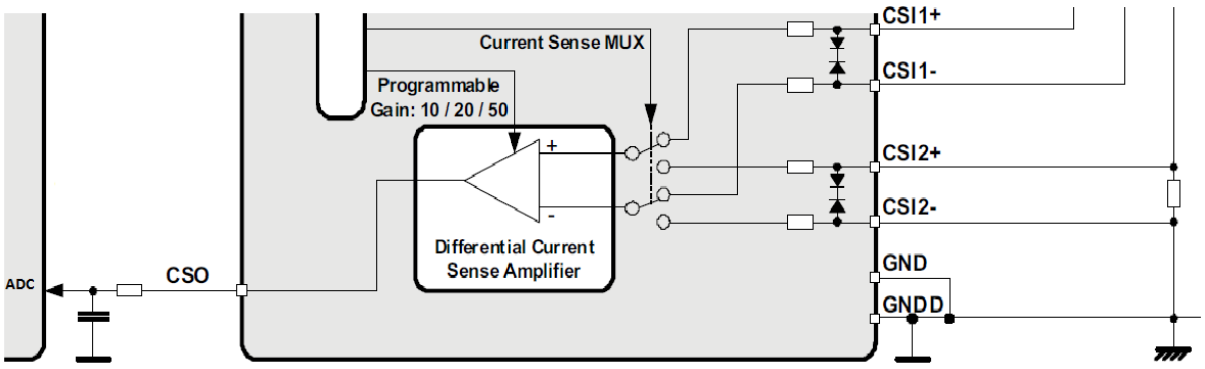
A sense resistor in the ground (below the lower MOSFETs) or supply (above the upper MOSFETs) shows no current when freewheeling. Placing a sense resistor in the motor “leg” allows for sensing freewheeling current. One other method would be to place two low side sense resistors, one on each leg. Then, freewheeling current could be sensed.

7.2 Selecting a current sense resistor value

The main concerns regarding current sense resistors are power dissipation and voltage drop. The goal is to accurately measure current without too much power dissipation or inaccuracy due to ADC tolerances.

An easy rule of thumb would be to choose the largest sense resistor size that the minimum gain and ADC voltage limits will allow. Then, if power dissipation is an issue back off on the value and, if necessary, increase the gain.

Figure 16. Current sense feedback circuit



The transfer equation from sensed current to ADC value can be calculated by the following equation:

$$Count_{ADC} = \left(R_{sense} I_{Motor} A_v + \frac{V_{CC}}{2}\right) \frac{2^{n_{ADC}}}{V_{Ref}} \quad (43)$$

Where:

- V_{Ref} = the ADC reference voltage
- V_{CC} = the logic supply voltage for the L99H02
- I_{motor} = the motor current to be measured
- A_v = the gain setting for the current sense amplifier
- n_{ADC} = the number of bits in the ADC

The current sense amplifiers provide a ½V_{CC} value for a zero current condition. This allows for bidirectional current sensing. This also reduces the voltage excursion for the output to ½ of the total voltage range of the L99H02 CSO pin or ADC V_{Ref}, whichever voltage is less. For a given gain and maximum current the maximum sense resistor value can then be defined by:

$$R_{sense}(\max) < \frac{V_{CSOh}}{2 \times I_{max} \times A_v} \quad (44)$$

Where:

- V_{CSOh} = the maximum L99H02 current sense output (CSO) voltage
- I_{max} = the maximum current to be measured
- A_v = the gain setting for the current sense amplifier

Note: the maximum voltage for the current sense output is determined by the L99H02 V_{CC} input voltage and is defined as:

$$\mathrm{V_{CSOh}} = \mathrm{V}_{CC} - 250\mathrm{mV} \quad (45)$$

If this value is higher than the maximum measurable ADC input voltage then the ADC maximum voltage should be used.

The maximum power dissipated in the sense resistor can be calculated by:

$$\mathrm{P_{sense\_max}} = I_{max}^2 \times \mathrm{R}_{sense} \quad (46)$$

For the minimum sense resistor value the equation is a bit different. Here the concern is with the ADC accuracy. Typically an ADC has an accuracy that is expressed in +/-counts. That is, the range of counts that a specific input voltage will be within. So, out of 2^n counts (where n represents the number of bits in the ADC) the error is usually small. A 12-bit ADC, for instance, can have an error of +/-6 counts. That is 6 counts out of a total of 4096 counts. That error is relatively small at the full range of the ADC. However, if the circuit is measuring just a few counts, at low current for instance, +/-6 counts may be 20% of what you are measuring. Even though we are measuring low currents at ½ Vcc the number of counts of error still applies.

The minimum sense resistor for a given gain can be expressed in terms of acceptable tolerance for a given ADC error as:

$$R_{sense(min)} > \frac{|Error_{counts}|^* V_{Ref}}{2^{n*} A_V^* Tolerance^* I_{min}} \quad (47)$$

Where:

- $Error_{counts}$ = the tolerance of the ADC in counts
- V_{Ref} = the ADC reference voltage
- I_{min} = the minimum current to be measured
- A_v = the gain setting for the current sense amplifier
- n = this is the number of bits in the ADC
- *Tolerance* = this is the tolerance that is required for the minimum current measured

The gain can be set to 10, 20 or 50. A higher gain setting allows for a smaller sense resistor value at a set tolerance. Actually, the gain can be adjusted depending on the current level being measured. This allows for low current accuracy with a high gain setting and high current measurement capability with a low gain setting. The current level thresholds for specific gain setting can be bounded by the maximum voltage on the CSO pin (maximum gain) and the maximum tolerance in the ADC (minimum gain).

$$\frac{|Error_{counts}|*V_{ref}}{2^{n}*R_{sense}*Tolerance*I_{load}} < A_v < \frac{V_{CSOh}}{R_{sense} \times 2 \times I_{load}} \quad (48)$$

The end result is that as the current goes down the gain can go up. The above equation is used to determine the gain setting needed for each current range. There will be considerable overlap in current ranges for each gain setting. A large amount of hysteresis is recommended to maintain stability. It is also recommended to maintain a gain as larger as possible. This minimizes the error due to the ADC.

Typically, when regulating to a current it might be best to stay at one gain setting while regulating. Error is only a concern at the regulation set point. As a result, the error due to a low current measurement still tells the PID controller that the current is low, the error is not an issue. As the current approached the regulation set point the proper gain setting allows for the proper tolerance.

7.3 Load current sensing with PWM control

When PWMming to regulate motor current, the voltage on the PWMmed side of the bridge transits from one rail to the other at the PWM frequency. The current sense amplifier inputs are susceptible to noise if exposed to these transitions.

To illustrate this Figure 17. Current sense during PWM below shows PWMming occurring on the “a” side of the bridge where the current sense resistor is placed. The voltage transition that occurs on that leg makes for a noisy current sense feedback (Figure 18. Current sense amplifier reaction to voltage swings).

Figure 17. Current sense during PWM

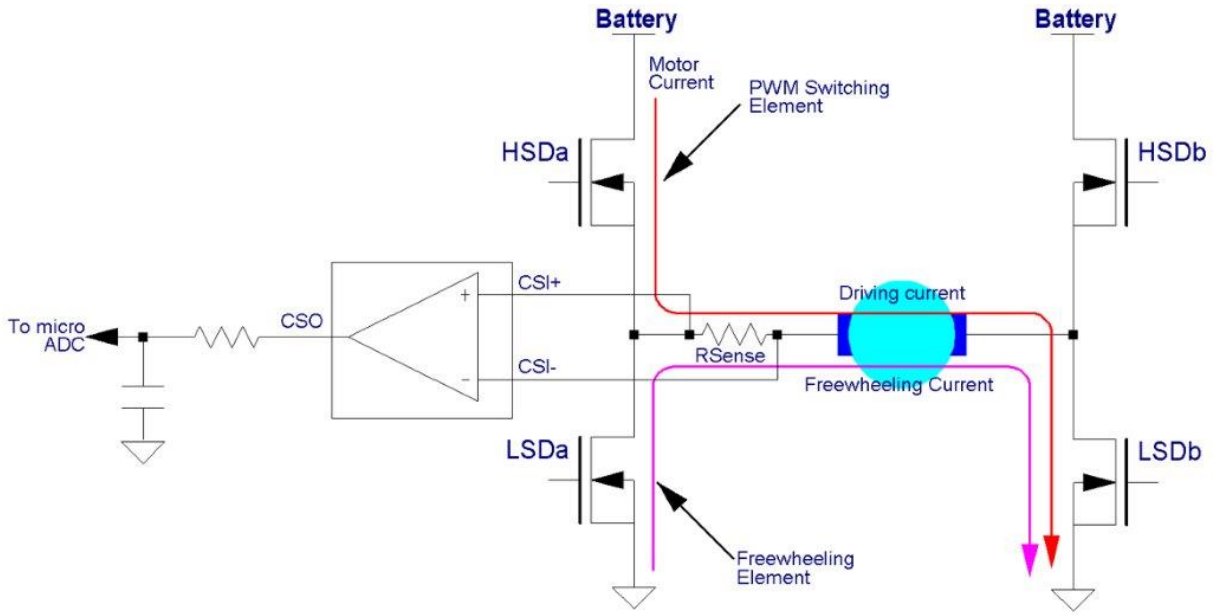
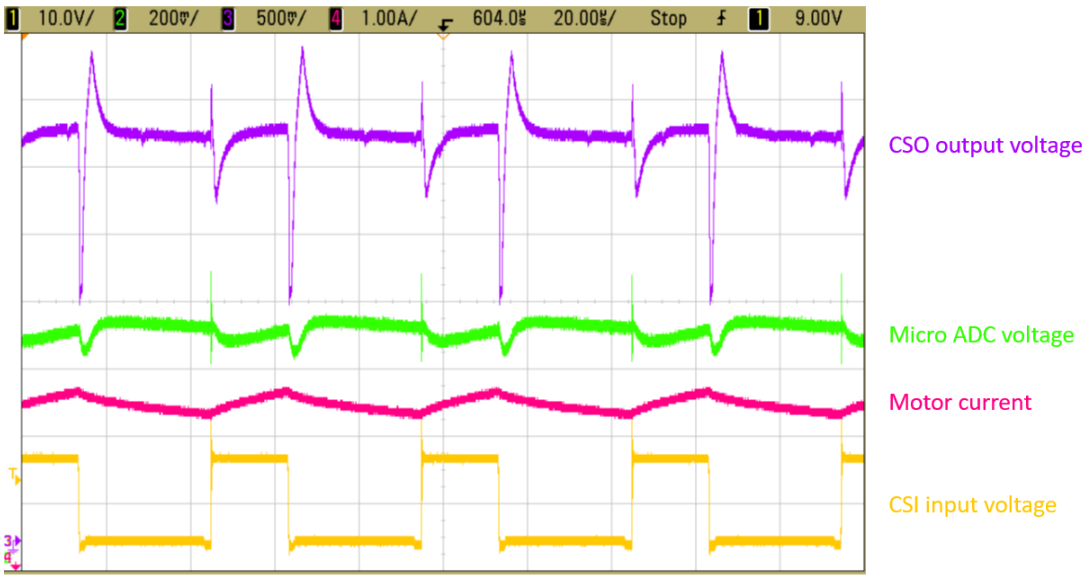


Figure 18. **Current sense amplifier reaction to voltage swings**



The solution is to maintain the PWM function on the opposite side of the current sense resistor. The L99H02 has the ability to select which leg is PWMmed by selecting which polarity is used (high side or low side PWMming). By PWMming only on the other side of the motor the noise in the current sense amplifier is minimized.

Figure 19. **Current sense on opposite side of PWM leg**

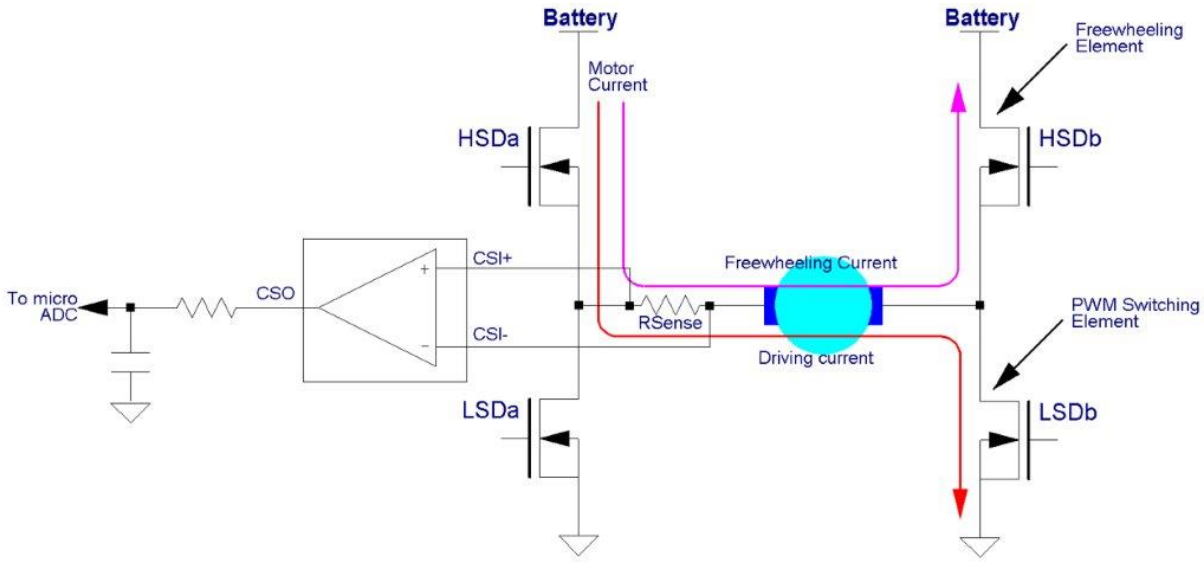
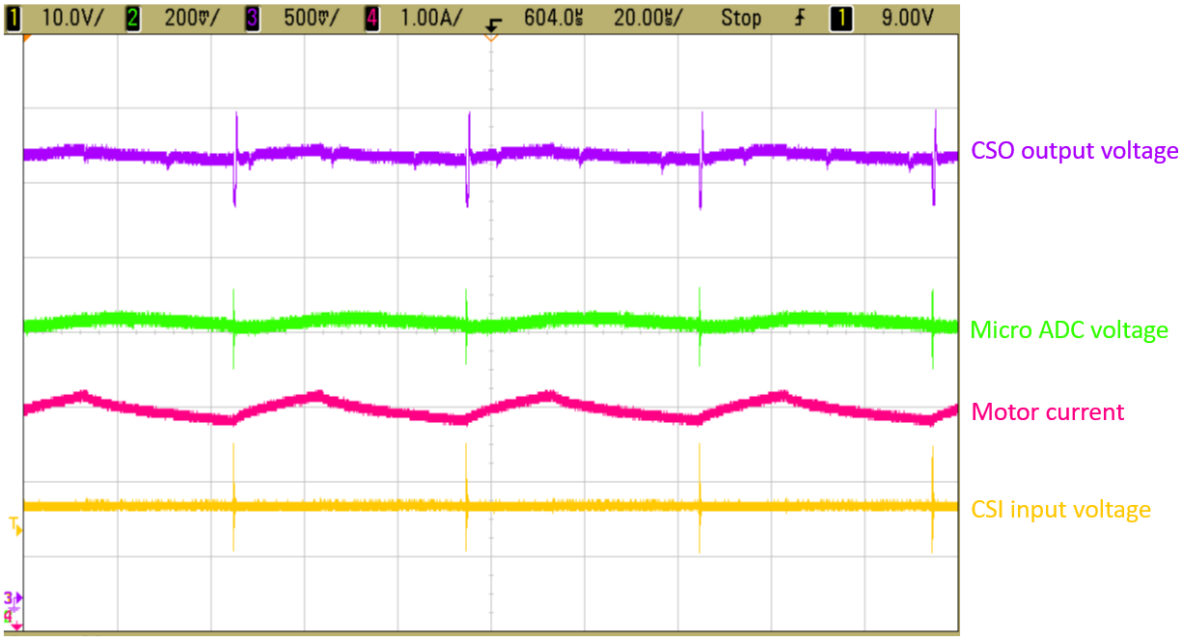


Figure 20. **Current sense amplifier behavior with PWM on the opposite leg**



8 Calibration

There are two steps to calibrate. The first is the input offset. This reduces any DC error due to input offset issues with the current sense amplifier. The second is gain correction. This simple one step operation can calibrate out the error due to both the gain in the amplifier as well as the error due to the resistor value. Between these two calibration steps, all errors are accounted for within the limits of the ADC. This includes R_{sense} tolerance, input offset tolerance, gain tolerance, and ADC reference voltage tolerance.

8.1 Input offset calibration

Input offset error is a DC error that shifts the current reading result up or down by a fixed amount regardless of the measured current. That error is included in the following transfer function equation.

$$V_{ADC} = (V_{CSO0} \pm V_{IOFFx} A_{Vx}) + I_{Shunt} R_{Shunt} A_{Vx} \quad (49)$$

Where:

- V_{ADC} = the voltage at the ADC input
- V_{CSO0} = ½ V_{CC}
- VI_{OFFx} = input offset voltage error at a specific gain (x)
- A_{Vx} = Gain setting (x = 10 ,20, 50)
- I_{Shunt} = Current in the shunt resistor
- R_{Shunt} = Shunt resistor value

The DC component is extracted out of that:

$$V_{CSO0}(V_{IOFFx}) = V_{CSO0} \pm V_{IOFFx} A_{Vx} \quad (50)$$

There are two ways to reduce the effects of input offset. The first is static. The second is dynamic.

The static input offset calibration is performed by reading the actual CSO voltage with the H-bridge off. This method is less accurate as it relies on the input offset of a matched transconductance amplifier to be the same as the actual amplifiers. Possible motor movement or external biasing might introduce errors while calibrating this parameter in this way.

The steps to this method of calibration are simple:

- Step 1: turn off the H-bridges so that there is zero current in the shunt resistor (s).
- Step 2: read ADC and store the zero current value(s) for future reference.

If there is no guarantee that the current sense inputs cannot be externally biased, then a dynamic input offset calibration tool is provided as mentioned in Section 7 Current sense design. This method is less accurate as it relies on the input offset of a matched transconductance amplifier to be as actual amplifiers. As a result there is some added tolerance associated with this method. The calibrated input offset values in the datasheet reflect this method of calibration. The steps to this method of calibration are:

- Step 1: Set the OFF_CAL bit to “1”. This is bit D5 in register 1 (01H).
- Step 2: Read ADC and store value for future reference (Cnt_{VCSOx} which is the ADC value of V_{CSO0}).
- Step 3: Clear the OFF_CAL bit (bit D5 = ”0”) in register 1 (01H).

Input offset calibration can be repeated throughout the life of the module. This is advised as the offset voltage can change with temperature. Input offset calibration will need to be done for each gain setting as well.

Eq. (49) then changes to reflect this calibration:

$$Cnt_{VCSOx} = \frac{V_{CSO0} \pm V_{IOFFx} A_{Vx}}{V_{ref}} 2^n \quad (51)$$

Where:

- Cnt_{VCSOx} = the adjusted digital representation of the VCSO0x after calibration. This value is used to calculate the measured currents and can be recalculated as often as necessary for optimum accuracy.
- V_{ref} = the ADC reference voltage
- 2^n = ADC bit count, n=12 for a 12 bit ADC.

8.2 Gain error calibration

Gain error calibration removes any error due to the device gain tolerance as well as the tolerance of the sense resistor. Once the input offset calibration is completed a gain error calibration can be done. This can only be done if the sensed current value is known. As a result, Gain error correction cannot be done dynamically when the module is in use. This calibration could be performed at the module end of line test and would need to be done once for every gain setting used.

The first step is to measure a reference current with the gain calibration in place. Assuming the offset, gain, and resistor tolerances were zero. This takes into account the above input offset calibration value of Cnt_{VCSOx} (Eq. (51)).

The ideal ADC count using the reference current, with the DC offset calibrated out, can be calculated by the following equation:

$$CNT_{VCSO\_ref} = I_{ref} R_{Shunt} A_{Vx} \frac{2^n}{V_{Ref}} + Cnt_{VCSOx} \tag{52}$$

The actual ADC count can then be used to generate the gain error correction term. This is calculated by the ratio of the actual measurement at the reference current to the theoretical value.

$$A_{Verror} = \frac{CNT_{VCSO\_meas}}{CNT_{VCSO\_ref}} \tag{53}$$

This value, A_{Verror}, is calculated and used for generating gain adjusted ADC thresholds at calibration. To calculate the gain adjusted threshold current values the gain error parameter is inserted into the standard current calculation below. Note that the offset is not included.

$$Cnt_{thesh}(I_{thresh}) = I_{thresh} R_{Shunt} A_{Vx} A_{Verror} \frac{2^n}{V_{Ref}} + Cnt_{VCSOx} \tag{54}$$

The offset (Cnt_{VCSOx}) is removed prior to storing in memory for reference. It will be inserted upon recalibration prior to each current measurement. This obtains the most accurate current reading. Of course, this does not need to be done if that level of accuracy is not needed.

$$Cnt_{thesh}(I_{thresh}) = I_{thresh} R_{Shunt} A_{Vx} A_{Verror} \frac{2^n}{V_{Ref}} \tag{55}$$

The calculated results from Eq. (55) are stored in memory for each threshold desired.

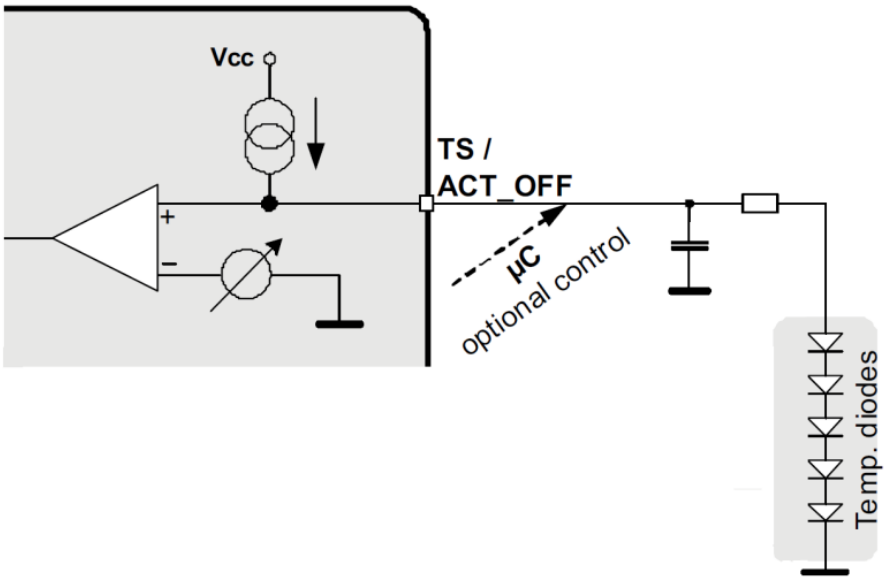
When a new current measurement is requested, an offset calibration can be performed first. That value (Eq. (51)) can then be subtracted from the ADC value measured. The result is then compared to the stored value for that threshold.

At the calibrated current value, the tolerance is typically less than 0.5 %. Any additional error is due to the ADC tolerance issues.

9 Thermal sensor operation

The TS/ACT_OFF pin provides for disabling output in fault conditions. This pin can be used as an H-bridge temperature sensor interface to disable the outputs in case of an overheating condition or as an external gate driver disable pin.

Figure 21. Thermal sensor circuit

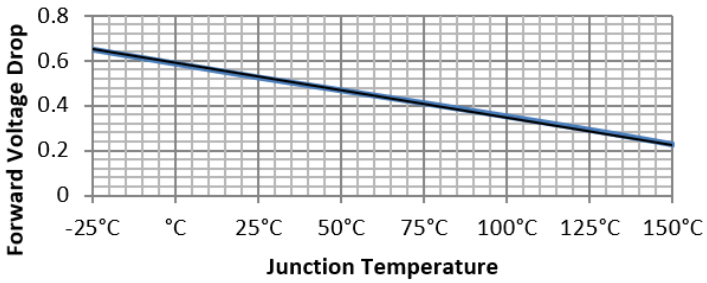


The TS/ACT_OFF pin is configurable via SPI by the EXT_TS bit. When configured as a thermal sensor the TS/ACT_OFF pin has a bias current, I_{TS_bias}. This current is used to bias a string of small signal diodes for the purposes of sensing their temperature. The I_{TS_bias} current is not present when the EN pin is pulled low.

9.1 Using discrete diodes

The thermal sensor function works by using the forward voltage negative thermal coefficient of a silicon diode. The forward voltage of a small signal diode is fairly predictable. Taking data from a standard small signal diode provides the following graph and equation.

Figure 22. Typical small signal diode forward voltage drop vs. temperature



From this graph numerical information can be estimated to generate an equation for diode forward voltage drop overtemperature.

$$V_{Diode} = n\left(0.588 - \frac{T_J}{413}\right) \quad (56)$$

For a string of diodes the equation is just multiplied by the number of diodes (*n*). The string of diodes can be placed near the MOSFET bridge to sense the circuit board temperature near the MOSFETs. This is imperfect but it does provide some safety. Carbonized FR4 is a reasonable conductor. Heating up the circuit board too much can cause uncontrolled high currents in the surrounding circuitry.

The L99H02 threshold is programmed using the 6 EXTH_X bits in application register 3 (see Section 13.2.2.3 Application register 03). The programming is broken down in two values that are used in the following equation.

$$V_{TS\ threshold} = n(0.31 + m \times 0.03) \quad (57)$$

The maximum allowable voltage is V_{cc}-1V. V_{cc} is the 5 V/3.3 V supply.

The simplest method is to first solve what the threshold voltage is. That is needed based on the string and type of diodes used applying the V_{Diode} equation (Eq. (56)). Then, to determine the value of *n*, divide in this section the Eq. (56) by an integer such that it results in a value that is between 0.31 and 0.52. These are the two end points for $V_{TS\ threshold}$ (Eq. (57)) parenthetical expression, (0.31 + *m x* 0.03), where *m* is at its minimum (0) and maximum values (7).

$$\frac{V_{Diode}}{0.52} < n\left(integer\right) < \frac{V_{Diode}}{0.31} \quad (58)$$

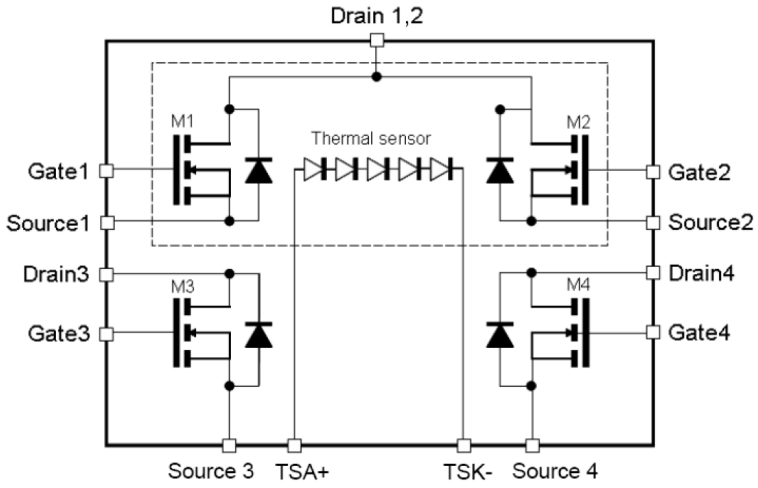
Then subtract 0.31 from V_{Diode}/n and divide by 0.03 to obtain the integer *m*.

$$m\left(integer\right) = \frac{\frac{V_{Diode}}{n} - 0.31}{0.03} \quad (59)$$

9.2 Using the VNH7013 thermal sensing diode string

The VNH7013 is four MOSFETs configured as a simple 13 mΩ per leg H-bridge in a single package. It has within the high side MOSFETs a string of diodes that can be used to sense the junction temperature of the high side MOSFETs.

Figure 23. VNH7013 block diagram



The string of diodes embedded in the high side drivers provide the thermal information to the TS/ACT_OFF pin. The TSA+ pin is tied to the TS/ACT_OFF pin and the TSA- pin is tied to the IC ground at the L99H01 or L99H02 ground pin(s). The bias current, I_{TS_bias}, sets up a voltage across the diode string that is measured by the L99H01 or L99H02. This voltage is set by the equation:

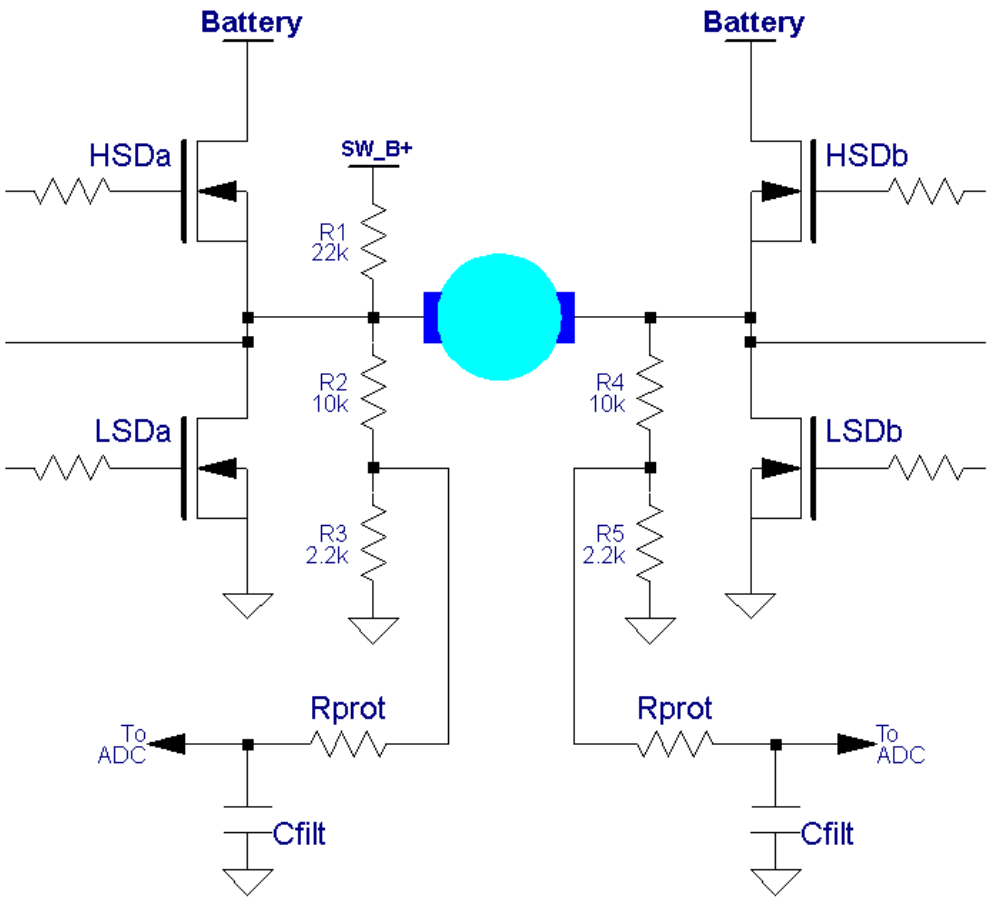
$$V_{TSA+} = V_F + S_F(T_{diode} - 25°C) \quad (60)$$

Where V_F is specified as 3.88 V and S_F is -8.3 mV/K. Again, the simplest method to determine the thermal sensor threshold integer values for *m* and *n* is to insert V_{TSA}+ from Eq. (60) in place of V_{Diode} in equations Eq. (58) and Eq. (59).

10 Off-state diagnostics

Detecting a faulted load prior to turn-on can be advantageous as it eliminates potential high stress events such as a turning on into a shorted load. While in the off state, the H-bridge can be checked for open load, short to ground or supply as well verify MOSFET integrity prior to actuation. This can be accomplished with a minimum of a few resistors and the incorporation of two ADC inputs as shown in the followig figure.

Figure 24. Off-State diagnostics using two ADC inputs

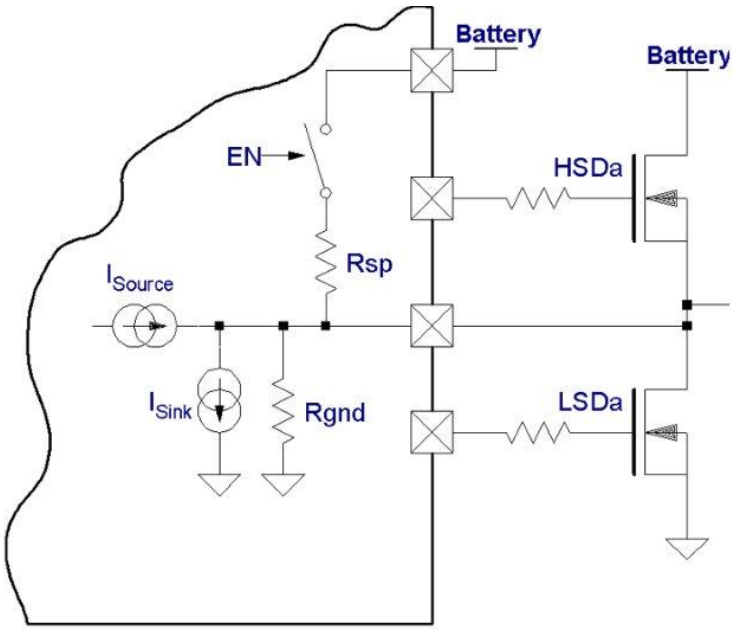


10.1 Modes of operation

When considering off-state diagnostics placing the H-bridge in tri-state allows for external circuitry to bias the bridge. With the bridge externally biased we can then determine shorts to ground or battery as well as open load. There are three modes where the L99H02 has the OUTPUT MOSFETs in tri-state. Two of which show up clearly in Figure 1. L99H02 regions of operation . The first two are standby. The first is when EN is low (standby) and the second is when EN is high and there has not yet been a valid SPI frame. Prior to a valid SPI frame and after the EN pin is high the L99H02 remains in standby. The reason we mention it is because the bias currents on the outputs change when EN is low and when EN is high but prior to a valid SPI frame. And the third is when TS/ACT_OFF is low (ACT Off or thermal shutdown). These three modes effectively turn off the H-bridge MOSFETs. However, the gate and source currents are not the same in these three states.

MOSFET integrity checking requires activating the individual MOSFETs. As a result, these tests should be performed after the off-state diagnostics have been completed with no faults reported.

Figure 25. L99H02 internal currents (one side)



When EN is low, I_{Sink} (see the figure above) is active and I_{Source} is disabled. This sink current can range from 375 µA to as much as 1.5 mA. As well as determining shorts to supply that current would overwhelm any reasonable bias circuit for determining the health and well-being of the H-bridge.

With EN high, TS/ACT_OFF low, prior to a valid SPI frame I_{Sink} remains active. However, the current is different than when EN is low. I_{Sink} current, prior to a valid SPI frame, ranges from 150 µA to 550 µA.

With EN high, TS/ACT_OFF low, and after a valid SPI frame I_{Source} (the figure above) is active and I_{Sink} is disabled. I_{Source} is an artifact of the active circuitry keeping the high side gate voltage tied to the source. This current ranges from 520 µA to 850 µA. With a minimum of external components, we can take advantage of I_{Source} to determine open load or shorts to ground of the H-bridge.

It should be noted that the presence of bias currents when EN is low does not have an effect on the quiescent current of the H-bridge system unless there are external circuits pulling up on the motor terminals. Since this off-state circuit makes that, it is recommended that the pull-up resistor R1 should be connected to a switched supply. Otherwise there will be additional current when EN is low.

Table 3. Bias currents in the different modes

PINs		Condition	I_{Sink}			I_{Source}		
TS/ACT_OFF	EN		Min	Typ	Max	Min	Typ	Max
Low	High	Prior to a valid SPI frame	150 µA	280 µA	550 µA	0 A	0 A	0 A
Low	High	After a valid SPI frame	0 A	0 A	0 A	280 µA	520 µA	850 µA
X	Low	All conditions	375 µA	750 µA	1.5 mA	0 A	0 A	0 A

The internal resistances (RGND and RSP) vary with process and temperature quite a bit. However, they tend to vary together. We can define their limits by the following table:

Table 4. **L99H02 internal resistances**

PINs		Condition	I_{Sink}			I_{Source}		
TS/ACT_OFF	EN		Min	Typ	Max	Min	Typ	Max
Low	High	Prior to a valid SPI frame	14 K	20 K	26 K	14 K	20K	26 K
Low	High	After a valid SPI frame	14 K	20 K	26 K	14 K	20K	26 K
X	Low	All conditions	N/A	N/A	N/A	14 K	20K	26 K

10.2 Off-state open load detection

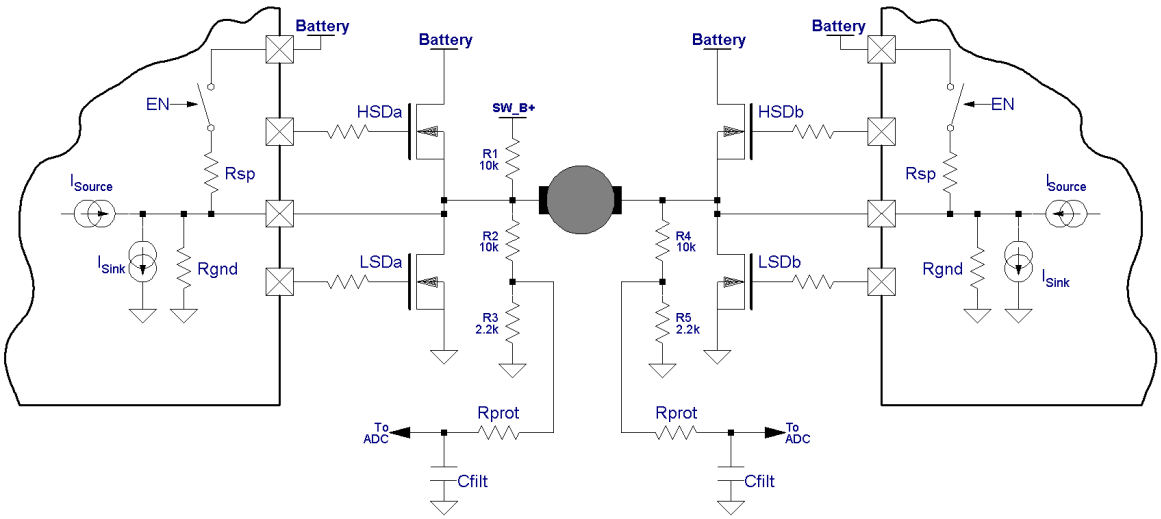
Referencing Figure 24. Off-State diagnostics using two ADC inputs, with the TS/ACT_OFF pin held low, I_{Source} is present. If there is a load connected, the ADCa and ADCb Voltages will be virtually identical. Once the load is removed $R_1//R_{SP}$ (R_1 in parallel with R_{SP}) will pull ADCa higher than ADCb. The difference will depend on the value if I_{Source} and the battery voltage.

10.2.1 Open load equations

In TS/ACT_OFF state the current contributors to the circuit are:

- Battery through $R_1//R_{SP}$
- I_{Source} out of SH1 (leg a)
- I_{Source} out of SH2 (leg b)

Figure 26. **Off-state diagnostic circuit**



First, to simplify the circuit we assume that R2=R4 and R3=R5 and then we make an equivalent resistance from the parallel resistances R_{GND} in parallel with the combination of R2 and R3 (Eq. (61)).

$$R_{EQ1} = \frac{R_{GND}(R_2 + R_3)}{R_2 + R_3 + R_{GND}} \quad (61)$$

We then simplify the supply side of the equation by making an equivalent resistance from R_1 and R_{SP} where R_{SP} is involved. R_{SP} disappears with EN low. With that we can generate the motor terminal voltages:

$$R_{EQ2} = \frac{R_1 * R_{sp}}{R_1 + R_{sp}} \quad (62)$$

The equation defining the ADC voltage when there is an open load is:

$$V_{ADCa\_OL} = \frac{\left(V_B + I_{Source} * R_{EQ2}\right) R_{EQ1}}{R_{EQ1} + R_{EQ2}} * \frac{R_3}{R_2 + R_3} \quad (63)$$

The range of voltages seen is between 1 V and 2 V with a battery voltage range of 9 V to 16 V.

The equation defining the voltage at ADCb is simpler as there is only R_{SP} pull-up resistor (equivalent resistance is not needed to simplify the equation):

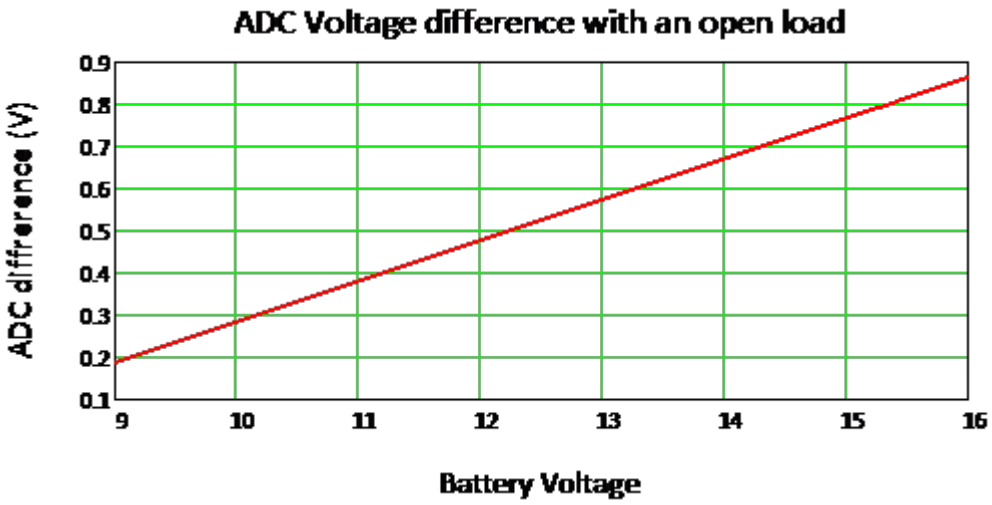
$$V_{ADCb\_OL} = \frac{I_{Source} * R_{EQ1} * R_5}{R_4 + R_5} \quad (64)$$

We can do some simplification where we understand that R2=R4 and R3=R5. Then subtracting the two equations provides the difference in ADC voltages required to detect an open load.

$$V_{ADCab\_OL} = \frac{R_3 * R_{GND} * \left(V_B - I_{Source} * R_{EQ1}\right)}{\left(R_{EQ1} + R_{EQ2}\right)\left(R_2 + R_3 + R_{GND}\right)} \quad (65)$$

The following figure illustrates how these equations look graphically. The trend for the differential is positive for both the source current (I_{Source}) and the switched battery voltage (V_B). Below is the worst-case (low) differential voltage. This occurs when the source current is the highest and the internal resistances are also the highest. Typically, the resistances vary inversely with the current in a semiconductor. Since we are not taking that into account here, this would then definitely be worst-case.

Figure 27. Worst case low ADC open load differential voltage

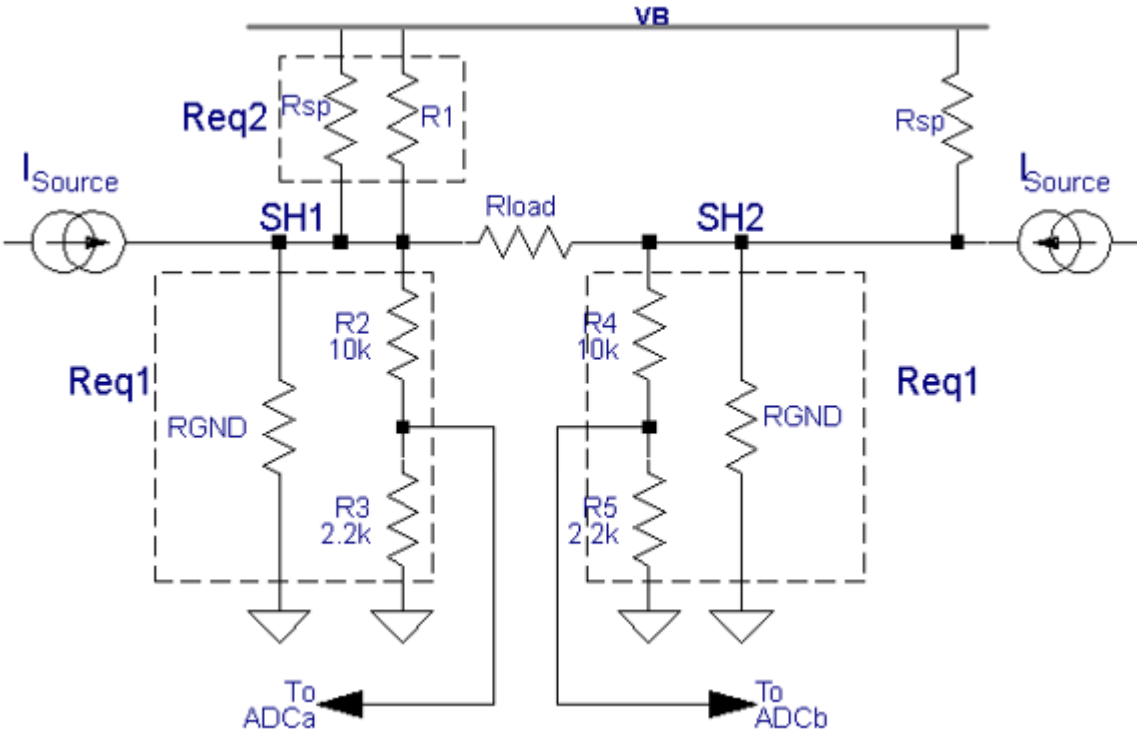


The worst case low voltage of off-state open load detection is 187 mV. Using a small margin knowing this is more than worst case we can use a 150 mV difference between the two ADC inputs as a safe threshold for detecting an open load. 150 mV translates to 38 counts of difference between the two inputs.

10.2.2 Normal load equations

In the normally loaded H-bridge a small load resistance between the SH1 and SH2 terminals exists. We can assume that the voltage between the motor terminals, when there is a motor present, is virtually zero. The only contributor to the current through the motor terminals is the current through R_1//R_{SP} (Figure 26. Off-state diagnostic circuit). Since the motor resistance will be orders of magnitude lower than that resistance, we can assume near zero voltage across it.

Figure 28. **Normally loaded off state equivalent circuit**



With TS/ACT_OFF low and EN High (and after a valid SPI command) R_{SP} and I_{Source} are involved. Again, we can simplify the circuit by assuming that R2=R4 and R3=R5 and then by making an equivalent resistance from the parallel resistances R_{GND} in parallel with the combination of R_2 and R_3 (Eq. (61)) as well as the R_1//R_{SP} resistances (Eq. (63)).

$$V_{SH1\_norm} = \frac{R^2_{EQ1}{}^{*}\left(V_B + 2^{*}I_{Source}{}^{*}R_{EQ2}\right) + R_{load}{}^{*}R_{EQ1}{}^{*}\left(V_B + I_{Source}{}^{*}R_{EQ2}\right)}{R^2_{EQ1} + 2R_{EQ1}{}^{*}R_{EQ2} + R_{load}{}^{*}R_{EQ1} + R_{load}{}^{*}R_{EQ2}} \quad (66)$$

Using the above definition for V_{SH1} we can insert that into the equation for V_{SH2} to obtain:

$$V_{SH2\_norm} = \frac{\left(V_{SH1\_norm} + I_{Source}{}^{*}R_{load}\right)R_{EQ1}}{R_{load} + R_{EQ1}} \quad (67)$$

Subtracting the two equations to find the off-state voltage across the motor we get:

$$V_{motor} = \frac{R_{load}{}^{*}\left(V_B - I_{Source}{}^{*}R_{EQ1}\right){}^{*}R_{EQ1}}{R^2_{EQ1} + 2R_{EQ1}{}^{*}R_{EQ2} + R_{load}{}^{*}R_{EQ1} + R_{load}{}^{*}R_{EQ2}} \quad (68)$$

The worst-case voltage difference using a 10 Ω motor is less than 7 mV (6.82 mV).

Having a 6.82 mV differential voltage at the motor terminals reduces by ~5 x at the ADC inputs. This difference between the ADC inputs is then a little more than 1.2 mV. That is right at a single bit for a 12-bit ADC on 5 V.

In normal operation, the ADC input voltages range from just under 1 V at 9 V and a minimum I_{Source} to 1.9 V at 16 V and a maximum I_{Source}. That is a conversion of 204 counts to 382 counts on a 5 V 10 bit ADC.

10.2.3 Short to ground

The short to ground diagnostic uses the TS/ACT_OFF pin to tri-state the outputs as well. With TS/ACT_OFF low and EN high the I_{Source} internal current is present (See Figure 25. L99H02 internal currents (one side)). This is the same condition for open load detection. As a result, both can be detected with the same ADC conversion.

In a short to ground condition the ADC reading will be at or near 0V (0 or close to 0 counts). This is then compared to what would be a “normal” ADC reading.

Under normal conditions there is no discernable voltage drop across the motor when the systems is in tri-state. With that, the effects of the load resistor on Eq. (66) are removed. Then, by forcing R2=R4 and R3=R5 further simplification can be made. From those two actions we can generate the equation for the expected voltage at both of the ADC inputs.

$$V_{ADC} = \frac{R_{EQ1}\left(R_{SP}{}^{*}V_B + R_{EQ2}{}^{*}V_B + 2{}^{*}I_{Source}{}^{*}R_{SP}{}^{*}R_{EQ2}\right)}{R_{SP}{}^{*}R_{EQ1} + 2{}^{*}R_{SP}{}^{*}R_{EQ2} + R_{EQ1}{}^{*}R_{EQ2}} * \frac{R_3}{R_2 + R_3} \quad (69)$$

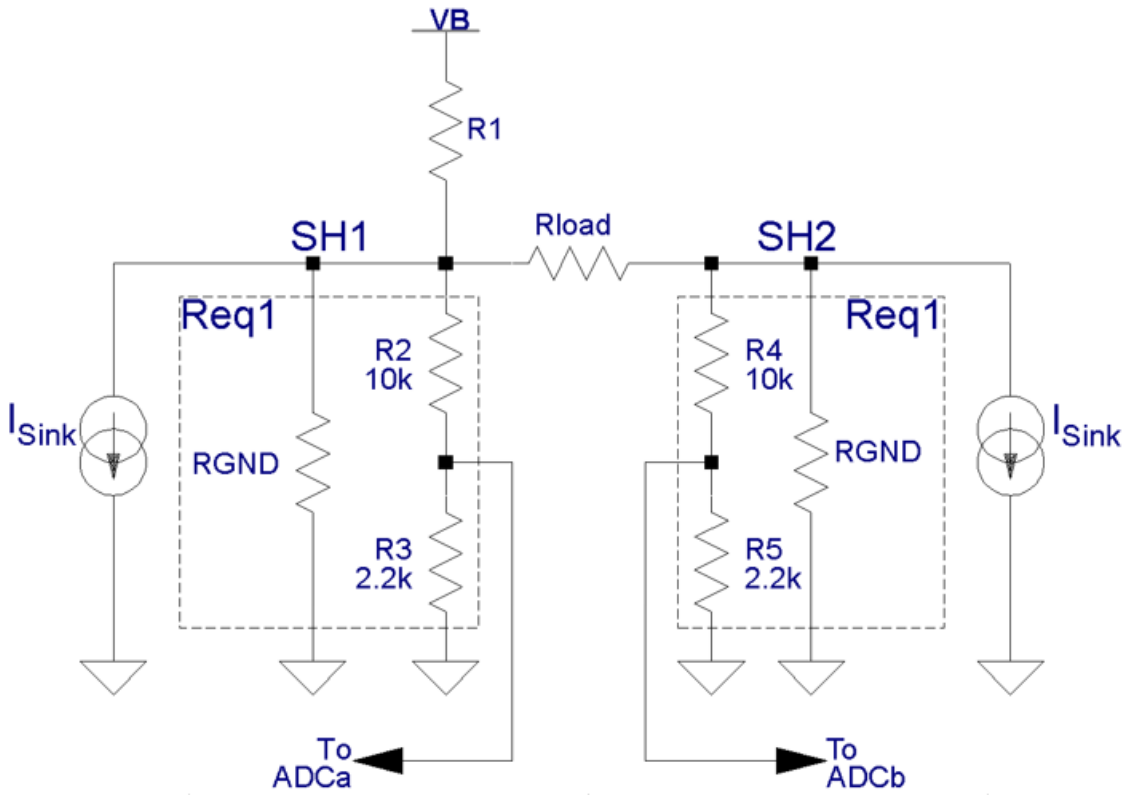
In normal operation, the ADC input voltage on ADCa range from just under 1 V at 9 V and a minimum I_{Source} to 1.9 V at 16 V and a maximum I_{Source}. That is a conversion of 204 counts to 382 counts using a 5 V, 10-bit ADC.

In the presence of a short to ground the ADC input voltages it will be at or near 0 V. Setting a threshold of 128 counts would be a safe margin. Therefore, any ADC reading below 128 (07F h) would indicate a shorted to ground condition.

10.2.4 Short to battery

Short to battery is a bit difficult as the voltages on the ADC while shorted to battery fall within the range of Eq. (69). To overcome this, we switch from using TS/ACT_OFF to using the Enable pin. With EN low the bias circuit changes from a source current to a sink current. This brings the worst case motor terminal voltages below 500 mV over all conditions (min and max resistances and currents, from 9 V to 16 V).

Figure 29. Off state diagnostic equivalent circuit with EN low



The equation that defines the ADC voltage measuring the voltage at SH1 with a normal load is defined by the following equation. This voltage is at most under 500 mV (450 mV max with I_{Sink} = 375 µA, V_B = 16 V). Whereas, the measured voltage with the output shorted to battery would be greater than 1.6 V (V_B = 9 V).

$$V_{ADCa\_ENlow} = \frac{R_{EQ1}\left(R_{EQ1}{}^{*}V_B - 2{}^{*}I_{Sink}{}^{*}R_1{}^{*}R_{EQ1} + R_{load}{}^{*}V_B - I_{Sink}{}^{*}R_1{}^{*}R_{load}\right)}{R^2{}_{EQ1} + 2{}^{*}R_1{}^{*}R_{EQ1} + R_1{}^{*}R_{load} + R_{EQ1}{}^{*}R_{load}} * \frac{R_3}{R_2 + R_3} \quad (70)$$

500 mV on a 5 V 10 bit ADC looks like 102 counts. At 1.6 V the count is over 330. Using a threshold of 256 counts (0FF h). Anything above 0FF h would be considered a short to battery.

10.2.5 Off-state diagnostics summary table and flow chart

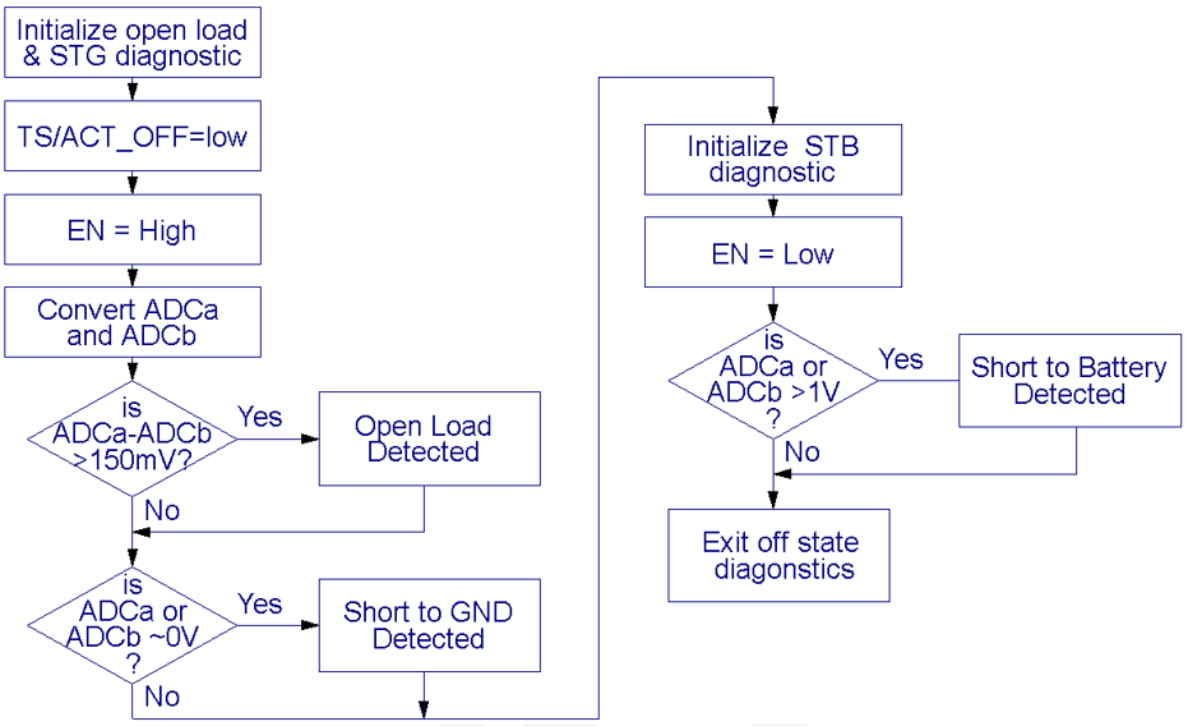
In this section there is a summary of the pin configurations for the off-state diagnostics with the expected results as seen at the ADC inputs.

Table 5. off-state diagnostic conditions

Diagnostic	PINs		Condition	ADC voltage	
	TS/ACT_OFF	EN		Pass	Fail
Off-state open load	Low	High	V_{ADCa} - V_{ADCb}	~0 V	>187 mV
Short to ground	Low	High	V_{ADCa}	>990 mV	~0 V
Short to supply	X	Low	V_{ADCa}	<500 mV	>1.6 V

The flow chart showed in the following figure, is one of the algorithm that can be used to detect open load, short to battery or short to ground. This flow does not drop out as soon as a single fault is detected. It is possible that there can be an open load with one terminal shorted to ground and the other shorted to battery. This algorithm does not report specific output conditions, only that the fault exists. More details can be parsed out if desired. To prevent unwanted actuations be sure to have TS/ACT_OFF low prior to allowing EN high. This chart also assumes that when EN is high, the Watchdog is being serviced (i.e. a valid SPI frame has occurred prior to measurement).

Figure 30. Off -state diagnostics flow chart



11 MOSFET integrity check

After performing, and passing, all of the off-state diagnostics, the external MOSFETs can be checked to verify that they respond to gate voltage control. It is important that the off-state diagnostics all pass prior to starting these tests as these tests turn on MOSFETs one at a time. Turning on MOSFETs in the face of faulted loads will at best provide false indications and at worst stress the drivers unnecessarily.

11.1 High side MOSFET integrity check

MOSFET integrity tests take advantage of passive freewheeling to enable a single MOSFET at a time. Setting the L99H02 to have passive freewheeling requires programming both FW_PAS (bit D6 in application register 1) and FW (bit D3 in application register 2) to “1” (see Table 10. Summary of registers in the Programmers guide below). Once set with DIR High and PWM low, GH1 will only drive the high side MOSFET for leg “a”. All other MOSFETs are off.

At this point, if the MOSFET is functioning properly, a short to battery indication should be seen on the ADCa and ADCb inputs. That is, a voltage above 1.6V as described in Section 10.2.4 Short to battery .

Changing the DIR input from a “1” to a “0” will check the functionality of the high side MOSFET in leg “b” of the H-Bridge.

Comparing the voltages with the voltages previously obtained during the off state open load testing will determine MOSFET functionality.

11.2 Low side MOSFET integrity check

As in the high side MOSFET integrity check, the Low side integrity check also uses the FS_PAS and SW bits. In this case the FW_PAS bit remains unchanged at “1”. However, the FW bit is changed to a 0 to incorporate low side freewheeling functionality (see Table 10. Summary of registers in the Programmers guide below). Once set with the DIR and PWM pins held low, GL1 will only drive the low side MOSFET for leg “a”. All other MOSFETs are off.

At this point, if the MOSFET is functioning properly, a short to ground indication (see Section 10.2.3 Short to ground) should be seen on the ADCa and ADCb inputs.

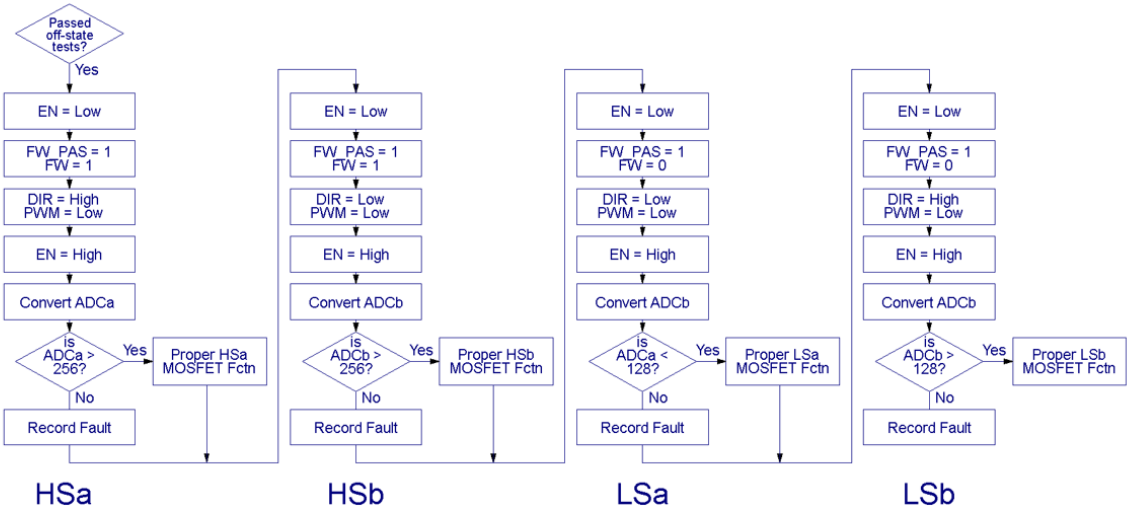
Changing the DIR input from a “0” to a “1” will check the functionality of the low side MOSFET in leg “b” of the H-bridge.

Comparing the voltages with the voltages previously obtained during the off state open load testing will determine MOSFET functionality.

11.3 MOSFET integrity check summary table and flow chart

The test flow for the MOSFET integrity check suggestion.

Figure 31. MOSFET integrity check flow chart



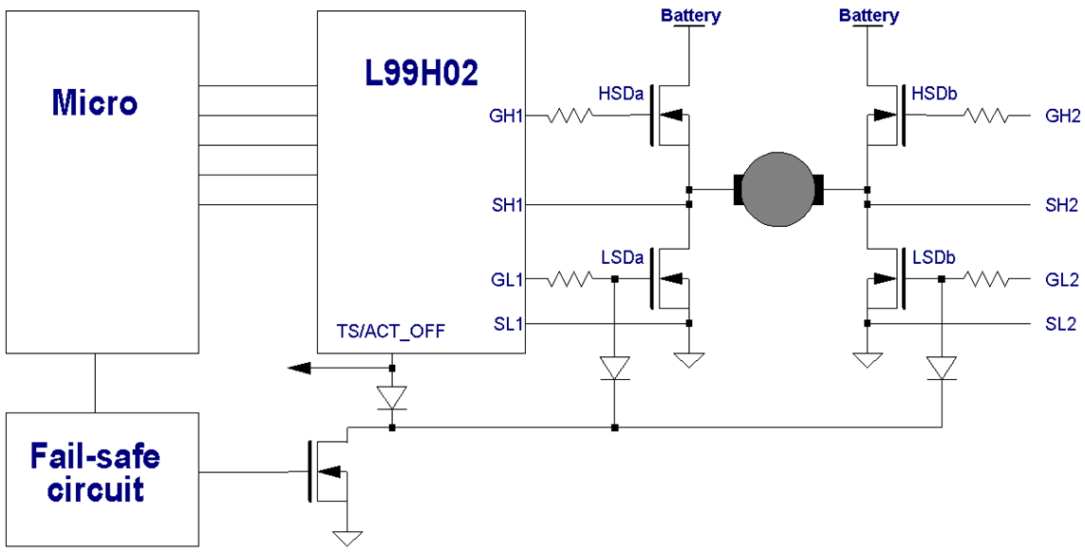
12 Fail safe circuit

In high current applications a failed MOSFET can cause dramatic thermal events that can be quite serious. Having the controller or the host micro fail can accidentally cause the H-bridge to actuate as well. Either scenario has potential for nasty outcomes. Fortunately, the L99H02 has a watchdog circuit that requires periodic attention or the device disables the outputs. That said, an external failsafe circuit that can disable the H-bridge or interrupt the circuit in case of something going wrong with the driver might be reasonable. We will explore a few options.

12.1 Disabling the elements

Considering the off-state diagnostics, most faulted outputs can be detected. With a short to ground or supply detectable the only failsafe functionality needed is if the micro or the L99H02 is not operating correctly. With the off-state diagnostics, shorted MOSFETs can be detected. The micro can then not request any action from the H-bridge avoiding any inadvertent exothermic behavior. With that said, an effective fail-safe circuit can protect the application by disabling the H-bridge low side elements at the element. This will prevent the controller or the L99H02 from trying to drive the load. In this case, the intent is to disable the low side drivers which will prevent any current path to ground at the motor. This is not a total fail-safe in that a low side MOSFET may be failed. Shorting its gate to ground will do nothing to turn that failed MOSFET off. This is somewhat mitigated by the ability to perform off-state diagnostics. However, the best solution would be to pull all MOSFET gates to ground or interrupt the supply in the face of a fail-safe event.

Figure 32. Failsafe intervention circuit example, disabling the low side MOSFETs



In the figure above the failsafe circuit disables both the L99H02 and the low side MOSFETs. This can be extended to the high side MOSFET gates as well with the addition of two diodes. This circuit does require that there be some gate resistance to guarantee the ability to override the L99H02 gate drive should it be damaged.

The TS/ACT_OFF pin can be pulled low by the failsafe circuit as well. If the TS/ACT_OFF pin is being driven by the micro, then a protection resistor between the micro and the TS/ACT_OFF pin is required. The value of this protection resistor is determined by the current capability of micro. Typically, 10 kΩ would be sufficient. If the thermal sensor with the bias current is used, then no resistance is needed and would actually cause problems.

The pull-down transistor, Q1, can be sized based on the expected current draw from the gate resistors. In a worst-case scenario, the voltages at the L99H02 pins would be just under battery. With TS/ACT_OFF low none of the gate drives would be high. However, if the L99H02 was damaged then the charge pump would be off. The gate drive outputs could be stuck at “high” which, without the charge pump, would be about two V_{BE}’s below battery.

The current in Q1 would be defined by the current draw through the gate resistors:

$$I_{Q1} = 2^{*}\frac{V_{Batt} - 2^{*}V_{BE}}{R_{GateL}} + 2^{*}\frac{V_{Batt} - 2^{*}V_{BE}}{R_{GateH}} \quad (71)$$

This equation includes the gate pull-down current from the upper transistors as well. If the upper transistors are not part of the failsafe circuit then the second half of the equation can be left off.

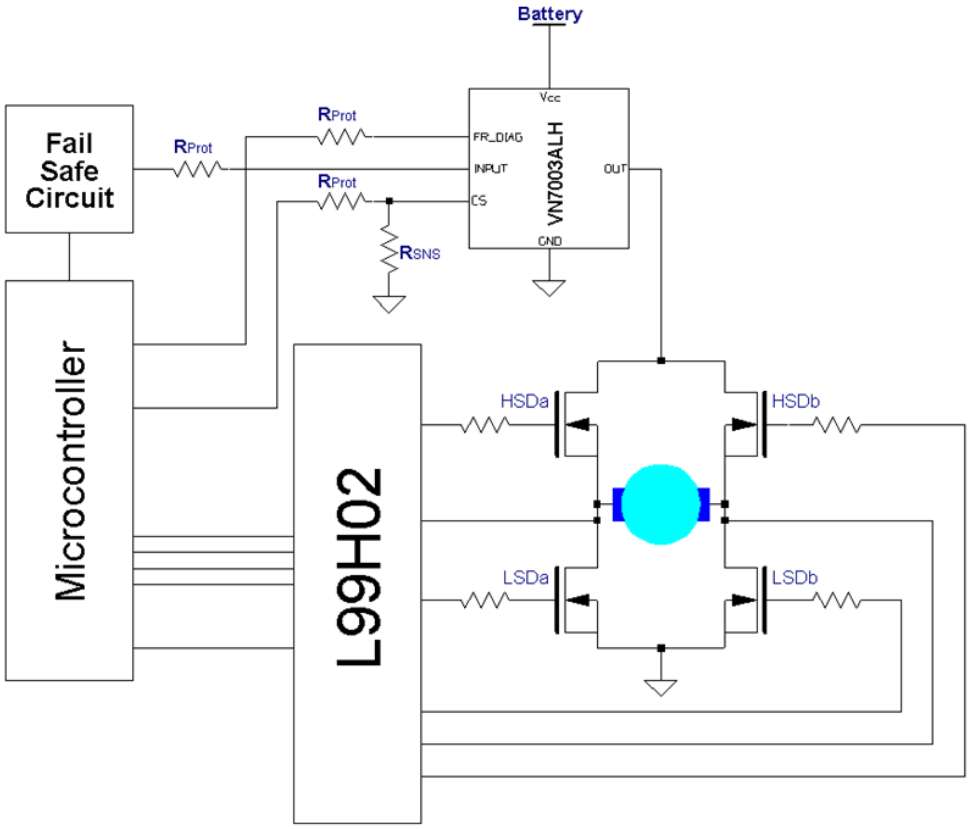
A simple 1 A diode will work for each of the 4 gate pull-downs. Using the already calculated gate resistances above the mode the current would be as well as under 1 A for all four gates. We need to keep the gate voltages well below the gate thresholds. I would suggest a 0.1 Ω MOSFET as the most. However, a calculation can be derived to ensure the gate voltages at turn off are below the gate thresholds.

$$R_{DSon} < \frac{V_{GSth} - V_{Diode}}{I_{Q1}} \quad (72)$$

12.2 Disconnecting the supply

A more secure failsafe circuit disconnects the supply from the H-bridge all together. This requires a lower Ohmic MOSFET that can handle the maximum currents the H-bridge can demand. ST has a number of low Ohmic protected high side drivers as well as MOSFET controllers that can be used to disable the supply. These drivers require a logic high signal to enable. As a result, a simple watchdog circuit that goes low when there is a failure would be sufficient.

Figure 33. High side switch failsafe circuit example



13 Programmer's guide

This section is intended to summarize the content there is in the datasheet. For more details please refer to the datasheet (see Section 14 Reference documents) .

13.1 SPI Parameters

The ST SPI bus clocks in data on the rising edge and clocks out data on the falling edge. The CSN pin is held low during SPI transmission. A SPI transmission is 16 bits long. The device receives an opcode and command byte and a data byte. It, in turn, responds with a global status byte and a data byte.

The command structure is broken down as follows:

Table 6. SPI command structure

Command byte								DI - Data byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC1	OC0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 7. SPI op-code and address

Command byte							
Op-code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 8. SPI op-code and address

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Clear Status>
1	1	<Read Device Information>

The return byte is configured as follows:

Table 9. SPI response structure

Global Status byte								DO - Data byte							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GL_ER	FE	STK_RESET_Q	TSD	TW	UV	OV	WDTO	D7	D6	D5	D4	D3	D2	D1	D0

The global status byte is returned with each SPI communication.

13.1.1 Global status byte Mnemonics

- GL_ER: Global error flag. This signal is a logical OR among all the errors of of the channels device.
- FE: Frame error. If the number of clock pulses within the previous frame is not 16 the frame is ignored and this bit is set.

- STK_RESET_Q: If a stuck at ‘1’ on SPI_DI during any SPI frame occurs, or if a power-on reset occurs. STK_RESET_Q is reset (‘1’) with any SPI command. When STK_RESET_Q is active (‘0’), the gate drivers are switched-off (for more details see Section 3.4: Resistive low in the datasheet). After a startup of the circuit the STK_RESET_Q is active because of the POR pulse and the gate drivers are switched-off. The Gate drivers can only be activated after the STK_RESET_Q has been reset with a SPI command.
- TSD: Thermal shutdown due to an internal sensor. All the gate drivers and the charge pump must be switched-off (see Section 3.4: Resistive low in the datasheet). The gate drivers can only be activated after the TSD has been reset with a SPI command.
- TW: thermal warning
- UV: logical OR among the filtered undervoltage signals.
- OV: logical OR among the filtered overvoltage signals.
- WDTO: watchdog time out

13.2 Register contents

There are three command registers (Addrs 01,02, 03) and one dedicated status register (Addr 00H).

Table 10. Summary of registers

Name	Access	Adress						Content							
		A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
StatReg0	Read/ clear	0	0	0	0	0	0	DS_MON_3	DS_MON_2	DS_MON_1	DS_MON_0	0	0	OT_EXT	CP_LOW
Appl Reg 1	Read/ write	0	0	0	0	0	1	RWD	FW_PAS	OFF_CAL	CLK_SPCTR	OVT	OV_UV_RD	DIAG_1	DIAG_0
Appl Reg 2	Read/ write	0	0	0	0	1	0	RWD	COPT_2	COPT_1	COPT_0	FW	MCSA	GCSA_1	GCSA_0
Appl Reg 3	Read/ write	0	0	0	0	1	1	RWD	EXT_TS	EXTTH_5	EXTTH_4	EXTTH_3	EXTTH_2	EXTTH_1	EXTTH_0

13.2.1 Status register 0 Mnemonics

The status register can only be read or read and cleared.

- DS_MON[3:0]: If the drain source voltage exceeds the defined thresholds, the DS_MON are set and the corresponding drivers go to sink mode. The DS_MON bits have to be cleared through a software reset to reactivate the drivers.

Table 11. Drain-source monitor fault table

Register	Deactivated driver
DS_MON_3	High-side 2
DS_MON_2	High-side 1
DS_MON_1	Low-side 2
DS_MON_0	Low-side 1

- OT_EXT: This bit reflects the TS/ACT_OFF state. If this bit is high then the TS/ACT_OFF pin voltage is below the threshold and outputs are disabled. The threshold is determined by the EXT_TS bit and the EXTTH bits. See Section 13.2.2.3 Application register 03
- CP_LOW: this bit indicates if the charge pump is below the minimum threshold.

13.2.2 Application registers Mnemonics

Each application register has a watchdog timer bit that must be set periodically (within 60 ms) or the drivers will reset and disable all of the outputs. See Section 1.4 Watchdog function for details.

These registers can be read or written to.

13.2.2.1 *Application register 01*

Table 12. Application register 1 default values

Bit	7	6	5	4	3	2	1	0
Name	RWD	FW_PAS	OFF_CAL	CLK_SPCTR	OVT	OV_UV_RD	DIAG1	DIAG0
<default>	0	0	0	0	0	0	0	0

- RWD: setting this bit restarts the watchdog timer. This will need to be done within the watchdog window. This bit is available in all three application registers.
- FW_PAS: setting this bit enables the passive freewheeling
- OFF_CAL: this bit enables the offset calibration mode for the current sense amplifier.
- CLK_SPCTR: setting this bit causes the charge pump clock to dither.
- OVT: Overvoltage threshold adjust. 0=20 V, 1=29 V
- OV_UV_RD: if set prevents the drivers from restarting after an over or under voltage event.
- DIAG[1:0]:these bits set up the drain-source monitoring threshold.

Table 13. Drain-source monitor programming thresholds

DIAG[1]	DIAG[0]	Threshold voltage
0	0	0.5 V
0	1	1 V
1	0	1.5 V
1	1	2 V

13.2.2.2 *Application register 02*

Table 14. Application register 2 default values

Bit	7	6	5	4	3	2	1	0
Name	RWD	COPT_2	COPT_1	COPT_0	FW	MCSA	GCSA_1	GCSA_0
<default>	0	0	0	0	0	0	0	0

- RWD: setting this bit restarts the watchdog timer. This will need to be done within the watchdog window. This bit is available in all three application registers.
- COPT[2:0]: these three bits define the Cross current filter or dead time delay.

Table 15. **Dead time delay parameters**

COPT_2	COPT_1	COPT_0	Dead time (ns)
0	0	0	250
0	0	1	500
0	1	0	750
0	1	1	1000
1	0	0	1250
1	0	1	1500
1	1	0	1750
1	1	1	2000

- FW: this bit, when set, enables high side freewheeling. The device defaults to low side freewheeling (“0”).
- MCSA: this bit determines which set of current sense resistors is observed. A “0” observes CSA2 inputs and a “1” observes CSA1 inputs.
- GCSA[0:1]: these bits determine the gain of the current sense amplifier.

Table 16. **Current sense amplifier programmable gain table**

GCSA_1	GCSA_0	Gain
0	0	10
0	1	20
1	0	50
1	1	N/A

13.2.2.3 *Application register 03*

Table 17. **Application register 3 default values**

Bit	7	6	5	4	3	2	1	0
Name	RWD	EXT_TS	EXTTH_5	EXTTH_4	EXTTH_3	EXTTH_2	EXTTH_1	EXTTH_0
<default>	0	0	0	0	0	0	0	0

This register sets up the external temperature sensor pin.

- RWD: setting this bit restarts the watchdog timer. This will need to be done within the watchdog window. This bit is available in all three application registers.
- EXT_TS: this bit enables the micro compatible output disable function (“0”) or the thermal sensor function (“1”). If a “0” then there is a bias current. If a “1” then there is no bias current. In either case, the threshold will still need to be programed.
- EXTTH[5:0]: these bits set the disable voltage threshold. These will need to be programmed for either the TS mode or the ACT_OFF mode. The threshold is calculated through the equations Section 9 Thermal sensor operation :

The values *n* and *m* are determined in the following table:

Table 18. **Thermal sensor threshold programming table part 1**

EXTTH_5	EXTTH_4	EXTTH_3	*n*
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

Table 19. **Thermal sensor threshold programming table part 2**

EXTTH_2	EXTTH_1	EXTTH_0	*m*
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

14 Reference documents

- Motor bridge driver for automotive applications, L99H01, DS6193.
- H-bridge gate driver for automotive applications, L99H02, DS12547.

Revision history

Table 20. **Document revision history**

Date	Version	Changes
06-Jun-2021	1	Initial release.
15-Jul-2021	2	Typos updated for L99H02 with references also to L99H01.
02-May-2022	3	Updated Equation 44 and Equation 48 in Section 7.2 Selecting a current sense resistor value.

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