AN6272

Application note

Short-circuit capability of STPower GaN Transistors and best practices for testing

Introduction

Today, 700 V STPOWER GaN transistors are intended for 400 V applications, and the value of the short-circuit withstand time (T_{SCW}) needs to be assessed and defined in the datasheet. This application note focuses on type I short-circuit (SC), which correspond to the switching ON of the power transistor while it is previously biased by a voltage source at its drain-to-source terminals. In this case, the device must withstand the bus voltage while limiting the current by the saturation of its channel. As a result, gallium nitride high electron mobility transistors (GaN HEMTs) with p-GaN gates present interesting characteristics in short-circuit tests, thanks to their strong drain current reduction at high temperatures [1].

Recently, GaN HEMT transistors have entered the semiconductor market, raising recurrent questions such as: What is the short-circuit withstand time (T_{SCW}) of GaN power transistors? How do GaN HEMT transistors behave in short-circuit conditions?

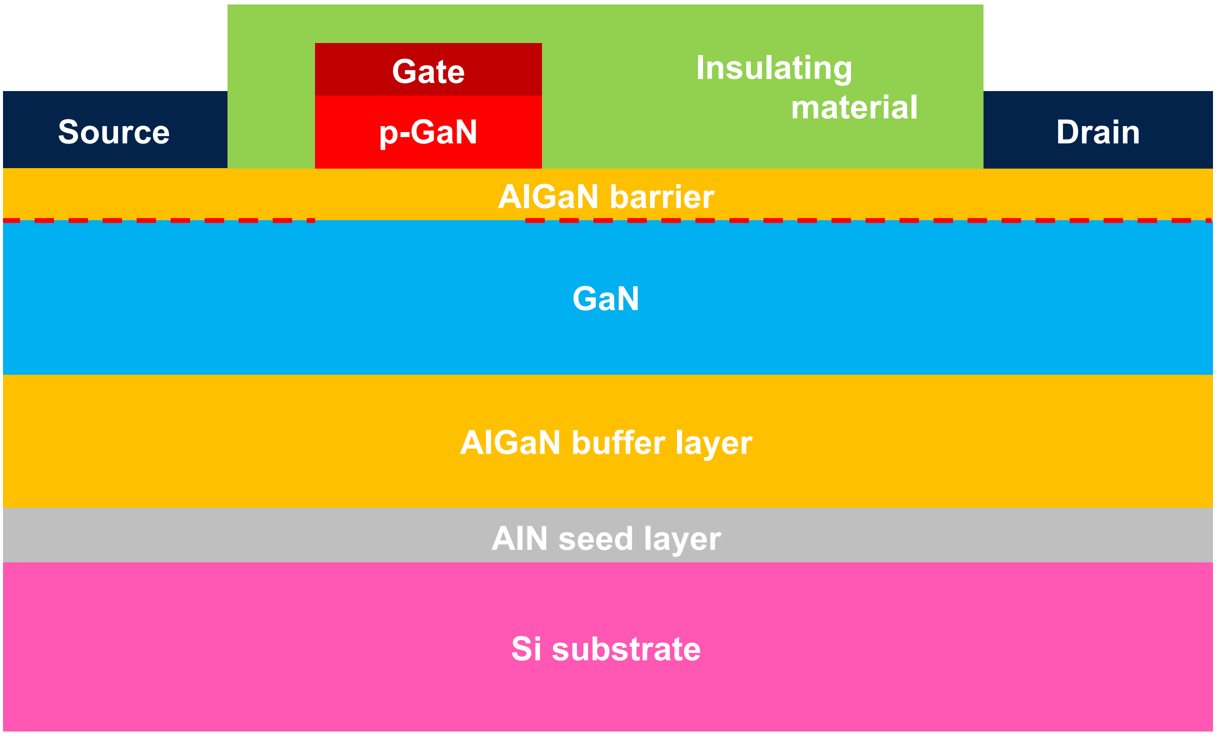
This application note demonstrates the impressive performance of GaN enhancement mode high electron mobility transistors (E-HEMTs) in type I short-circuit conditions and provides recommendations for characterizing them under optimal conditions. Section 1 discusses STPOWER GaN technology, specifically the p-GaN structure. Section 2 analyzes the behavior and performance of GaN E-HEMTs in short-circuit conditions. Section 3 outlines the requirements for testing GaN E-HEMTs in short-circuit conditions, focusing on board design, and the measurement methods used to perform the tests.

1 STPower GaN technology

1.1 Enhancement-mode HEMT structure

STMicroelectronics uses a p-doped GaN layer under the gate area to create a normal OFF GaN transistor. The structure of a GaN HEMT with a p-GaN layer is different from that of other transistor technologies. Today, silicon (Si) MOSFETs use a vertical structure, while GaN HEMTs use a lateral structure. GaN is grown on a Si substrate, followed by an AlGaN (aluminum gallium nitride) layer. Si substrates are preferred because their larger wafer sizes make mass production easier and lower cost. However, the large difference in thermal expansion coefficients between GaN and Si can cause stress during cooling after crystal growth, potentially leading to cracks. A buffer layer is used to relieve this stress. The growth of a thin AlGaN film on GaN creates a piezoelectric effect, causing electrons to gather at the interface. This forms a high-mobility two-dimensional electron gas (2DEG) layer that allows current to flow. The p-GaN layer above the AlGaN barrier and the GaN channel forms a p–i–n diode. When the device is on, this diode may gradually turn ON, increasing the gate current. The amount of current strongly depends on the properties of the metal/p-GaN interface. Generally, most single-metal contacts to p-GaN have a Schottky-like nature due to the wide bandgap of GaN (3.4 eV) and its large electron affinity.

Figure 1. Cross section of typical p-GaN HEMT structure



1.2 D-mode (cascode) vs E-mode (p-GaN)

In the cascode configuration, a high-voltage normally ON GaN HEMT is connected in series with a low-voltage Si MOSFET in the switching circuit. The Si MOSFET controls the ON and OFF states of the GaN HEMT. When a positive gate voltage above the threshold is applied to the MOSFET, the GaN HEMT gate voltage is nearly zero, turning the device ON. Since the two devices are in series, applying a voltage to the HEMT drain causes current to flow through both the HEMT and MOSFET. Conversely, when no gate voltage is applied to the MOSFET, it turns OFF, preventing current from flowing through the HEMT. The HEMT handles any increase in drain voltage, ensuring high reliability. This configuration takes advantage of the positive threshold voltage of the MOSFET, the lower ON-resistance of the 2DEG, and the high breakdown field of the GaN HEMT in the OFF state. However, this approach limits high-temperature operation due to the presence of the Si device. Additionally, it increases packaging complexity (size) and introduces parasitic inductances, which may affect the circuit's switching performance.

Table 1. **E-mode vs D-mode characteristics comparison**

Parameter	E-mode	D-mode
Structure	1 die HEMT	Two dies HEMT + MOSFET
Current capability	Lower due to P-GaN implant	Higher
Slew rate control	Direct gate control	Indirect gate control
Package	Easier package (lower inductance)	More complex package
Power	Conductivity reduced due to p-Gate	Best channel conductivity
Integration	Easy to drive and parallel	Difficult to parallel
Losses	Zero reverse recovery (Qrr)	Reverse recovery losses
Gate robustness	- 6 V / + 7 V	± 20 V

Moreover, the p-GaN structure offers many other benefits compared to cascode devices for high-power applications. First, it is an intrinsic enhancement-mode device, which means that the device has three simple terminals, and it is possible to control the dV/dt through the gate. The second advantage is the gate drive. It works like a Si MOSFET by applying six volts to turn ON and zero volts or negative voltage to turn OFF. It is very easy for customers to design the gate driver and to parallel the devices. Due to the absence of a body diode, there is no reverse recovery when e-mode devices operate in the third quadrant, which results in fewer losses in applications.

2 GaN E-HEMTs behavior in short-circuit conditions

2.1 Short-circuit test

There are two main types of short-circuits:

1. **Type I short-circuit (Hard switching fault):**
   This occurs when the power transistor conducts while being biased by a voltage source at its terminals. The transistor must withstand the bus voltage and limit the current by saturating its channel. Figure 2, and Figure 3 shows a typical characterization diagram for this type (refer to JEDEC standards document JESD24-9) [2].
2. **Type II short-circuit (fault under load):**
   This happens when one transistor conducts while the corresponding transistor in the same arm was previously conducting. During the fault, the bus voltage biases the previously conducting transistor through the parasitic impedance of the power loop, leading to channel saturation. Electrically, a type II fault is distinguished by the presence of an ohmic dv/dt at its terminals, followed by a Miller effect. A partial short-circuit can occur due to degraded insulation material or a component failure that creates a resistive path between two circuit nodes.
   The values of the pulse duration in the Figure 3 are for example.

Figure 2. **Simplified electrical schematics short-circuit type I or hard switching fault**

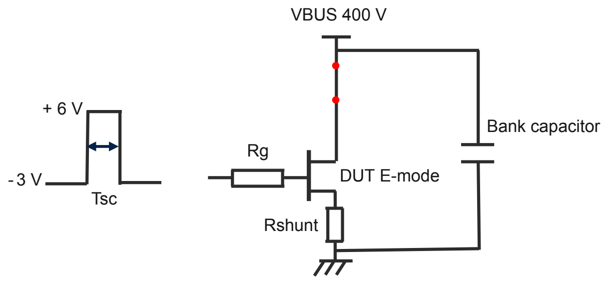
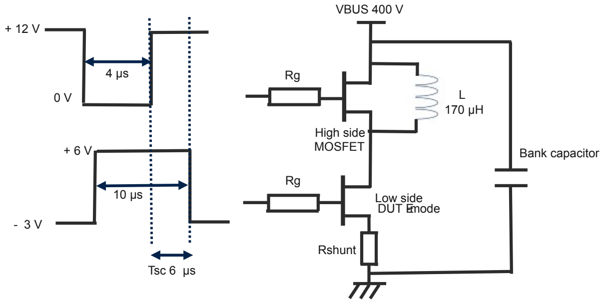


Figure 3. **Simplified electrical schematics short-circuit type II or fault under load**



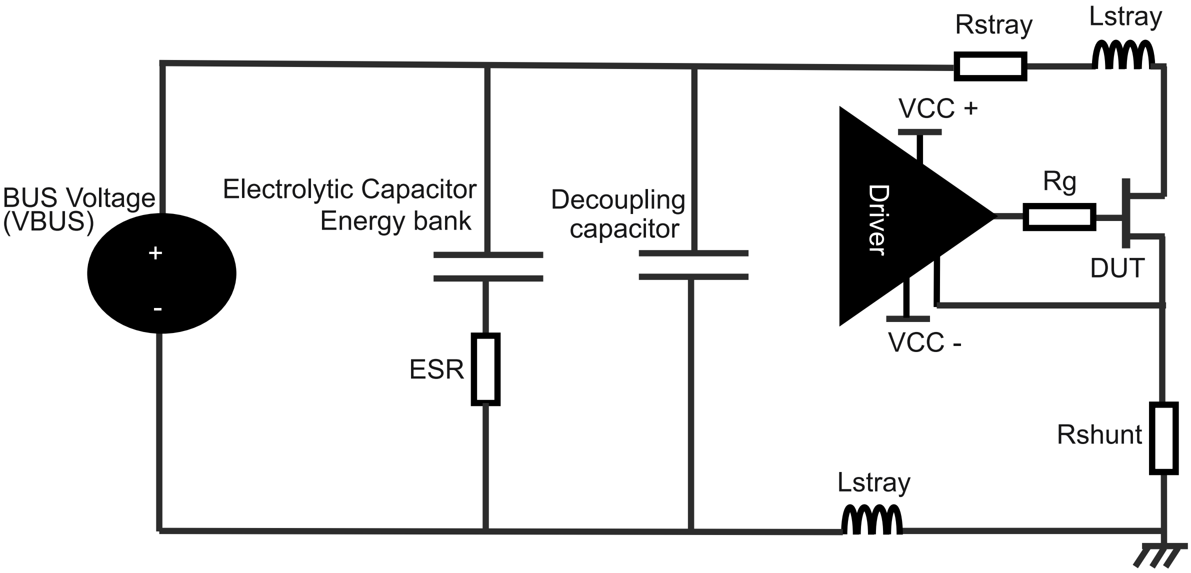
When a short-circuit occurs, the transistor experiences a sudden surge in current. This is because the resistance of the short-circuit path is very low, allowing a large current to flow through the transistor. The increased current flowing through the transistor during a short-circuit can result in higher power dissipation. This can lead to the device heating up quickly, potentially causing thermal stress and damage if not controlled.

2.2 Standards short-circuit (type I) test conditions

Based on the IGBT, the T_{SCW} is typically rated at about 10 µs, while the current silicon carbide (SiC) transistors are typically rated in the 2-3 µs range. This value of a few µs corresponds to the response time of the system to detect the short-circuit and to react to avoid the damage.

Testing transistors with a 10 µs short-circuit duration ensures that they are robust and reliable, capable of withstanding brief but severe fault conditions. Manufacturers use this standard to ensure the quality and durability of their transistors, providing confidence to designers and end users.

Figure 4. **Short-circuit (type I) Schematic with parasitic elements**



Parasitic inductance in the power loop (illustrated with L_{STRAY} in the Figure 4) can cause significant voltage spikes during short-circuit events due to the fast slew rate. Minimizing the stray inductance of the power loop in short-circuit conditions is crucial to protect the device under test (DUT) from overvoltage stress that could lead to failure. For that reason, reducing the length of the PCB traces is essential to test STPOWER GaN transistors in the best conditions.

Another parasitic parameter to consider is the R_{STRAY} creating a V_{DS} drop voltage at the start of the short-circuit due to the high inrush current. A reasonable value of this drop voltage is equal to or less than 10% of the bus voltage (see Figure 6). Moreover, it is recommended to use an electrolytic capacitor with a low equivalent series resistance (ESR) and placing a decoupling ceramic capacitor to provide huge transient current capability limiting the V_{DS} drop voltage.

To maintain and provide the gate current of an e-mode transistor during the short-circuit, it is crucial to use a driver with a high current capability (a few amps) like the STGAP2GS.

GaN transistors can go into linear operation where the V_{DS} can become relatively high, causing a very destructive development of heat generation (higher I_{DS} requires higher I_G).

2.3 Thermal and electrical characteristics of GaN E-HEMTs

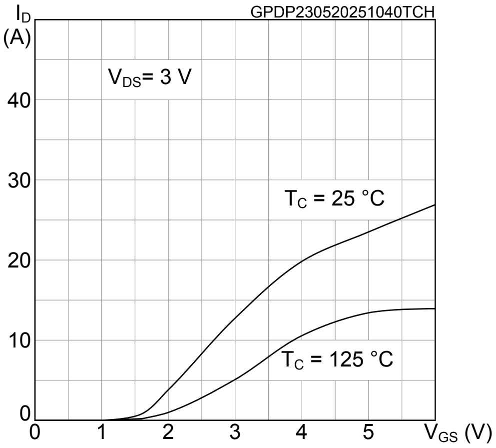
GaN E-HEMTs offer several benefits in thermal management due to their specific characteristics and operational advantages. E-mode transistors typically have lower ON-state resistance compared to other types of transistors. This lower resistance results in reduced power dissipation and heat generated during operation, leading to improved thermal performance. GaN E-HEMTs exhibit good temperature stability, meaning their electrical characteristics remain relatively consistent over a range of operating temperatures. This stability contributes to reliable performance in varying thermal conditions.

Improved thermal conductivity allows GaN transistors to dissipate heat more effectively, reducing the risk of thermal runaway and enhancing performance under short-circuit conditions.

One of the factors that contribute to the drain saturation current reduction is the temperature-dependent transconductance in the 2DEG channel of GaN E-HEMT.

The transconductance of an enhancement-mode (e-mode) transistor is a key parameter that characterizes its performance. Transconductance, denoted as *gm*, is a measurement of how much the output current I_{DS} of the transistor changes in response to a change in the input voltage V_{GS} [3].

Figure 5. **Typical transfer characteristics I_D vs V_{GS} of e-mode transistor**



The second factor that contributes to the reduction in saturation current is related to the gate. It has been demonstrated that a rapid increase in temperature affects the gate current. As the temperature rises, the gate current increases. Consequently, this leads to a larger voltage drop across the external gate resistor, which can further contribute to the reduction in saturation current.

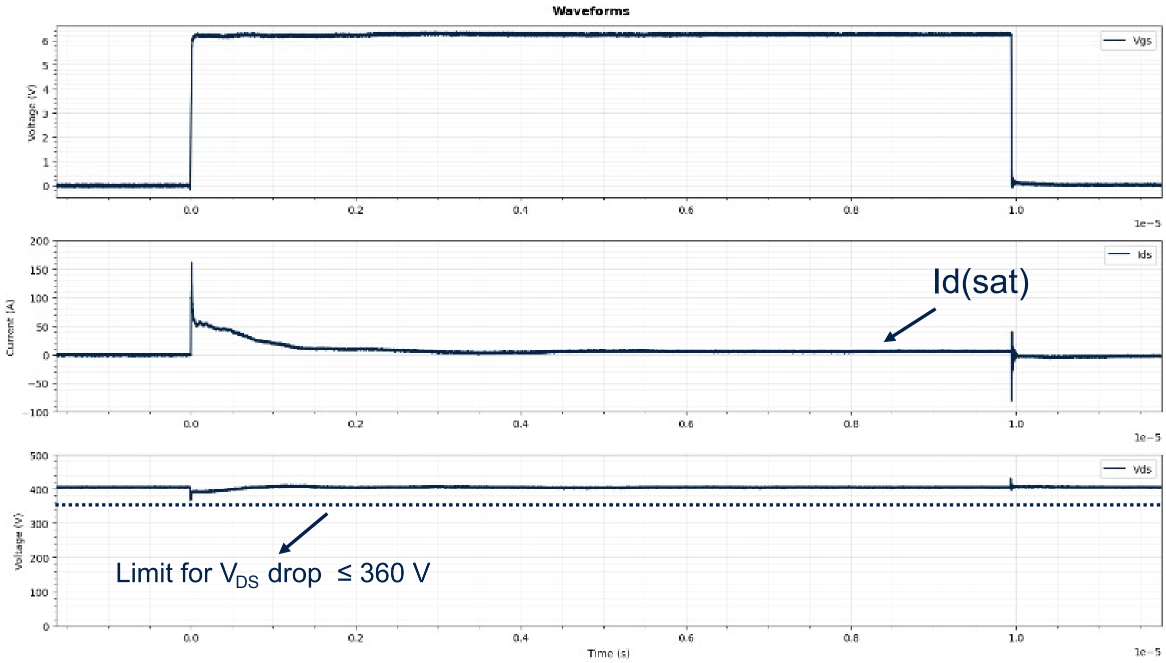
2.4 Short-circuit capability with GaN E-HEMTs

GaN HEMTs have emerged as a superior alternative to traditional silicon-based transistors in high-power and high-frequency applications. One of the critical aspects of their performance is their short-circuit capability, which refers to the transistor's ability to withstand and manage short-circuit conditions without sustaining damage.

In short-circuit scenarios, the rapid rise in current and the associated thermal stress can lead to catastrophic failure in less robust devices. However, GaN E-HEMTs are designed to manage these stresses through their unique material properties and advanced device structures. Their ability to quickly switch OFF and limit current flow helps to minimize energy dissipation and heat generation, thereby protecting the device and the circuit.

Understanding the short-circuit capability of GaN E-HEMTs is crucial for designers and engineers who aim to develop reliable and efficient power electronic systems. This capability ensures that the devices can operate safely under fault conditions, providing a higher level of performance and durability in demanding applications such as electric vehicles, renewable energy systems, and high-frequency communication devices.

Figure 6. Measured short-circuit waveforms of SGT130R70FDC in normal operation - single SC (type I) event at 400 V / 10 µs

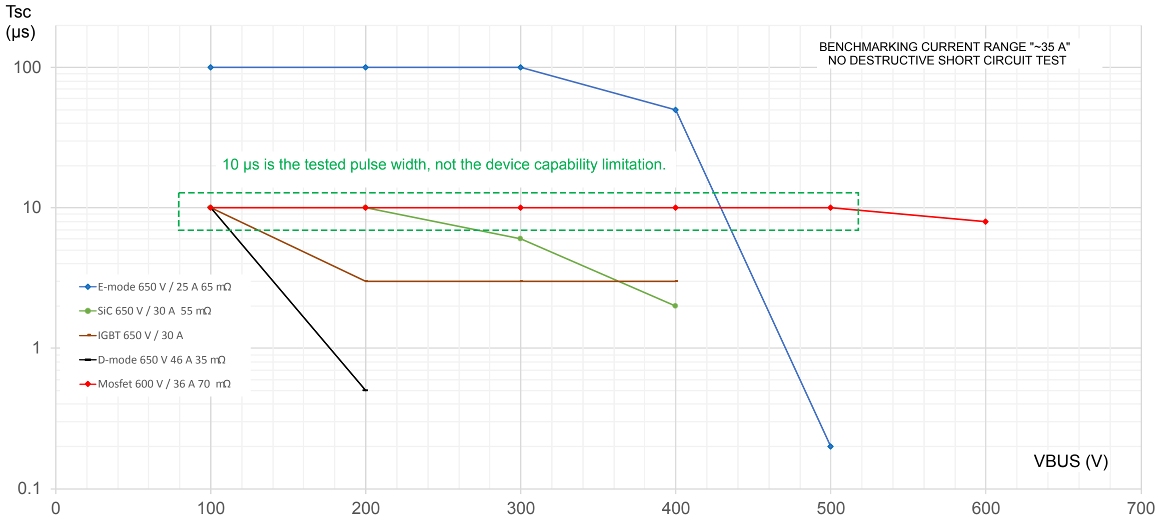


In short-circuit (type I) conditions, the waveforms of a GaN E-HEMT [4] typically exhibit a fast rise in drain current followed by a swift V_{DS} drop, highlighting the device's ability to quickly limit current flow and minimize energy dissipation, as illustrated in Figure 6. We observe that the drain-source voltage V_{DS} drops significantly during the start of the short-circuit because the power loop has very low impedance. The gate-source voltage V_{GS} is typically controlled externally and remains relatively decreased with a drop voltage across the gate resistor during the short-circuit due to the increasing of the I_G. However, during extreme conditions, it increases due to the very high junction temperature (T_J) in the short-circuit. We observe on I_{DS} signal a decrease after reaching its saturation value $I_{D(sat)}$. This decrease is attributed to the reduction in carrier mobility due to the higher junction temperature of the DUT and the reduction in V_{GS}.

GaN E-HEMTs offer several inherent advantages that enhance their robustness under short-circuit conditions. These advantages include no avalanche, faster switching speeds, lower ON-resistance, and superior thermal conductivity. These properties not only improve the overall efficiency and reliability of power electronic systems but also ensure that GaN E-HEMTs can handle extreme conditions more effectively than their silicon counterparts.

By exploring the distinct features and benefits of GaN E-HEMTs in short-circuit tests, we aim to highlight their potential advantages over other transistor technologies and their implications for robust and reliable power electronics applications.

Figure 7. Power transistor comparison of short-circuit withstand times vs bus voltage



GaN E-HEMTs have a serious advantage compared to the other technologies [4] which is their unique behavior regarding the transconductance and thermal derating. With this feature, the e-mode transistors limit their power dissipation and this behaves like a self-protection to withstand long short-circuit time (until 100 µs at 400 V but does not correspond to the max T_{SCW}) [5]. Compared to SiC transistors, which are generally limited to 2 or 3 µs maximum at 400 V, GaN E-HEMTs have lower current capability and energy dissipation during the short-circuit.

2.5 Investigation of E-mode behavior

Recent studies have shown that the value of $I_{DS(peak)}$ is crucial in determining the e-mode devices single pulse robustness and that even extremely high V_{DS} values can be safely tolerated if the gate drive is modified.

Figure 8. **Experimental results on impact of R_{GON} - Single SC type I characterization**

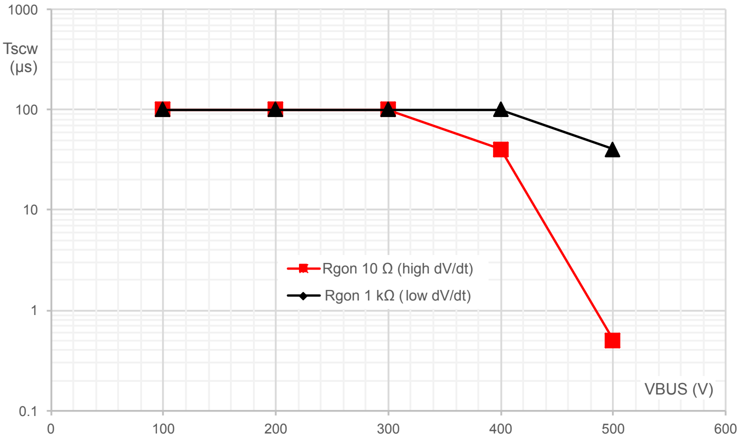


Figure 9. **Waveforms V_{GS} vs R_{GON} at 300 V / 100 µs–Single SC type I characterization**

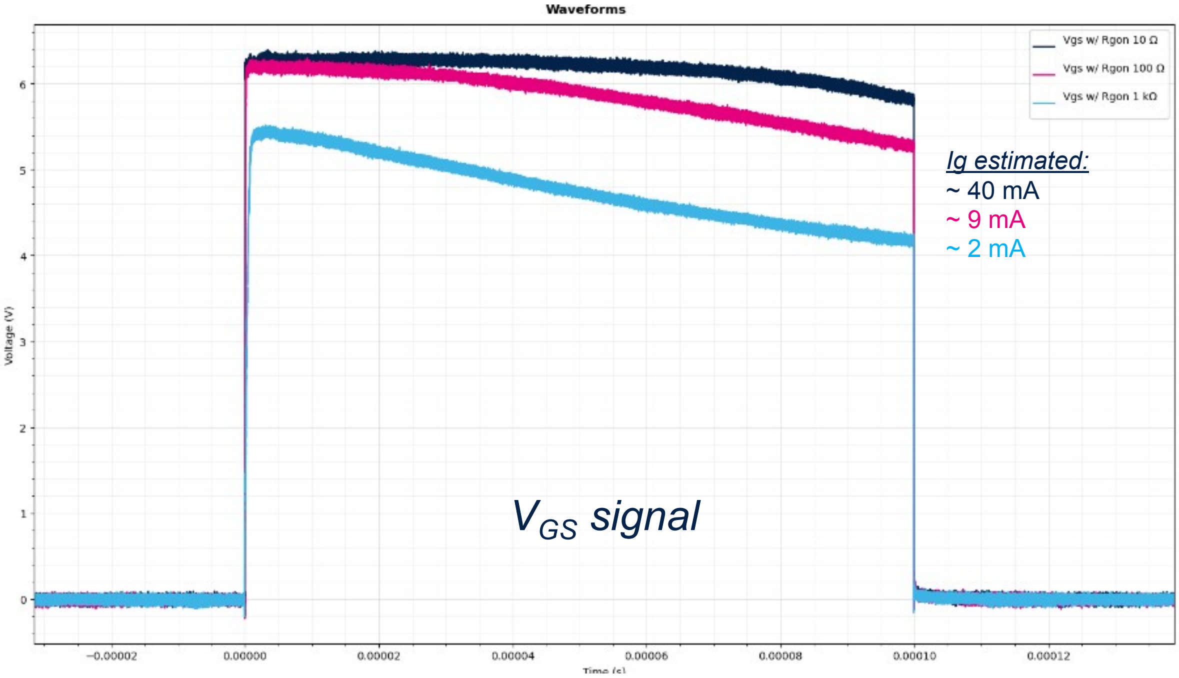
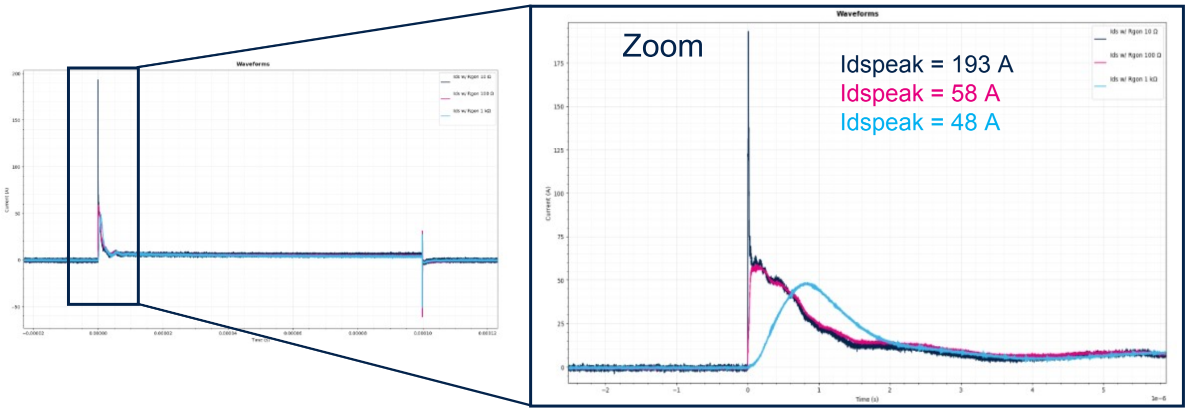


Figure 10. **Waveforms $I_{DS(peak)}$ vs R_{GON} at 300 V / 100 μs - Single SC type I characterization**



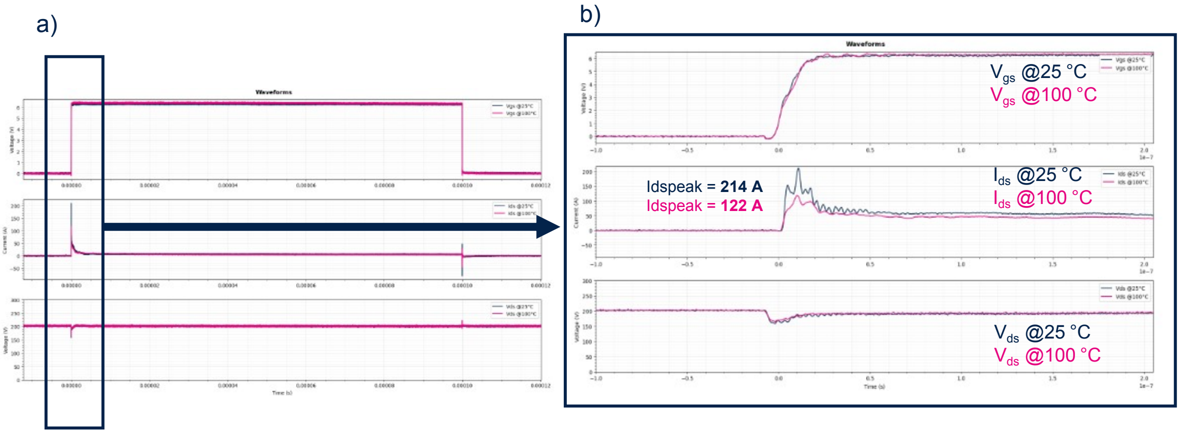
The drain current and hence the energy generated during the short-circuit can be decreased by adjusting the ON gate resistor (R_{GON}) value, the junction temperature, or both. In short-circuit operation, the ON gate current is a key factor to determine the drain current value (I_D) for e-mode transistors.

The value of R_{GON} can also modify the dv/dt and the di/dt at the beginning of the short-circuit, which helps to reduce the peak amplitude of the drain current during the transient short-circuit state (see Figure 10). By increasing the R_{GON} value, we can reduce the gate current during the short-circuit faults, which helps to achieve a lower short-circuit energy. As shown in Figure 8, the R_{GON} value can extend the short-circuit withstand time and prevent the device from degradation.

Table 2. **R_{GON} impact on short-circuit robustness**

Parameter	dV/dt	I_G	$I_{DS(peak)}$	$I_{DS(sat)}$	SC robustness
If R_{GON}↗	↘	↘	↘	↘	↗

Figure 11. **Experimental results of SC type I–a) $I_{DS(peak)}$ vs case temperature at 200 V / 100 μs b) zoom on the start of the SC**



Another advantage of increasing the short-circuit capability of the GaN E-HEMTs is the temperature. As shown in Figure 11, the peak current ($I_{DS(peak)}$) can be reduced with the increasing case temperature at t0. Indeed, the current capability is lower at high temperatures for e-mode transistors with fixed V_{GS} (see Figure 5). Regarding the failure mechanism, the significant current rise combined with the applied voltage, creates massive power dissipation in the DUT. A highly localized electric field causes the device channel to fail when high drain current and bus voltage are present [6].

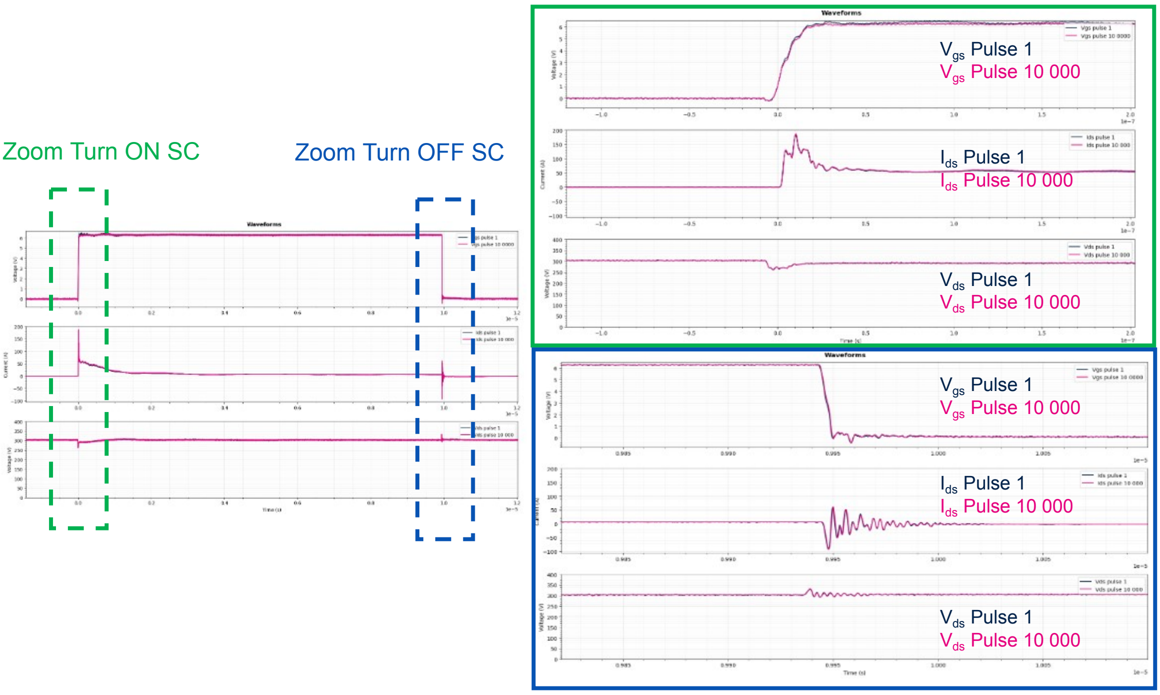
Table 3. **Temperature impact on short-circuit robustness**

Parameter	$I_{DS(peak)}$	$I_{DS(sat)}$	SC robustness
If temperature ↗	↘	↘	↗

2.6 Repetitive short-circuit (type I) test conditions

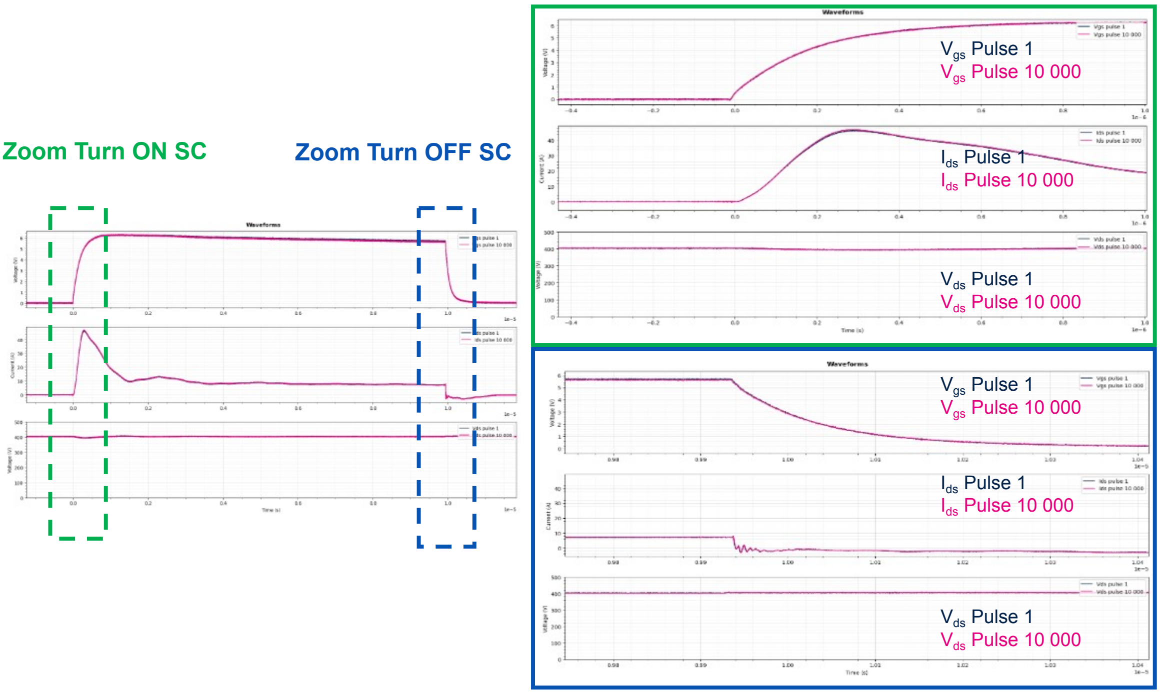
Repetitive short-circuit tests help to determine the durability of transistors by evaluating their ability to withstand repeated stress without degradation or failure. Understanding GaN transistors' behavior under repetitive short-circuit conditions can help us ensure their suitability for demanding applications [7].

Figure 12. **Experimental results of repetitive SC type I, on SGT130R70FDC (Test conditions: VBUS = 300 V, N_{PULSE} = 10000, pulse width = 10 µs, pulse delay every 1 second, T_{case} = 25 °C, R_{GON}/R_{GOFF} = 10/2 Ω)**



The choice of a 1 second repetition rate between pulses (T_{SC} = 10 µs) is made to avoid temperature build-up effects during the tests. Moreover, VBUS must be set at a lower value than the failure voltage. As shown in Figure 12, STPOWER GaN transistors do not present any drift or degradation (also tested at the final test on ATE) after 10 000 short-circuit events, all the signals are similar between the first and last pulse.

Figure 13. **Experimental results of repetitive SC type I, on SGT130R70FDC (Test conditions: VBUS = 400 V, N_{PULSE} = 10000, pulse width = 10 µs, pulse delay every 1 second, T_{case} = 100 °C, R_{GON}/R_{GOFF} = 130/75 Ω, R and C in series between gate-source = 10 Ω and 1 nF)**



As demonstrated in Section 2.5: Investigation of E-mode behavior, the p-GaN transistor exhibits unique behavior under short-circuit test conditions due to its transconductance characteristics. By increasing the R_{GON} and the case temperature of the transistor, it is possible to enhance its short-circuit capability. Figure 13 presents the waveforms during repetitive short circuits under high temperature and low dV/dt conditions. These devices can operate under such conditions in motor control applications, for example, at temperatures above 100 °C and a slew rate of approximately 5–10 V/ns during turn-off and turn-on.

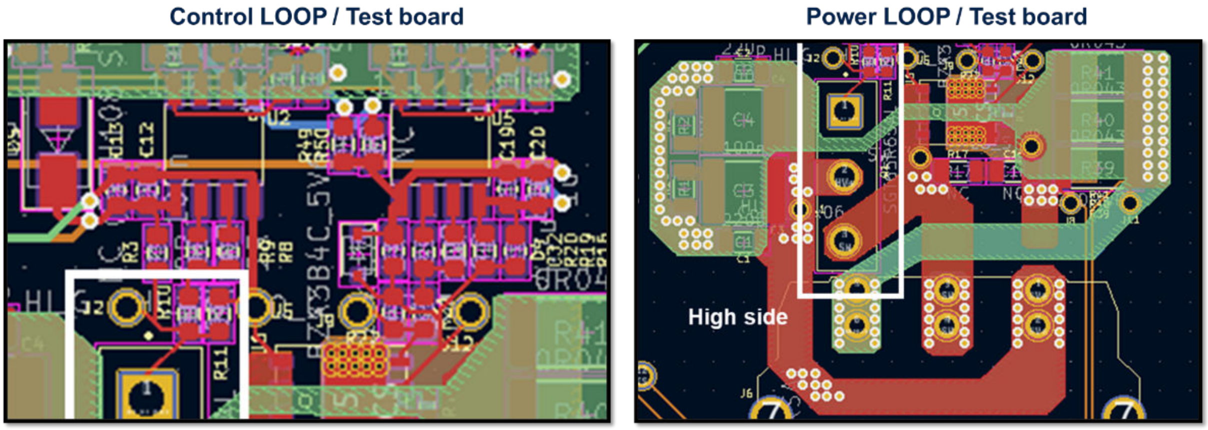
As shown in Figure 13, we observe exceptional performance under these test conditions. The STPOWER GaN transistors can sustain 10 000 short-circuit events without any visible degradation or drift in electrical parameters. Moreover, the waveforms are nearly identical between the first and last short circuit events, indicating excellent stability and reliability.

3 Recommendations for testing

3.1 PCB boards design

Designing a printed circuit board (PCB) for short-circuit testing of Power GaN transistors requires careful consideration of various factors to ensure accurate and safe testing procedures. Here are some guidelines to follow when designing a PCB for short-circuit testing of Power GaN transistors.

Figure 14. **PCB layout short-circuit test board**



Control LOOP / Test board

Power LOOP / Test board

Design PCB traces with sufficient width and thickness to handle high current levels during short-circuit tests. This helps prevent overheating and ensures reliable current flow.

Minimize trace lengths and use wide short traces to reduce inductance. Low inductance helps in achieving faster response times and accurate measurements during short-circuit tests. Reducing the connection distance may avoid significant ringing during the experimental short-circuit test.

Ensure good isolation between high-power traces and sensitive circuitry to prevent damage to components during short-circuit events. Incorporate thermal vias and heat dissipation techniques to manage the heat generated during short-circuit tests. Efficient thermal management helps prevent overheating and ensures accurate results. Add test points at critical locations on the PCB to facilitate easy connection for measuring voltage, current, and other parameters during short-circuit testing.

The Figure 14 represents a PCB layout of a short -circuit test board with the different components, layers. The DUT is placed very close to the driver to minimize the control loop.

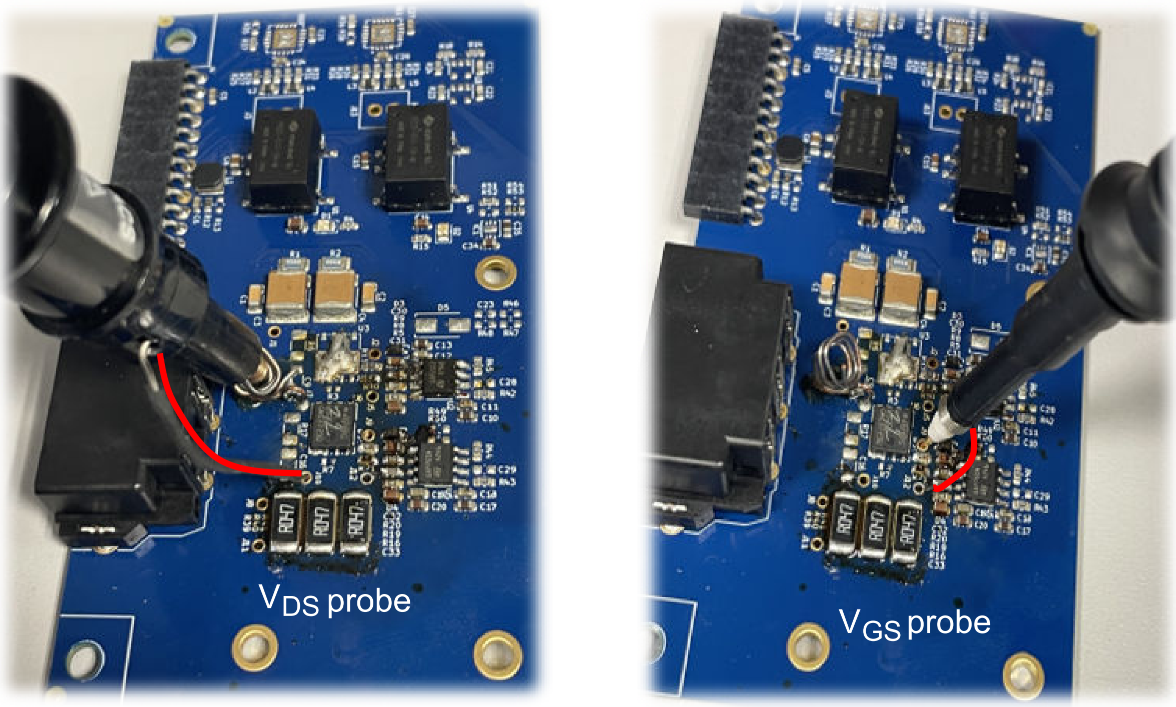
By adhering to these rules and best practices, you can design a robust PCB for short-circuit testing of Power GaN transistors, ensuring accurate measurements, reliable performance, and safety during testing procedures.

3.2 Equipment and setup

Using the right equipment and setup is crucial when performing short-circuit tests on GaN transistors. Proper equipment and setup help maintain a safe testing environment by preventing electrical hazards and minimizing the risk of damage to the transistors and other components. Safety features in the equipment protect operators and prevent accidents during testing. High-quality equipment ensures accurate measurement and monitoring of critical parameters during the short-circuit test, such as current, voltage, and temperature.

- **Equipment Needed**:
  - Power supply capable of delivering the required voltage and current.
  - Oscilloscope for monitoring voltage and current waveforms.
  - Test circuit board designed for the Power GaN transistor.
  - Voltage probes.
  - Safety equipment (e.g., gloves, safety glasses, box, ear-muffs).
- **Safety Precautions**:
  - Ensure all equipment is properly grounded.
  - Wear appropriate safety gear.
  - Be aware of the high voltage and current levels involved in the test.
- **Test setup recommendations**:
  - Use a bank of electrolytic capacitor with low ESR to maintain VBUS and the current saturation of the DUT during the short-circuit.
  - The low-voltage part of the test board can be protected by using an isolated driver like the STGAP2GS.
  - Connect the source kelvin connection to avoid ringing during the tests.
  - Utilize passive high bandwidth probes (recommended 500 MHz B/W or better, e.g., TPP1000 by TEKTRONIX)
  - Use a low shunt resistor value to observe the drain to source current signal with a high bandwidth voltage probe due to high di/dt and to avoid limiting the current capability of the test setup.
  - Use a decoupling ceramic capacitor of at least 1 µF / VBUS to minimize the drop voltage V_{ds} at the start of the SC.

Figure 15. **Probe voltage measurement method**

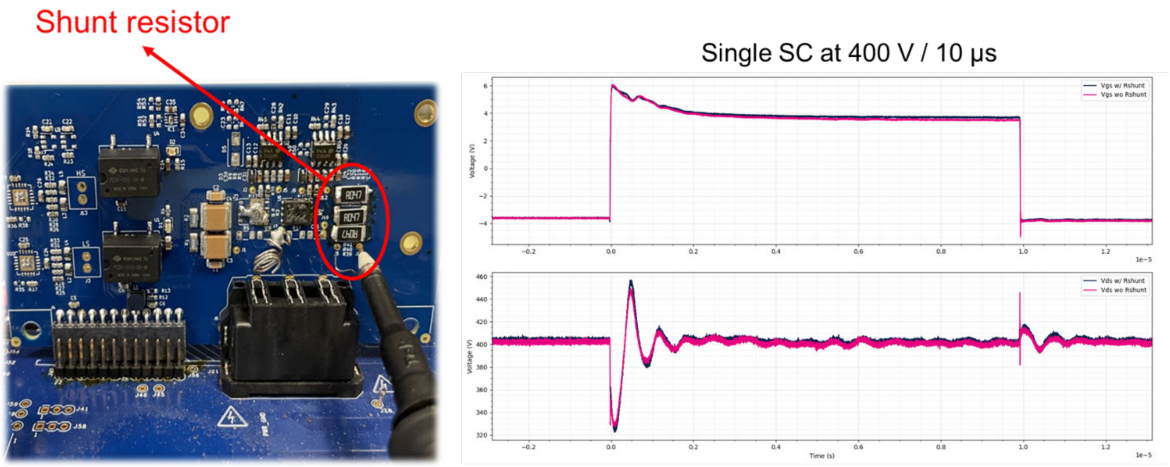


It is also important to avoid using the standard connection (the so-called “alligator clip") due to the long ground wire. For that reason, we recommend placing on the PCB 2 plated through hole (PTH) points for each signal (V_{DS}, I_{DS} and V_{GS}). In this case we get an optimized probe insertion with a short loop connection (see Figure 15). For more information regarding the probing considerations for Power GaN transistors you can refer to the application note AN5770 [8].

3.3 Current measurement

Today, there are several methods to measure switching current in electronic circuits (coaxial current shunt, Rogowski coil, current transformer, sensor, shunt resistor, etc.), each with its own advantages and applications. The solution used for the short-circuit characterization for STPOWER GaN transistors is the current shunt resistor on account of the very low parasitic inductive effect on the power loop. More than the current shunt resistors offer high accuracy and are commonly used in precision current measurements (very high bandwidth). By placing a small resistor (shunt resistor) in series with the DUT, the voltage drops across the resistor can be measured and used to calculate the current using ohm's law (I = V/R) on the scope (math function).

Figure 16. **Effect of shunt resistor on SC waveforms**



It is important to use a low value (< 20 mΩ) to avoid increasing the internal resistance and limiting the current capability of the power loop. Moreover, as you can see in the Figure 16, it is possible to place a few shunt resistors in parallel to reduce the stray inductance.

By using the shunt resistor correctly, we can observe across the Figure 16 that there is no effect regarding the waveforms and the results due to the low stray inductance of the power loop.

4 Conclusion

In conclusion, using the right equipment and setup for short-circuit testing of GaN transistors is essential for achieving accurate, safe, reliable, and efficient testing procedures. It ensures the integrity of the data collected, protects the transistors from damage, and provides valuable insights into their performance characteristics under extreme conditions. STPOWER GaN transistors offer interesting short-circuit capabilities, making them a preferred choice for certain high-power applications that require reliable and efficient performance under challenging conditions. By following best practices for testing and incorporating appropriate protection measures, engineers can leverage the full potential of GaN E-HEMTs in demanding environments while ensuring the longevity and stability of their power electronics systems.

5 References

Table 4. **Reference name and description**

Ref. name	Document name	Document links
[1]	“A Reliable Short-Circuit Protection Method with Ultra-Fast Detection for GaN based Gate Injection Transistors “: Ke Wang, Yousef M. Abdullah, Xiao Li, Diang Xing and Jin Wang, 2019	
[2]	“Short Circuit Withstand Time Test Method”: JEDEC Standard JESD24-9, 2002	
[3]	700 V, 106 mOhm typ., 17 A, e-mode PowerGaN transistor	SGT140R70ILB
[4]	700 V, 101 mOhm typ., 16 A, e-mode PowerGaN transistor	SGT130R70FDC
[5]	“The Behaviour Of GaN Power HEMTs Subjected to Short circuit”: Omar CHIHANI ALTER, 2022	
[6]	“Short Circuit Study of 600 V GaN GITs“: EE aige Williford1, Fred Wang1,2, Sandeep Bala3, and Jing Xu3, 2019	
[7]	“Short Circuit Capability Characterization and Analysis of p-GaN Gate High Electron-Mobility Transistors Under Single and Repetitive Tests”: Jiahui Sun, JinWei, Zheyang Zheng and Kevin J. Chen, 2021	
[8]	“Probing considerations for PowerGaN transistors”: STMicroelectronics Application note AN5770, 2022	AN5770

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
04-Mar-2025	1	Initial release.
26-Nov-2025	2	Updated with new portfolio STPOWER GaN transistors.

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