Hardware specifications for Teseo-LIV3FL

Introduction

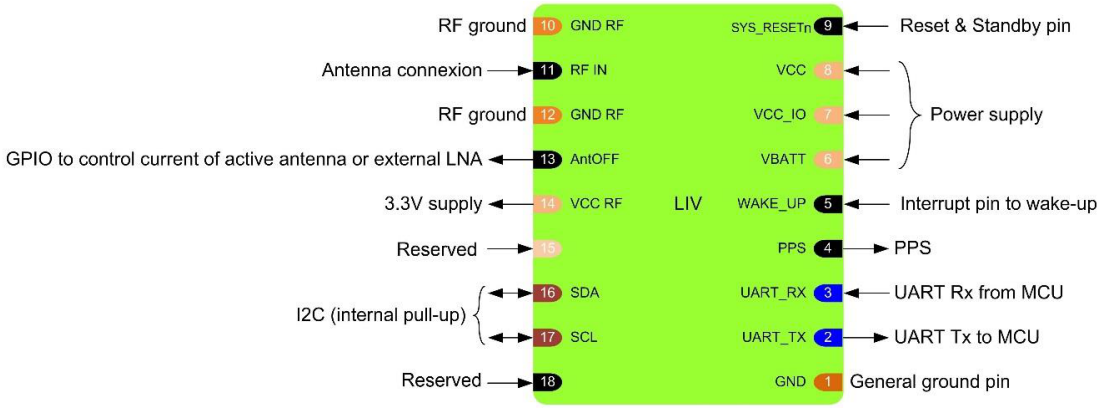
Teseo-LIV3FL is a GNSS module sized 9.7 mm × 10.1 mm × 2.5 mm featuring the STMicroelectronics positioning receiver TeseoIII.

It is a standalone positioning receiver, which embeds the new ST GNSS positioning engine capable of receiving signals from multiple satellite navigation systems, including GPS, Galileo and Glonass or BeiDou.

It embeds 16 M-bit serial Flash.

The following figure reports the pinout of the module.

Figure 1. Teseo-LIV3FL pinout



1 Power

Teseo-LIV3FL is supplied by 3 power pins:

- VCC (pin #8)
- VCC_IO (pin #7)
- VBAT (pin #6)

1.1 VCC (pin #8)

VCC is the main supply. Depending on VCC_IO voltage the VCC has different limiting values.

VCC range is reported in the following table.

Table 1. VCC voltage characteristics against VCC_IO

Symbol	Parameter	VCC_IO	Min	Typ	Max	Unit
VCC	Digital supply voltage	1.8	1.755	1.8	4.2	V
VCC	Digital supply voltage	3.3	3.0	3.3	4.2	V

A start-up or during low-power application current can change suddenly. It is important that supply IC can provide this current variation.

1.2 VBAT (pin #6)

VBAT is the supply for the low-power domain backup: backup RAM and RTC.

VBAT can be either connected to VCC or it can be provided by a dedicated supply always ON. When VBAT supply is kept ON during low-power mode to allow fast recovery of GNSS fix.

VBAT is preventing current flow as soon as VBAT is lower than VCC. It is important when VBAT is supplied with small battery and especially if the battery is not rechargeable.

Depending on VCC_IO voltage the VBAT has different limiting values.

VBAT range is reported in the following table.

Table 2. VBAT voltage characteristics against VCC_IO

Symbol	Parameter	VCC_IO	Min	Typ	Max	Unit
VBAT	Backup input supply voltage	1.8	1.755	1.8	4.2	V
VBAT	Backup input supply voltage	3.3	3.0	3.3	4.2	V

1.3 VCC_IO (pin #7)

VCC_IO range is reported in the following table.

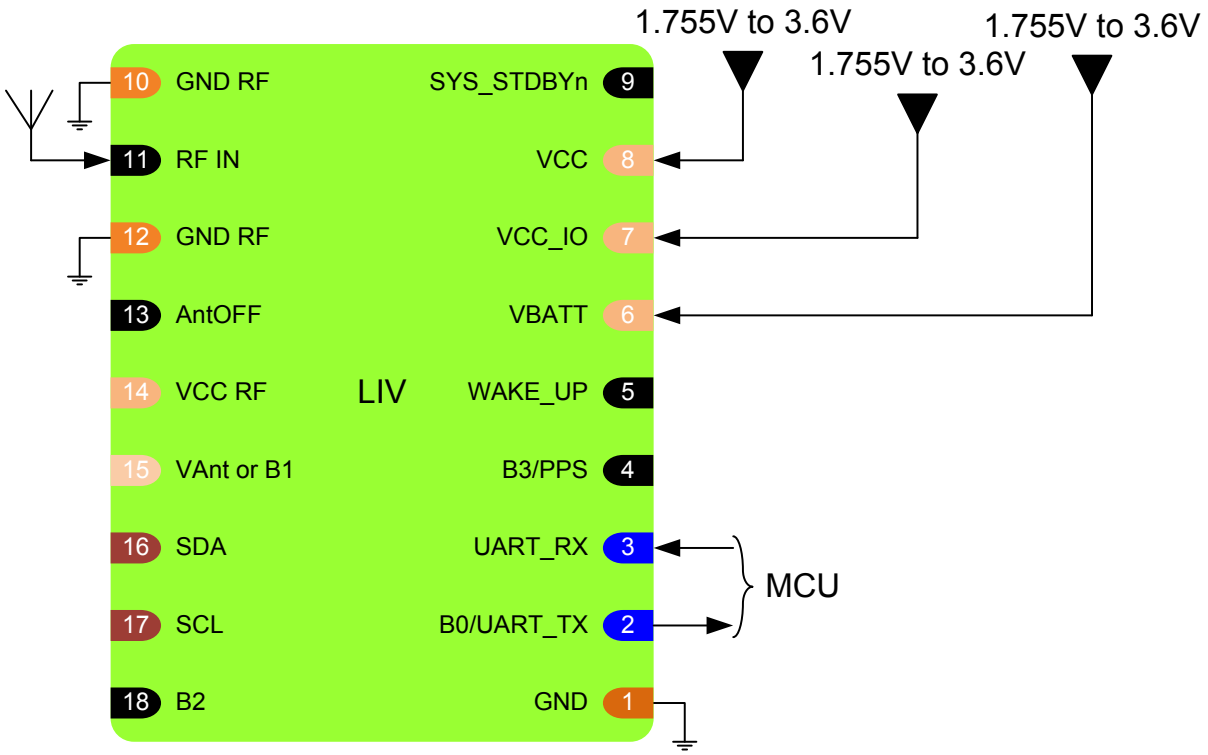
Table 3. VCC_IO voltage supported range

Symbol	Parameter	Min	Typ	Max	Unit
VCC_IO	IO supply voltage	1.755	1.8	1.98	V
VCC_IO	IO supply voltage	3.0	3.3	3.6	V

Take care that VCC_IO must be equal or lower than VCC and VBAT.

The following figure shows the minimum connection to make Teseo-LIV3F GNSS working.

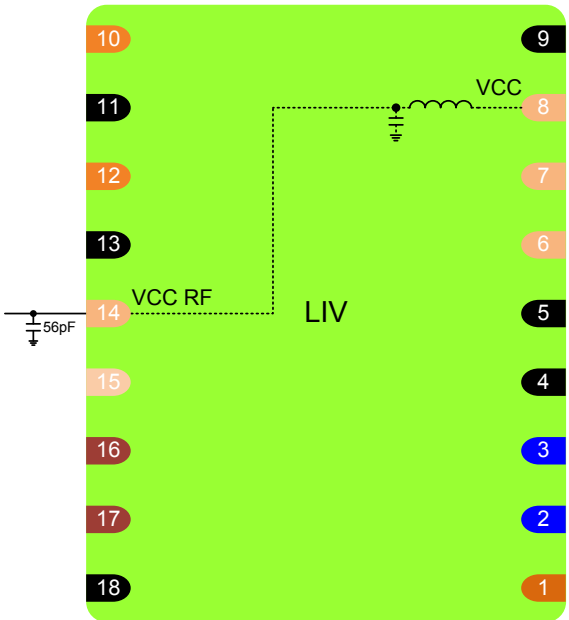
Figure 2. Teseo-LIV3FL minimum connection



1.4 VCC_RF (pin #14)

VCC_RF is an output image of VCC with a filtering for LNA or active antenna supply as shown in the figure below. It can be filtered to remove high frequency noise. This filtering can be planned and not mounted.

Figure 3. Output supply filtering



1.5 Power supply design reference

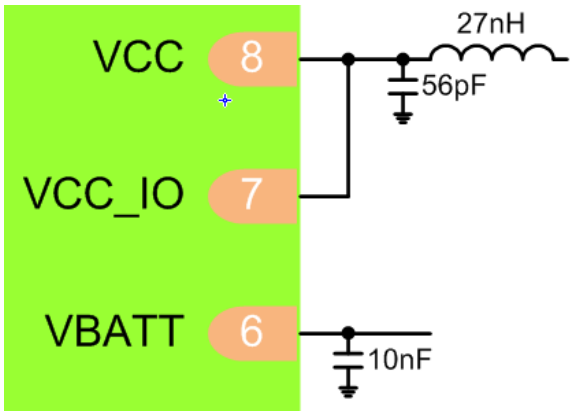
If supplies are without disturbances, no filtering is required.

Nevertheless, it could be planned for a first PCB wave to have soldering pads as shown in the figure below for the following filtering.

27 nH inductor can be 0 Ω and replace by a line for a second PCB.

If one wave is plan, use only a capacitor footprint and not the inductor.

Figure 4. Power supply filtering

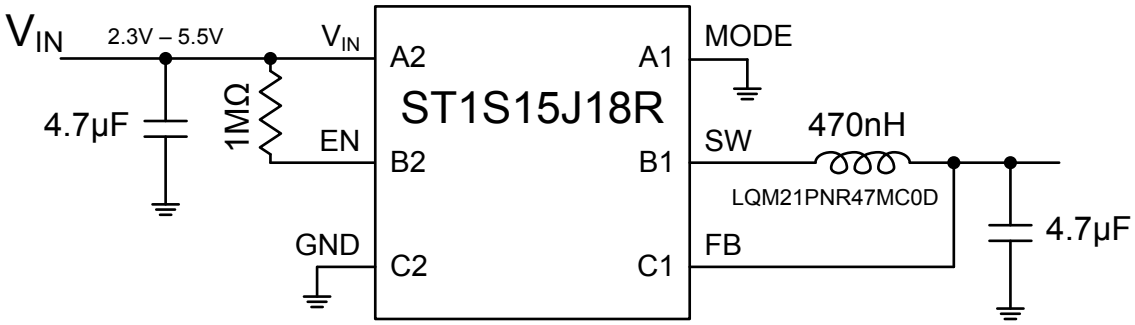


1.6 Current consumption optimization

Use of an SMPS at 1.8 V to supply VCC is recommended to optimize current consumption.

Next figure is an application example with ST1S15J18R with an efficiency around 85%.

Figure 5. Example of SMPS to improve current consumption



If VCC_IO is also supplied by an SMPS, this will reach the lowest current consumption.

2 Interfaces

2.1 I2C (pin #16, #17)

I2C is in slave only.

Internal pull-up resistor on VCC_IO are present. It is important to avoid other pull-up for current leakage in low-power mode.

2.2 UART (pin #2, #3)

UART is a universal asynchronous receiver/transmitter that support much of the functionality of the industry-standard 16C650 UART.

These UARTs vary from industry-standard 16C650 on some minor points, which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The delta of the modem status signals are not available
- 1.5 stop bits are not supported
- Independent receive clock feature is not supported

3 I/O pins

3.1 PPS (pin #4)

PPS is the time pulse every one second. It can be configured with different condition of pulses.

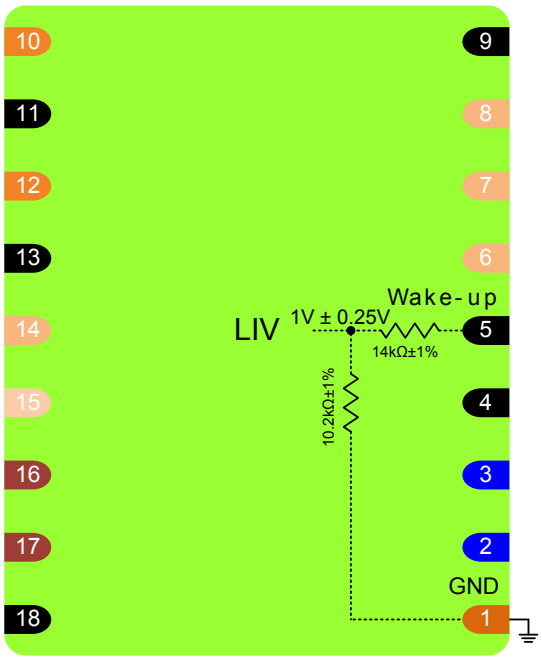
3.2 Wake-up (pin #5)

It is an external interrupt that is used to wake up Teseo-LIV3FL for asynchronous wake-up during standby.

If not used, leave it floating.

Internal circuitry, shown in the following figure, is done with resistor bridge to ensure 1 V ± 0.25 V level. Take care to not change resistor bridge value to avoid to be out of 0.75 V - 1.25 V.

Figure 6. Wake-up pin internal circuitry



3.3 SYS_RESETn (pin #9)

It can force a Teseo-LIV3FL under reset.

Reset signal is active low.

Host processor must have full control of this pin to guarantee the Teseo-LIV3FL's firmware upgrade support.

3.4 RF_IN (pin #10)

It is the RF input.

No DC is present in the RF input. Decoupling capacitor inside.

3.5 AntOFF (pin #13)

AntOFF is a GPIO used to switch OFF external LNA or switch OFF current for the active antenna.

A 10 kΩ pull-down is necessary to ensure a low level during the standby period.

3.6 GPIO (pin #18)

This pin is a free GPIO that can be used for antenna detection for instance or other topics.

3.7 Reserved (pin #15)

In Teseo-LIV3FL pin #15 and pin #18 are reserved.

4 Standby modes

Standby mode is the mode where only low-power backup domain is running. It means that VBAT must be always maintained. It allows to have very low current consumption and fast GNSS reacquisition at the end of the standby time due to RTC.

Teseo-LIV3FL offers 3 different ways of standby:

- HW standby
- SW standby
- VCC + VCC_IO

As IO buffers are not supplied during standby mode, it is important to keep all IO without external voltage to avoid any current leakage. UART_RX is an exception it can be left high.

4.1 HW standby

HW standby is ensured forcing the Teseo-LIV3FL under reset mode by setting SYS_RESETn (pin #9) to 0V level. It can be activated asynchronously from GNSS binary by one GPIO from the host.

During this reset time, all supplies are kept ON.

It ensures a current below 30 µA.

Be careful that VCC_RF is ON during this reset, then in case of active antenna or external LNA, it is important to switch them OFF.

4.2 SW standby

SW standby is activated by the binary for periodic standby. More details how to set it are in the software manual. As HW standby, all supplies are kept ON.

Periodic fixes are from 5 s up to 24 hours between 2 fixes.

It ensures a current below 10 µA. Be careful that VCC_RF is ON during this standby, then in case of active antenna or external LNA, it is important to switch them OFF.

4.3 VCC+VCC_IO standby

This standby is ensured by switching OFF VCC and VCC_IO supplies. It can be activated asynchronously from GNSS binary with one GPIO switching OFF the supplies from a host.

During this standby only VBAT is kept ON.

It ensures a current below 17 µA. During this standby mode, VCC_RF is OFF.

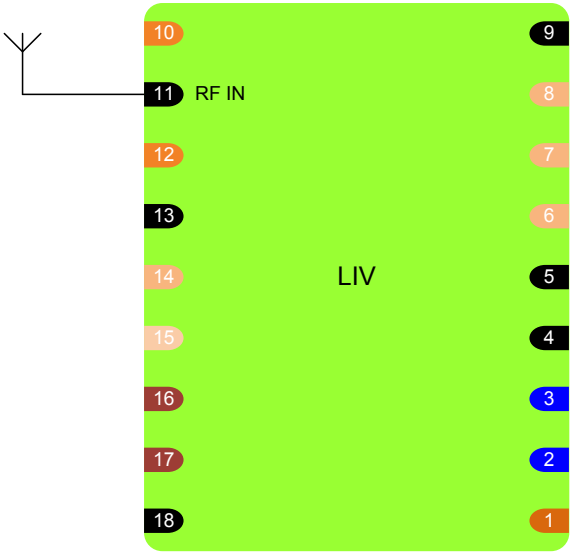
5 Front ends management

The RF input impedance is 50 Ω.

5.1 Passive antenna

A passive antenna, as shown in the following figure, can be directly connected to Teseo-LIV3FL. Take care that the antenna must be close to the module. In addition, it could be possible that a matching component must be necessary to match the antenna.

Figure 7. Teseo-LIV3FL passive antenna

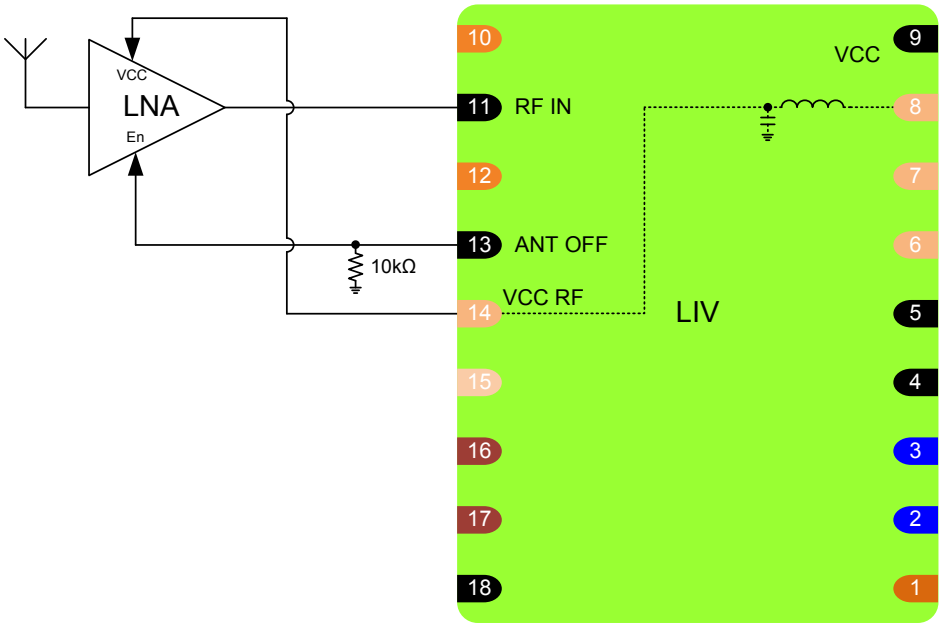


5.2 External LNA

External LNA means a passive antenna used with a LNA on the same PCB than Teseo-LIV3FL module. To optimize power consumption during low-power mode if needed, the LNA should have an enable pin compatible with VCC_IO to be switched OFF/ON.

Next figure is a block diagram describing the connection:

Figure 8. **External LNA control**

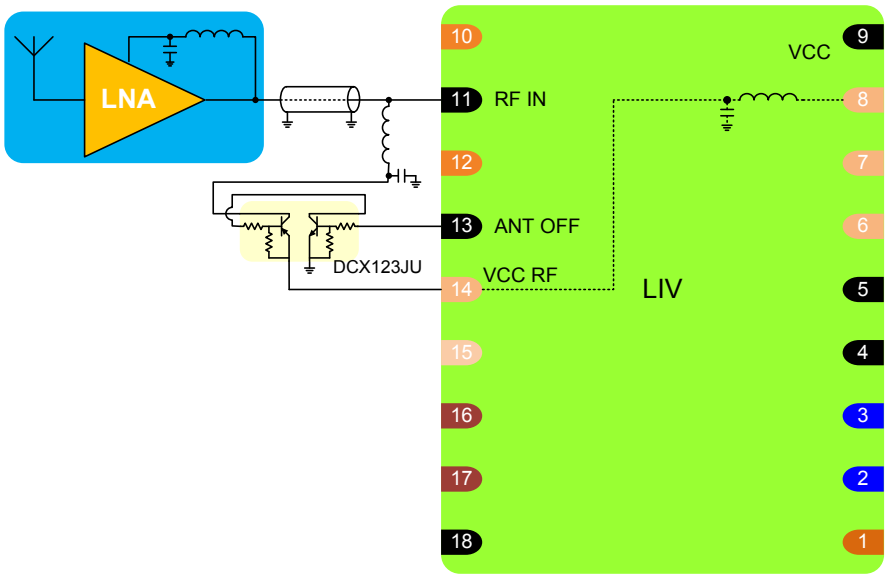


5.3 Active antenna

5.3.1 Teseo-LIV3FL module without current sensing

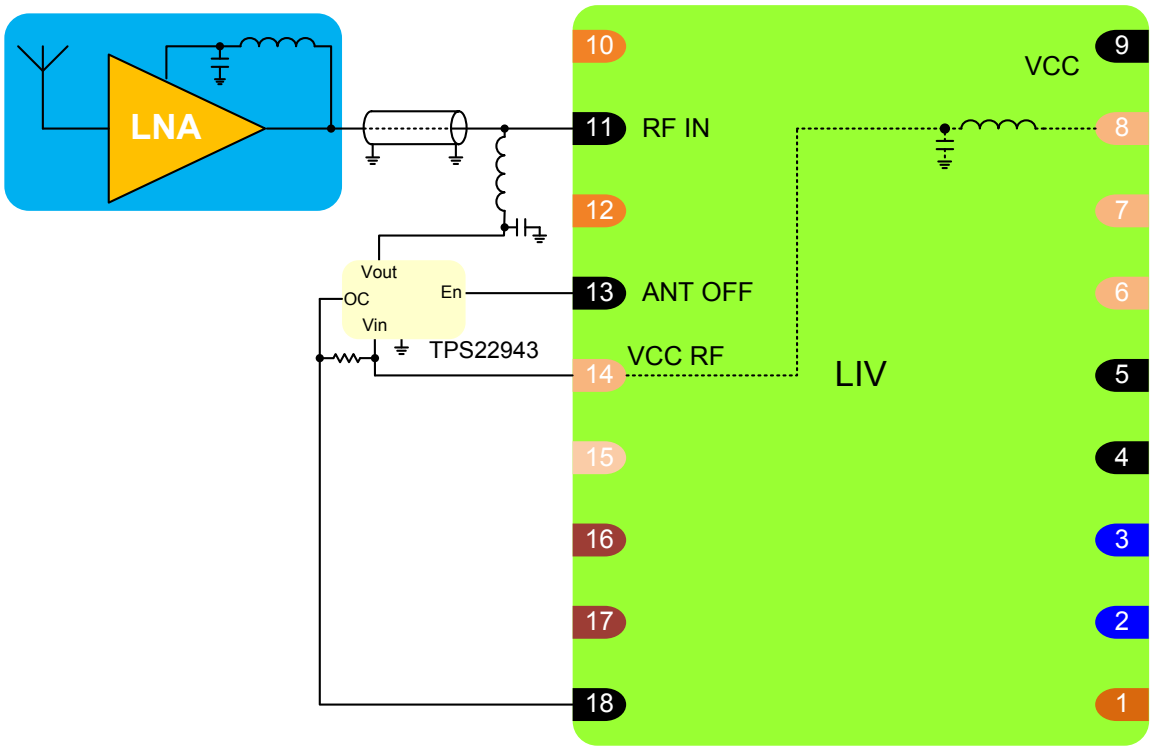
To optimize the current during low-power operating mode, the active antenna, as shown in the following figure, can be used with a switch to cut the current flow.

Figure 9. **Active antenna current switch control**



To improve the functionality, a current limiter, as shown in the figure below, could be used to prevent any short-circuit on the antenna by using the antenna detect config script:

Figure 10. **Active antenna current sense without on-module antenna sensing**



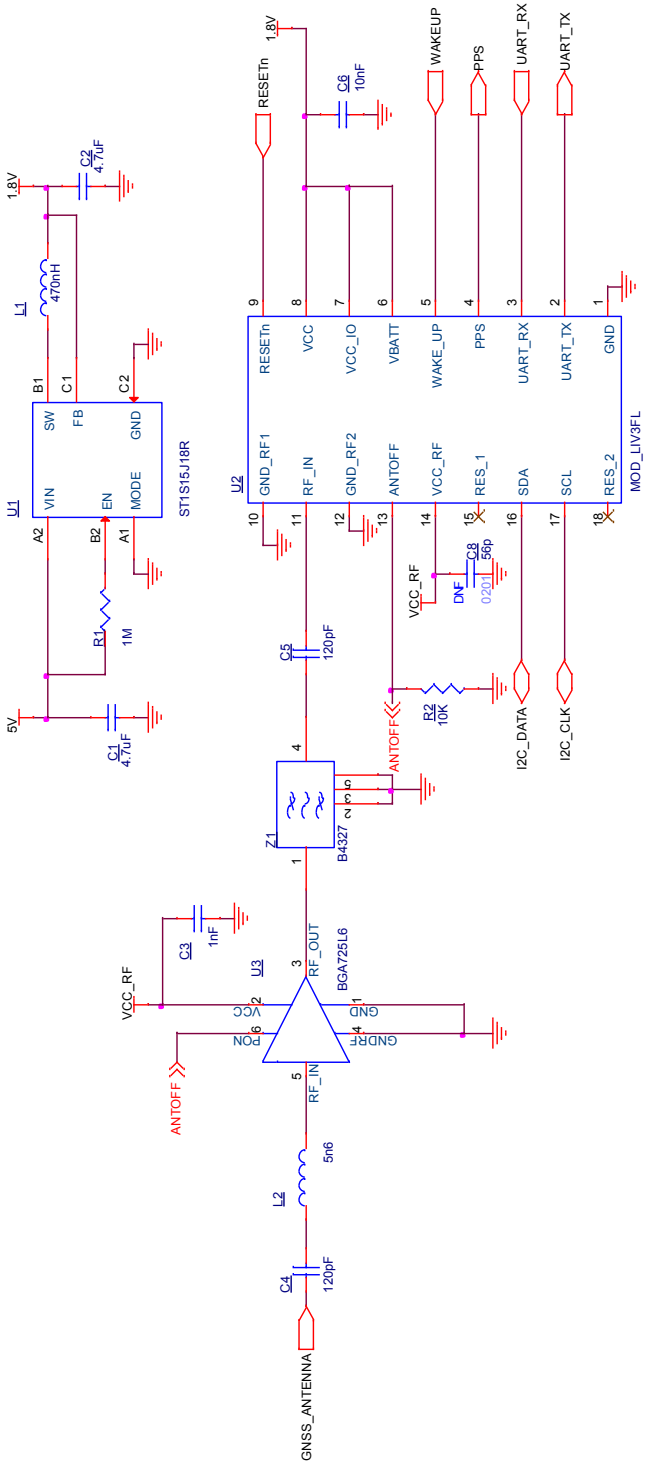

```
# GPIO High/Low status
206 -> fffffeff
207 -> 00000000
# Activate and configure antenna sensing
226 -> 3483F01F
# Antenna status message
228 -> 00020010
# Configure GPIO
242 -> 18140008
243 -> 01030001
244 -> 00000101
# GPIO alternate function
253 -> FFF7C3F0
254 -> 00100000
```

Antenna detects the config script.

6 Reference schematic and BOM

6.1 Schematic

Figure 11. **General schematic**



6.2 Bill of material

Table 4. **Bill of material**

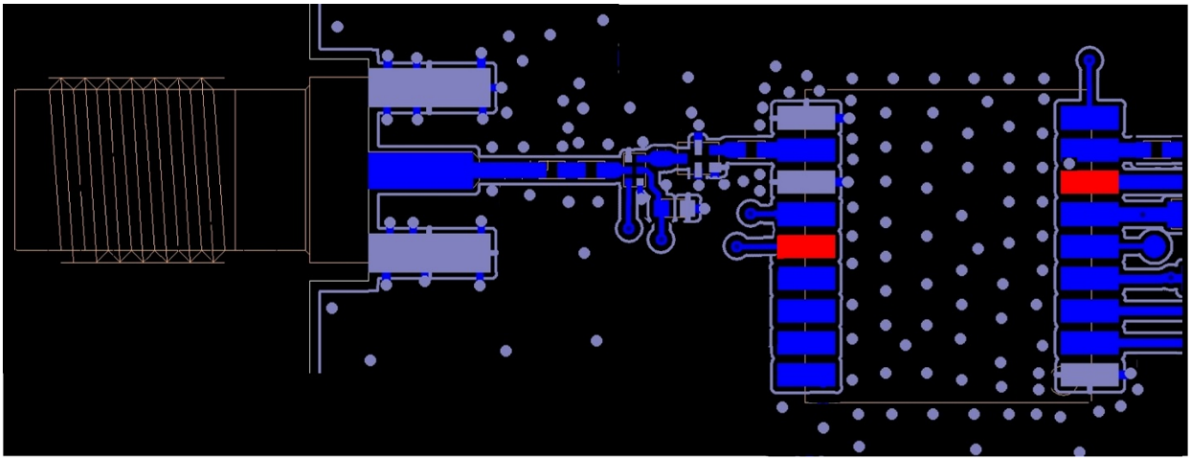
Refs.	Value	Description	Manfacturer 1		Manfacturer 2	
			Name	Part number	Name	Part number
C1	4.7µF	Surface mount 0402 capacitor ceramic 4.7µF, 20% 6.3V X5R	Murata	GRM155R60J475ME87		
C2	4.7µF	Surface mount 0402 capacitor ceramic 4.7µF, 20% 4V X5R	Murata	GRM155R60G475ME87		
C3	1nF	Automotive Grade Surface mount 0402 capacitor ceramic 1nF, 10% 50V X7R 1nF; 50; X7R	Murata	GCM155R71H102KA37	TDK	CGA2B2X7R1H102K050BA
C7	10nF	Multilayer Ceramic Capacitors MLCC - SMD/SMT SOFT 0402 50V 0.01µF X7R 10% T: 0.5mm	TDK	CGA2B3X7R1H103K050BE	Murata	GCM155R71H103JA55D
C4,C5	120pF	Automotive Grade Surface mount 0402 capacitor ceramic 120pF, 5% 50V C0G 120pF; C0G	Murata	GCM1555C1H121JA16	TDK	CGA2B2C0G1H121J050BA
L1	470nH	Surface mount 0805 Multilayer type Inductor 470nF, 20%, 1.1A	Murata	LQM21PNR47MC0D		
L2	5n6H	Surface mount wire wound inductor. 5n6H; 3%; 0.76A	Coilcraft	0402CS-5N6XJLU	Murata	LQW15AN5N6G80D+00-21
L3	27nH	Unshielded Multilayer Inductor, 27nH, 350mA, 460 mOhm Max, 0402 (1005 Metric)	Murata	LQG15HS27NJ02	TDK	MLG1005S27NJT000
C6,C8,C9, C10,C11	NM	56pF surface mount, general purpose multilayer ceramic chip capacitor, COG, 0201, 50V, +/-2%	Murata	GRM0335C1H560GA01	TDK	CGA1A2C0G1H560J030BA
R1	1M	Surface mount chip resistor 1M; 5%; 1/16W	Yageo	RC0402JR-071ML		
R2	68K	Surface mount chip resistor 68K; 1%; 1/16W	Yageo	AC0402FR-0768KL		
R3	15K	Surface mount chip resistor 15K; 1%; 1/16W	Yageo	RC0402FR-1315KL		
R4	10k	Surface mount chip resistor 10K; 5%; 1/16W	Yageo	RC0402JR-0710KP		
U1	ST1S12GR	Synchronous rectification adjustable step-down switching regulator ST1S12GR; 0.7; 1.7	ST	ST1S12GR TSOT23-5L		
U2	BGA725L6	Low Noise Amplifier for GPS, GLONASS, Galileo and Compass BGA725L6	Infineon	BGA725L6		
Z1	B4327	Automotive SAW RF filter for GPS+COMPASS+GLONASS	Epcos	B39162B4327P810		

Refs.	Value	Description	Manfacturer 1		Manfacturer 2	
			Name	Part number	Name	Part number
U3	LIV3FL	TESEOIII module SMPS version	ST	LIV3FL		

7 Layout recommendations

The following figure presents a layout recommendation to ensure the best performance of the Teseo-LIV3FL.

Figure 12. Teseo-LIV3FL PCB layout example



It is important to have a whole ground plane below the Teseo-LIV3FL module.

For RF passive components, ST recommends to use the 0402 (1×0.5 mm) components. Please choose the RF ground layer to be able to get 50 Ω RF line width as close as possible to the components pads.

On 50 Ω RF line it is important to avoid all possible stubs:

- For parallel components place one pad on the RF line
- If a bypass is needed, superimpose the 2 pads in one

Figure 13. Parallel component pads position

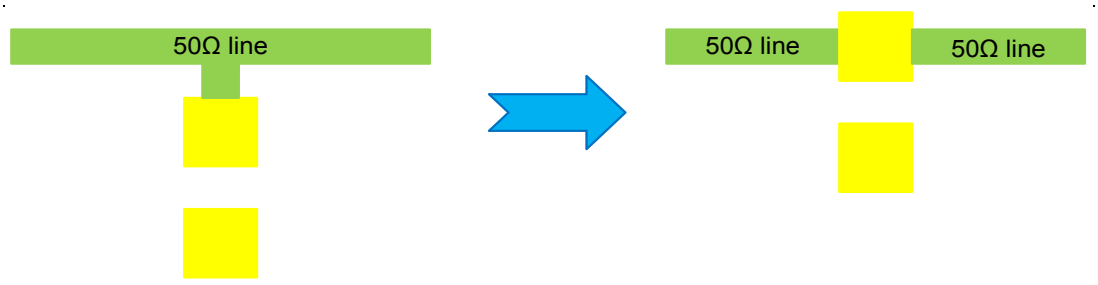
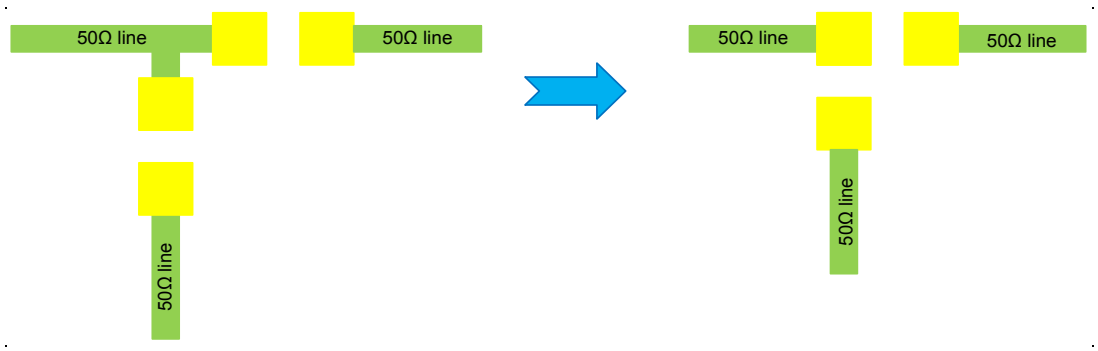


Figure 14. Bypass components pads position



8 Antenna recommendations

8.1 Patch antennas

Patch antennas have different sizes from 25×2 5mm, 18×1 8mm and 12×12 mm.

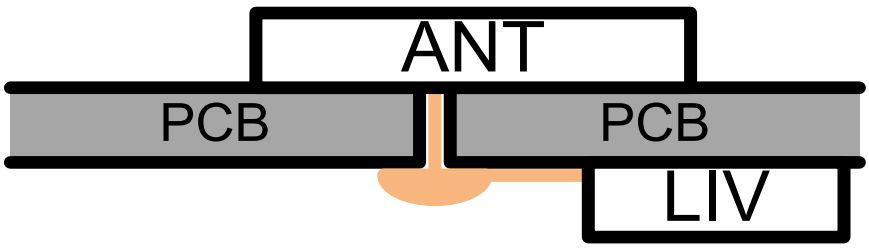
They have the advantage to be cheap, with good efficiency and highly directive. They can be used when mounted on horizontal support.

As far as performance are concerned, bigger are the antennas and better are the performances.

8.1.1 Antenna on the opposite side

Patch antennas are mounted with pin soldered on the PCB on the opposite side, where is mounted Teseo-LIV3FL and other RF components as follows.

Figure 15. Antenna vs Teseo-LIV3FL placement



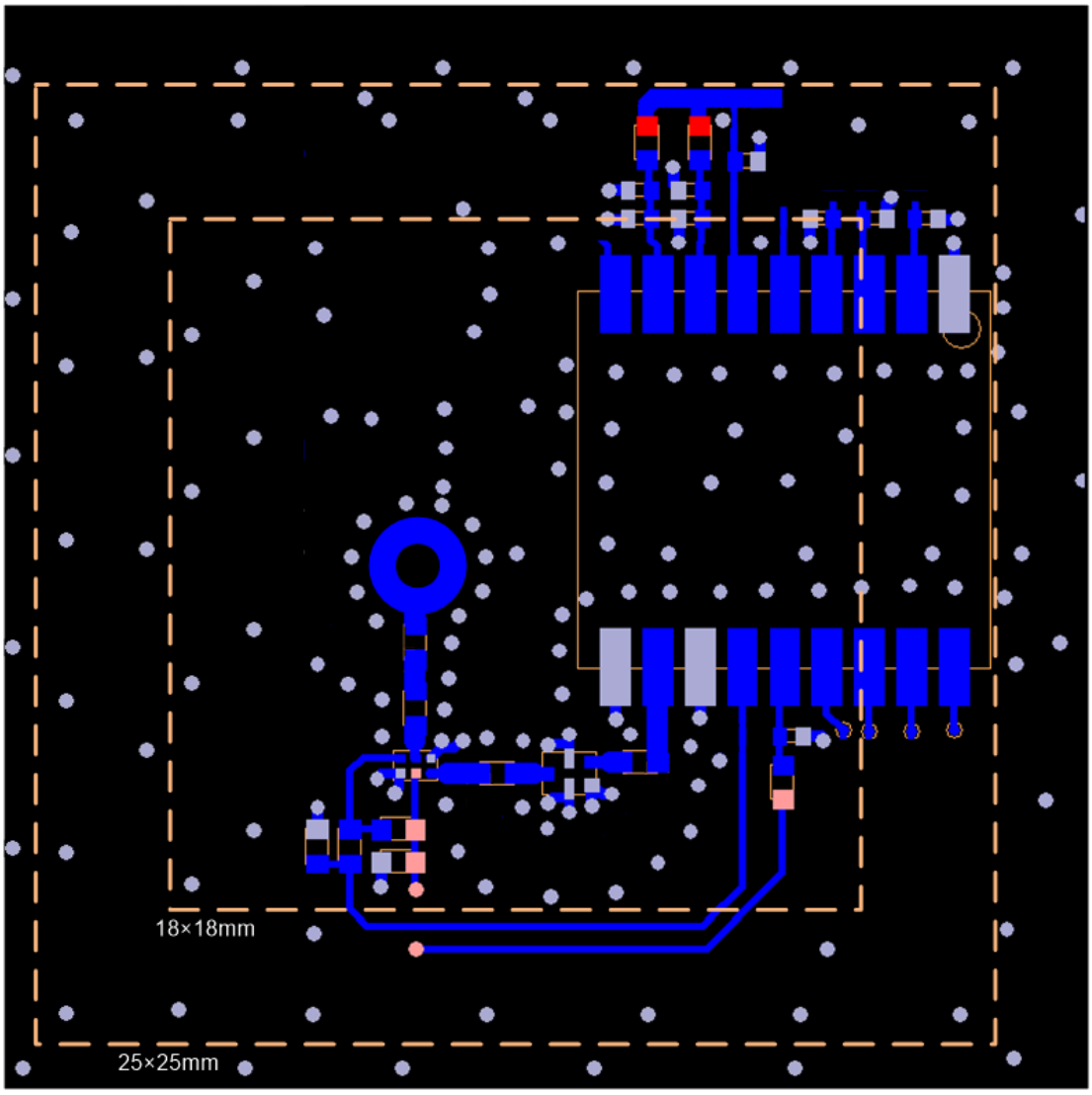
The following table gives some antenna part number compatible.

Table 5. Antenna part number compatible

Manufacturer	Part number	Constellation	Size (mm)
Taoglas	CGGBP.25.4.A.02	GPS+Glonass+Beidou	25×25
	CGGBP.25.2.A.02		25×25
	CGGP.18.4.C.02	GPS+Glonass	18×18
Yageo	ANT2525B00DT1516S		18×18
	ANT1818B00CT1575S		25×25

Here is an example of a layout with the antenna on the opposite side of the components.

Figure 16. **Antenna on bottom layer and Teseo-LIV3FL on top layout example**



On the antenna side, there is only a ground pad as large as the antenna with one large via for antenna pin. If the ground plane can be larger than the antenna size, it improves the antenna performance.

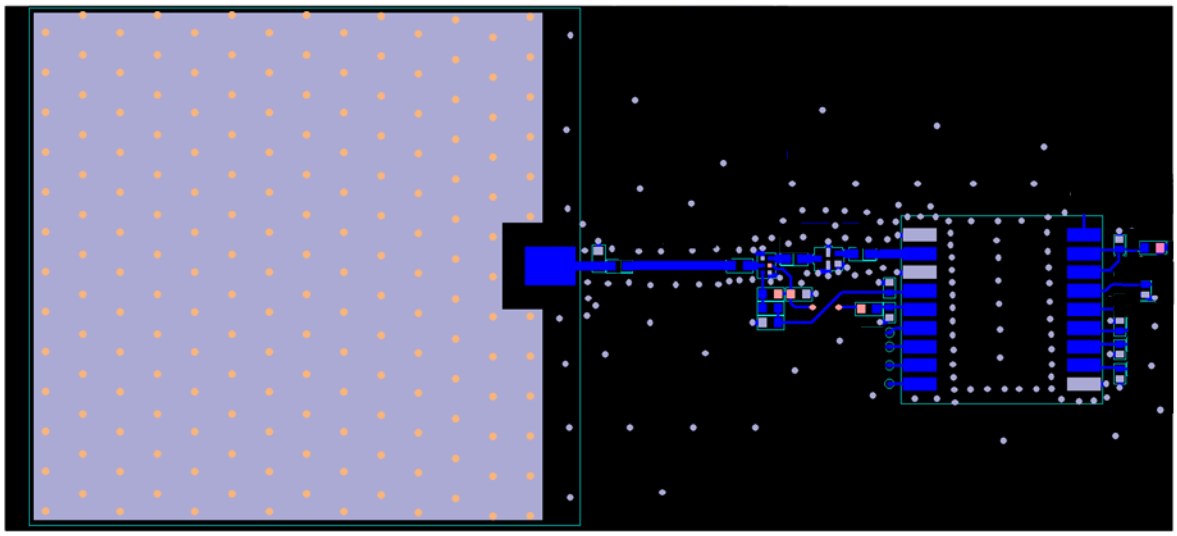
8.1.2 Antenna on the same side than Teseo-LIV3FL

The following table gives some antenna part number compatible GPS+Glonass

Table 6. **Antenna part number compatible GPS+Glonass**

Manufacturer	Part number	Constellation	Size (mm)
Taoglas	SGGP.25.4.A.02	GPS+Glonass	25×25
	SGGP.18.4.A.02		18×18
Yageo	ANT1818B00BT1516S		
	ANT2525B00BT1516S		25×25

Figure 17. **25×25 mm SMD antenna and Teseo-LIV3F on same layer example**

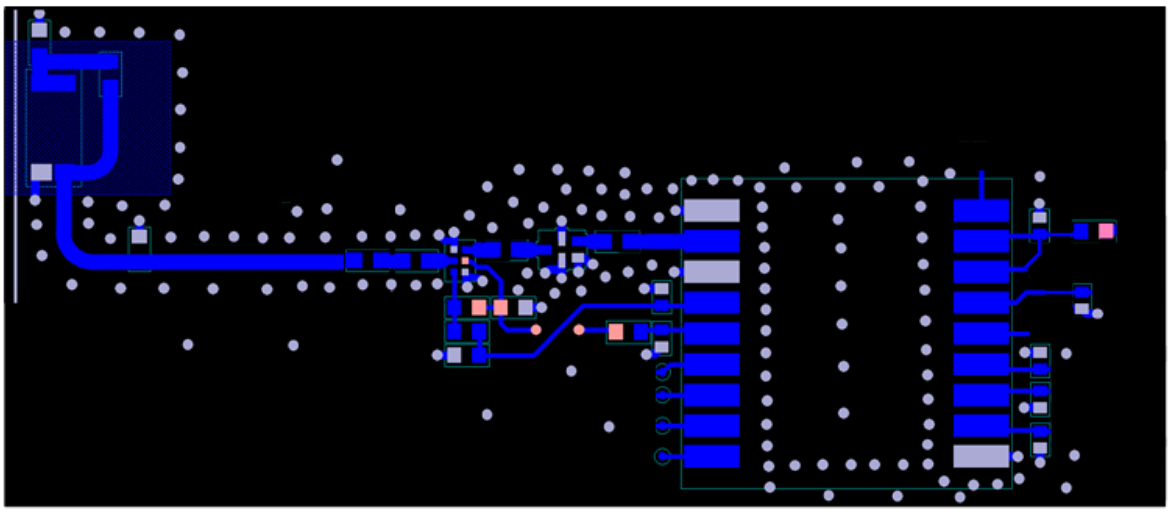


8.2 Chip antenna

Chip antenna has the advantage to be small. They are less directive than patch antenna with spherical radiation. Most of the time the PCB must be empty of copper below the antenna position with a certain aperture.

The following picture shows the example of the chip antenna (Taoglas GGBLA.01.A - GPS+Glonass+Beidou) mounted on the edge of the PCB.

Figure 18. **Chip antenna mounted on the edge of the PCB**



It is necessary to follow the layout Teseo-LIV3FL recommendations in Section 7 Layout recommendations.

8.3 Remote antenna

Remote antenna means antenna connected to PCB where Teseo-LIV3FL is soldered with an RF connector. In case of active antenna, there is no need to mount LNA on the PCB. In case of passive remote antenna, it is much better to mount an external LNA + SAW filter in front of the Teseo-LIV3FL and to have a short-coaxial cable.

Each dB lost in the cable, is lost in sensitivity capability.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
13-Jan-2022	1	Initial release.

Contents

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List of figures