# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN CMG-DTV/04/677

# TDA8177 : switch to E-STV8172A

| | PCN CMG-DTV/04/677 |
|---|---|
| Product Family /Commercial Product | TDA8177 |
| Type Of Change | Package assembly material change |
| Reason For Change | New material : Eco package |
| Description of change | TDA8177 is on end of life and it will be replaced by the product E-STV8172A lead free package to be in adequation with ecologic norm. |
| Forecasted date of change | 15-Jan-2005 |
| Forecasted date of samples for customer | 09-Aug-2004 |
| Forecasted date for **STMicroelectronics** change qualification report availability | 09-Aug-2004 |
| Marking to identify changed product | "E" on the finish goods label |
| Description of qualification program | See Attached Qualification Plan |
| Product Line(s) and/or Part Number(s) | See Attached List |
| Manufacturing Location(s) | |
| Estimated Date of first shipment | 15-Jan-2005 |

| | | |
|---|---|---|
| Division Product Manager | P.BERGER | Date: Aug.09 ,04 |
| Division Q.A. Manager | M.PICCOLI | Date: Aug.09 ,04 |

Customer Acknowledgement of Receipt PCN CMG-DTV/04/677

Please sign and return to STMicroelectronics Sales Office

| | |
|---|---|
| ☐ Qualification Plan Denied | Name: |
| ☐ Qualification Plan Approved | Title: |
| | Company: |
| ☐ Change Denied | Date: |
| ☐ Change Approved | Signature: |

Remark

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# RELIABILITY REPORT

## E-STV8172A

Ecopack (Lead free) qualification

**CONSUMER & MICROCONTROLLER GROUPS**
**DISPLAY & TV DIVISION**

**Report prepared by** : Y. Lavignasse **CMG/DTV QA Product Manager** **Date:** June 2004

# 1 - CONTENT

1 - CONTENT

2 – GENERAL, CONCLUSION

3 - DEVICE INFORMATION

4 - ESD and LATCH-UP RESULTS

5 - RELIABILITY TEST RESULTS

ATTACHMENT 1

# 2 - GENERAL

## DESCRIPTION

The product E-STV8172A is a vertical deflection booster designed for monitor and TV applications and assembled in Ecopack (Lead free) HEPTAWATT package.

## MAIN FEATURES

- Power amplifier
- Fly-back Generator
- Thermal protection
- Ecopack (Lead free) package

## CONCLUSION

No defect has been registered during the qualification exercise.

**The product E-STV8172A is qualified with its new Ecopack (Lead free) Heptawatt package.**

# 3 - DEVICE INFORMATION

| | |
|---|---|
| **TYPE** | **: E-STV8172A** |
| **FUNCTION** | **: Vertical deflection amplifier** |

## PROCESS : B50II

| | |
|---|---|
| METALLIZATION | : Al-Si |
| FINAL PASSIVATION | : NITRIDE |
| BACKSIDE METALLIZATION | : CHROMIUM/NICKEL/GOLD |

## PACKAGE : Ecopack HEPTAWATT (Lead free)

| | |
|---|---|
| MOULD MATERIAL | : Epoxy resin |
| LEAD FRAME MATERIAL | : Copper |
| DIE ATTACH | : Soft Solder |
| WIRE MATERIAL | : Copper |
| WIRE DIAMETER | : 51 µm (2.0Mils) |

## LOCATIONS

| | |
|---|---|
| FRONT END PLANT | : STMicroelectronics ANG-MO-KIO (Singapore) |
| BACK END PLANT | : STMicroelectronics BOUSKOURA(Morocco) |
| FINAL TEST PLANT | : STMicroelectronics BOUSKOURA(Morocco) |
| DIVISION QUALITY ASSURANCE | : STMicroelectronics GRENOBLE (France) |

# 4 - ESD and LATCH-UP RESULTS

## ESD

To evaluate adequate pins protection to electrostatic discharge.

**CONDITIONS**

**NORM HBM (human body model):** 100pF / 1.5 kOhms

" All the pins withstand +/- 2.2 KV versus Ground and Vcc"

**NORM MM (machine model) :** 200pF / 0 Ohm

" All the pins withstand +/- 220 V versus Ground and Vcc"

## LATCH-UP

To verify the latch-up sensitivity of each pin.

**Positive injection:** No latch on 4 parts with 200mA pulses..

**Negative injection:** No latch on 4 parts with 200mA pulses.

# 5 - RELIABILITY TESTS RESULTS

## A - ELECTRICAL TESTS (Die oriented tests)

| TEST | CONDITIONS | LOT# | HOURS | SAMPLES | FAILURE |
|---|---|---|---|---|---|
| **HTRB** | Tj = 150 °C<br>Vcc = 30V<br>Pd = 1W | 1 | 1000 | 72 | 0 |
| **OLT** | Tj = 150 °C<br>Vcc = 35 V<br>Iout = 3 App | 1 | 1000 | 72 | 0 |

## B – PACKAGE ORIENTED TESTS

| TEST | CONDITIONS | LOT# | STEPS | SAMPLES | FAILURE |
|---|---|---|---|---|---|
| **TMC** | -65°C/+150°C | 1 | 1000c | 50 | 0 |
| **PPT** | 120°C/2atm/<br>100%RH | 1 | 240H | 50 | 0 |

(Please refer to attachment 1 for reliability test description)

## ATTACHMENT 1: RELIABILITY TESTS DESCRIPTION

| TEST NAME | DESCRIPTION | PURPOSE |
|---|---|---|
| **OLT:** Operating Life Test | The device is stressed in dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature, load current, internal power dissipation. | To simulate the worst-case application stress conditions. The typical failure modes are related to electromigration, wire-bonds degradation, oxide faults. |
| **HTRB**: High Temperature Reverse Bias test | The device is stressed in static configuration, trying to satisfy as much as possible the following conditions:<br>-) low power dissipation<br>-) max. supply voltage compatible with diffusion process and internal circuitry limitations<br>-) max. junction temperature | To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. |
| **ESD:** Electrostatic Discharge | The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. | To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge. |
| **LU:** Latch-up | The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed. | To verify the presence of bulk parasitic effects inducing latch-up. |
| **TMC:** Temperature Cycles Test | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere. | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die-attach layer degradation. |
| **PPT:** Pressure Pot Test | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature. | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. |

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