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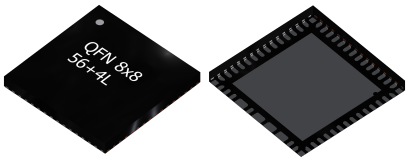
SPSB100

Data brief

Automotive power management IC for highly integrated processors



QFN 8x8 56+4L

Product status link
SPSB100

Product summary		
Order code	**Package**	**Packing**
SPSB100	QFN 8x8 56L+4 WF	Tray
SPSB100TR		Tape and reel
SPSB100B		Tray
SPSB100BTR		Tape and reel

Features

- AEC-Q100 qualified
- 2 configurable (6.5 V, 5 V, 3.3 V) buck converters and peak switching current limit of 3.0 A @ 2.4 MHz or 400 kHz
- 1 configurable (3.3 V, 1.25 V, 1.2 V, 1.1 V, 0.97 V) buck converter and peak switching current limit up to 6.0 A @ 2.4 MHz, with fine tuning configurability around 0.97 (0.94 V to 1.0 V)
- Overcurrent detection and limitation for all bucks
- Integrated soft start on buck stages
- Boost controller 8-9.5 V and peak switching current limit of 4.2 A @ 400 kHz, for sustaining low battery conditions and deep cranking pulse (external power components can be optionally populated)
- One 5 V voltage regulator (120 mA, 2% acc.) for CAN FD supply
- One configurable (5 V or 3.3 V) low drop voltage tracker of all regulators for µC ADC reference supply (10 mA, +/-10 mV)
- One high-side driver for contact monitoring (R_{ON} = 55 Ω) with open-load and overcurrent diagnosis
- Dedicated interrupt pin for failure communication
- Device operates in low power mode
- Very low quiescent current in deep-sleep state
- MCU reset generator
- Configurable window watchdog with extended long open window up to 8s and enable/disable function through NVM bit
- 1 CAN-FD transceiver (ISO 11898-2/2016 and SAE J2284 & SAE J2962-2 compliant), fully deactivable via SPI, with local failure and bus failure diagnosis (only for SPSB100 version)
- Device contains temperature warning and protection
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- STMicroelectronics standard serial peripheral interface (32Bit/ST_SPI) including 4-bit CRC
- 1 fail safe output
- 1 input pin supporting static and dynamic error signal reporting
- Programmable periodic system wake-up feature
- Documentation available for customers that need support when dealing with ASIL requirements as per ISO26262

Applications

- Central gateway module
- Telematic control unit
- Body control module
- Vehicle control unit
- Zone control module

Description

The SPSB100 is a fully integrated power management system IC, especially designed for highly integrated application processors (for example, the Stellar G and P MCU families), offering low -power mode and high current capability. The device comes with enhanced system power supply functionality and CAN FD physical communication layer (only for SPSB100 version).

It combines three switch mode power supply together with one integrated linear regulator, and one reference supply to track one of buck converters. The device integrates further two wake-up inputs and advanced fail-safe functionalities.

The boost controller is intended to sustain cold cranking pulses, start stop and weak battery conditions.

Different combinations enable to supply the system microcontroller, the integrated CAN FD transceiver and external peripheral loads and sensors in several and adjustable voltage and current ranges.

The STMicroelectronics standard SPI interface allows control and diagnosis of the device and enables generic software development.

The device offers a set of features to support applications that need to fulfill functional safety requirements as defined by the automotive safety integrity level (ASIL).

1 Block diagram and pin description

1.1 Block diagram

Figure 1. **SPSB100 block diagram**

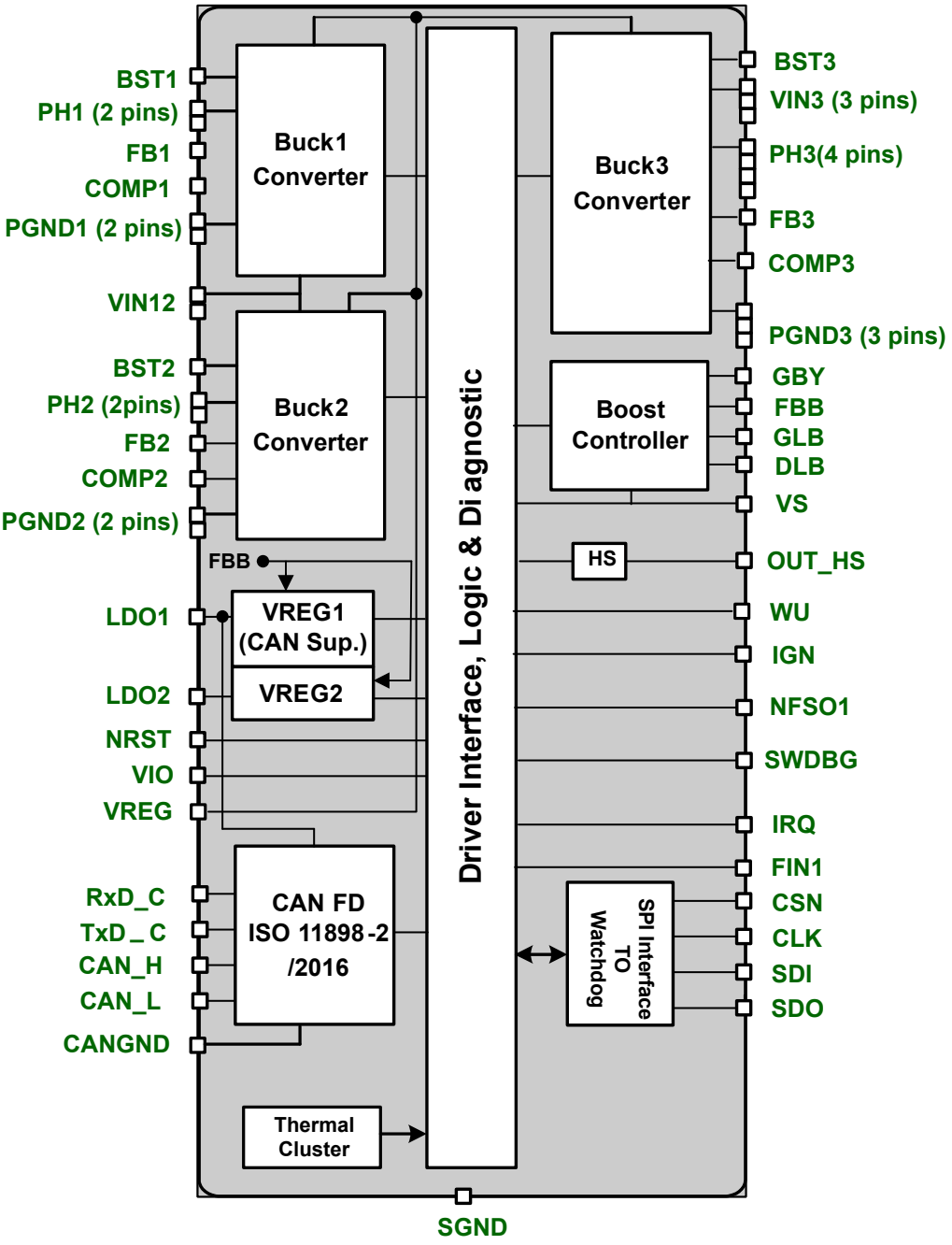
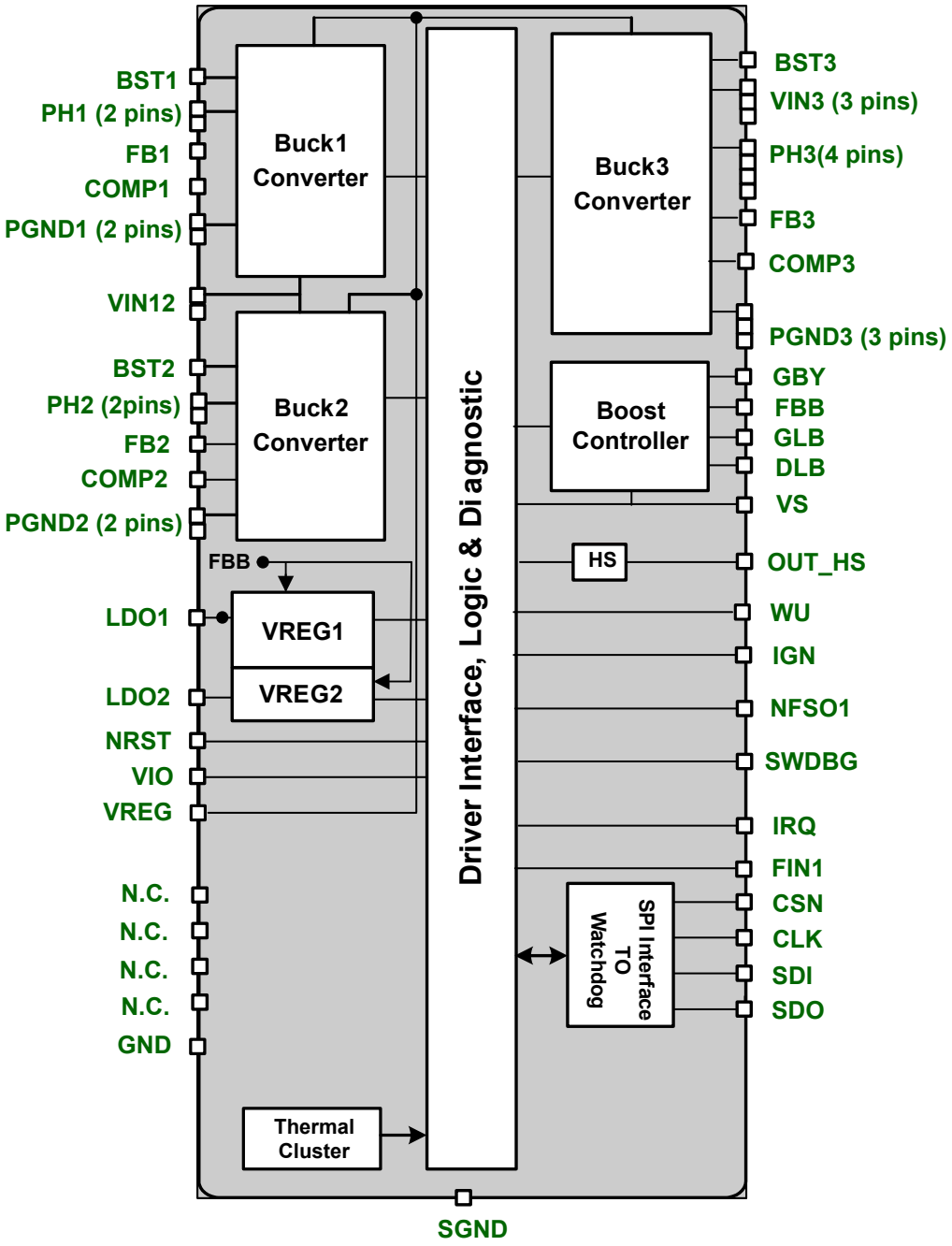


Figure 2. **SPSB100B block diagram**



1.2 Pin description

Figure 3. **SPSB100 pin connection (top view)**

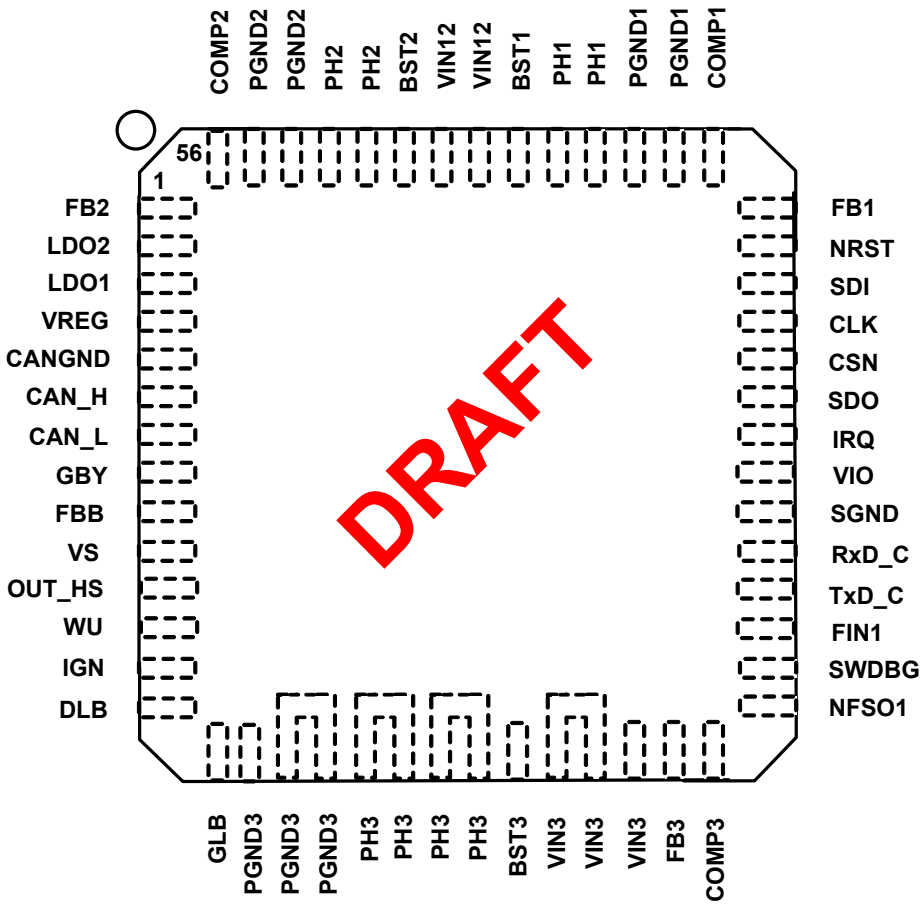


Figure 4. **SPSB100B pin connection (top view)**

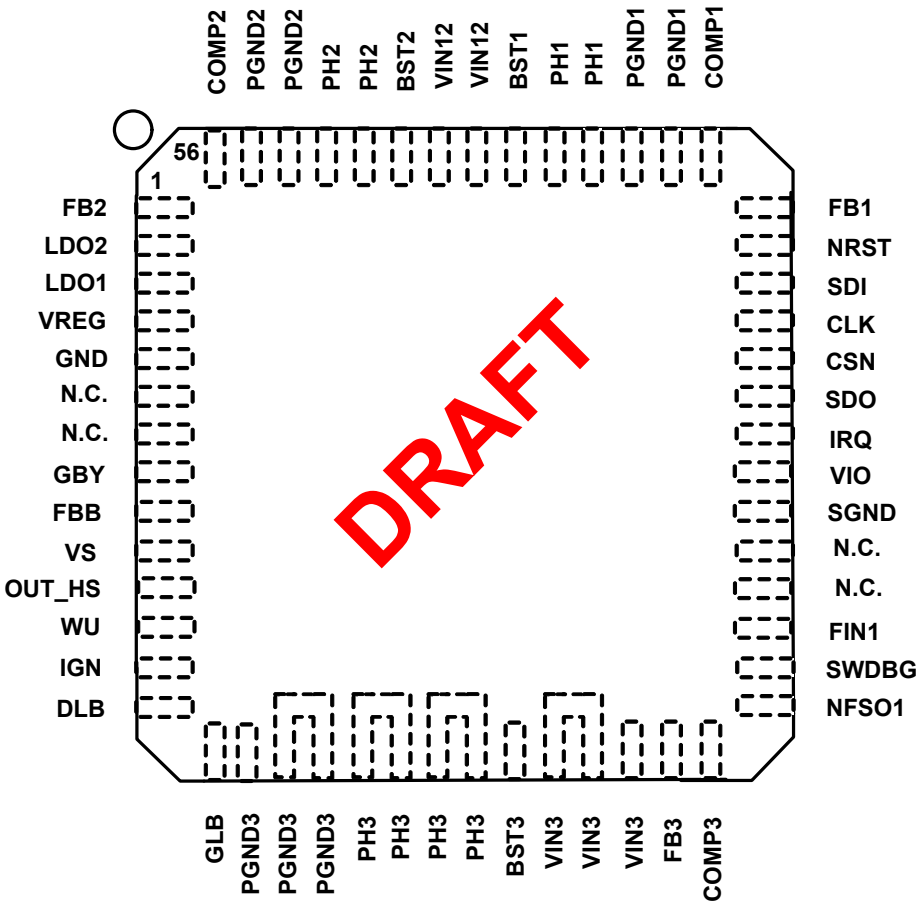


Table 1. **Pin function**

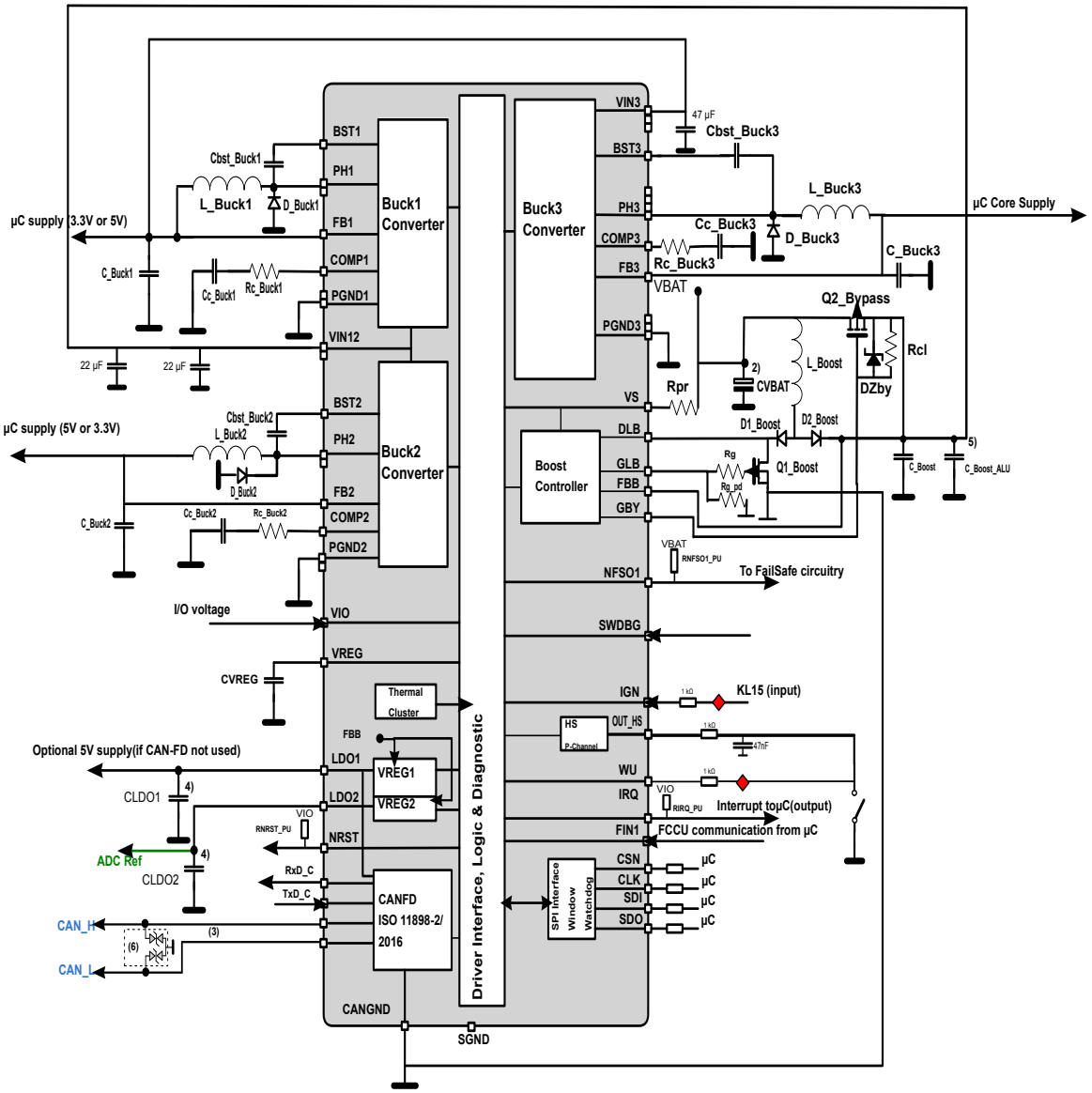
Pin number	PinSPSB100	Pin SPSB100B	Description	I/O type
1	FB2	FB2	BUCK2 feedback voltage (to internal voltage monitors)	I
2	LDO2	LDO2	Voltage regulator 5 V/3.3 V - tracker of Bucks output (supply for microcontroller)	O
3	LDO1	LDO1	5 V voltage regulator 1 output (for CAN-FD supply)	O
4	VREG	VREG	3.3 V regulator output for buck bootstrap	O
5	CANGND	GND	CAN Ground / DS monitoring Ground	
6	CAN_H	N.C.	CAN high level voltage I/O	I/O
7	CAN_L	N.C.	CAN Low level voltage I/O	I/O
8	GBY	GBY	Gate driver of external MOS bypass BOOST	O
9	FBB	FBB	BOOST feedback pin and supply for LDO1 & LDO2, OUT_HS, VREG, WU, and IGN	I
10	VS	VS	Boost input	I
11	OUT_HS	OUT_HS	High-side-driver output to supply contacts	O

Pin number	PinSPSB100	Pin SPSB100B	Description	I/O type
12	WU	WU	Wake up input for static or cyclic monitoring of external contact	I
13	IGN	IGN	Wake up input for static or cyclic monitoring of external contact with KL15 feature	I
14	DLB	DLB	Drain monitoring of external low-side MOS of BOOST	I
15	GLB	GLB	Gate driver of external low-side MOS of BOOST	O
16	PGND3	PGND3	BUCK3 power Ground	
17	PGND3, second pin	PGND3, second pin	Current capability (pin description see above)	
18	PGND3, third pin	PGND3, third pin	Current capability (pin description see above)	
19	PH3	PH3	Switching node BUCK3	I/O
20	PH3, 2ndpin	PH3, 2ndpin	Current capability (pin description see above)	O
21	PH3, 3rdpin	PH3, 3rdpin	Current capability (pin description see above)	O
22	PH3, 4thpin	PH3, 4thpin	Current capability (pin description see above)	O
23	BST3	BST3	Boot-strap capacitor to supply BUCK3 high-side MOS gate-driver circuitry	
24	VIN3	VIN3	Input voltage BUCK3	I
25	VIN3, Second pin	VIN3, Second pin	Current capability (pin description see above)	I
26	VIN3, Third pin	VIN3, Third pin	Current capability (pin description see above)	I
27	FB3	FB3	BUCK3 feedback voltage (to internal voltage monitors)	I
28	COMP3	COMP3	BUCK3 error amplifier compensation network	
29	NFSO1	NFSO1	Fail safe output (active Low, open drain)	O
30	SWDBG	SWDBG	Debug input to deactivate the window watchdog (active high) and entering pin for NVM emulation mode	I
31	FIN1	FIN1	FCCU sequence input	I
32	TxD_C	N.C.	CAN transmit data input	I
33	RxD_C	N.C.	CAN receive data output	O
34	SGND	SGND	Signal Ground	
35	VIO	VIO	I/O power supply (3.3V or 5V)	I
36	IRQ	IRQ	Interrupt (open drain)	O
37	SDO	SDO	SPI serial data output	O
38	CSN	CSN	SPI chip select not input	I
39	CLK	CLK	SPI serial clock input	I
40	SDI	SDI	SPI serial data input	I
41	NRST	NRST	Reset output to microcontroller, internal pull-up (open drain)	O
42	FB1	FB1	BUCK1 feedback voltage (to internal voltage monitors)	I
43	COMP1	COMP1	BUCK1 error amplifier compensation network	
44	PGND1	PGND1	BUCK1 power Ground	
45	PGND1, 2ndpin	PGND1, 2ndpin	Current capability (pin description see above)	
46	PH1	PH1	Switching node BUCK1	I/O
47	PH1, 2ndpin	PH1, 2ndpin	Current capability (pin description see above)	O

Pin number	PinSPSB100	Pin SPSB100B	Description	I/O type
48	BST1	BST1	Boot-strap capacitor to supply BUCK1 high-side MOS gate-driver circuitry	
49	VIN12	VIN12	Input voltage BUCK1 and BUCK2	I
50	VIN12	VIN12	Current capability (pin description see above)	I
51	BST2	BST2	Boot-strap capacitor to supply BUCK2 high-side MOS gate-driver circuitry	
52	PH2	PH2	Switching node BUCK2	I/O
53	PH2, 2ndpin	PH2, 2ndpin	Current capability (pin description see above)	O
54	PGND2,	PGND2,	BUCK2 power Ground	
55	PGND2, second pin	PGND2, second pin	Current capability (pin description see above)	

2 Application circuit

Figure 5. **Typical application circuit for SPSB100**



1)Capacitance to be dimensioned according load current (rule of thumb 500 µF each 10A)
2)Capacitance to be dimensioned e.g. according voltage drop out requirements
3)OEM requirements and external components for CAN to be fulfilled
4)For EMC optimization purposes, capacitance could be redimensioned (2.2 µF recommended)
5)Optional to improve ripple on boost voltage
6)ST ESDCAN04-2BWY is needed only for SAE J2962-2 compliance

ESD Protectionfor ECU pins

Revision history

Table 2. **Document revision history**

Date	Version	Changes
31-Mar-2023	1	Initial release.